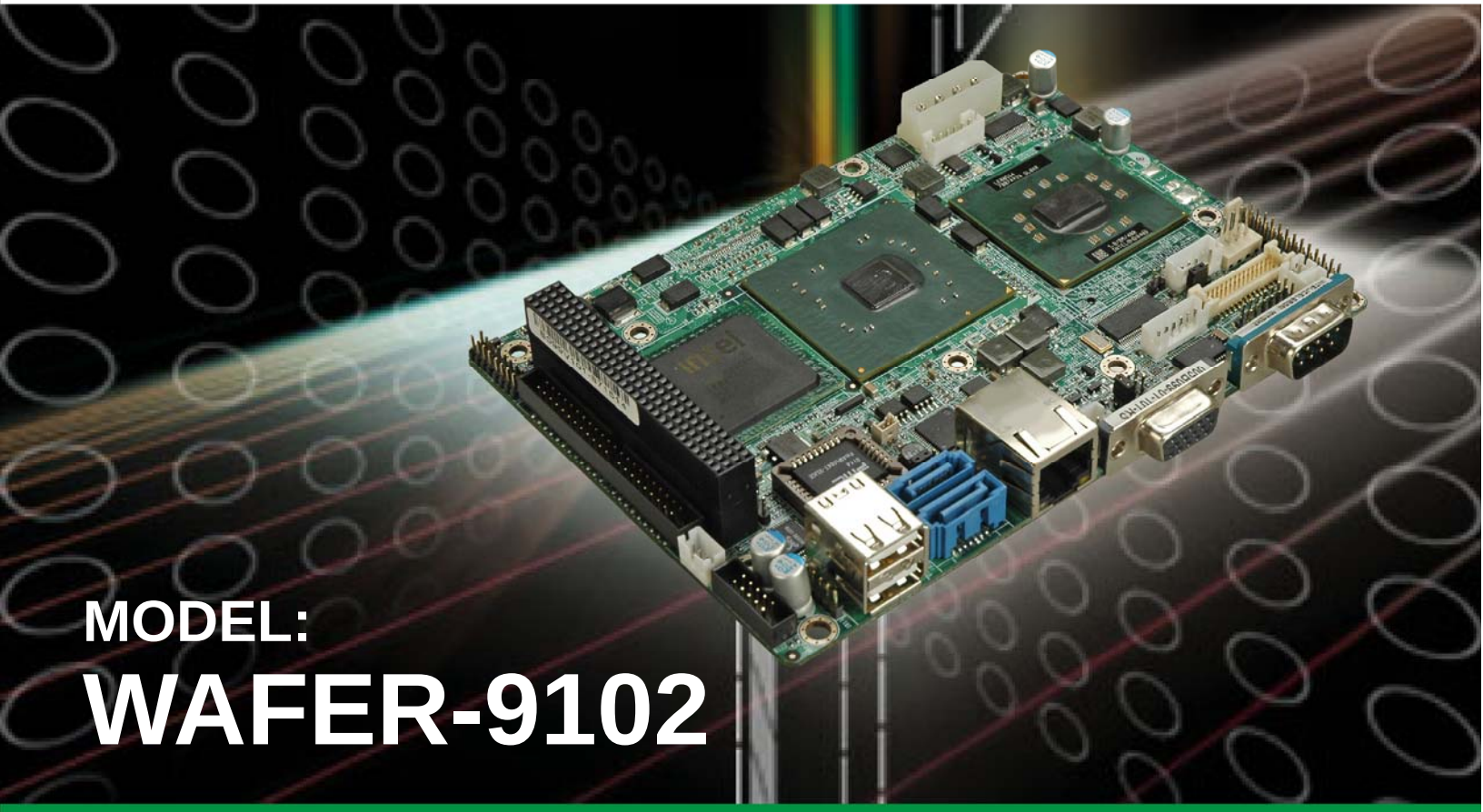
IEI Technology Corp.



MODEL:

WAFER-9102

3.5" SBC with Socket 479 for Pentium® M or Celeron® M DDR2 SO-DIMM (up to 2 GB), VGA, Dual-Channel 24-bit LVDS, PCIe GbE, CompactFlash®, Dual SATA and PCI-104

User Manual

Rev. 1.00 – 10 November, 2008

RoHS Lead Free

Revision

Date	Version	Changes
10 November, 2008	1.00	Initial release

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Manual Conventions

WARNING!

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously. Warnings are easy to recognize. The word “warning” is written as “**WARNING**,” both capitalized and bold and is followed by text. The text is the warning message. A warning message is shown below:

WARNING:

This is an example of a warning message. Failure to adhere to warning messages may result in permanent damage to the WAFER-9102 or personal injury to the user. Please take warning messages seriously.

CAUTION!

Cautionary messages should also be heeded to help reduce the chance of losing data or damaging the WAFER-9102. Cautions are easy to recognize. The word “caution” is written as “**CAUTION**,” both capitalized and bold and is followed. The text is the cautionary message. A caution message is shown below:

CAUTION:

This is an example of a caution message. Failure to adhere to cautions messages may result in permanent damage to the WAFER-9102. Please take caution messages seriously.

NOTE:

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes. Notes are easy to recognize. The word “note” is written as “**NOTE**,” both capitalized and bold and is followed by text. The text is the cautionary message. A note message is shown below:

NOTE:

This is an example of a note message. Notes should always be read. Notes contain critical information about the WAFER-9102. Please take note messages seriously.

Packing List

NOTE:

If any of the components listed in the checklist below are missing, please do not proceed with the installation. Contact the IEI reseller or vendor you purchased the WAFER-9102 from or contact an IEI sales representative directly. To contact an IEI sales representative, please send an email to sales@iei.com.tw.

The items listed below should all be included in the WAFER-9102 package.

- 1 x WAFER-9102 3.5" SBC
- 2 x SATA cable
- 1 x Keyboard/mouse cable
- 1 x Audio cable
- 1 x Cooler (WAFER-9102-R10 only)
- 1 x Mini jumper pack
- 1 x Utility CD
- 1 x QIG (quick installation guide)

Images of the above items are shown in **Chapter 3**.

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Chapter

1

Introduction

1.1 Introduction

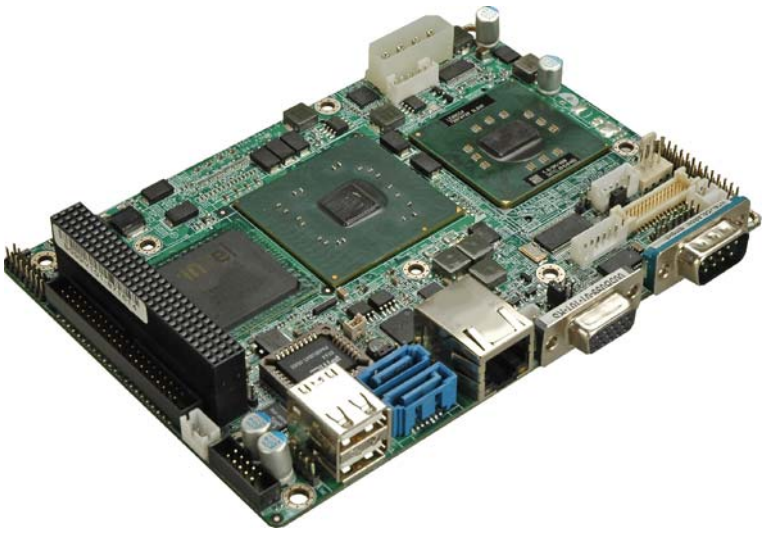


Figure 1-1: WAFER-9102

The WAFER-9102 3.5" SBC motherboards are Intel® Pentium® M and Intel® Celeron® M processor platforms. CPU options include Pentium® M or Celeron® M processors on the WAFER-9102-R10 Socket 479 model. Embedded Celeron® M 1.0 GHz processor options include the WAFER-9102-1GZ-R10 with zero cache and the WAFER-9102-1G512-R10 with 512 KB of cache. The WAFER-9102 also supports one 200-pin 400 MHz 2.0 GB (max.) DDR2 SDRAM SO-DIMM. The board comes with VGA and 24-bit dual-channel LVDS video outputs. The WAFER-9102 also comes with a PCI Express (PCIe) Gigabit Ethernet (GbE) connector, onboard AC'97 audio, an RS-232 serial ports, an RS-232/422/485 serial port, a CompactFlash® slot, six USB 2.0 ports, IDE connector and PCI-104 expansion slot.

1.2 WAFER-9102 Overview

1.2.1 Overview Photo

The WAFER-9102 has a wide variety of peripheral interface connectors. **Figure 1-2** is a labeled photo of the peripheral interface connectors on the WAFER-9102.

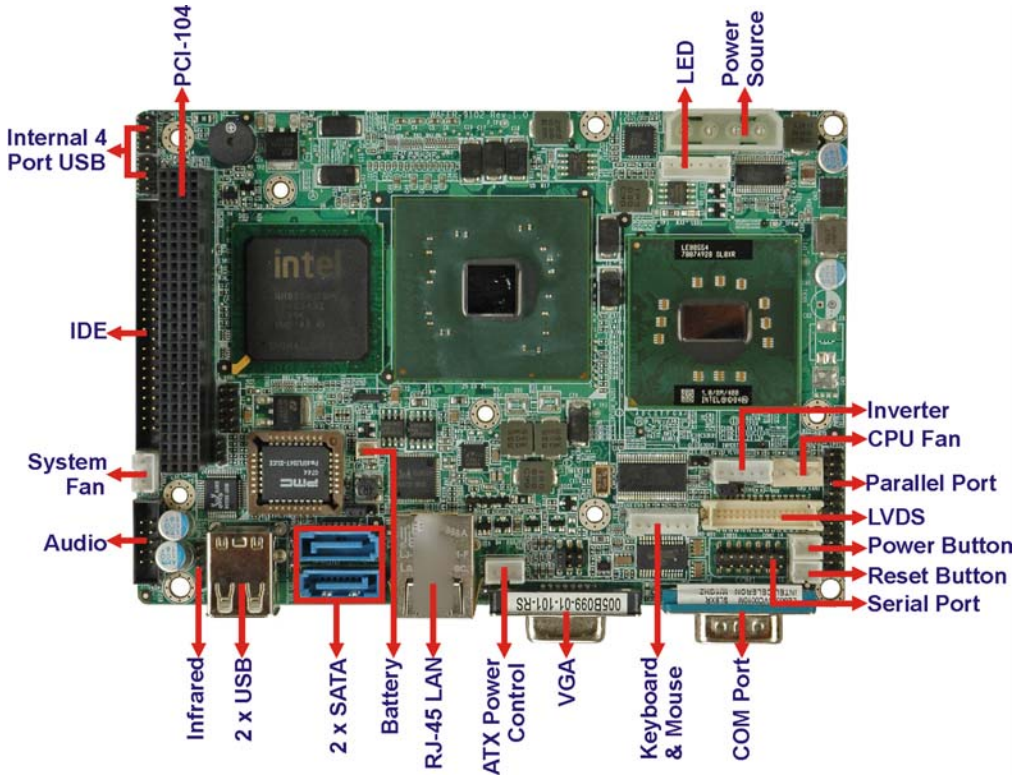


Figure 1-2: WAFER-9102 Overview (Front)

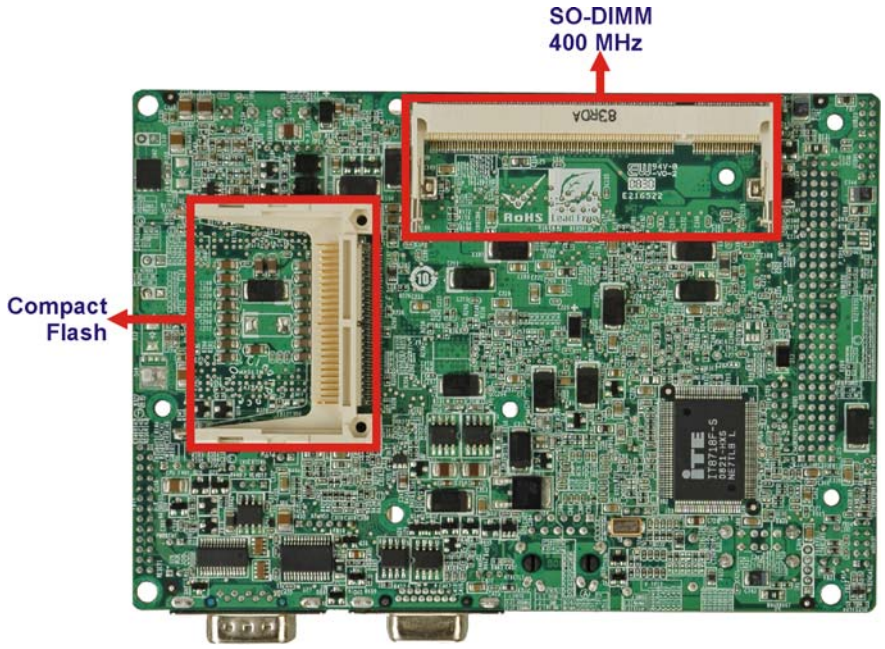


Figure 1-3: WAFER-9102 Overview (Rear)

1.2.2 Peripheral Connectors and Jumpers

The WAFER-9102 has the following connectors on-board:

- 1 x ATX power connector
- 1 x ATX power control connector
- 1 x Audio connector
- 1 x CompactFlash® slot
- 1 x CPU fan connector
- 1 x DDR2 SO-DIMM connector
- 1 x Digital I/O connector
- 1 x Front panel indicators connector
- 1 x IDE connector
- 1 x Infrared connector
- 1 x Keyboard/mouse connector
- 1 x LCD backlight inverter connector
- 1 x LVDS panel connector
- 1 x Parallel port connector
- 1 x PCI-104 connector
- 1 x Power button connector
- 1 x Reset button connector
- 1 x RS-232/422/485 connector
- 2 x SATA connectors
- 1 x System fan connector
- 2 x USB connectors (4 ports)

The WAFER-9102 has the following external peripheral interface connectors on the board rear panel.

- 1 x LAN
- 1 x RS-232 serial ports
- 2 x USB 2.0
- 1 x VGA

The WAFER-9102 has the following on-board jumpers:

- AT power mode setting

- Clear CMOS
- CompactFlash® card setup
- COM2 port mode setting
- LVDS voltage selection

1.2.3 Technical Specifications

WAFER-9102 technical specifications are listed in **Table 1-1**. See **Chapter 2** for details.

Specification	WAFER-9102
Form Factor	3.5" SBC
System CPU	Socket 479 Intel® Pentium® M or Celeron® M (WAFER-9102-R10) Embedded Intel® Celeron® M with zero cache (WAFER-9102-1GZ-R10) Embedded Intel® Celeron® M with 512 KB cache (WAFER-9102-1G512-R10)
Front Side Bus (FSB)	400 MHz
System Chipset	Northbridge: Intel® 910GMLE Southbridge: Intel® ICH6M
Memory	One 200-pin SO-DIMM socket supports one 400 MHz 2.0 GB (max.) DDR2 SDRAM SO-DIMM
CompactFlash®	One CompactFlash® socket
Super I/O	iTE IT8718
Display	VGA Dual-channel 24-bit LVDS
BIOS	AMI BIOS label
Audio	Realtek ALC655 AC'97 codec
LAN	Realtek RTL8111C PCIe GbE controller
COM	One RS-232 serial port One RS-232/422/485 serial port

Specification	WAFER-9102
USB2.0	Six USB 2.0 devices supported (four internal, two external)
Hard Drives	One 44-pin IDE connector
SATA	Two 1.5 Gb/s SATA drives supported
Keyboard/mouse	One keyboard/mouse connector
Digital I/O	One 8-bit digital input/output connector; 4-bit input/4-bit output through the iTE IT8718 super I/O
Watchdog Timer	Software programmable 1-255 sec. through the iTE IT8718 super I/O
Infrared	One infrared connector supports Serial Infrared (SIR) Amplitude Shift Keyed IR (ASKIR)
Power Supply	ATX and AT power supported
Power Consumption	5 V @ 3.11 A. 12 V @ 0.37 A (Intel® Celeron® M 373 1.0 GHz with 1.0 GB DDR2 memory) 5 V @ 2.94 A. 12 V @ 1.57 A (Intel® Pentium® M 725 1.6 GHz with 1.0 GB DDR2 memory)
Temperature	0ºC – 60ºC (32ºF - 140ºF)
Humidity (operating)	5%~95% non-condensing
Dimensions (LxW)	146 mm x 102 mm
Weight (GW/NW)	700 g / 230 g

Table 1-1: Technical Specifications

Chapter

2

Detailed Specifications

2.1 Dimensions

2.1.1 Board Dimensions

The dimensions of the board are listed below:

- **Length**: 102 mm
- **Width**: 146 mm

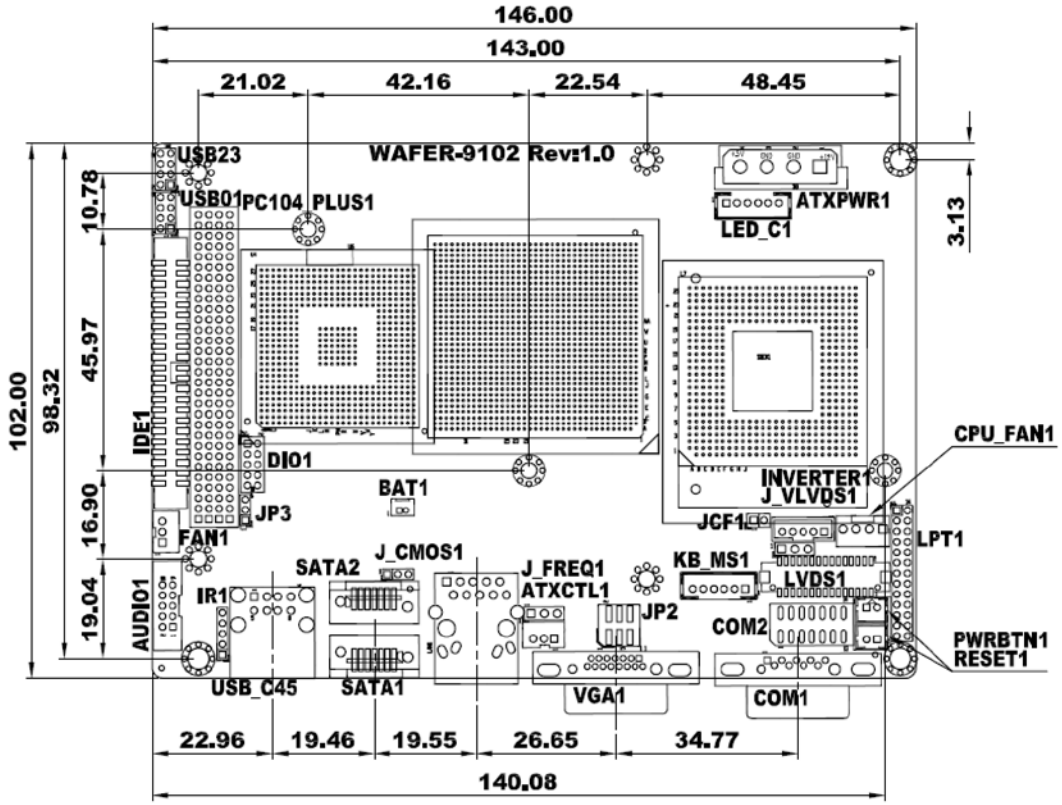


Figure 2-1: WAFER-9102 Dimensions (Front) (mm)

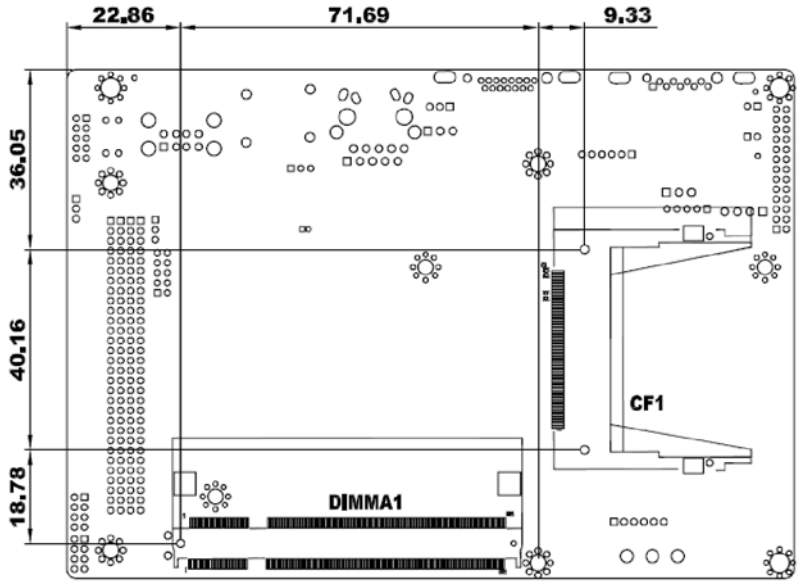


Figure 2-2: WAFER-9102 Dimensions (Rear) (mm)

2.1.2 External Interface Panel Dimensions

External peripheral interface connector panel dimensions are shown in **Figure 2-3**.

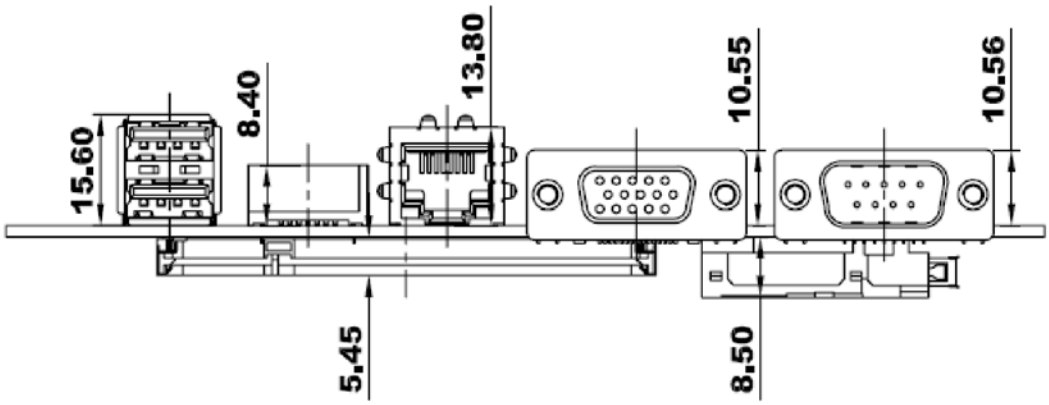


Figure 2-3: External Interface Panel Dimensions (mm)

2.2 Data Flow

Figure 2-4 shows the data flow between the two on-board chipsets and other components installed on the motherboard and described in the following sections of this chapter.

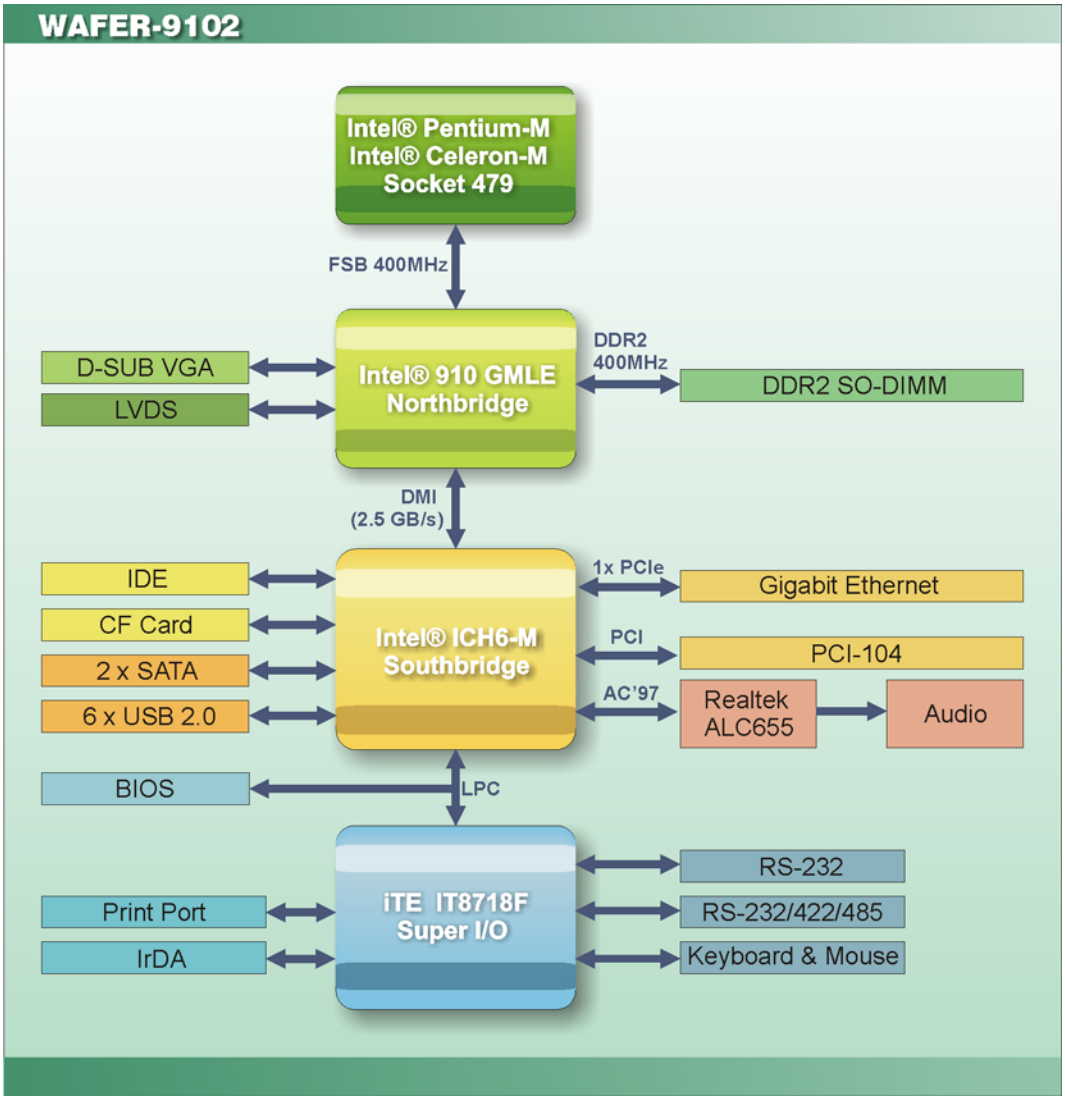


Figure 2-4: Data Flow Block Diagram

2.3 Intel® Celeron® M / Pentium® M Processor

The WAFER-9102 comes with an Intel® Pentium® M or Intel® Celeron® M processor. There are options for embedded processors or a socket 479 CPU socket. The processor

supports a 400 MHz FSB and cache varies between processors. The processor is shown in **Figure 2-5** below.

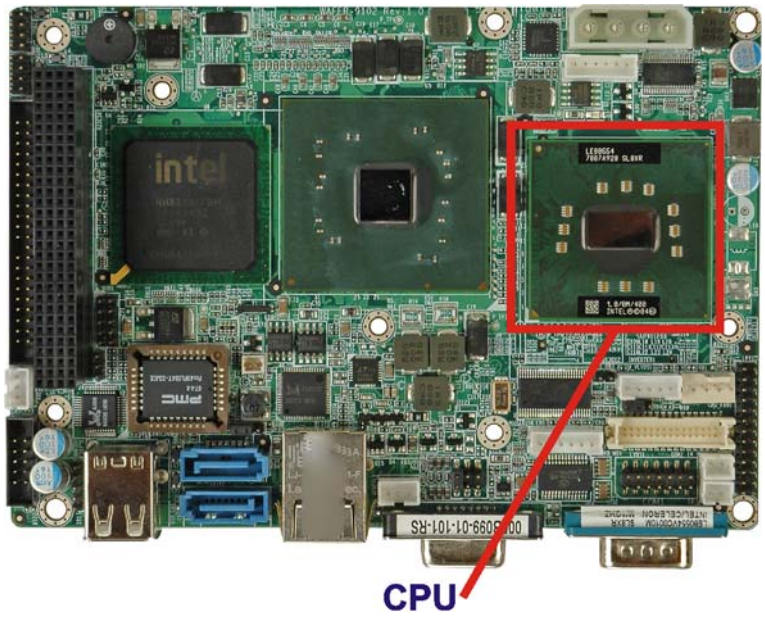


Figure 2-5: CPU

2.3.1 Intel® Celeron® M Features

Intel® Celeron® M processors are cheaper processors for embedded computing. Reduced computing power makes them ideal for applications that don't require lots of processing power. The low-power requirements reduce power consumption, saving on power for systems based on the Intel® Celeron® M. Some of the specifications of Intel® Celeron® M processors are listed below:

- Manufactured on 90 nm process with copper interconnects
- Supports Intel® architecture with dynamic execution
- 32 KB instruction cache and 32 KB write-back data cache, both on-die
- On-die second level cache (512 KB, 1 MB or none) with advanced transfer cache architecture, 8-way set associativity and ECC support
- Data Prefetch logic
- Streaming SIMD extensions 2

2.3.2 Intel® Pentium® M Features

Intel® Pentium® M processors are more expensive, but offer more power. Increased processing power makes them ideal for mobile applications that still require a decent amount of processing power. Typically, the processor will require some active cooling like a fan. Some of the specifications of Intel® Pentium® M processors are listed below:

- Supports Intel® architecture with dynamic execution
- On-die, primary 32 KB instruction cache and 32 KB write-back data cache
- On-die, 2 MB second level cache with advanced transfer cache architecture
- Data Prefetch logic
- Streaming SIMD extensions 2
- Manufactured on 90 nm process with copper interconnects
- Support for MMX™ technology and Internet streaming SIMD instructions

2.4 Intel® 910GMLE Graphics and Memory Controller Hub

The Intel® 910GMLE GMCH has the Intel® Graphics Media Accelerator 900 (Intel® GMA 900) to support integrated graphics. The integrated graphics and memory controller hub (GMCH) facilitates the flow of information primarily between the following four interfaces:

- Front Side Bus (FSB)
- System Memory Interface
- Graphics Interface
- Direct Media Interface (DMI)

2.4.1 Intel® 910GMLEFront Side Bus (FSB) Support

The Intel® 910GMLE GMCH supports processors with a 400 MHz FSB. The FSB connection between the CPU and the Intel® 910GMLE is shown in **Figure 2-6**.

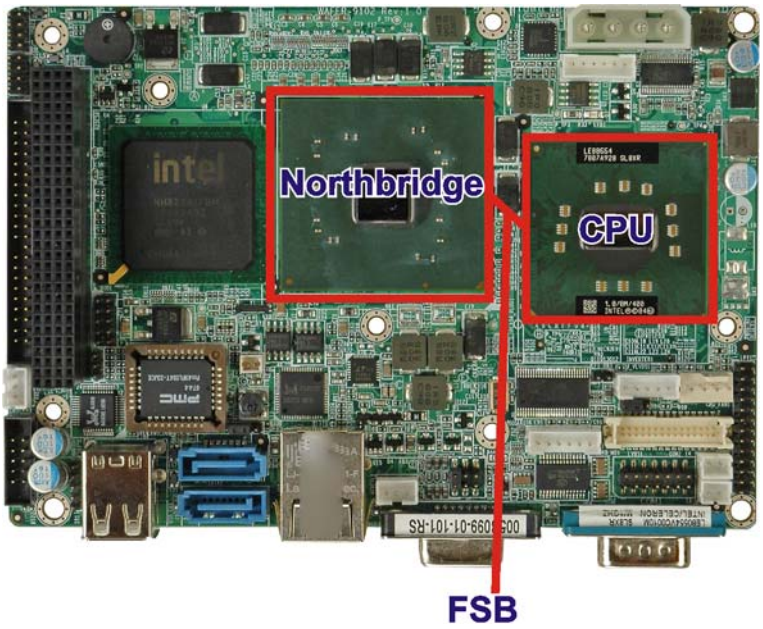


Figure 2-6: Front Side Bus (FSB)

2.4.2 Intel® 910GMLEMemory Support

The Intel® 910GMLE GMCH on the WAFER-9102 supports one 200-pin DDR2 SO-DIMM with the following features:

- One 200-pin DIMM
- DDR2
- Single-channel
- Capacities of 256 MB, 512 MB, 1.0 GB or 2.0 GB
- Transfer speeds of 400 MHz
- 64-bit wide channel

The memory sockets are shown in **Figure 2-7**.

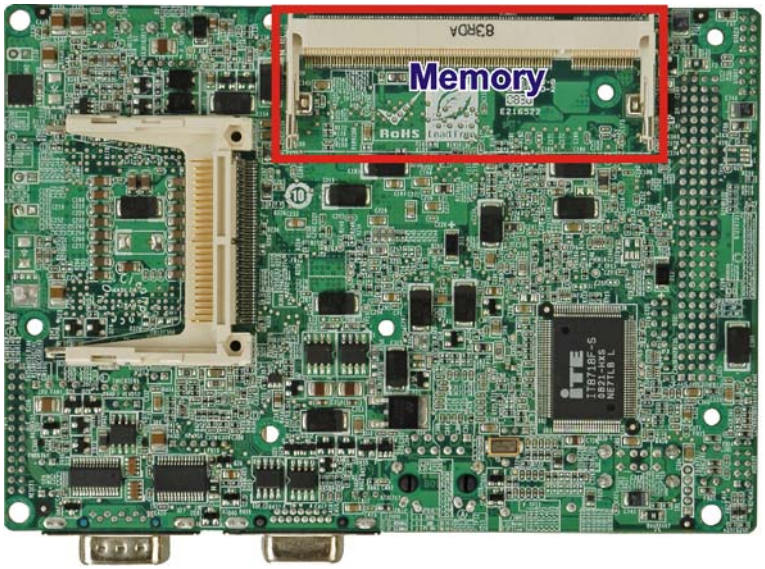


Figure 2-7: 200-pin DDR2 SO-DIMM Socket

2.4.3 Intel® 910GMLEIntegrated Graphics

The Intel® 910GMLE GMCH has a mobile Intel® Graphics Media Accelerator 900 integrated graphics engine and supports the following display devices:

- Analog CRT
- LVDS

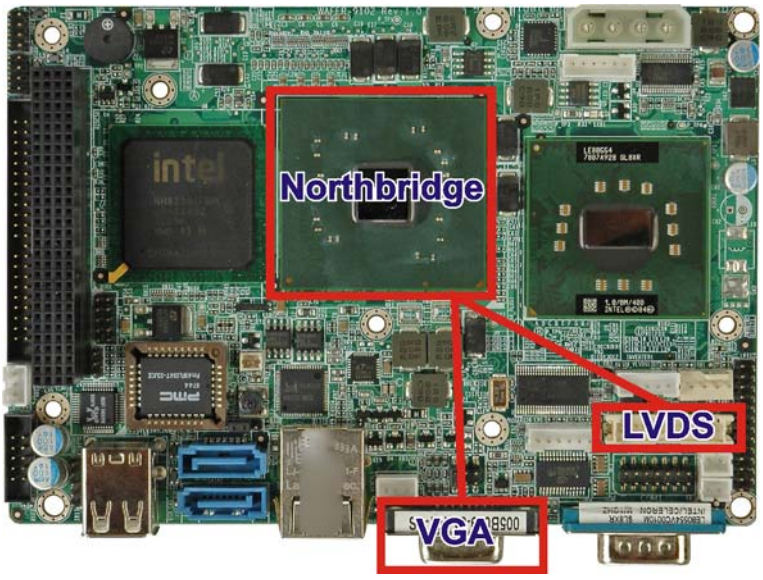


Figure 2-8: Integrated Graphics Interfaces

2.4.3.1 Intel® 910GMLEAnalog CRT Support

A DB-15 VGA connector on the external peripheral interface connector panel is interfaced to the Intel® 910GMLE graphics engine. The Intel® 910GMLE internal graphics engine supports:

- Max DAC frequency up to 400 MHz
- 24-bit RAMDAC
- Analog CRT monitors up to QXGA (2048 x 1536).

2.4.3.2 Intel® 910GMLELVDS Support

A 30-pin LVDS crimp connector is interfaced to the Intel® 910GMLE graphics engine. The Intel® 910GMLE internal graphics engine supports LVDS displays with the following features:

- Compliant with ANSI/TIA/EIA -644-2001 spec
- Integrated dual channel LVDS interface supported on Display Pipe B only
- Supports 25 MHz to 112 MHz single/dual channel LVDS interface
  - Single channel LVDS interface support: 1 x 24-bit
  - Dual channels LVDS interface support: 2 x 24-bit
- TFT panel type supported
- Maximum Panel size supported up to UXGA
- Maximum Wide panel size supported up to WUXGA
- Ambient Light Sense support for automatic backlight brightness adjustments
- Intel Display Power Savings Technology 2.0 support
- Supports Single pipe simultaneous display with the CRT DAC and the LVDS ports under the following conditions:
  - Timings must match for both display
- Panel Fitting. Panning, and Center mode supported
- Spatial Dithering support to emulate up to 16 million colors for 18-bit TFT panels
- Spread spectrum clocking (SSC) supported
  - Supports down and center SSC via an SSC clock from an external SSC clock chip.

- Supports down spread of – 2.5% or center spread of ± -1.25% in reference 30-50 KHz modulation rate

- SSC must be disabled for LVDS port and CRT DAC single pipe simultaneous display mode.
- Panel Power Sequencing support
  - Power down state can be either zero volt or high impedance
- Integrated PWM interface for LCD Backlight Inverter Control
- Up to UXGA monitors with a maximum resolution of 1600 x 1200
- 24-bit 25 MHz to 112 MHz single-channel or dual-channel LVDS screens
- CPIS 1.5 compliant LVDS screens

2.4.4 Intel® 910GMLEDirect Management Interface (DMI)

The Direct Media Interface (DMI) is the communication bus between the Intel® 910GMLE GMCH and the Intel® ICH6M I/O controller hub (ICH). The DMI is a high-speed interface that integrates advanced priority-based servicing and allows for concurrent traffic and true isochronous transfer capabilities. The DMI is shown in **Figure 2-9**.

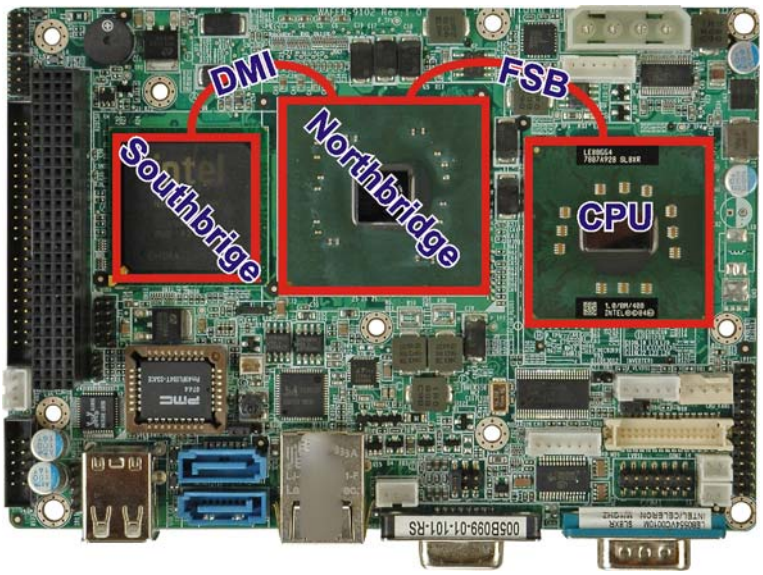


Figure 2-9: DMI Chip-to-Chip Connection

Features of the Intel® 910GMLE DMI are listed below:

- 2.0 GB/s (1.0 GB/s in each direction) bus speed
- Configurable as x2 or x4 DMI lanes

- 32-bit downstream address

2.5 Intel® ICH6M Southbridge Chipset

The Intel® ICH6M Southbridge chipset is connected to the Intel® 910GMLE Northbridge GMCH through the chip-to-chip Direct Media Interface (DMI). Some of the features of the Intel® ICH6M are listed below.

- Complies with PCI Express Base Specification, Revision 1.0a
- Complies with PCI Local Bus Specification, Revision 2.3 and supports 33 MHz PCI operations
- Supports ACPI Power Management Logic
- Contains:
  - Enhanced DMA controller
  - Interrupt controller
  - Timer functions
- Integrated SATA host controller with DMA operations interfaced to two SATA connectors on the WAFER-9102
- Integrated IDE controller supports Ultra ATA 100/66/33
- Supports the four USB 2.0 devices on the WAFER-9102 with four UHCI controllers and one EHCI controller
- Complies with System Management Bus (SMBus) Specification, Version 2.0
- Supports Audio Codec ’97 (AC’97) Revision 2.3 (through suitable CODEC)
- Contains Low Pin Count (LPC) interface
- Supports Firmware Hub (FWH) interface

2.5.1 Audio Codec ’97 Controller

The Audio Codec ’97 (AC’97) controller integrated into the ICH6M complies with AC’97 Component Specification, Version 2.3. The AC’97 controller is interfaced to the onboard audio connector through the Realtek RTL655 audio codec. The audio connector is connected to speakers and a microphone.

2.5.2 IDE Interface

The integrated IDE interface on the ICH6M Southbridge supports two IDE hard disks and ATAPI devices. PIO IDE transfers up to 16 MB/s and Ultra ATA transfers of 100 MB/s. The IDE interface is connected to the following connectors (shown in Figure 2-10):

- CompactFlash® connector
- 44-pin IDE connector

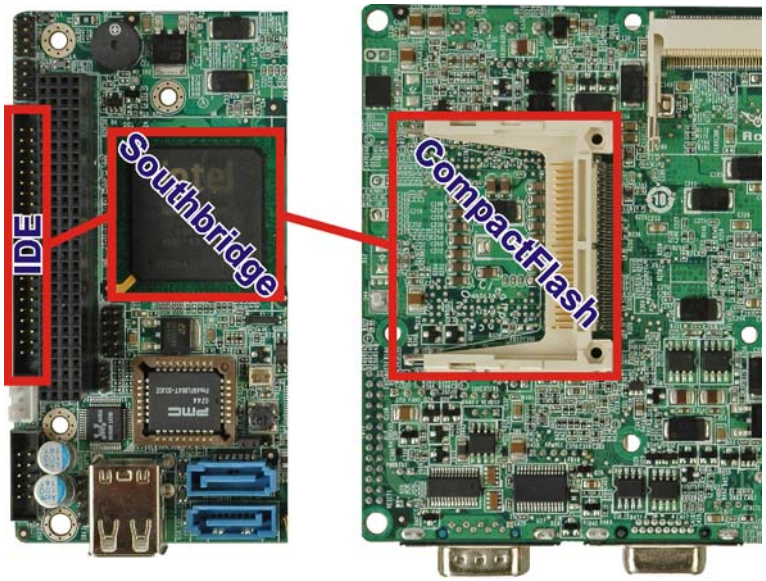


Figure 2-10: IDE Interface

The integrated IDE interface is able to support the following transfer rates:

Specification	Ultra ATA/100	Ultra ATA/66	Ultra ATA/33
IDE devices	2	2	2
PIO Mode	0 – 4	0 – 4	0 – 4
PIO Max Transfer Rate	16.6 MB/s	16.6 MB/s	16.6 MB/s
DMA/UDMA designation	UDMA 5	UDMA 4	UDMA 2
DMA/UDMA Max Transfer	100 MB/s	66 MB/s	33 MB/s
Controller Interface	5 V	5 V	5 V

Table 2-1: Supported HDD Specifications

2.5.3 Low Pin Count (LPC) Interface

The ICH6M LPC interface complies with the LPC 1.1 specifications. The LPC bus from the ICH6M is connected to the following components:

- BIOS chip
- Super I/O chip

2.5.4 PCI Interface

The PCI interface on the ICH6M is compliant with the PCI Revision 2.3 implementation. Some of the features of the PCI interface are listed below.

- PCI Revision 2.3 compliant
- 33 MHz
- 5 V tolerant PCI signals (except PME#)
- Integrated PCI arbiter supports up to seven PCI bus masters

The PCI bus is connected to a PCI-104 connector for adding PCI-104 expansion cards to the WAFER-9102.

2.5.5 Real Time Clock

256 bytes of battery backed RAM is provided by the Motorola MC146818 A real time clock (RTC) integrated into the ICH6M. The RTC operates on a 3 V battery and 32.768 KHz crystal. The RTC keeps track of the time and stores system data even when the system is turned off.

2.5.6 SATA Controller

The integrated SATA controller on the ICH6M Southbridge supports two SATA drives on the WAFER-9102 with independent DMA operations. SATA controller specifications are listed below.

- Supports two SATA drives
- Supports 1.5 Gb/s data transfer speeds
- Supports Serial ATA Specification, Revision 1.0a

2.5.7 USB Controller

Up to six high-speed, full-speed or low-speed USB devices are supported by the ICH6M on the WAFER-9102. High-speed USB 2.0, with data transfers of up to 480 MB/s, is enabled with the ICH6M integrated Enhanced Host Controller Interface (EHCI) compliant host controller. USB full-speed and low-speed signaling is supported by the ICH6M integrated Universal Host Controller Interface (UHCI) controllers.

Four of the USB ports are accessible though pin headers and two are on the external connector panel. See Figure 2-11.

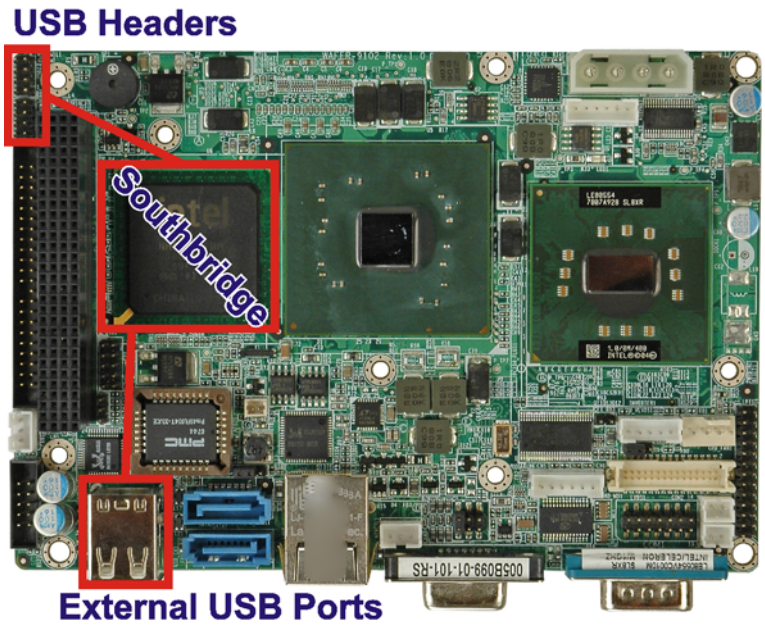


Figure 2-11: Onboard USB Implementation

2.5.8 PCIe Interface

The Intel® ICH6M Southbridge chipset has four PCIe x1 lanes. One PCIe x1 lane is connected to the Realtek RTL8111C PCIe GbE controller.

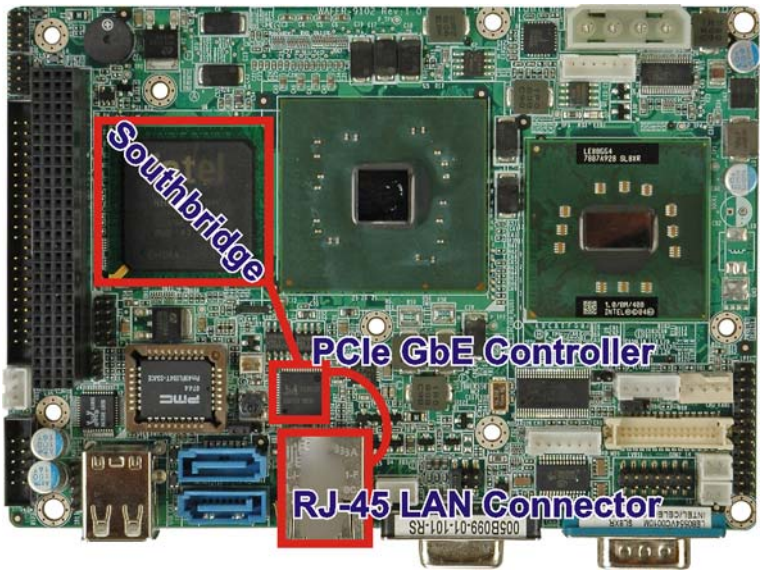


Figure 2-12: Realtek RTL8111C PCIe GbE Controllers

The Realtek RTL8111C PCIe GbE controllers combine a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, 32-bit PCI bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, they offer high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10 Mb/s only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

Some of the features of the Realtek RTL8111C PCIe GbE controllers are listed below.

- Integrated 10/100/1000 transceiver
- Auto-Negotiation with Next Page capability
- Supports PCI rev.2.3, 32-bit, 33/66 MHz
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Wake-on-LAN and remote wake-up support
- Microsoft® NDIS5 Checksum Offload (IP, TCP, UDP) and largesend offload support
- Supports Full Duplex flow control (IEEE 802.3x)
- Fully compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab

- Supports IEEE 802.1P Layer 2 Priority Encoding
- Supports IEEE 802.1Q VLAN tagging
- Serial EEPROM
- 3.3/1.8/1.5 V signaling, 5 V PCI I/O tolerant
- 0.15µm CMOS process
- Transmit/Receive FIFO (8K/64K) support
- Supports power down/link down power saving
- Supports PCI Message Signaled Interrupt (MSI)

2.6 LPC Bus Components

The LPC bus is connected to components listed below:

- BIOS chipset
- Super I/O chipset

The LPC bus connections are shown in **Figure 2-13** below.

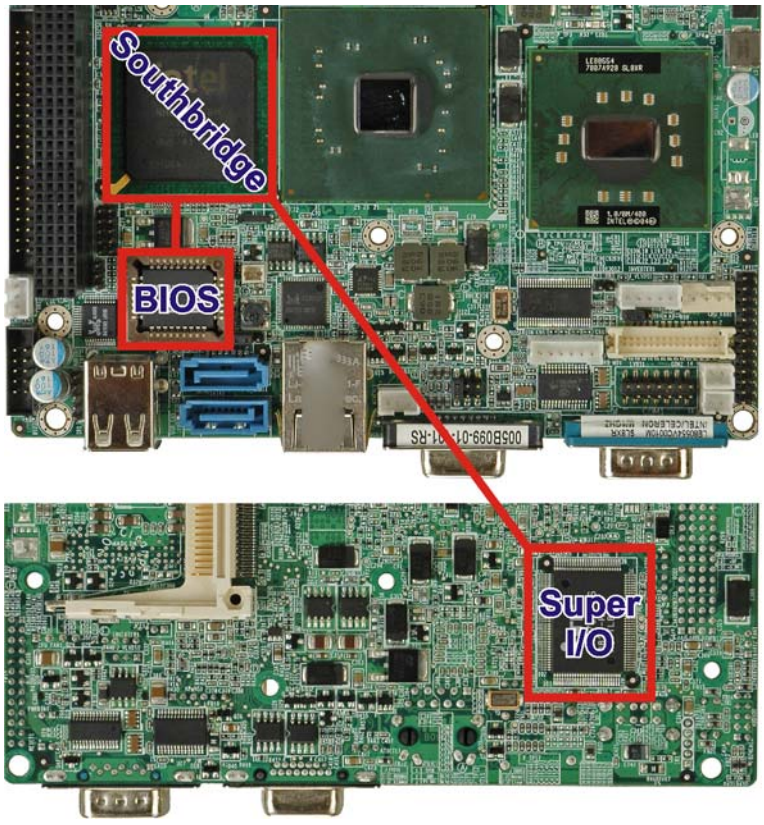


Figure 2-13: LPC Interface

2.6.1 BIOS Chipset

The BIOS chipset has a licensed copy of AMI BIOS installed on the chipset. Some of the BIOS features are listed below:

- AMI Flash BIOS
- SMIBIOS (DMI) compliant
- Console redirection function support
- PXE (Pre-boot Execution Environment) support
- USB booting support

2.6.2 iTE IT8718F Super I/O chipset

The iTE IT8718F Super I/O chipset is connected to the ICH6M Southbridge through the LPC bus. The iTE IT8718F is an LPC interface-based Super I/O device that comes with Environment Controller integration. Some of the features of the iTE IT8718F chipset are listed below:

- ACPI and LANDesk Compliant
- Enhanced Hardware Monitor
- Fan Speed Controller
- Two 16C550 UARTs for serial port control
- One IEEE 1284 Parallel Port
- Keyboard Controller
- Watchdog Timer

Some of the Super I/O features are described in more detail below:

2.6.2.1 LPC Interface

The LPC interface on the Super I/O complies with the Intel® Low Pin Count Specification Rev. 1.0. The LPC interface supports both LDRQ# and SERIRQ protocols as well as PCI PME# interfaces.

2.6.2.2 16C550 UARTs

The onboard Super I/O has two integrated 16C550 UARTs that can support the following:

- Two standard serial ports (COM1 and COM2)
- IrDa 1.0 and ASKIR protocols

2.6.2.3 Digital Input/Output

The input mode supports switch debouncing or programmable external IRQ routing. The output mode supports two sets of programmable LED blinking periods.

2.6.2.4 Enhanced Hardware Monitor

The Super I/O Enhanced Hardware Monitor monitors three thermal inputs, VBAT internally, and eight voltage monitor inputs. These hardware parameters are reported in the BIOS and can be read from the BIOS Hardware Health Configuration menu.

2.6.2.5 Fan Speed Controller

The Super I/O fan speed controller enables the system to monitor the speed of the fan. One of the pins on the fan connector is reserved for fan speed detection and interfaced to the fan speed controller on the Super I/O. The fan speed is then reported in the BIOS.

2.6.2.6 Keyboard/Mouse Controller

The Super I/O keyboard/mouse controller can execute the 8042 instruction set. Some of the keyboard controller features are listed below:

- The 8042 instruction is compatible with a PS/2 keyboard and PS/2 mouse
- Gate A20 and Keyboard reset output
- Supports multiple keyboard power on events
- Supports mouse double-click and/or mouse move power on events

2.6.2.7 Parallel Port

The multi-mode high-performance parallel port supports the bi-directional Standard Parallel Port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP) modes.

2.7 Environmental and Power Specifications

2.7.1 System Monitoring

Thermal inputs on the WAFER-9102 Super I/O monitor the following temperatures:

- CPU temperature
- System temperature

Voltage inputs on the WAFER-9102 Super I/O monitor the following voltages:

- CPU core
- VCC
- +3.30 V
- +5.00 V
- +12.0 V
- +1.5 V
- +1.8 V
- 5 VSB
- VBAT

The WAFER-9102 Super I/O monitors the following fans' speeds:

- CPU fan speed
- System fan speed

The values for the above environmental parameters are all recorded in the BIOS Hardware Health Configuration menu.

2.7.2 Operating Temperature and Temperature Control

The maximum and minimum operating temperatures for the WAFER-9102 are listed below.

- Minimum Operating Temperature: 0ºC (32°F)
- Maximum Operating Temperature: 60°C (140°F)

A cooling fan and heat sink must be installed on the CPU. Thermal paste must be smeared on the lower side of the heat sink before it is mounted on the CPU. Heat sinks

are also mounted on the GMCH and ICH chipsets to ensure the operating temperature of these chips remain low.

2.7.3 Power Consumption

Table 2-2 shows power consumption with a 1.0 GHz Intel® Celeron® M 373 with 1.0 GB DDR2.

Voltage	Current
+5 V	3.11 A
+12 V	0.37 A

Table 2-2: Power Consumption

Table 2-3 shows power consumption with a 1.6 GHz Intel® Pentium® M 725 with 1.0 GB DDR2.

Voltage	Current
+5 V	2.94 A
+12 V	1.57 A

Table 2-3: Power Consumption

Chapter

3

Unpacking

3.1 Anti-static Precautions

WARNING!

Failure to take ESD precautions during the installation of the WAFER-9102 may result in permanent damage to the WAFER-9102 and severe injury to the user.

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the WAFER-9102. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the WAFER-9102, or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- ***Wear an anti-static wristband***: - Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- ***Self-grounding***:- Before handling the board touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- ***Use an anti-static pad***: When configuring the WAFER-9102, place it on an antic-static pad. This reduces the possibility of ESD damaging the WAFER-9102.
- ***Only handle the edges of the PCB***:- When handling the PCB, hold the PCB by the edges.

3.2 Unpacking

3.2.1 Unpacking Precautions

When the WAFER-9102 is unpacked, please do the following:

- Follow the anti-static precautions outlined in **Section 3.1**.
- Make sure the packing box is facing upwards so the WAFER-9102 does not fall out of the box.
- Make sure all the components shown in **Section 3.3** are present.

3.3 Unpacking Checklist

NOTE:

If any of the components listed in the checklist below are missing, do not proceed with the installation. Contact the IEI reseller or vendor the WAFER-9102 was purchased from or contact an IEI sales representative directly by sending an email to sales@iei.com.tw.

3.3.1 Package Contents

The WAFER-9102 is shipped with the following components:

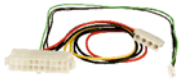
Quantity	Item and Part Number	Image
1	WAFER-9102	
2	SATA cable (P/N: 32000-062800-RS)	
1	KB/MS PS/2 Y-cable (P/N: 32000-023800-RS)	
1	Audio cable (P/N: 32000-072100-RS)	
1	CPU cooler (WAFER-9102-R10 only)	
1	Mini jumper pack (P/N:33100-000033-RS)	

Quantity	Item and Part Number	Image
1	Utility CD	
1	Quick Installation Guide	

Table 3-1: Packing List

3.3.2 Optional Items

The WAFER-9102 is shipped with the following components:

Item and Part Number	Image
Dual USB cable (wo bracket) (**P/N**: 32000-070300-RS)	
RS-232/422/485 cable (**P/N**: 32200-026500-RS)	
LPT cable (wo bracket) (P/N: 32200-015100-RS)	
ATX cable (P/N: 32100-043403)	
HDD cable (P/N: 32200-000009-RS)	
IDE-cable (P/N: 32200-008800)	

Item and Part Number	Image
SATA power cable (P/N: 32100-088600-RS)	

Table 3-2: Power Consumption

Chapter

4

Connectors

4.1 Peripheral Interface Connectors

This chapter outlines all internal and external connectors on the WAFER-9102.

4.1.1 Layout

Figure 4-1 shows the on-board peripheral connectors, rear panel peripheral connectors and on-board jumpers.

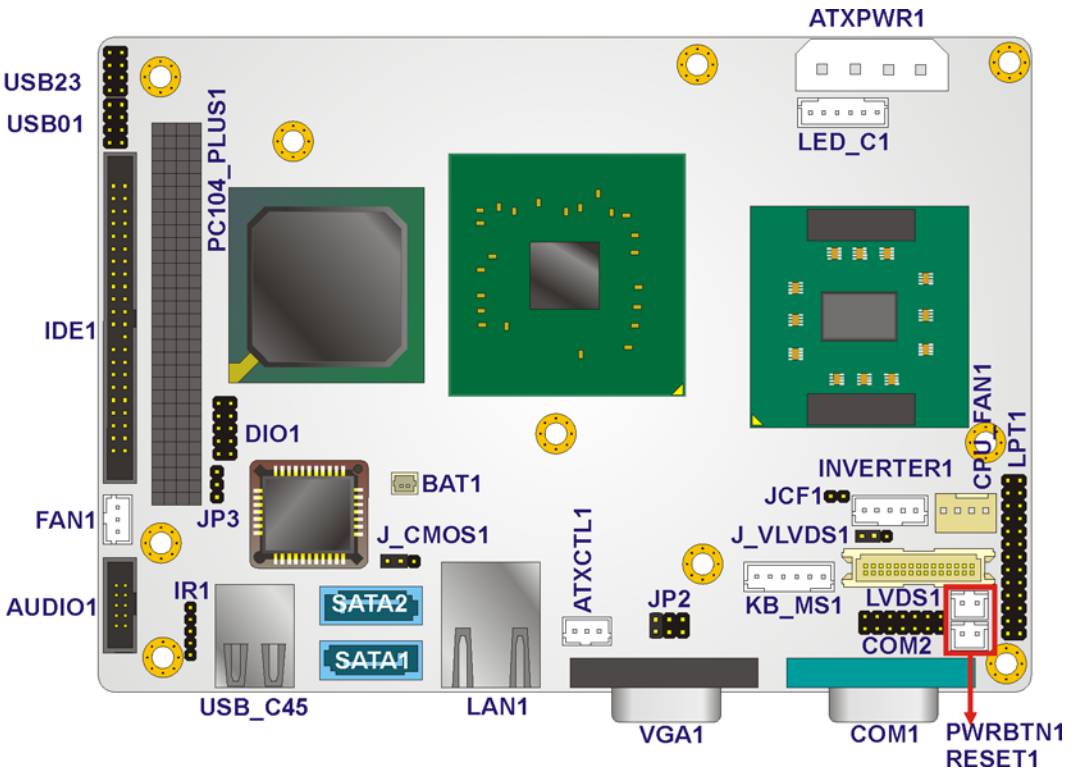


Figure 4-1: Connector and Jumper Locations [Front Side]

Figure 4-2 shows the solder side of the WAFER-9102.

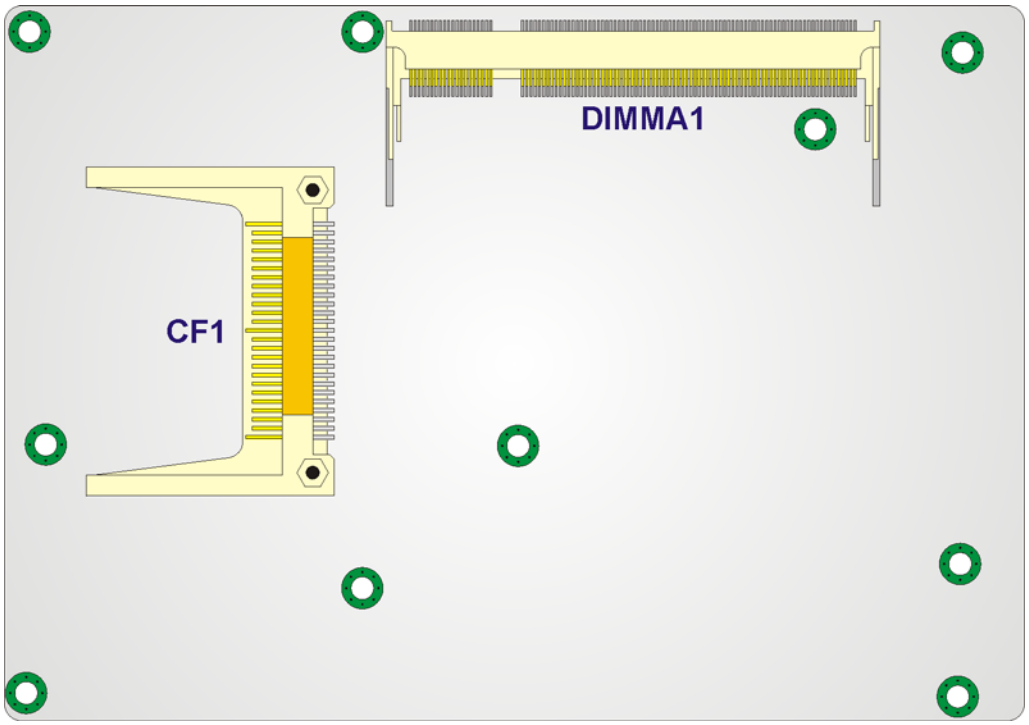


Figure 4-2: Connector and Jumper Locations [Solder Side]

4.2 Peripheral Interface Connectors

Table 4-1 shows a list of the peripheral interface connectors on the WAFER-9102. Detailed descriptions of these connectors can be found below.

Connector	Type	Label
ATX power connector	4-pin power connector	ATXPWR1
ATX power control connector	3-pin wafer	ATXCTL1
Audio connector	10-pin box header	AUDIO1
Backlight inverter connector	5-pin box header	INVERTER1
CompactFlash® slot	CF slot	CF1
CPU fan connector	4-pin wafer	CPU_FAN1
Digital I/O connector	10-pin header	DIO1
IDE connector	44-pin box header	IDE1

Connector	Type	Label
Infrared interface connector	5-pin header	IR1
Keyboard and mouse connector	6-pin box header	KB_MS1
LED indicator connector	6-pin header	LED_C1
LVDS connector	30-pin crimp	LVDS1
Parallel port connector	26-pin header	LPT1
PCI-104 connector	PCI-104 connector	PC104_PLUS1
Power button connector	2-pin box header	PWRBTN1
Reset button connector	2-pin box header	RESET1
SATA port connector	SATA port	SATA1
SATA port connector	SATA port	SATA2
Serial port connector	14-pin header	COM2
System fan connector	3-pin header	FAN1
USB 2.0 connector	8-pin header	USB01
USB 2.0 connector	8-pin header	USB23

Table 4-1: Peripheral Interface Connectors

4.2.1 External Interface Panel Connectors

Table 4-2 lists the rear panel connectors on the WAFER-9102. Detailed descriptions of these connectors can be found in **Section 4.4** on **page 60**.

Connector	Type	Label
LAN connector	RJ-45	LAN1
Serial port	9-pin male	COM1
USB port	Dual USB port	USB_C45
VGA port connector	15-pin female	VGA1

Table 4-2: Rear Panel Connectors

4.3 Internal Peripheral Connectors

Internal peripheral connectors are found on the motherboard and are only accessible when the motherboard is outside of the chassis. This section has complete descriptions of all the internal, peripheral connectors on the WAFER-9102.

4.3.1 ATX Power Source Connector

CN Label:	**ATXPWR1**
CN Type:	4-pin molex connector (1x4)
CN Location:	See **Figure 4-3**
CN Pinouts:	See **Table 4-3**

The 4-pin AT power connector is connected to an AT power supply.

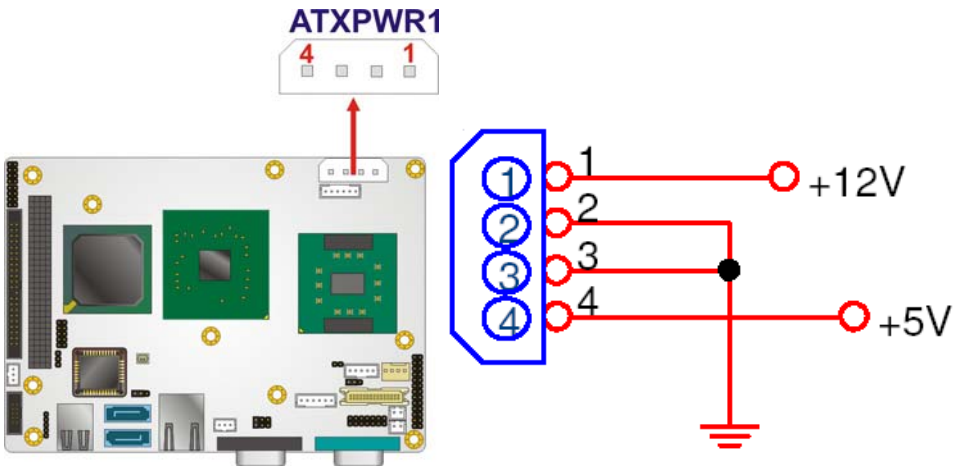


Figure 4-3: AT Power Connector Location

PIN NO.	DESCRIPTION
1	+12 V
2	GND
3	GND
4	+5 V

Table 4-3: AT Power Connector Pinouts

4.3.2 ATX Power Supply Enable Connector

CN Label: **ATXCTL1**

CN Type: 3-pin wafer (1x3)

CN Location: See **Figure 4-4**

CN Pinouts: See **Table 4-4**

The ATX power supply enable connector connects to an ATX power supply and signals the power-on and power-off events.

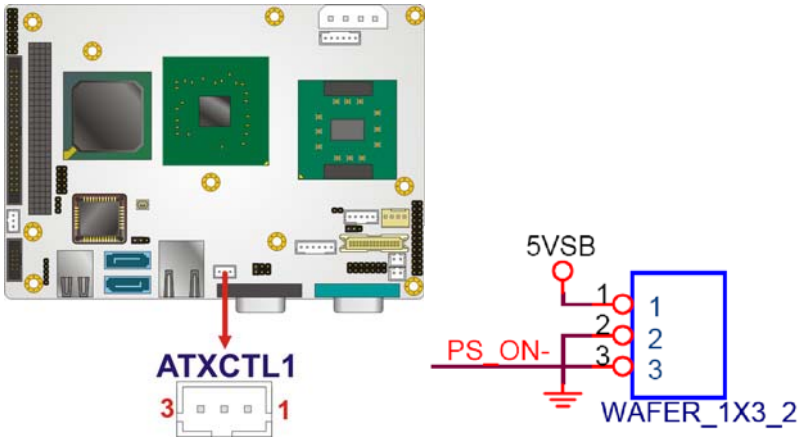


Figure 4-4: ATX Power Supply Enable Connector Location

PIN NO.	DESCRIPTION
1	+5 VSB
2	GND
3	PS_ON#

Table 4-4: ATX Power Supply Enable Connector Pinouts

4.3.3 Audio Kit Connector

CN Label: **AUDIO1**

CN Type: 10-pin header (2x5)

CN Location: See **Figure 4-5**

CN Pinouts: See **Table 4-5**

The 10-pin audio connector can be connected to speakers and a microphone.

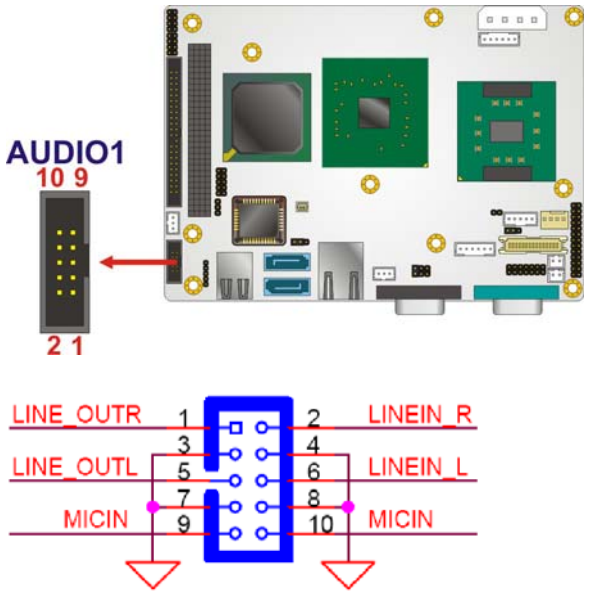


Figure 4-5: Audio Connector Location (9-pin)

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	LINE_OUTR	2	LINEIN_R
3	GND_AUDIO	4	GND_AUDIO
5	LINE_OUTL	6	LINEIN_L
7	GND_AUDIO	8	GND_AUDIO
9	MICIN	10	MICIN

Table 4-5: Audio Connector Pinouts

4.3.4 CompactFlash® Socket

CN Label: **CF1**

CN Type: 50-pin header (2x25)

CN Location: See **Figure 4-6**

CN Pinouts: See **Table 4-6**

The CompactFlash® card slot allows a CompactFlash® type I or II card to be installed.

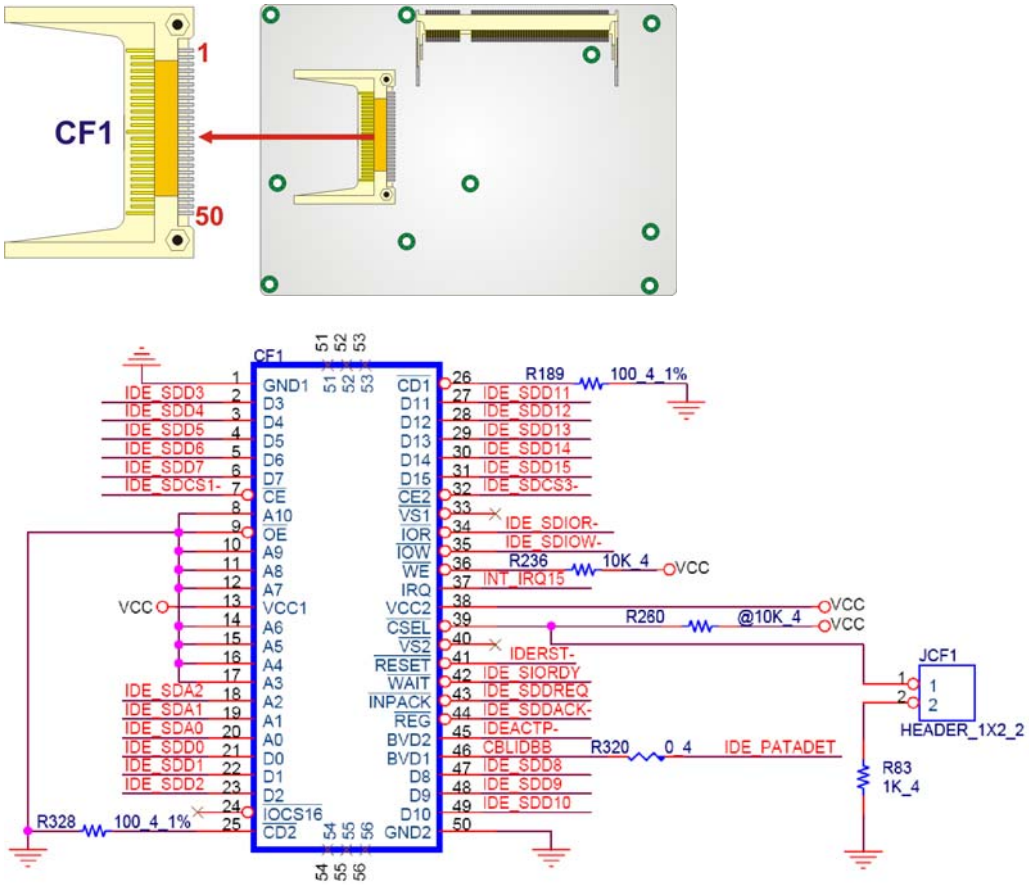


Figure 4-6: CF Card Socket Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GROUND	26	CD1#
2	DATA 3	27	DATA 11
3	DATA 4	28	DATA 12
4	DATA 5	29	DATA 13
5	DATA 6	30	DATA 14
6	DATA 7	31	DATA 15
7	CE#	32	CE2#
8	A10	33	VS1#
9	OE#	34	IOR#
10	A9	35	IOW#
11	A8	36	WE#
12	A7	37	IRQ

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
13	VCC	38	VCC
14	A6	39	CSEL#
15	A5	40	VS2#
16	A4	41	RESET#
17	A3	42	WAIT#
18	A2	43	INPACK#
19	A1	44	REG#
20	A0	45	BVD2
21	DATA 0	46	BVD1
22	DATA 1	47	DATA 8
23	DATA 2	48	DATA 9
24	IOCS16#	49	DATA 10
25	CD2#	50	GND2

Table 4-6: CF Card Socket Pinouts

4.3.5 CPU Fan Connector

CN Label: **CPU_FAN1**

CN Type: 4-pin wafer

CN Location: See **Figure 4-7**

CN Pinouts: See **Table 4-7**

This connector connects to a CPU cooling fan. The connector has a "rotation" pin to get rotation signals from fans and notify the system so the system BIOS can recognize the fan speed. Please note that only specified fans can issue the rotation signals.

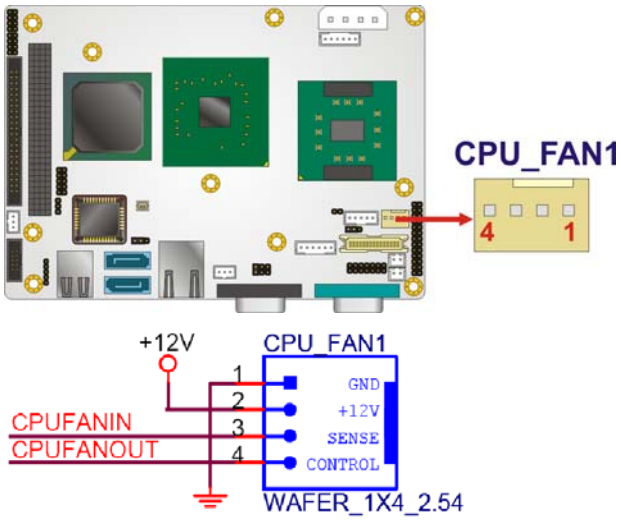


Figure 4-7: CPU Fan Connector Location

PIN NO.	DESCRIPTION
1	GND
2	+12 VCC
3	Rotation Signal
4	Control

Table 4-7: CPU Fan Connector Pinouts

4.3.6 Digital I/O Connector

CN Label: **DIO1**

CN Type: 10-pin header (2x5)

CN Location: See **Figure 4-8**

CN Pinouts: See **Table 4-8**

The digital input/output connector is managed through a Super I/O chip. The DIO connector pins are user programmable.

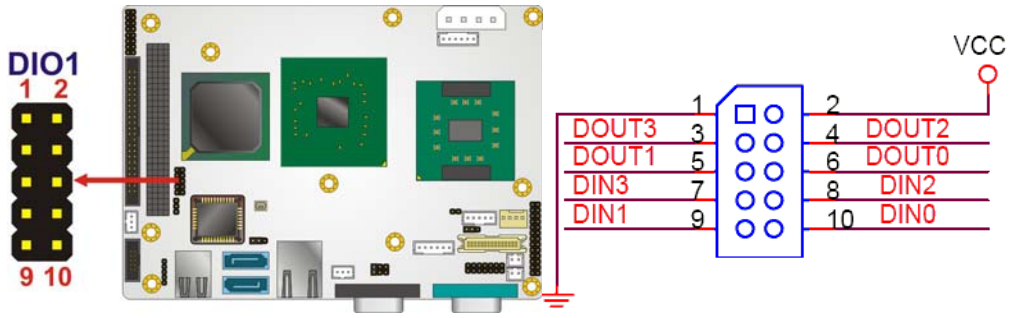


Figure 4-8: Digital I/O Connector Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	VCC
3	Output 3	4	Output 2
5	Output 1	6	Output 0
7	Input 3	8	Input 2
9	Input 1	10	Input 0

Table 4-8: DIO Connector Pinouts

4.3.7 IDE Connector

CN Label: **IDE1**

CN Type: 44-pin header (2x22)

CN Location: See **Figure 4-9**

CN Pinouts: See **Table 4-9**

One 44-pin IDE device connector on the WAFER-9102 supports connectivity to two hard disk drives.

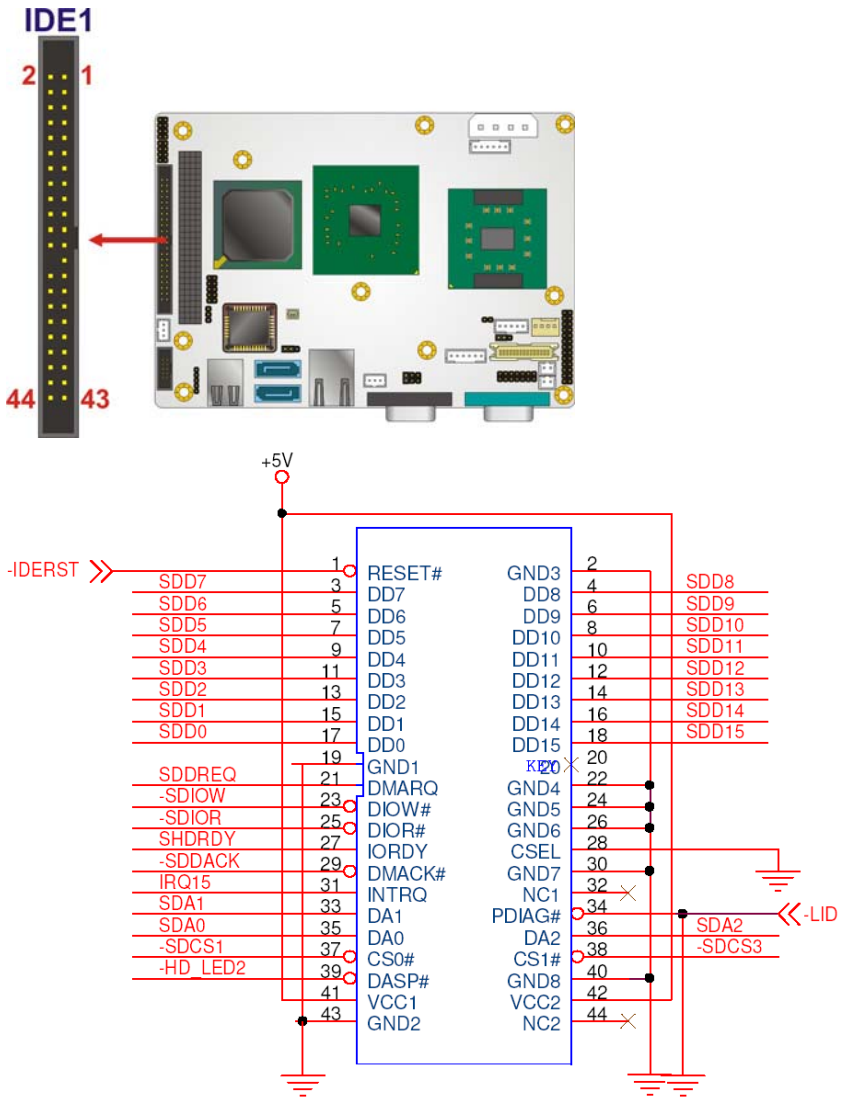


Figure 4-9: IDE Device Connector Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	RESET#	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
17	DATA 0	18	DATA 15
19	GROUND	20	N/C
21	IDE DRQ	22	GROUND
23	IOW#	24	GROUND
25	IOR#	26	GROUND
27	IDE CHRDY	28	BALE-DEFAULT
29	IDE DACK	30	GROUND
31	INTERRUPT	32	N/C
33	SA1	34	PDIAG#
35	SA0	36	SA2
37	HDC CS0#	38	HDC CS1#
39	HDD ACTIVE#	40	GROUND
41	VCC	42	VCC
43	GND	44	N/C

Table 4-9: IDE Connector Pinouts

4.3.8 Infrared Interface Connector

CN Label: **IR1**

CN Type: 5-pin header (1x5)

CN Location: See **Figure 4-10**

CN Pinouts: See **Table 4-10**

The infrared interface connector supports both Serial Infrared (SIR) and Amplitude Shift Key Infrared (ASKIR) interfaces.

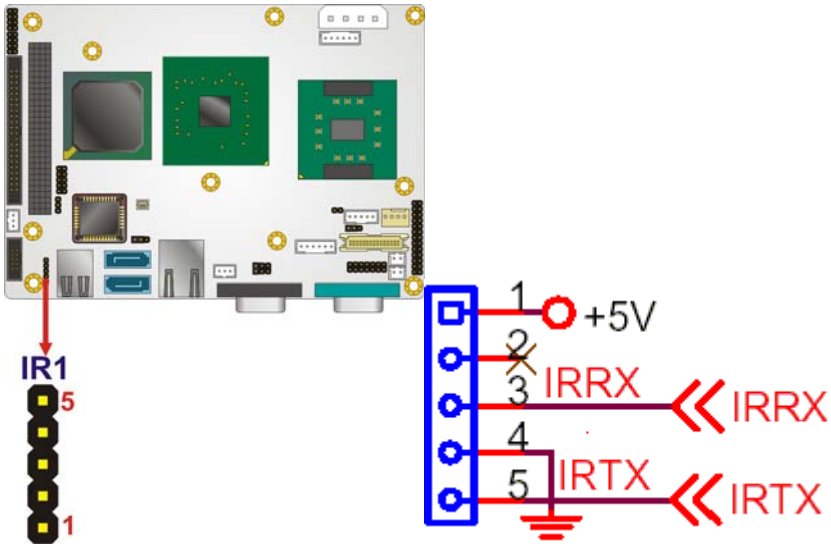


Figure 4-10: Infrared Connector Pinout Locations

PIN NO.	DESCRIPTION
1	VCC
2	NC
3	IR-RX
4	GND
5	IR-TX

Table 4-10: Infrared Connector Pinouts

4.3.9 Keyboard and Mouse Connector

CN Label: **KB_MS1**

CN Type: 6-pin header (1x6)

CN Location: See **Figure 4-11**

CN Pinouts: See **Table 4-11**

The keyboard and mouse connector is connected to a PS/2 mouse and PS/2 keyboard using the included cable.

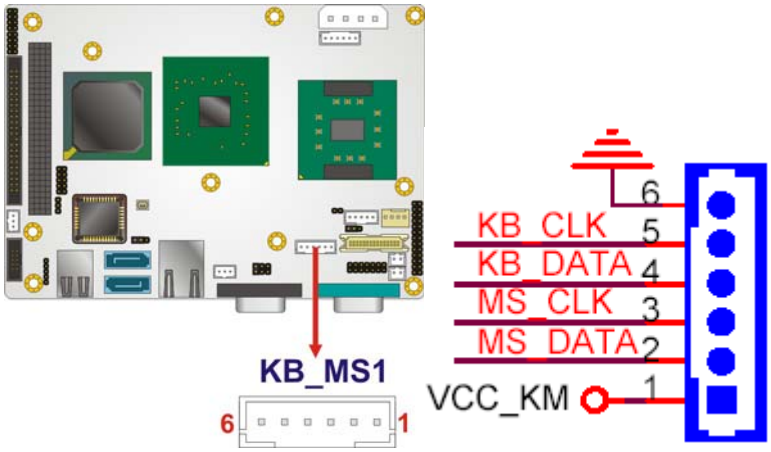


Figure 4-11: Keyboard and Mouse Connector Location

PIN NO.	DESCRIPTION
1	VCC
2	Mouse Data
3	Mouse Clock
4	Keyboard Data
5	Keyboard Clock
6	GND

Table 4-11: Keyboard and Mouse Connector Pinouts

4.3.10 LED Connector

CN Label: **LED_C1**

CN Type: 6-pin wafer (1x6)

CN Location: See **Figure 4-12**

CN Pinouts: See **Table 4-12**

The LED connector connects to an HDD indicator LED and a power LED on the system chassis to inform the user about HDD activity and the power on/off status of the system.

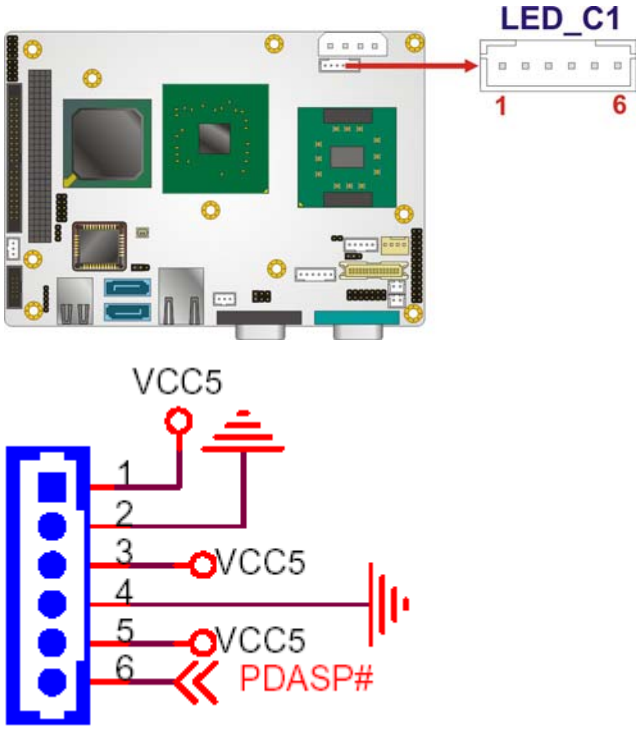


Figure 4-12: LED Connector Locations

PIN NO.	DESCRIPTION
1	+5 V
2	GND
3	Power LED+
4	Power LED-
5	HDD LED+
6	HDD LED-

Table 4-12: LED Connector Pinouts

4.3.11 LCD Backlight Inverter Connector

CN Label: **INVERTER1**

CN Type: 5-pin wafer (1x5)

CN Location: See **Figure 4-13**

CN Pinouts: See **Table 4-13**

The backlight inverter connector provides the backlight of the connected LCD display with +12 V of power.

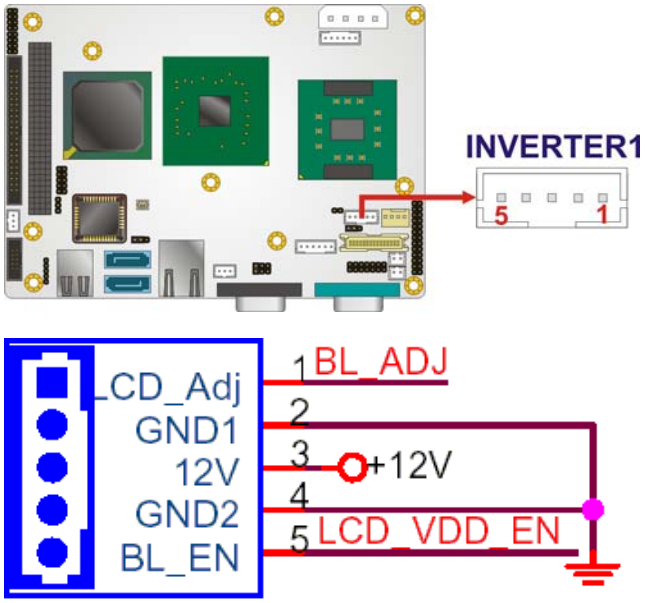


Figure 4-13: Panel Backlight Connector Pinout Locations

PIN NO.	DESCRIPTION
1	LCD_BKLTCTL
2	GND
3	12 V
4	GND
5	BACKLIGHT ENABLE

Table 4-13: Panel Backlight Connector Pinouts

4.3.12 LCD LVDS Connector

CN Label: **LVDS1**

CN Type: 20-pin crimp (2x10)

CN Location: See **Figure 4-14**

CN Pinouts: See **Table 4-14**

The 20-pin TFT LCD LVDS can be connected to a TFT LCD screen directly.

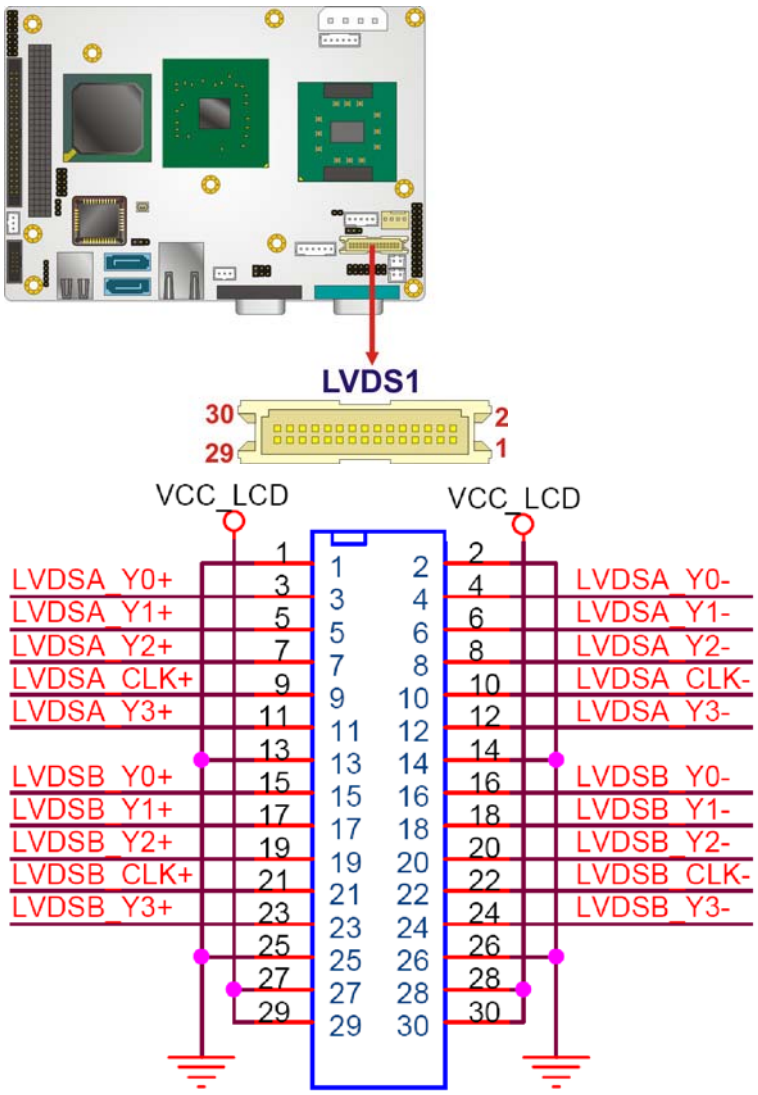


Figure 4-14: TFT LCD LVDS Connector Pinout Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND1	2	GND2
3	A_Y0	4	A_Y0#
5	A_Y1	6	A_Y1#
7	A_Y2	8	A_Y2#
9	A_CK	10	A_CK#
11	A_Y3	12	A_Y3#
13	GND3	14	GND4
15	B_Y0	16	B_Y0#

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
17	B_Y1	18	B_Y1#
19	B_Y2	20	B_Y2#
21	B_CK	22	B_CK#
23	B_Y3	24	B_Y3#
25	GND5	26	GND6
27	VCC_LCD	28	VCC_LCD
29	VCC_LCD	30	VCC_LCD

Table 4-14: TFT LCD LVDS Port Connector Pinouts

4.3.13 Parallel Port Connector

CN Label: **LPT1**

CN Type: 26-pin box header

CN Location: See **Figure 4-15**

CN Pinouts: See **Table 4-15**

The 26-pin parallel port connector connects to a parallel port connector interface or some other parallel port device such as a printer.

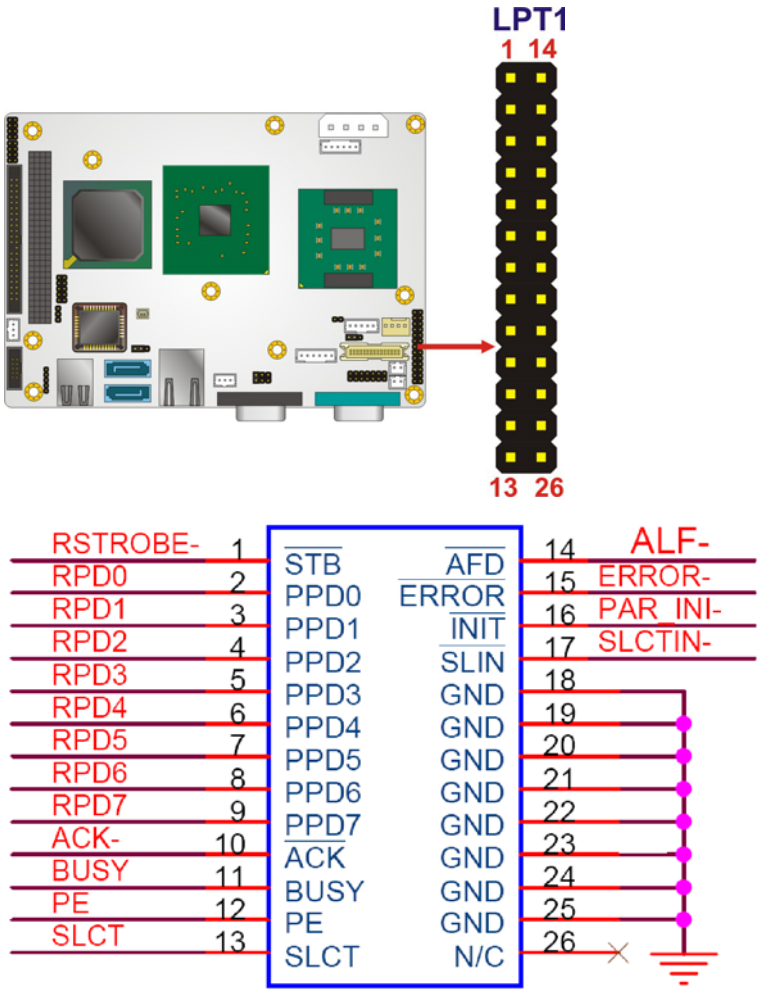


Figure 4-15: Parallel Port Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	STROBE#	14	AUTO FORM FEED #
2	DATA 0	15	ERROR#
3	DATA 1	16	INITIALIZE#
4	DATA 2	17	PRINTER SELECT LN#
5	DATA 3	18	GROUND
6	DATA 4	19	GROUND
7	DATA 5	20	GROUND
8	DATA 6	21	GROUND
9	DATA 7	22	GROUND
10	ACKNOWLEDGE#	23	GROUND

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
11	BUSY	24	GROUND
12	PAPER EMPTY	25	GROUND
13	PRINTER SELECT	26	NC

Table 4-15: Parallel Port Connector Pinouts

4.3.14 PCI-104 Slot

CN Label: **PC104_PLUS1**

CN Type: 120-pin PCI-104 slot

CN Location: See **Figure 4-16**

CN Pinouts: See **Table 4-16**

The PCI-104 slot enables a PCI-104 compatible expansion module to be connected to the board.

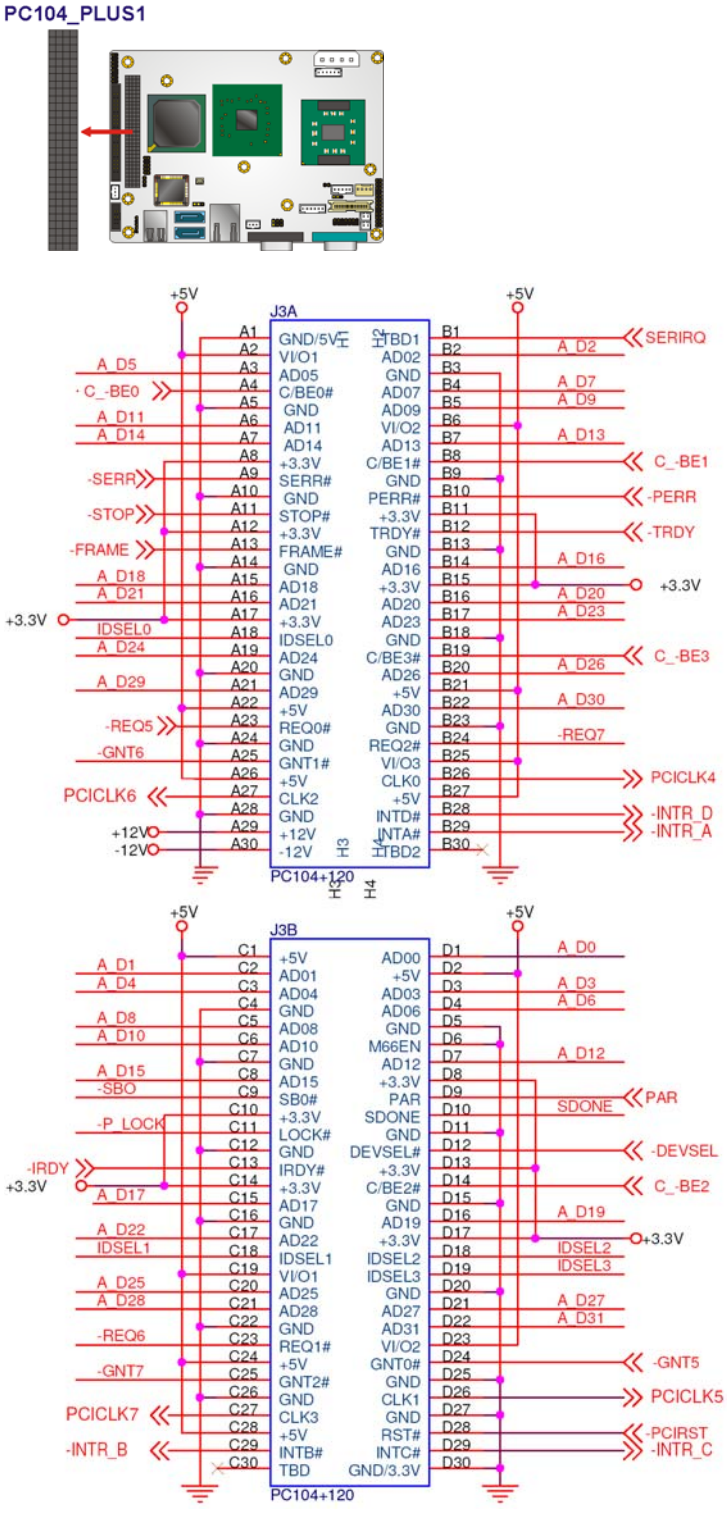


Figure 4-16: PCI-104 Slot Location

Pin No.	Column A	Column B	Column C	Column D
1	GND/5 V	TBD1	5 V	AD00
2	VI/O1	AD02	AD01	+5 V
3	AD05	GND	AD04	AD03
4	C/BE0#	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O2	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3 V	C/BE1#	AD15	+3.3 V
9	SERR#	GND	SB0#	PAR
10	GND	PERR#	+3.3 V	SDONE
11	STOP#	+3.3 V	LOCK#	GND
12	+3.3 V	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	+3.3 V
14	GND	AD16	+3.3 V	C/BE2#
15	AD18	+3.3 V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3 V	AD23	AD22	+3.3 V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	VI/O1	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5 V	AD28	AD27
22	+5 V	AD30	GND	AD31
23	REQ0#	GND	REQ1#	VI/O2
24	GND	REQ2#	+5 V	GNT0#
25	GNT1#	VI/O3	GNT2#	GND
26	+5 V	CLK0	GND	CLK1
27	CLK2	+5 V	CLK3	GND
28	GND	INTD#	+5 V	RST#
29	+12 V	INTA#	INTB#	INTC#

Pin No.	Column A	Column B	Column C	Column D
30	-12 V	TBD2	TBD	GND/3.3 V

Table 4-16: PCI-104 Slot Connector Pinouts

4.3.15 Power Button Connector

CN Label: **PWRBTN1**

CN Type: 2-pin wafer (1x2)

CN Location: See **Figure 4-17**

CN Pinouts: See **Table 4-17**

The power button connector is connected to a power switch on the system chassis to enable users to turn the system on and off.

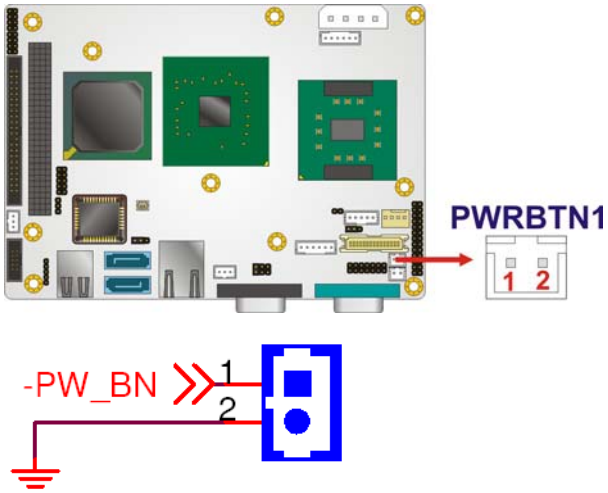


Figure 4-17: Power Button Connector Location

PIN NO.	DESCRIPTION
1	Power Switch
2	GND

Table 4-17: Power Button Connector Pinouts

4.3.16 Reset Button Connector

CN Label:	**RESET1**
CN Type:	2-pin wafer (1x2)
CN Location:	See **Figure 4-18**
CN Pinouts:	See **Table 4-18**

The reset button connector is connected to a reset switch on the system chassis to enable users to reboot the system when the system is turned on.

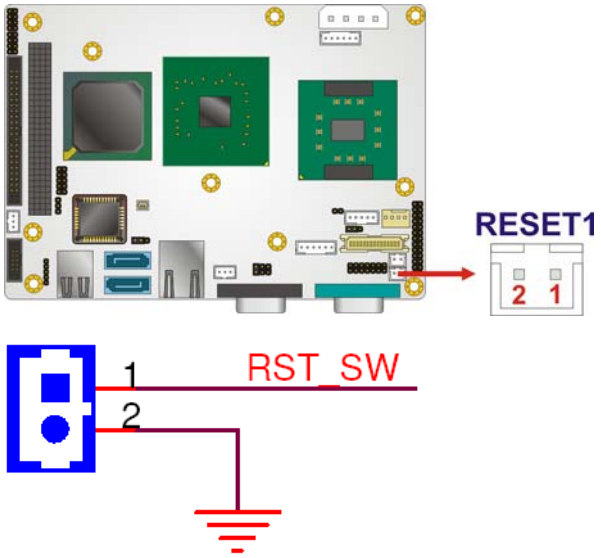


Figure 4-18: Reset Button Connector Locations

PIN NO.	DESCRIPTION
1	Reset Switch
2	GND

Table 4-18: Reset Button Connector Pinouts

4.3.17 SATA Drive Connectors

CN Label:	**SATA1, SATA2**
CN Type:	7-pin SATA drive connectors
CN Location:	See **Figure 4-19**

CN Pinouts: See **Table 4-19**

The four SATA drive connectors are each connected to a first generation SATA drive. First generation SATA drives transfer data at speeds as high as 150 Mb/s. The SATA drives can be configured in a RAID configuration.

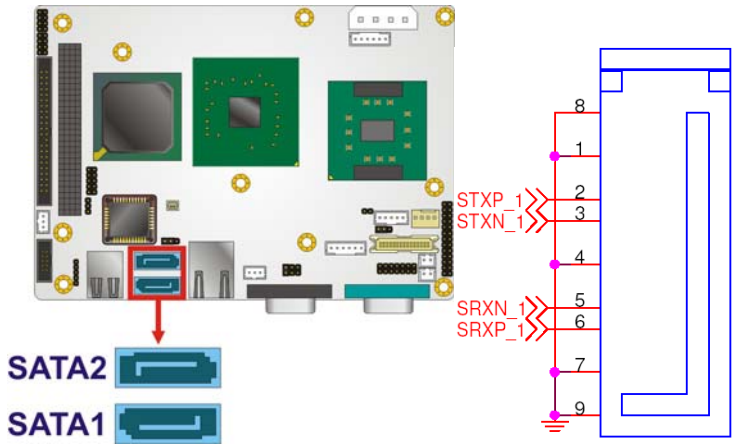


Figure 4-19: SATA Drive Connector Locations

PIN NO.	DESCRIPTION
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

Table 4-19: SATA Drive Connector Pinouts

4.3.18 Serial Port Connector

CN Label: **COM2**

CN Type: 14-pin header (2x5)

CN Location: See **Figure 4-20**

CN Pinouts: See **Table 4-20**

The 14-pin serial port connector provides RS-232, RS-422 and RS-485 communications.

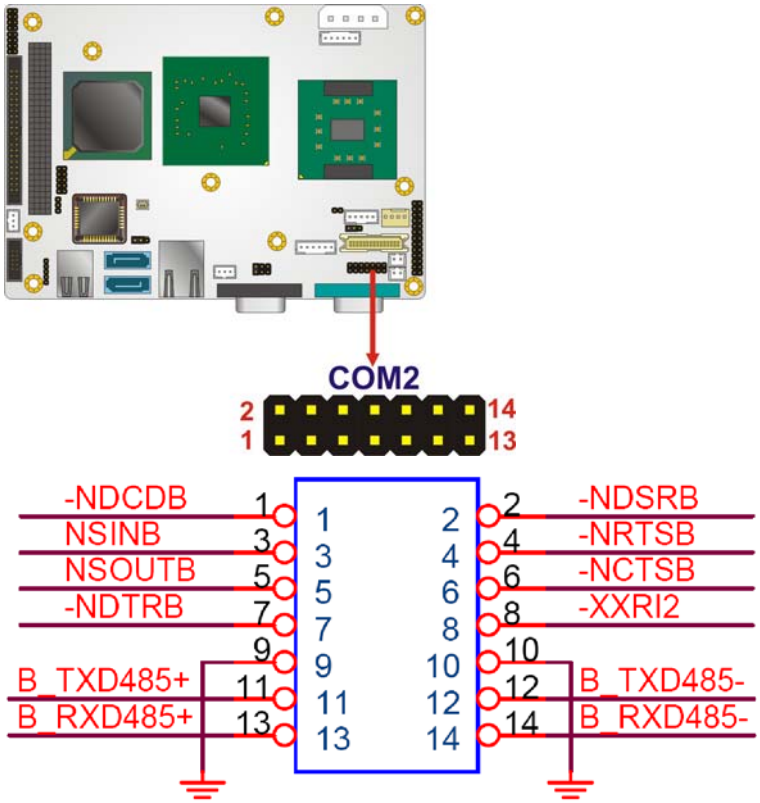


Figure 4-20: COM Connector Pinout Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	Data Carrier Direct (DCD)	2	Data Set Ready (DSR)
3	Receive Data (RXD)	4	Request To Send (RTS)
5	Transmit Data (TXD)	6	Clear To Send (CTS)
7	Data Terminal Ready (DTR)	8	Ring Indicator (RI)
9	Ground (GND)	10	Ground (GND)
11	TXD485+	12	TXD485-
13	RXD485+	14	RXD485-

Table 4-20: COM Connector Pinouts

4.3.19 System Fan Connector

CN Label: **FAN1**

CN Type: 3-pin wafer

CN Location: See **Figure 4-21**

CN Pinouts: See **Table 4-21**

The cooling fan connector provides 5 V to the cooling fan. The connector has a "rotation" pin to get rotation signals from fans and notify the system so the system BIOS can recognize the fan speed. Please note that only specified fans can issue the rotation signals.

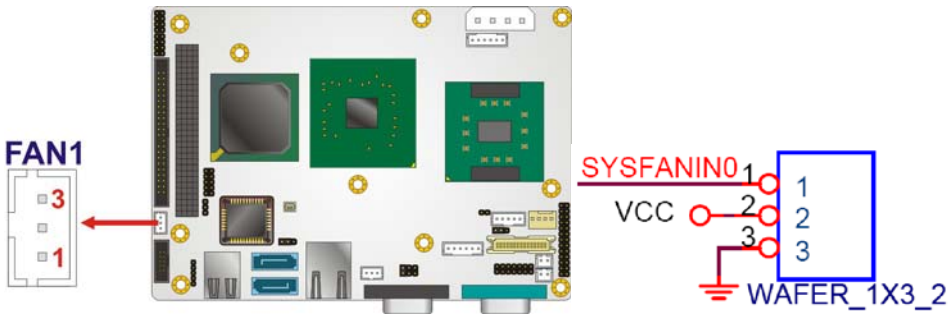


Figure 4-21: System Fan Connector Location

PIN NO.	DESCRIPTION
1	SYSFANIN
2	VCC
3	GND

Table 4-21: System Fan Connector Pinouts

4.3.20 USB Connectors

CN Label: **USB01 and USB23**

CN Type: 8-pin header (2x4)

CN Location: See **Figure 4-22**

CN Pinouts: See **Table 4-22**

The 2x4 USB pin connectors each provide connectivity to two USB 1.1 or two USB 2.0 ports. Each USB connector can support two USB devices. Additional external USB ports are found on the rear panel. The USB ports are used for I/O bus expansion.

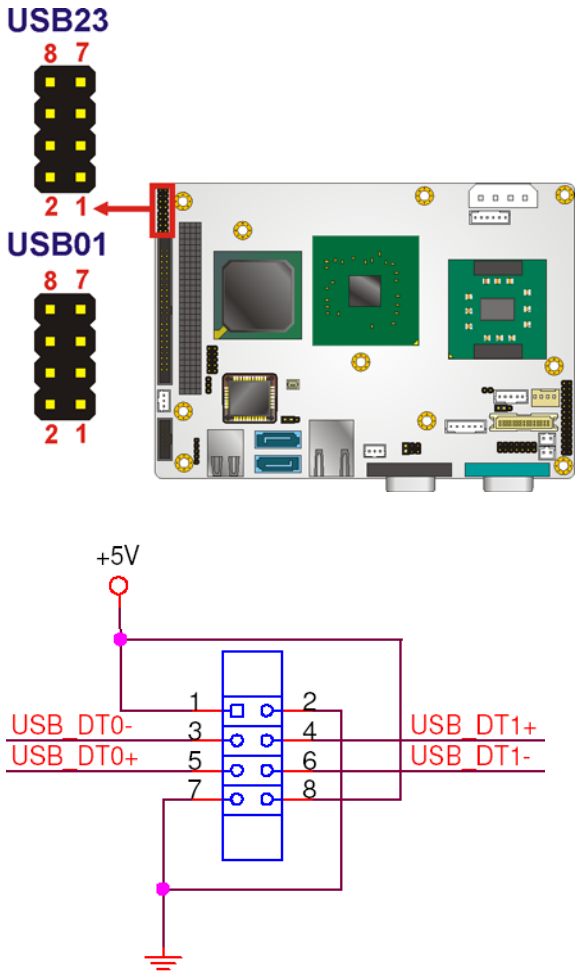


Figure 4-22: USB Connector Pinout Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	VCC	2	GND
3	DATA-	4	DATA+
5	DATA+	6	DATA-
7	GND	8	VCC

Table 4-22: USB Port Connector Pinouts

4.4 External Peripheral Interface Connector Panel

Figure 4-23 shows the WAFER-9102 external peripheral interface connector (EPIC) panel. The WAFER-9102 EPIC panel consists of the following:

- 1 x RJ-45 LAN connectors
- 1 x Serial port connectors
- 2 x USB connectors
- 1 x VGA connector

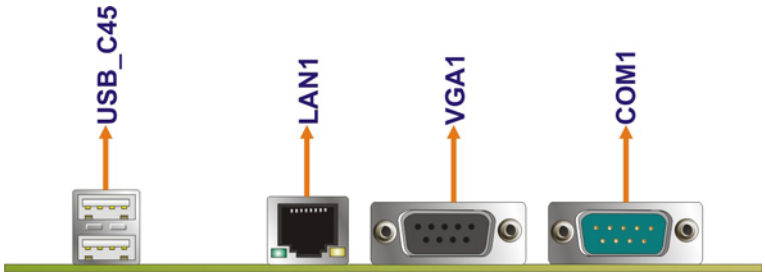


Figure 4-23: WAFER-9102 External Peripheral Interface Connector

4.4.1 Serial Port Connector

CN Label: **COM1**

CN Type: DB-9 connector

CN Location: See **Figure 4-23**

CN Pinouts: See **Table 4-23** and **Figure 4-24**

The 9-pin DB-9 COM1 serial port connector is connected to RS-232 serial communications devices.

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	Data Carrier Detect(DCD)	6	Data Set Ready (DSR)
2	Receive Data (RXD)	7	Request To Send (RTS)
3	Transmit Data (TXD)	8	Clear To Send (CTS)
4	Data Terminal Ready (DTR)	9	Ring Indicator (RI)
5	Ground (GND)		

Table 4-23: RS-232 Serial Port (COM 1) Pinouts

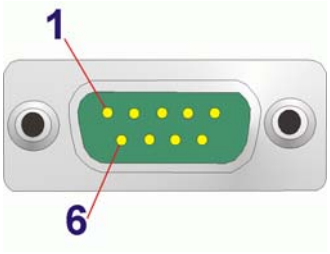


Figure 4-24: COM1 Pinout Locations

4.4.2 LAN Connectors

CN Label: **LAN1 & LAN2**

CN Type: RJ-45

CN Location: See **Figure 4-23**

CN Pinouts: See **Table 4-24**

The WAFER-9102 is equipped with two built-in RJ-45 Ethernet controllers. The controllers can connect to the LAN through two RJ-45 LAN connectors. There are two LEDs on the connector indicating the status of LAN. The pin assignments are listed in the following table:

PIN	DESCRIPTION	PIN	DESCRIPTION
1	MDIA3-	5	MDIA1+
2	MDIA3+	6	MDIA2+
3	MDIA2-	7	MDIA0-
4	MDIA1-	8	MDIA0+

Table 4-24: LAN Pinouts

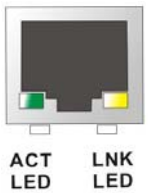


Figure 4-25: RJ-45 Ethernet Connector

The RJ-45 Ethernet connector has two status LEDs, one green and one yellow. The green LED indicates activity on the port and the yellow LED indicates the port is linked. See **Table 4-25**.

STATUS	DESCRIPTION	STATUS	DESCRIPTION
GREEN	Activity	YELLOW	Linked

Table 4-25: RJ-45 Ethernet Connector LEDs

4.4.3 USB Connectors

CN Label: **USB_C1**

CN Type: USB port

CN Location: See **Figure 4-23**

CN Pinouts: See **Table 4-26**

The WAFER-9102 has one external USB 2.0 port. The ports connect to both USB 2.0 and USB 1.1 devices.

PIN	DESCRIPTION	PIN	DESCRIPTION
1	VCC	5	VCC
2	DATA-	6	DATA-
3	DATA+	7	DATA+
4	Ground	8	Ground

Table 4-26: USB Port Pinouts

4.4.4 VGA Connector

CN Label: **VGA1**

CN Type: 15-pin Female

CN Location: See **Figure 4-23**

CN Pinouts: See **Figure 4-26** and **Table 4-27**

The WAFER-9102 has a single 15-pin female connector for connectivity to standard display devices.

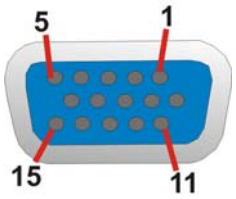


Figure 4-26: VGA Connector

PIN	DESCRIPTION	PIN	DESCRIPTION
1	RED	2	GREEN
3	BLUE	4	NC
5	GND	6	CRT_PLUG-
7	GND	8	GND
9	VCC	10	GND
11	NC	12	DDC DAT
13	HSYNC	14	VSYNC
15	DDCCLK		

Table 4-27: VGA Connector Pinouts

Chapter

5

Installation

5.1 Anti-static Precautions

WARNING:

Failure to take ESD precautions during the installation of the WAFER-9102 may result in permanent damage to the WAFER-9102 and severe injury to the user.

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the WAFER-9102. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the WAFER-9102, or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- ***Wear an anti-static wristband***: - Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- ***Self-grounding***:- Before handling the board touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- ***Use an anti-static pad***: When configuring the WAFER-9102, place it on an antic-static pad. This reduces the possibility of ESD damaging the WAFER-9102.
- ***Only handle the edges of the PCB***:-: When handling the PCB, hold the PCB by the edges.

5.2 Installation Considerations

NOTE:

The following installation notices and installation considerations should be read and understood before the WAFER-9102 is installed. All installation notices pertaining to the installation of the WAFER-9102 should be strictly adhered to. Failing to adhere to these precautions may lead to severe damage of the WAFER-9102 and injury to the person installing the motherboard.

5.2.1 Installation Notices

WARNING:

The installation instructions described in this manual should be carefully followed in order to prevent damage to the WAFER-9102, WAFER-9102 components and injury to the user.

Before and during the installation please **DO** the following:

- Read the user manual:
  - The user manual provides a complete description of the WAFER-9102 installation instructions and configuration options.
- Wear an electrostatic discharge cuff (ESD):
  - Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the body and helps prevent ESD damage.
- Place the WAFER-9102 on an antistatic pad:
  - When installing or configuring the motherboard, place it on an antistatic pad. This helps to prevent potential ESD damage.
- Turn all power to the WAFER-9102 off:
  - When working with the WAFER-9102, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

Before and during the installation of the WAFER-9102 **DO NOT:**

- **DO NOT** remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- **DO NOT** use the product before verifying all the cables and power connectors are properly connected.
- **DO NOT** allow screws to come in contact with the PCB circuit, connector pins, or its components.

5.2.2 Installation Checklist

The following checklist is provided to ensure the WAFER-9102 is properly installed.

- All the items in the packing list are present
- A compatible memory module is properly inserted into the slot
- The CF Type I or CF Type II card is properly installed into the CF socket
- The jumpers have been properly configured
- The WAFER-9102 is inserted into a chassis with adequate ventilation
- The correct power supply is being used
- The following devices are properly connected
  - Primary and secondary IDE device
  - SATA drives
  - Power supply
  - USB cable
  - Serial port cable
- The following external peripheral devices are properly connected to the chassis:
  - VGA screen
  - Keyboard
  - Mouse
  - RS-232 serial communications device
  - USB devices

5.3 Unpacking

When the WAFER-9102 is unpacked, please check all the unpacking list items listed in Chapter 3 are indeed present. If any of the unpacking list items are not available please

contact the WAFER-9102 vendor reseller/vendor where the WAFER-9102 was purchased or contact an IEI sales representative.

5.3.1 Socket 479 CPU Installation (WAFER-9102-R10)

WARNING:

CPUs are expensive and sensitive components. When installing the CPU please be careful not to damage it in anyway. Make sure the CPU is installed properly and ensure the correct cooling kit is properly installed.

To install a socket 479 CPU onto the WAFER-9102, follow the steps below:

WARNING:

When handling the CPU, only hold it on the sides. DO NOT touch the pins at the bottom of the CPU.

Step 1: **Unlock the CPU retention screw.** When shipped, the retention screw of the CPU socket should be in the unlocked position. If it is not in the unlocked position, use a screwdriver to unlock the screw. See **Figure 5-1**.

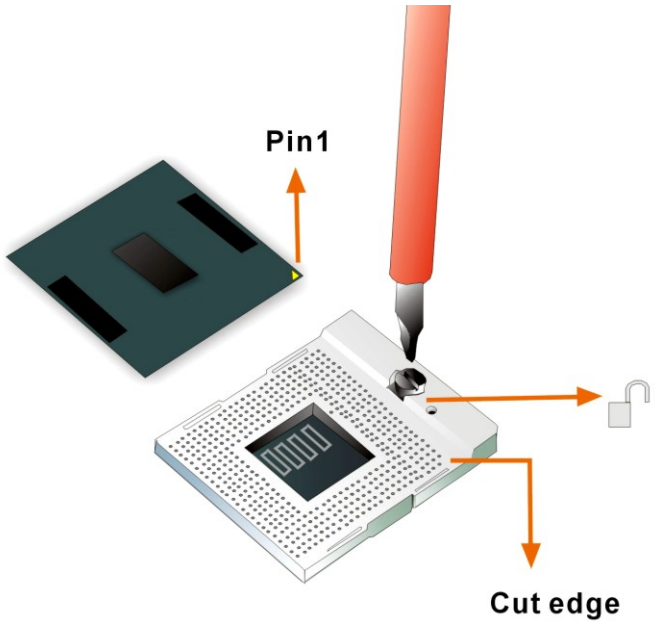


Figure 5-1: Make sure the CPU socket retention screw is unlocked

Step 2: **Inspect the CPU socket.** Make sure there are no bent pins and make sure the socket contacts are free of foreign material. If any debris is found, remove it with compressed air.

Step 3: **Correctly Orientate the CPU**. Make sure the IHS (integrated heat sink) side is facing upwards.

Step 4: **Correctly position the CPU.** Match the Pin 1 mark with the cut edge on the CPU socket. See **Figure 5-1**.

Step 5: **Align the CPU pins.** Carefully align the CPU pins with the holes in the CPU socket.

Step 6: **Insert the CPU.** Gently insert the CPU into the socket. If the CPU pins are properly aligned, the CPU should slide into the CPU socket smoothly.

Step 7: **Lock the retention screw.** Rotate the retention screw into the locked position. See **Figure 5-2**.

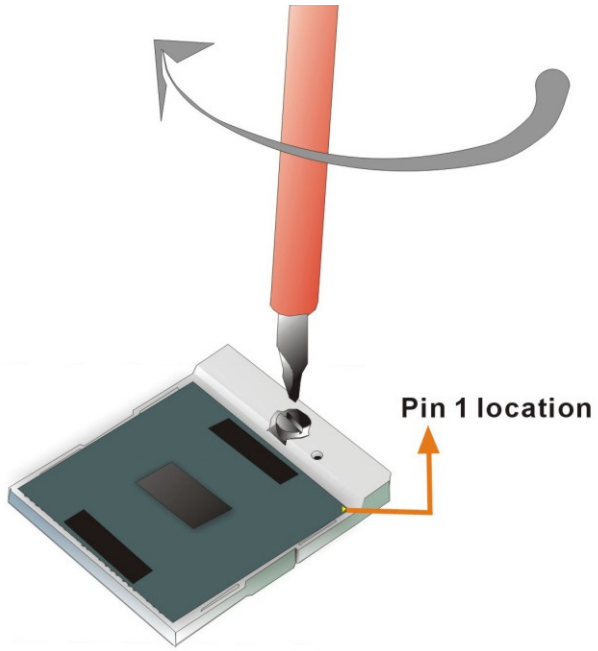


Figure 5-2: Lock the CPU Socket Retention Screw

5.3.2 SO-DIMM Installation

WARNING:

Using incorrectly specified SO-DIMM may cause permanently damage the WAFER-9102. Please make sure the purchased SO-DIMM complies with the memory specifications of the WAFER-9102. SO-DIMM specifications compliant with the WAFER-9102 are listed in Chapter 2.

To install a SO-DIMM into a SO-DIMM socket, please follow the steps below and refer to **Figure 5-3**.

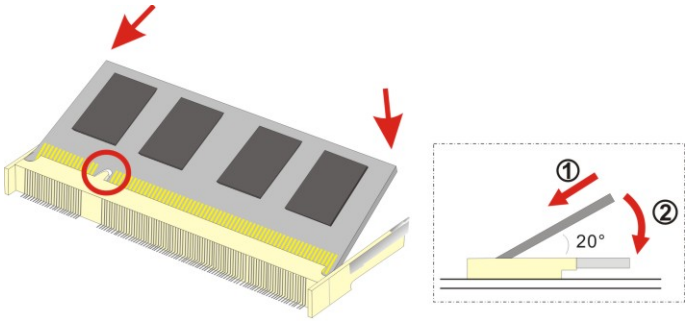


Figure 5-3: SO-DIMM Installation

Step 1: **Locate the SO-DIMM socket**. Place the WAFER-9102 on an anti-static pad with the solder side facing up.

Step 2: **Align the SO-DIMM with the socket**. The SO-DIMM must be oriented in such a way that the notch in the middle of the SO-DIMM must be aligned with the plastic bridge in the socket.

Step 3: **Insert the SO-DIMM**. Push the SO-DIMM chip into the socket at an angle. (See **Figure 5-3**)

Step 4: **Open the SO-DIMM socket arms**. Gently pull the arms of the SO-DIMM socket out and push the rear of the SO-DIMM down. (See **Figure 5-3**)

Step 5: **Secure the SO-DIMM**. Release the arms on the SO-DIMM socket. They clip into place and secure the SO-DIMM in the socket.

5.3.3 CF Card Installation

NOTE:

The WAFER-9102 can support both CF Type I cards and CF Type II cards. For the complete specifications of the supported CF cards please refer to Chapter 2.

To install the a CF card (Type 1 or Type 2) onto the WAFER-9102, please follow the steps below:

Step 1: **Locate the CF card socket**. Place the WAFER-9102 on an anti-static pad with the solder side facing up. Locate the CF card.

Step 2: **Align the CF card**. Make sure the CF card is properly aligned with the CF socket.

Step 3: **Insert the CF card**. Gently insert the CF card into the socket making sure the socket pins are properly inserted into the socket. See **Figure 5-4**.

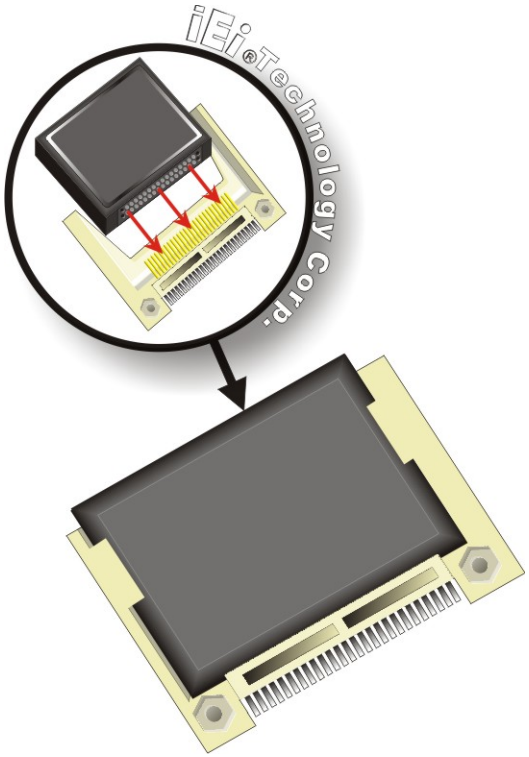
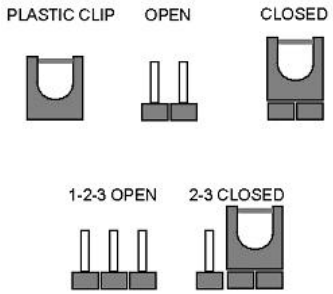


Figure 5-4: CF Card Installation

5.4 Jumper Settings

NOTE:

A jumper is a metal bridge used to close an electrical circuit. It consists of two or three metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To CLOSE/SHORT a jumper means connecting the pins of the jumper with the plastic clip and to OPEN a jumper means removing the plastic clip from a jumper.



Jumper Locations

Before the WAFER-9102 is installed in the system, the jumpers must be set in accordance with the desired configuration. The jumpers on the WAFER-9102 are listed in **Table 5-1**.

Description	Label	Type
AT power mode setting	ATXCTL1	3-pin header
Clear CMOS	J_CMOS1	6-pin header
COM2 port mode setting	JP2	3-pin header
CompactFlash® card setting	JCF1	2-pin header
LVDS voltage setting	J_VLVDS1	3-pin header

Table 5-1: Jumpers

5.4.1 AT Power Mode Setting

Jumper Label: **ATXCTL1**

Jumper Type: 3-pin header

Jumper Settings: See **Table 5-2**

Jumper Location: See Figure 5-5

The AT Power Select jumper specifies the systems power mode as AT or ATX. AT Power Select jumper settings are shown in **Table 5-2**.

AT Power Select	Description	
2-3	Use AT power	Default
Open	Use ATX power	

Table 5-2: AT Power Mode Settings

The location of the AT Power Select jumper is shown in Figure 5-5 below.

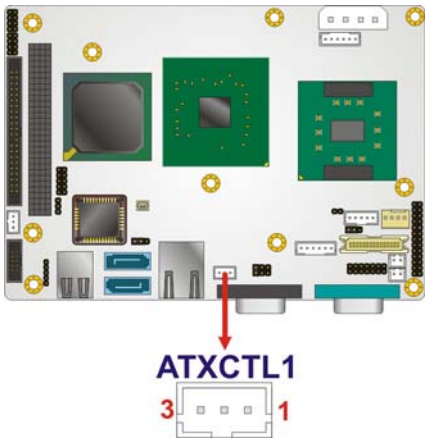


Figure 5-5: AT Power Mode Jumper Location

5.4.2 Clear CMOS Jumper

Jumper Label: **J_CMOS1**

Jumper Type: 3-pin header

Jumper Settings: See **Table 5-3**

Jumper Location: See **Figure 5-6**

If the WAFER-9102 fails to boot due to improper BIOS settings, the clear CMOS jumper clears the CMOS data and resets the system BIOS information. To do this, use the jumper cap to close pins 2 and 3 for a few seconds then reinstall the jumper clip back to pins 1 and 2.

If the “CMOS Settings Wrong” message is displayed during the boot up process, the fault may be corrected by pressing the F1 to enter the CMOS Setup menu. Do one of the following:

- Enter the correct CMOS setting
- Load Optimal Defaults
- Load Failsafe Defaults.

After having done one of the above, save the changes and exit the CMOS Setup menu.

The clear CMOS jumper settings are shown in **Table 5-3**.

AT Power Select	Description	
1-2	Keep CMOS Setup	Default
2-3	Clear CMOS Setup	

Table 5-3: Clear CMOS Jumper Settings

The location of the clear CMOS jumper is shown in **Figure 5-6** below.

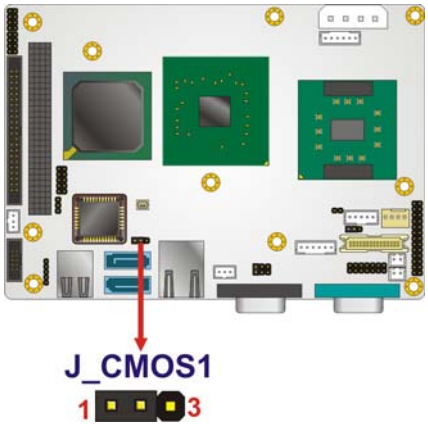


Figure 5-6: Clear CMOS Jumper

5.4.3 COM2 Mode Selection

Jumper Label: **JP2**

Jumper Type: 6-pin header

Jumper Settings: See **Table 5-4**

Jumper Location: See **Figure 5-7**

The COM2 serial port mode selection jumper sets COM2 to use the RS-232, RS-422 or RS-485 communication protocol. The jumper settings are shown in **Table 5-4**.

Setting	Description	
1-2	RS-232	Default
3-4	RS-422	
5-6	RS-485	

Table 5-4: COM2 Mode Selection Settings

The jumper location is shown in **Figure 5-7**.

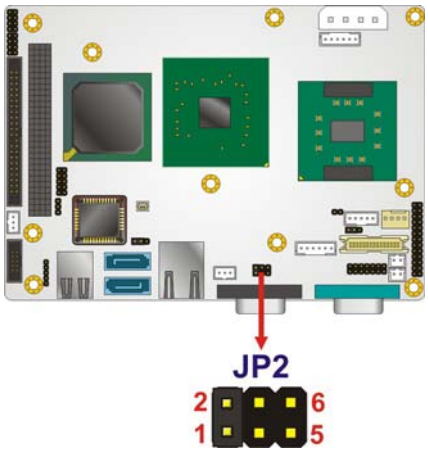


Figure 5-7: COM2 Mode Selection Jumper Location

5.4.4 CF Card Setup

Jumper Label: **JCF1**

Jumper Type: 2-pin header

Jumper Settings: See Table 5-5

Jumper Location: See Figure 5-8

The CF Card Setup jumper sets the CF Type I card or CF Type II cards as either the slave device or the master device. CF Card Setup jumper settings are shown in Table 5-5.

CF Card Setup	Description	
Open	Slave	Default
Closed	Master	

Table 5-5: CF Card Setup Jumper Settings

The CF Card Setup jumper location is shown in Figure 5-8.

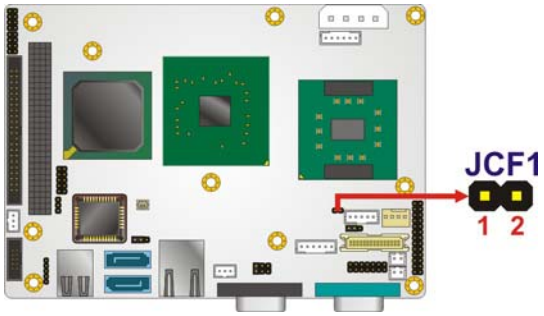


Figure 5-8: CF Card Setup Jumper Location

5.4.5 LVDS Voltage Selection

WARNING:

Permanent damage to the screen and WAFER-9102 may occur if the wrong voltage is selected with this jumper. Please refer to the user guide that cam with the monitor to select the correct voltage.

Jumper Label: **J_VLVDS1**

Jumper Type: 3-pin header

Jumper Settings: See **Table 5-6**

Jumper Location: See **Figure 5-9**

The **LVDS Voltage Selection** jumper allows the LVDS screen voltage to be set. The **LVDS Voltage Selection** jumper settings are shown in **Table 5-6**.

LCD Voltage Select	Description	
Short 1-2	+3.3 V LVDS	Default
Short 2-3	+5 V LVDS	

Table 5-6: LVDS Voltage Selection Jumper Settings

The LVDS Voltage Selection jumper location is shown in **Figure 5-9**.

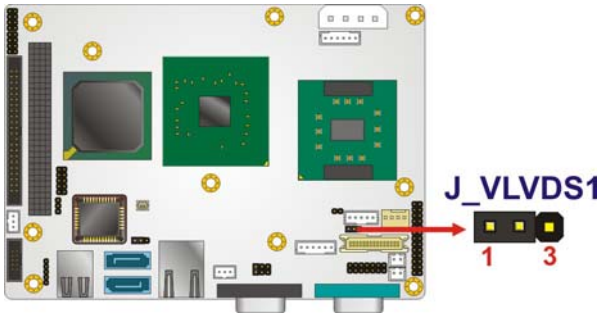


Figure 5-9: LVDS Voltage Selection Jumper Pinout Locations

5.5 Chassis Installation

5.5.1 Airflow

WARNING:

Airflow is critical to the cooling of the CPU and other onboard components. The chassis in which the WAFER-9102 must have air vents to allow cool air to move into the system and hot air to move out.

The WAFER-9102 must be installed in a chassis with ventilation holes on the sides allowing airflow to travel through the heat sink surface. In a system with an individual power supply unit, the cooling fan of a power supply can also help generate airflow through the board surface.

NOTE:

IEI has a wide range of backplanes available. Please contact your WAFER-9102 vendor, reseller or an IEI sales representative at sales@iei.com.tw or visit the IEI website (http://www.ieiworld.com.tw) to find out more about the available chassis.

5.5.2 Motherboard Installation

To install the WAFER-9102 motherboard into the chassis please refer to the reference material that came with the chassis.

5.6 Internal Peripheral Device Connections

The cables listed in **Table 5-7** are shipped with the WAFER-9102.

Quantity	Type
1	Audio cable
1	Keyboard and Mouse Y-cable
2	SATA drive cable

Table 5-7: IEI Provided Cables

Some optional items that can be purchased separately and installed on the WAFER-9102 include:

- Dual port USB cable
- Parallel port cable
- RS-232/422/485 cable
- LVDS cable

5.6.1 ATA Flat Cable Connection

The ATA 66/100 flat cable connects to the WAFER-9102 to one or two IDE devices. To connect an IDE HDD to the WAFER-9102 please follow the instructions below.

Step 1: **Locate the IDE connector**. The location/s of the IDE device connector/s is/are shown in **Chapter 3**.

Step 2: **Insert the connector**. Connect the IDE cable connector to the onboard connector. See **Figure 5-10**. A key on the front of the cable connector ensures it can only be inserted in one direction.

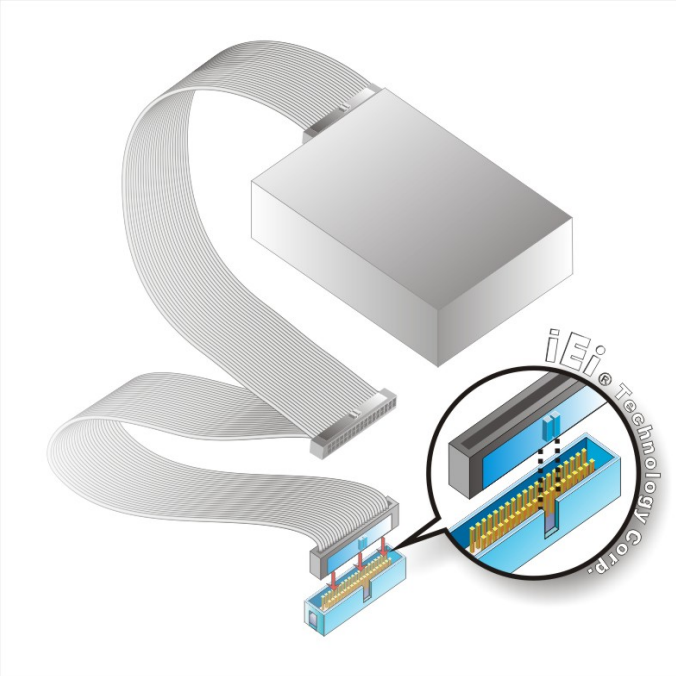


Figure 5-10: IDE Cable Connection

Step 3: **Connect the cable to an IDE device**. Connect the two connectors on the other side of the cable to one or two IDE devices. Make sure that pin 1 on the cable corresponds to pin 1 on the connector.

5.6.2 Audio Kit Installation

The Audio Kit that came with the WAFER-9102 connects to the 10-pin audio connector on the WAFER-9102. The audio kit consists of three audio jacks. One audio jack, Mic In, connects to a microphone. The remaining two audio jacks, Line-In and Line-Out, connect to two speakers. To install the audio kit, please refer to the steps below:

Step 1: **Locate the audio connector.** The location of the 10-pin audio connector is shown in **Chapter 4**.

Step 2: **Align pin 1**. Align pin 1 on the on-board connector with pin 1 on the audio kit connector. Pin 1 on the audio kit connector is indicated with a white dot. See **Figure 5-11**.

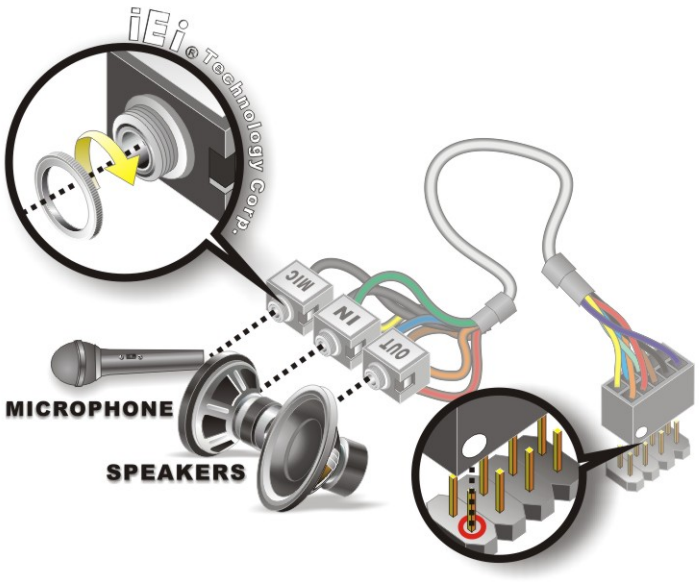


Figure 5-11: Audio Kit Cable Connection

Step 3: **Connect the audio devices**. Connect one speaker to the line-in audio jack, one speaker to the line-out audio jack and a microphone to the mic-in audio jack.

Figure 5-12: SATA Power Drive Connection

5.6.3 Dual RS-232 Cable with Slot Bracket

The dual RS-232 cable slot connector consists of two connectors attached to two independent cables. Each cable is then attached to a D-sub 9 male connector that is mounted onto a slot. To install the dual RS-232 cable, please follow the steps below.

Step 1: **Locate the connectors**. The locations of the RS-232 connectors are shown in **Chapter 3**.

Step 2: **Insert the cable connectors**. Insert one connector into each serial port box headers. See **Figure 5-13**. A key on the front of the cable connectors ensures the connector can only be installed in one direction.

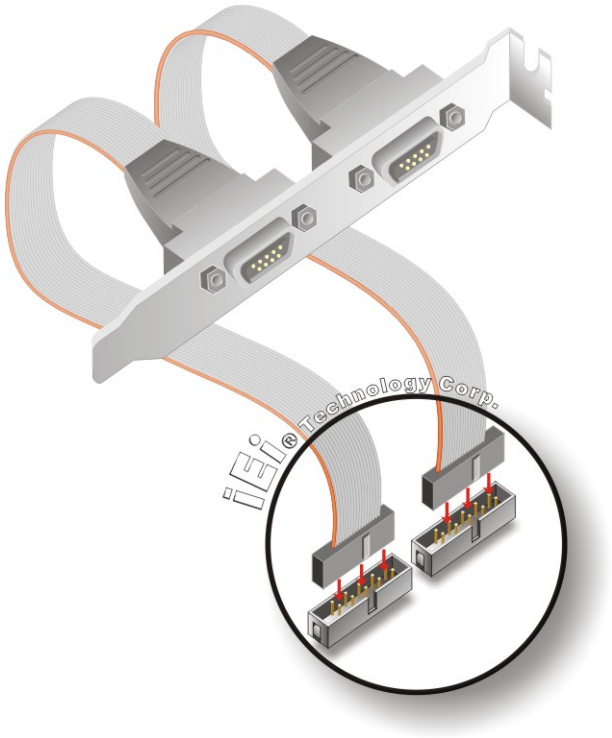


Figure 5-13: Dual RS-232 Cable Installation

Step 3: **Secure the bracket**. The dual RS-232 connector has two D-sub 9 male connectors secured on a bracket. To secure the bracket to the chassis please refer to the reference material that came with the chassis.

5.6.4 Keyboard/Mouse Y-cable Connector

The WAFER-9102 is shipped with a keyboard/mouse Y-cable connector. The keyboard/mouse Y-cable connector connects to a keyboard/mouse connector on the WAFER-9102 and branches into two cables that are each connected to a PS/2 connector, one for a mouse and one for a keyboard. To connect the keyboard/mouse Y-cable connector please follow the steps below.

Step 1: **Locate the connector**. The location of the keyboard/mouse Y-cable connector is shown in **Chapter 3**.

Step 2: **Align the connectors**. Correctly align pin 1 on the cable connector with pin 1 on the WAFER-9102 keyboard/mouse connector. See **Figure 5-14**.

Step 3: **Insert the cable connectors** Once the cable connector is properly aligned with the keyboard/mouse connector on the WAFER-9102, connect the cable connector to the on-board connectors. See **Figure 5-14**.

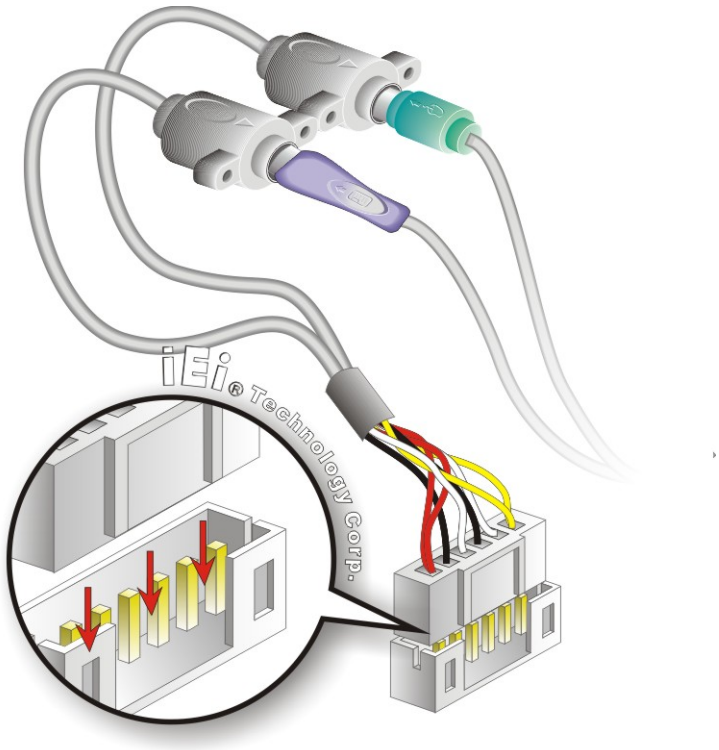


Figure 5-14: Keyboard/mouse Y-cable Connection

Step 4: **Attach PS/2 connectors to the chassis**. The keyboard/mouse Y-cable connector is connected to two PS/2 connectors. To secure the PS/2 connectors to the chassis please refer to the installation instructions that came with the chassis.

Step 5: **Connect the keyboard and mouse**. Once the PS/2 connectors are connected to the chassis, a keyboard and mouse can each be connected to one of the PS/2 connectors. The keyboard PS/2 connector and mouse PS/2 connector are both marked. Please make sure the keyboard and mouse are connected to the correct PS/2 connector.

5.6.5 LVDS LCD Installation

The WAFER-9102 can be connected to a TFT LCD screen through the 30-pin LVDS crimp connector on the board. To connect a TFT LCD to the WAFER-9102, please follow the steps below.

Step 1: **Locate the connector**. The location of the LVDS connector is shown in **Chapter 3**.

Step 2: **Insert the cable connector**. Insert the connector from the LVDS PCB driving board to the LVDS connector. When attaching the connector make sure the pins are properly aligned.

WARNING:

The diagram below is merely for illustration. The configuration and connection of the cables from the TFT LCD screen being installed may be different. Please refer to the installation manual that came with the TFT LCD screen.

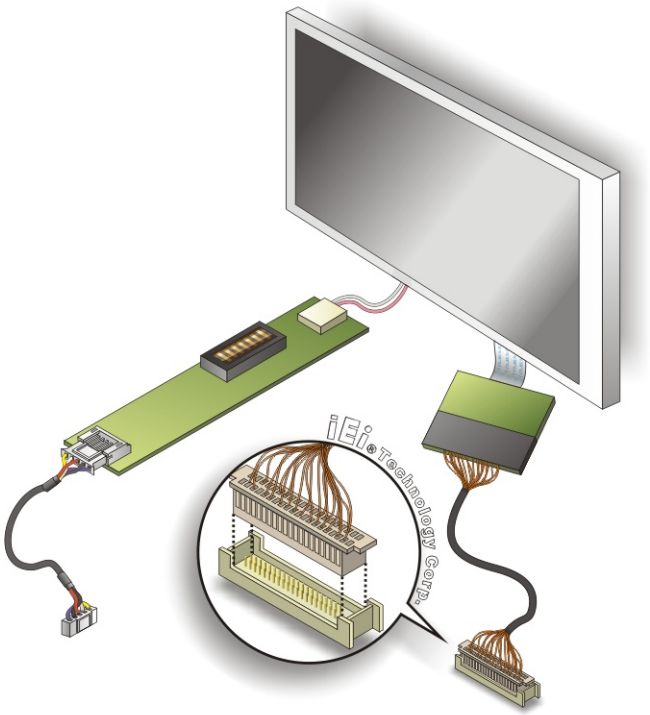


Figure 5-15: LVDS Connector

Step 3: **Locate the backlight inverter connector.** The location of the backlight inverter connector is shown in **Chapter 3**.

Step 4: **Connect backlight connector**. Connect the backlight connector to the driver TFT LCD PCB as shown in Figure 5-16. When inserting the cable connector, make sure the pins are properly aligned.

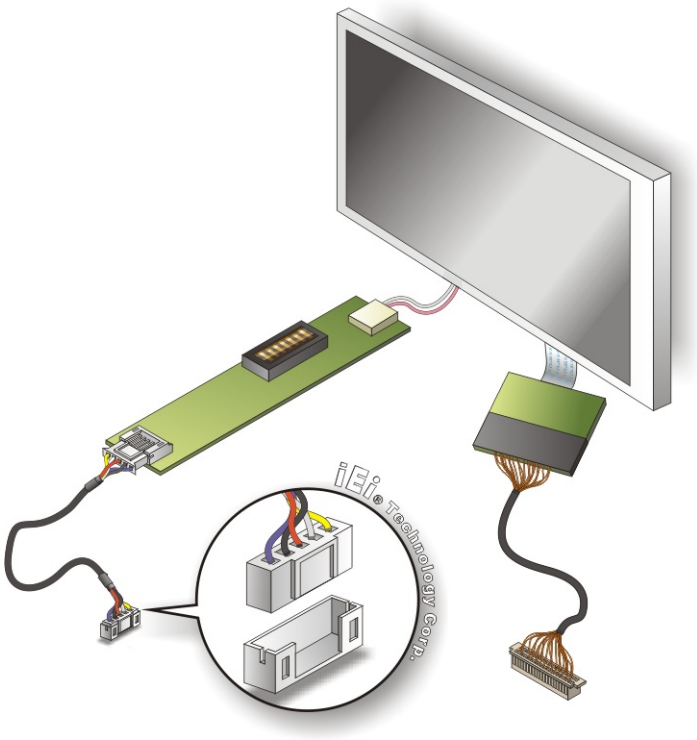


Figure 5-16: Backlight Inverter Connection

5.6.6 Parallel Port Cable without Bracket

The optional parallel port (LPT) cable respectively connects the on-board LPT 26-pin box header to an external LPT device (like a printer). The cable comprises a 26-pin female header, to be connected to the on-board LPT box-header, on one side and on the other side a standard external LPT connector. To connect the LPT cable, please follow the steps below.

Step 1: **Locate the connector**. The LPT connector location is shown in **Chapter 4**.

Step 2: **Align the connectors**. Correctly align pin 1 on the cable connector with pin 1 on the WAFER-9102 LPT box-header connector. See Figure 5-21.

Step 3: **Insert the cable connectors** Once the cable connector is properly aligned with the 26-pin box-header connector on the WAFER-9102, connect the cable connector to the on-board connector. See **Figure 5-21.**

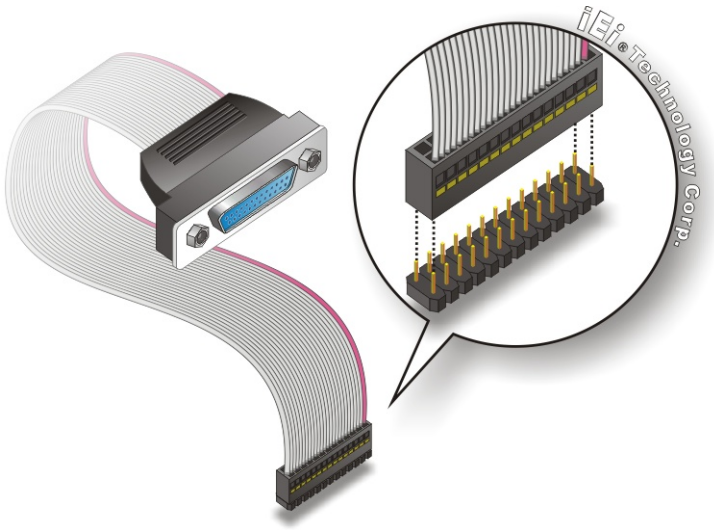


Figure 5-17: LPT Cable Connection

Step 4: **Attach the LPT connector to the chassis**. To secure the LPT interface connector to the chassis please refer to the installation instructions that came with the chassis.

Step 5: **Connect LPT device**. Once the LPT interface connector is connected to the chassis, the LPT device can be connected to the LPT interface connector. See **Figure 5-22**

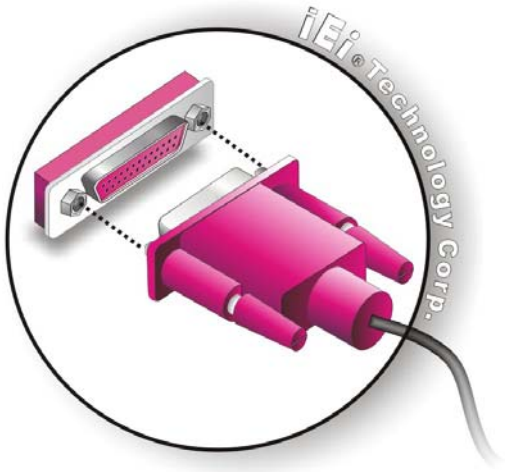


Figure 5-18: Connect the LPT Device

5.6.7 SATA Drive Connection

The WAFER-9102 is shipped with two SATA drive cables and one SATA drive power cable. To connect the SATA drives to the connectors, please follow the steps below.

Step 1: **Locate the connectors**. The locations of the SATA drive connectors are shown in **Chapter 3**.

Step 2: **Insert the cable connector**. Press the clip on the connector at the end of the SATA cable and insert the cable connector into the onboard SATA drive connector. See **Figure 5-19**.

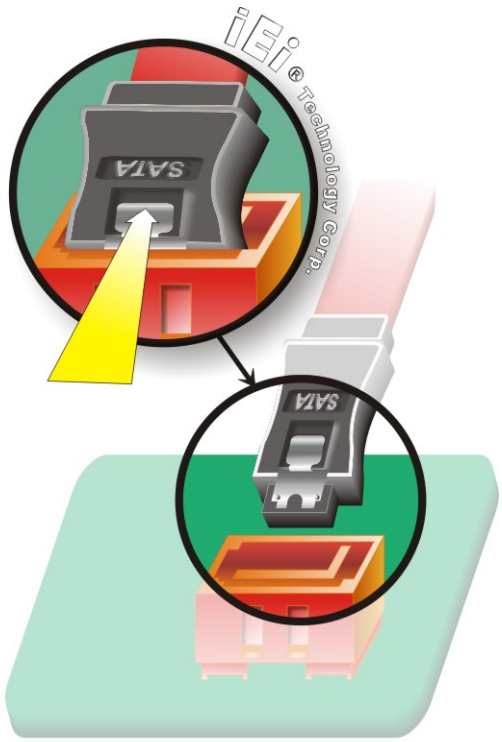


Figure 5-19: SATA Drive Cable Connection

Step 3: **Connect the cable to the SATA disk**. Connect the connector on the other end of the cable to the connector at the back of the SATA drive. See **Figure 5-12**.

Step 4: **Connect the SATA power cable**. Connect the SATA power connector to the back of the SATA drive. See **Figure 5-12**.

5.6.8 USB Cable (Dual Port) with Slot Bracket

The WAFER-9102 is shipped with a dual port USB 2.0 cable. To connect the USB cable connector, please follow the steps below.

Step 1: **Locate the connectors**. The locations of the USB connectors are shown in **Chapter 3**.

WARNING:

If the USB pins are not properly aligned, the USB device can burn out.

Step 2: **Align the connectors**. The cable has two connectors. Correctly align pin 1on each cable connector with pin 1 on the WAFER-9102 USB connector.

Step 3: **Insert the cable connectors.** Once the cable connectors are properly aligned with the USB connectors on the WAFER-9102, connect the cable connectors to the on-board connectors. See **Figure 5-20**.

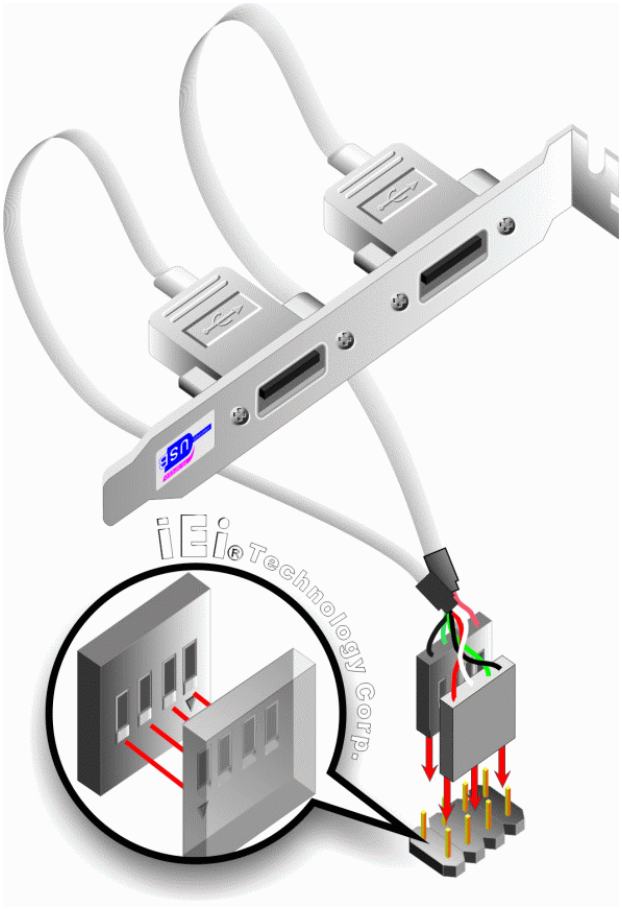


Figure 5-20: Dual USB Cable Connection

Step 4: **Attach the bracket to the chassis**. The USB 2.0 connectors are attached to a bracket. To secure the bracket to the chassis please refer to the installation instructions that came with the chassis.

5.6.9 Parallel Port Cable without Bracket

The optional parallel port (LPT) cable respectively connects the on-board LPT 26-pin box header to an external LPT device (like a printer). The cable comprises a 26-pin female header, to be connected to the on-board LPT box-header, on one side and on the other side a standard external LPT connector. To connect the LPT cable, please follow the steps below.

Step 1: **Locate the connector**. The LPT connector location is shown in **Chapter 4**.

Step 2: **Align the connectors**. Correctly align pin 1 on the cable connector with pin 1 on the WAFER-9102 LPT box-header connector. See Figure 5-21.

Step 3: **Insert the cable connectors** Once the cable connector is properly aligned with the 26-pin box-header connector on the WAFER-9102, connect the cable connector to the on-board connector. See **Figure 5-21.**

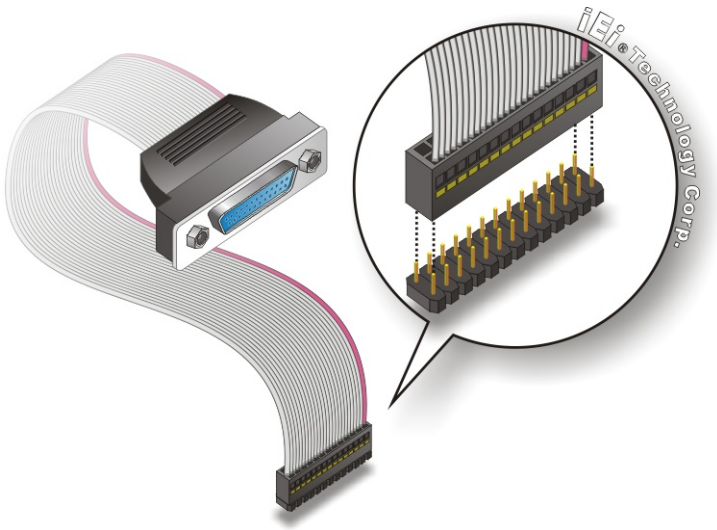


Figure 5-21: LPT Cable Connection

Step 4: **Attach the LPT connector to the chassis**. To secure the LPT interface connector to the chassis please refer to the installation instructions that came with the chassis.

Step 5: **Connect LPT device**. Once the LPT interface connector is connected to the chassis, the LPT device can be connected to the LPT interface connector. See **Figure 5-22**

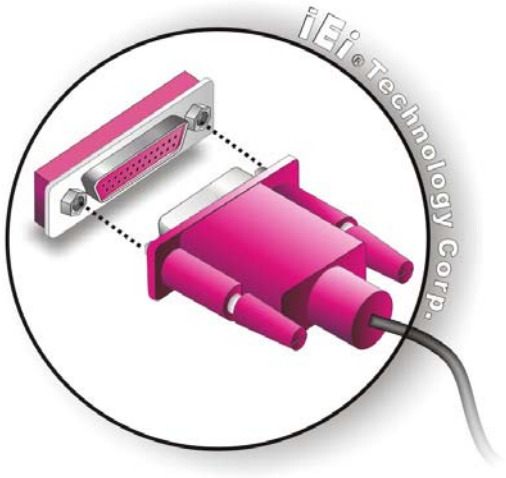


Figure 5-22: Connect the LPT Device

5.7 External Peripheral Interface Connection

The following external peripheral devices can be connected to the external peripheral interface connectors.

- RJ-45 Ethernet cable connectors
- PS/2 devices
- Serial port devices
- USB devices
- VGA monitors

To install these devices, connect the corresponding cable connector from the actual device to the corresponding WAFER-9102 external peripheral interface connector making sure the pins are properly aligned.

5.7.1 LAN Connection (Single Connector)

There are two external RJ-45 LAN connectors. The RJ-45 connectors enable connection to an external network. To connect a LAN cable with an RJ-45 connector, please follow the instructions below.

Step 1: **Locate the RJ-45 connectors**. The locations of the USB connectors are shown in **Chapter 4**.

Step 2: **Align the connectors.** Align the RJ-45 connector on the LAN cable with one of the RJ-45 connectors on the WAFER-9102. See **Figure 5-23**.

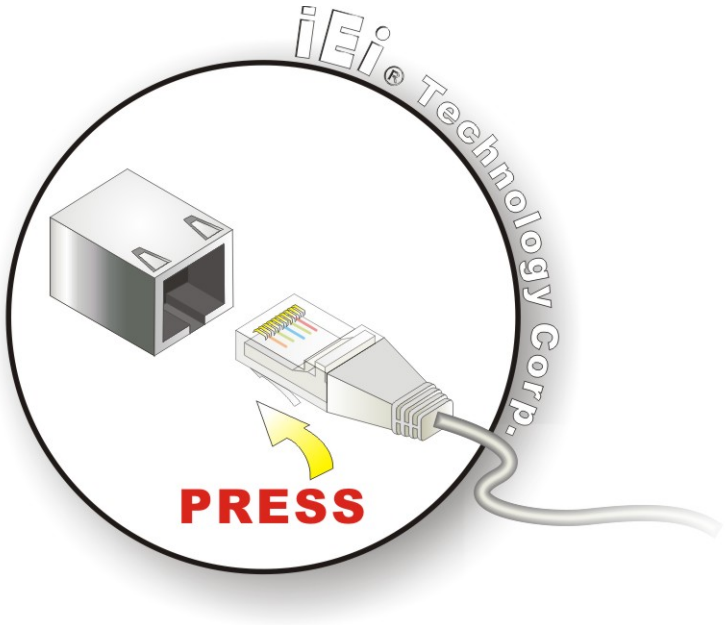


Figure 5-23: LAN Connection

Step 3: **Insert the LAN cable RJ-45 connector.** Once aligned, gently insert the LAN cable RJ-45 connector into the onboard RJ-45 connector.

5.7.2 Serial Device Connection

The WAFER-9102 has a single female DB-9 connector on the external peripheral interface panel for a serial device. Follow the steps below to connect a serial device to the WAFER-9102.

Step 1: **Locate the DB-9 connector**. The location of the DB-9 connector is shown in **Chapter 3**.

Step 2: **Insert the serial connector**. Insert the DB-9 connector of a serial device into the DB-9 connector on the external peripheral interface. See **Figure 5-24**.

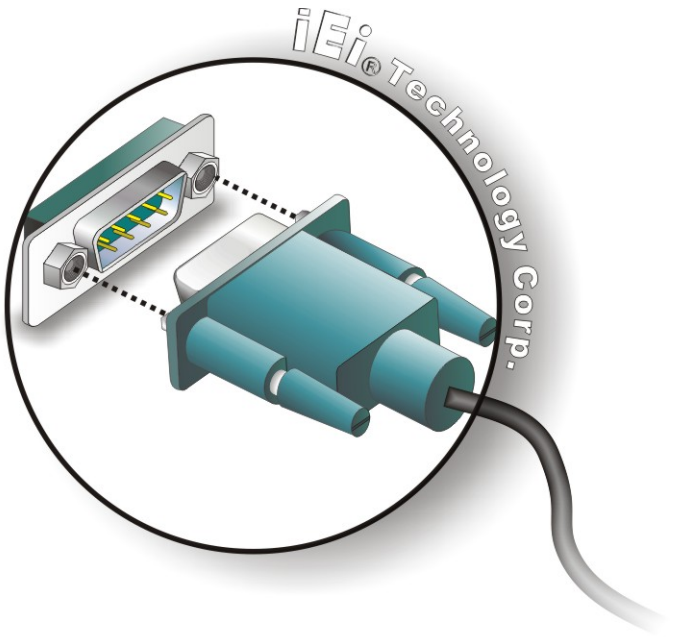


Figure 5-24: Serial Device Connector

Step 3: **Secure the connector**. Secure the serial device connector to the external interface by tightening the two retention screws on either side of the connector.

5.7.3 USB Connection (Dual Connector)

The external USB Series "A" receptacle connectors provide easier and quicker access to external USB devices. Follow the steps below to connect USB devices to the WAFER-9102.

Step 1: **Locate the USB Series "A" receptacle connectors**. The location of the USB Series "A" receptacle connectors are shown in **Chapter 3**.

Step 2: **Insert a USB Series "A" plug**. Insert the USB Series "A" plug of a device into the USB Series "A" receptacle on the external peripheral interface. See **Figure 5-25**.

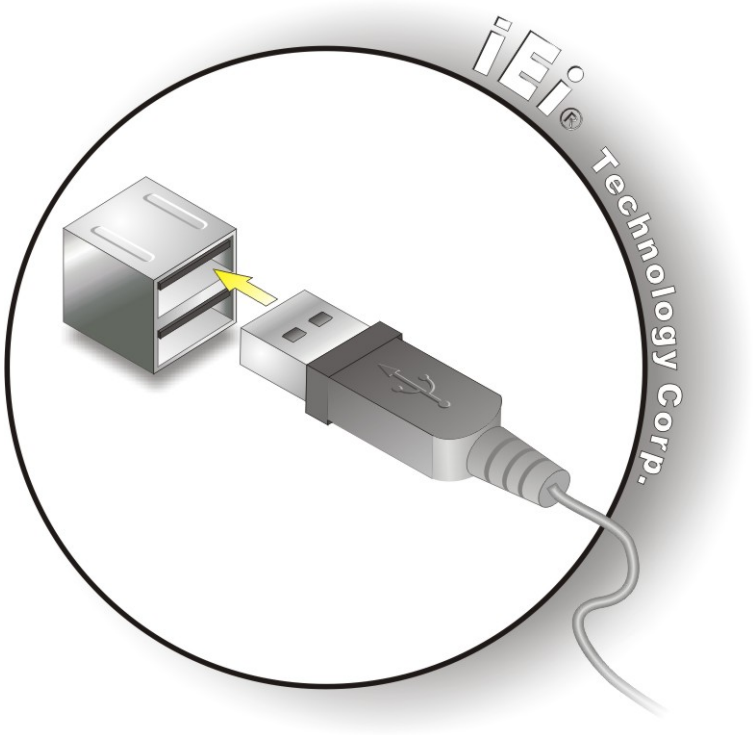


Figure 5-25: USB Connector

5.7.4 VGA Monitor Connection

The WAFER-9102 has a single female DB-15 connector on the external peripheral interface panel. The DB-15 connector is connected to a CRT or VGA monitor. To connect a monitor to the WAFER-9102, please follow the instructions below.

Step 1: **Locate the female DB-15 connector**. The location of the female DB-15 connector is shown in **Chapter 3**.

Step 2: **Align the VGA connector**. Align the male DB-15 connector on the VGA screen cable with the female DB-15 connector on the external peripheral interface.

Step 3: **Insert the VGA connector**. Once the connectors are properly aligned with the insert the male connector from the VGA screen into the female connector on the WAFER-9102. See **Figure 5-26**.

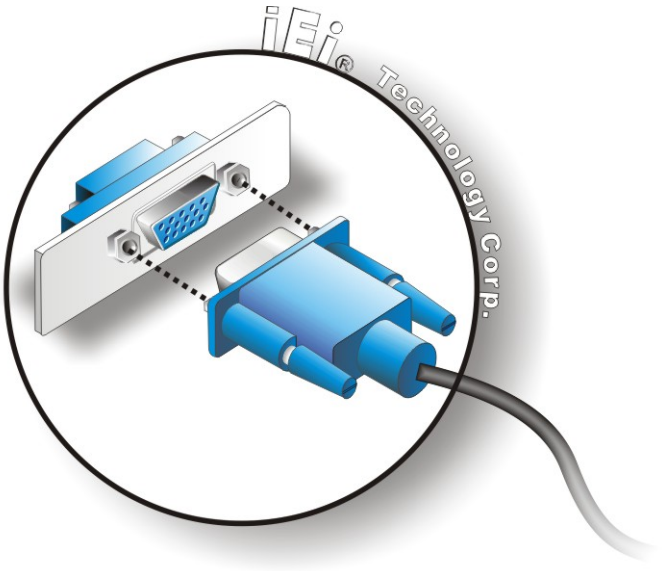


Figure 5-26: VGA Connector

Step 4: **Secure the connector**. Secure the DB-15 VGA connector from the VGA monitor to the external interface by tightening the two retention screws on either side of the connector.

Chapter

6

BIOS Setup

6.1 Introduction

A licensed copy of AMI BIOS is preprogrammed into the ROM BIOS. The BIOS setup program allows users to modify the basic system configuration. This chapter describes how to access the BIOS setup program and the configuration options that may be changed.

6.1.1 Starting Setup

The AMI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. Press the **DELETE** key as soon as the system is turned on or
2. Press the **DELETE** key when the "**Press Del to enter SETUP**" message appears on the screen.

If the message disappears before the **DELETE** key is pressed, restart the computer and try again.

6.1.2 Using Setup

Use the arrow keys to highlight items, press **ENTER** to select, use the PageUp and PageDown keys to change entries, press **F1** for help and press **ESC** to quit. Navigation keys are shown in.

Key	Function
Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item on the left hand side
Right arrow	Move to the item on the right hand side
Esc key	Main Menu – Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
Page Up key	Increase the numeric value or make changes
Page Dn key	Decrease the numeric value or make changes

Key	Function
F1 key	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2 /F3 key	Change color from total 16 colors. F2 to select color forward.
F10 key	Save all the CMOS changes, only for Main Menu

Table 6-1: BIOS Navigation Keys

6.1.3 Getting Help

When **F1** is pressed a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window press **Esc** or the **F1** key again.

6.1.4 Unable to Reboot After Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the jumper described in **Chapter 5**.

6.1.5 BIOS Menu Bar

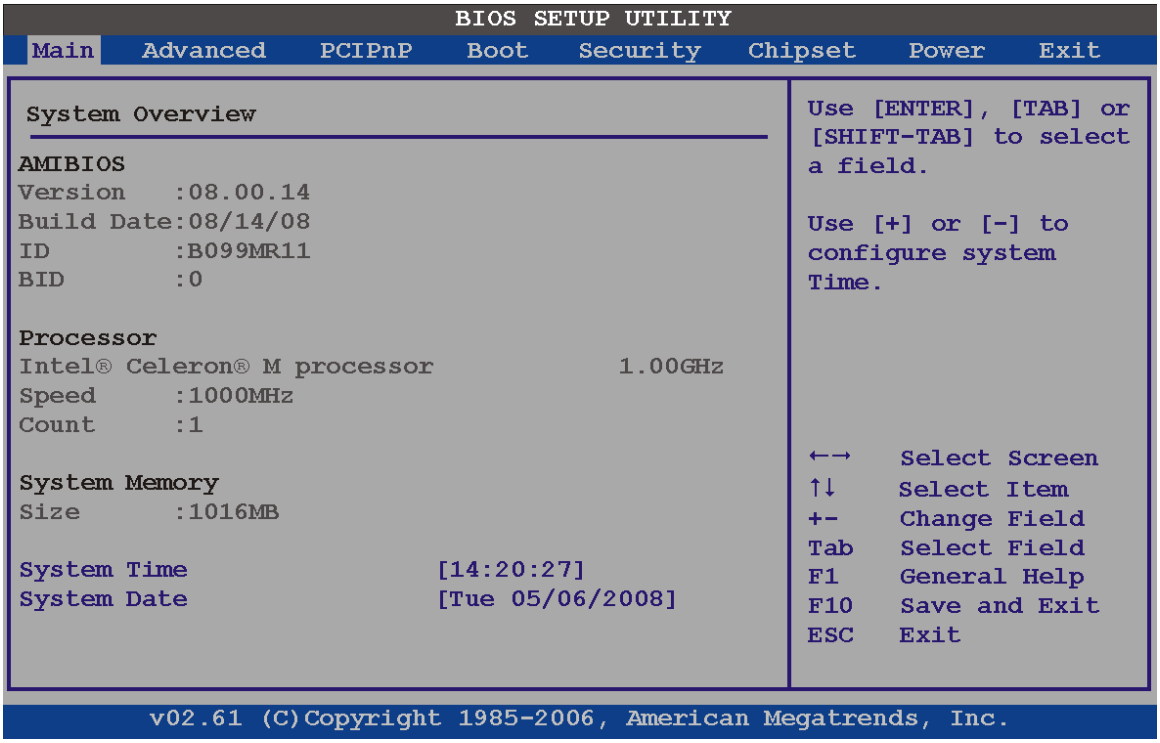
The **menu bar** on top of the BIOS screen has the following main items:

- **Main** Changes the basic system configuration.
- **Advanced** Changes the advanced system settings.
- **PCIPnP** Changes the advanced PCI/PnP Settings
- **Boot** Changes the system boot configuration.
- **Security** Sets User and Supervisor Passwords.
- **Chipset** Changes the chipset settings.
- **Power** Changes power management settings.
- **Exit** Selects exit options and loads default settings

The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

6.2 Main

The **Main** BIOS menu (**BIOS Menu 1**) appears when the **BIOS Setup** program is entered. The **Main** menu gives an overview of the basic system information.



BIOS Menu 1: Main

➔ System Overview

The **System Overview** lists a brief summary of different system components. The fields in **System Overview** cannot be changed. The items shown in the system overview include:

- **AMI BIOS**: Displays auto-detected BIOS information
  - Version: Current BIOS version
  - Build Date: Date the current BIOS version was made
  - ID: Installed BIOS ID
- **Processor**: Displays auto-detected CPU specifications
  - Type: Names the currently installed processor
  - Speed: Lists the processor speed
  - Count: The number of CPUs on the motherboard

- **System Memory**: Displays the auto-detected system memory.
  - Size: Lists memory size

The System Overview field also has two user configurable fields:

➔ **System Time [xx:xx:xx]**

Use the **System Time** option to set the system time. Manually enter the hours, minutes and seconds.

➔ **System Date [xx/xx/xx]**

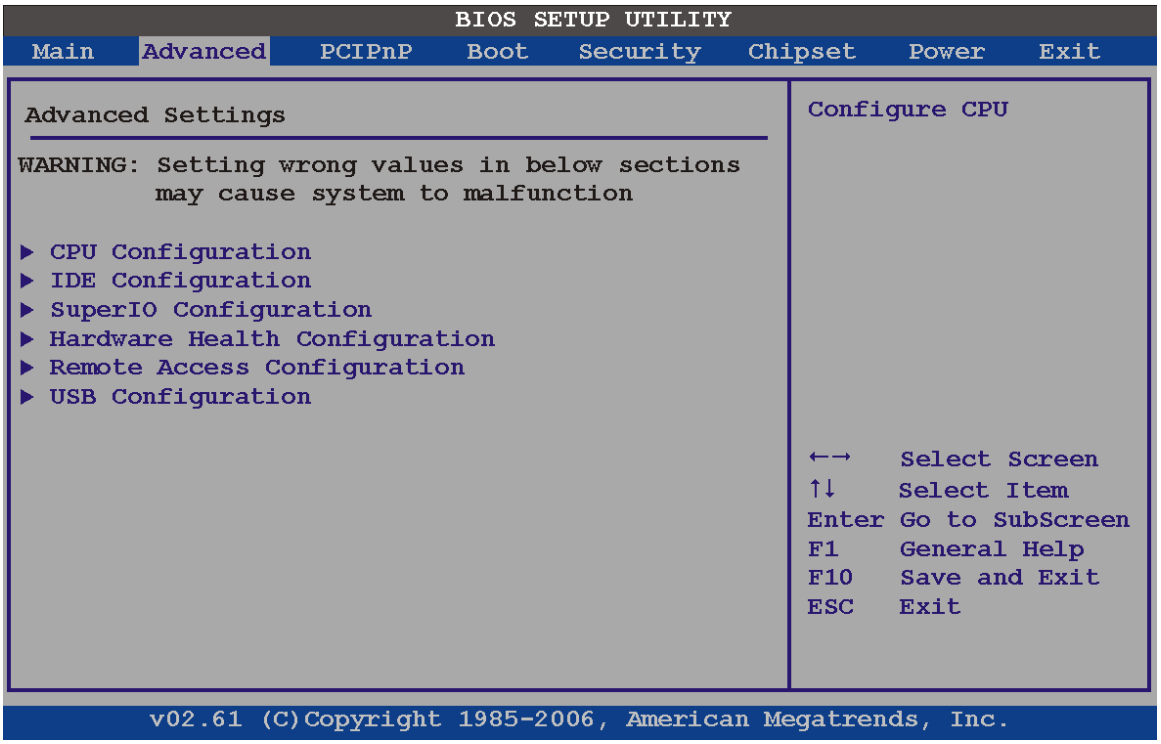
Use the **System Date** option to set the system date. Manually enter the day, month and year.

6.3 Advanced

Use the **Advanced** menu (**BIOS Menu 2**) to configure the CPU and peripheral devices through the following sub-menus:

WARNING:

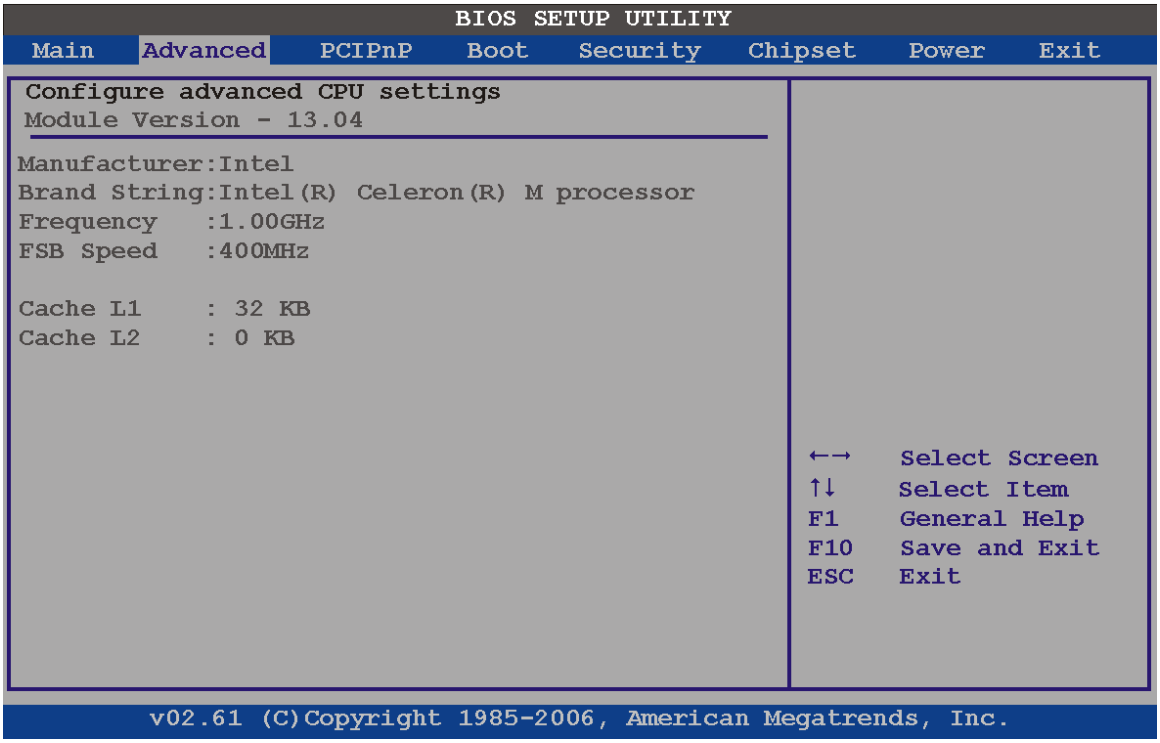
Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.



BIOS Menu 2: Advanced

6.3.1 CPU Configuration

Use the **CPU Configuration** menu (BIOS Menu 3) to view detailed CPU specifications and configure the CPU.



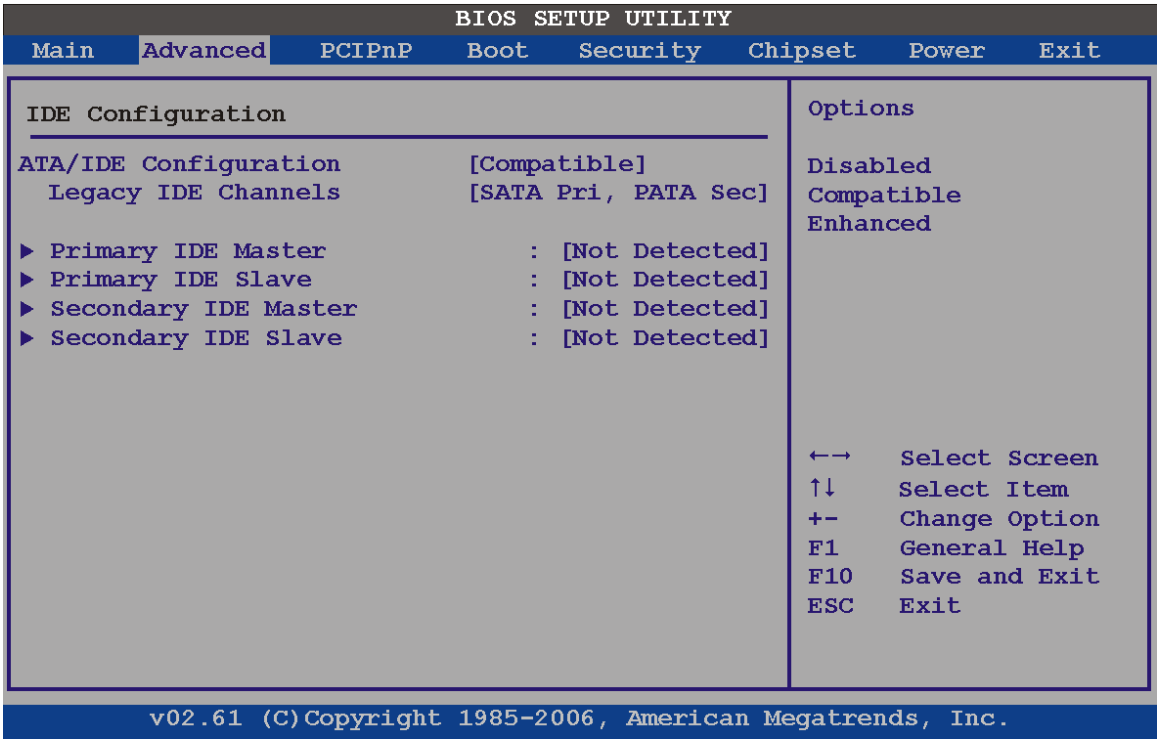
BIOS Menu 3: CPU Configuration

The CPU Configuration menu (BIOS Menu 3) lists the following CPU details:

- **Manufacturer**: Lists the name of the CPU manufacturer
- **Brand String**: Lists the brand name of the CPU being used
- **Frequency:** Lists the CPU processing speed
- **FSB Speed**: Lists the FSB speed
- **Cache L1**: Lists the CPU L1 cache size
- **Cache L2**: Lists the CPU L2 cache size

6.3.2 IDE Configuration

Use the **IDE Configuration** menu (**BIOS Menu 4**) to change and/or set the configuration of the IDE devices installed in the system.



BIOS Menu 4: IDE Configuration

➔ **ATA/IDE Configuration [Compatible]**

Use the **ATA/IDE Configurations** option to configure the ATA/IDE controller.

➔ **Disabled** Disables the on-board ATA/IDE controller.

➔ **Compatible** **DEFAULT** Configures the on-board ATA/IDE controller to be in compatible mode. In this mode, a SATA channel will replace one of the IDE channels. This mode supports up to 4 storage devices.

➔ **Enhanced** Configures the on-board ATA/IDE controller to be in Enhanced mode. In this mode, IDE channels and SATA channels are separated. This mode supports up to 6 storage devices. Some legacy OS do not support this mode.

➔ **Legacy IDE Channels [SATA Pri, PATA Sec]**

➔ **SATA Only** Only the SATA drives are enabled.

➔ **SATA Pri, PATA Sec** **DEFAULT** The SATA drives are enabled on the Primary IDE channel. The PATA drives are enabled on the Secondary IDE channel.

➔ **PATA Only** The IDE drives are enabled on the primary and secondary IDE channels. SATA drives are disabled.

➔ **IDE Master and IDE Slave**

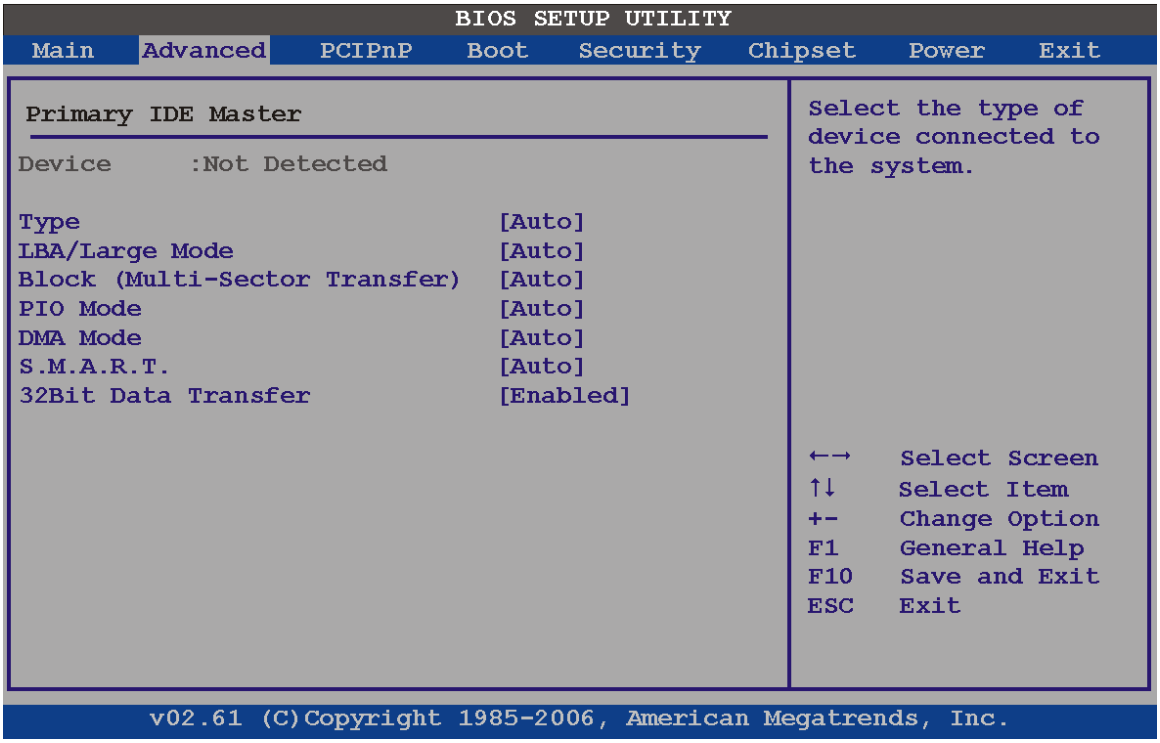
When entering setup, BIOS auto detects the presence of IDE devices. BIOS displays the status of the auto detected IDE devices. The following IDE devices are detected and are shown in the **IDE Configuration** menu:

- Primary IDE Master
- Primary IDE Slave
- Secondary IDE Master
- Secondary IDE Slave

The **IDE Configuration** menu (**BIOS Menu 4**) allows changes to the configurations for the IDE devices installed in the system. If an IDE device is detected, and one of the above listed four BIOS configuration options are selected, the IDE configuration options shown in **Section 6.3.2.1** appear.

6.3.2.1 IDE Master, IDE Slave

Use the **IDE Master** and **IDE Slave** configuration menu to view both primary and secondary IDE device details and configure the IDE devices connected to the system.



BIOS Menu 5: IDE Master and IDE Slave Configuration

➔ **Auto-Detected Drive Parameters**

The “grayed-out” items in the left frame are IDE disk drive parameters automatically detected from the firmware of the selected IDE disk drive. The drive parameters are listed as follows:

- **Device**: Lists the device type (e.g. hard disk, CD-ROM etc.)
- **Type**: Indicates the type of devices a user can manually select
- **Vendor**: Lists the device manufacturer
- **Size**: List the storage capacity of the device.
- **LBA Mode**: Indicates whether the LBA (Logical Block Addressing) is a method of addressing data on a disk drive is supported or not.

- **Block Mode**: Block mode boosts IDE drive performance by increasing the amount of data transferred. Only 512 bytes of data can be transferred per interrupt if block mode is not used. Block mode allows transfers of up to 64 KB per interrupt.
- **PIO Mode**: Indicates the PIO mode of the installed device.
- **Async DMA**: Indicates the highest Asynchronous DMA Mode that is supported.
- **Ultra DMA**: Indicates the highest Synchronous DMA Mode that is supported.
- **S.M.A.R.T.**: Indicates whether or not the Self-Monitoring Analysis and Reporting Technology protocol is supported.
- **32Bit Data Transfer**: Enables 32-bit data transfer.

➔ **Type [Auto]**

Use the **Type** BIOS option select the type of device the AMIBIOS attempts to boot from after the Power-On Self-Test (POST) is complete.

➔ **Not Installed**		BIOS is prevented from searching for an IDE disk drive on the specified channel.
➔ **Auto**	**DEFAULT**	The BIOS auto detects the IDE disk drive type attached to the specified channel. This setting should be used if an IDE hard disk drive is attached to the specified channel.
➔ **CD/DVD**		The CD/DVD option specifies that an IDE CD-ROM drive is attached to the specified IDE channel. The BIOS does not attempt to search for other types of IDE disk drives on the specified channel.
➔ **ARMD**		This option specifies an ATAPI Removable Media Device. These include, but are not limited to: ZIP LS-120

➔ **LBA/Large Mode [Auto]**

Use the **LBA/Large Mode** option to disable or enable BIOS to auto detects LBA (Logical Block Addressing). LBA is a method of addressing data on a disk drive. In LBA mode, the maximum drive capacity is 137 GB.

➔ **Disabled**		BIOS is prevented from using the LBA mode control on the specified channel.
➔ **Auto**	**DEFAULT**	BIOS auto detects the LBA mode control on the specified channel.

➔ **Block (Multi Sector Transfer) [Auto]**

Use the **Block (Multi Sector Transfer)** to disable or enable BIOS to auto detect if the device supports multi-sector transfers.

➔ **Disabled**		BIOS is prevented from using Multi-Sector Transfer on the specified channel. The data to and from the device occurs one sector at a time.
➔ **Auto**	**DEFAULT**	BIOS auto detects Multi-Sector Transfer support on the drive on the specified channel. If supported the data transfer to and from the device occurs multiple sectors at a time.

➔ **PIO Mode [Auto]**

Use the **PIO Mode** option to select the IDE PIO (Programmable I/O) mode program timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases.

➔ **Auto**	**DEFAULT**	BIOS auto detects the PIO mode. Use this value if the IDE disk drive support cannot be determined.
➔ **0**		PIO mode 0 selected with a maximum transfer rate of 3.3 MB/s
➔ **1**		PIO mode 1 selected with a maximum transfer rate of 5.2 MB/s
➔ **2**		PIO mode 2 selected with a maximum transfer rate of 8.3 MB/s

- **3** PIO mode 3 selected with a maximum transfer rate of 11.1 MB/s
- **4** PIO mode 4 selected with a maximum transfer rate of 16.6 MB/s

  (This setting generally works with all hard disk drives manufactured after 1999. For other disk drives, such as IDE CD-ROM drives, check the specifications of the drive.)

➔ **DMA Mode [Auto]**

Use the **DMA Mode** BIOS selection to adjust the DMA mode options.

- **Auto** **DEFAULT** BIOS auto detects the DMA mode. Use this value if the IDE disk drive support cannot be determined.
- **SWDMA0** Single Word DMA mode 0 selected with a maximum data transfer rate of 2.1 MB/s
- **SWDMA1** Single Word DMA mode 1 selected with a maximum data transfer rate of 4.2 MB/s
- **SWDMA2** Single Word DMA mode 2 selected with a maximum data transfer rate of 8.3 MB/s
- **MWDMA0** Multi Word DMA mode 0 selected with a maximum data transfer rate of 4.2 MB/s
- **MWDMA1** Multi Word DMA mode 1 selected with a maximum data transfer rate of 13.3 MB/s
- **MWDMA2** Multi Word DMA mode 2 selected with a maximum data transfer rate of 16.6 MB/s
- **UDMA1** Ultra DMA mode 0 selected with a maximum data transfer rate of 16.6 MB/s
- **UDMA1** Ultra DMA mode 1 selected with a maximum data transfer rate of 25 MB/s
- **UDMA2** Ultra DMA mode 2 selected with a maximum data transfer rate of 33.3 MB/s

➔ **UDMA3**		Ultra DMA mode 3 selected with a maximum data transfer rate of 44 MB/s (To use this mode, it is required that an 80-conductor ATA cable is used.)
➔ **UDMA4**		Ultra DMA mode 4 selected with a maximum data transfer rate of 66.6 MB/s (To use this mode, it is required that an 80-conductor ATA cable is used.)
➔ **UDMA5**		Ultra DMA mode 5 selected with a maximum data transfer rate of 99.9 MB/s (To use this mode, it is required that an 80-conductor ATA cable is used.)

➔ **S.M.A.R.T [Auto]**

Use the **S.M.A.R.T** option to auto-detect, disable or enable Self-Monitoring Analysis and Reporting Technology (SMART) on the drive on the specified channel. **S.M.A.R.T** predicts impending drive failures. The **S.M.A.R.T** BIOS option enables or disables this function.

➔ **Auto**	**DEFAULT**	BIOS auto detects HDD SMART support.
➔ **Disabled**		Prevents BIOS from using the HDD SMART feature.
➔ **Enabled**		Allows BIOS to use the HDD SMART feature

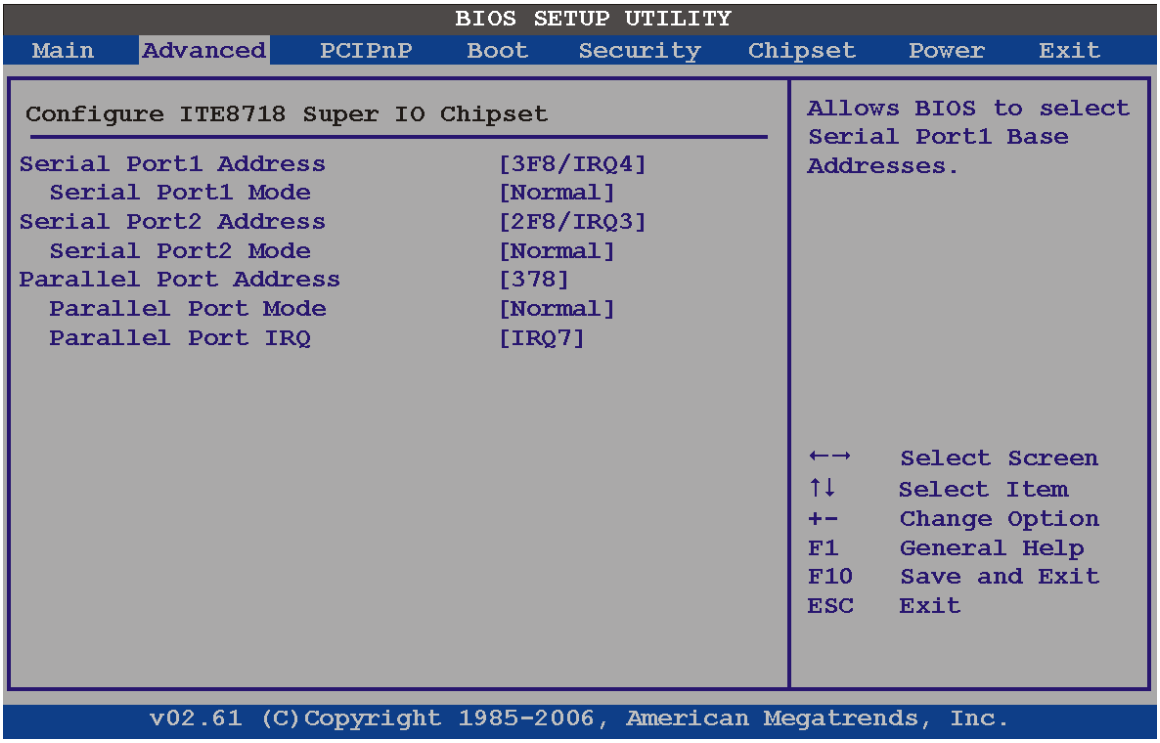
➔ **32Bit Data Transfer [Enabled]**

Use the **32Bit Data Transfer** BIOS option to enables or disable 32-bit data transfers.

➔ **Disabled**		Prevents the BIOS from using 32-bit data transfers.
➔ **Enabled**	**DEFAULT**	Allows BIOS to use 32-bit data transfers on supported hard disk drives.

6.3.3 Super IO Configuration

Use the **Super IO Configuration** menu (**BIOS Menu 6**) to set or change the configurations for the FDD controllers, parallel ports and serial ports.



BIOS Menu 6: Super IO Configuration

➔ **Serial Port1 Address [3F8/IRQ4]**

Use the **Serial Port1 Address** option to select the Serial Port 1 base address.

➔ **Disabled**		No base address is assigned to Serial Port 1
➔ **3F8/IRQ4**	**DEFAULT**	Serial Port 1 I/O port address is 3F8 and the interrupt address is IRQ4
➔ **3E8/IRQ4**		Serial Port 1 I/O port address is 3E8 and the interrupt address is IRQ4
➔ **2E8/IRQ3**		Serial Port 1 I/O port address is 2E8 and the interrupt address is IRQ3

➔ **Serial Port1 Mode [Normal]**

Use the **Serial Port1 Mode** option to select the transmitting and receiving mode for the first serial port.

➔ **Normal**	**DEFAULT**	Serial Port 1 mode is normal
➔ **IrDA**		Serial Port 1 mode is IrDA
➔ **ASK IR**		Serial Port 1 mode is ASK IR

➔ **Serial Port2 Address [2F8/IRQ3]**

Use the **Serial Port2 Address** option to select the Serial Port 2 base address.

➔ **Disabled**		No base address is assigned to Serial Port 2
➔ **2F8/IRQ3**	**DEFAULT**	Serial Port 2 I/O port address is 3F8 and the interrupt address is IRQ3
➔ **3E8/IRQ4**		Serial Port 2 I/O port address is 3E8 and the interrupt address is IRQ4
➔ **2E8/IRQ3**		Serial Port 2 I/O port address is 2E8 and the interrupt address is IRQ3

➔ **Serial Port2 Mode [Normal]**

Use the **Serial Port2 Mode** option to select the Serial Port2 operational mode.

➔ **Normal**	**DEFAULT**	Serial Port 2 mode is normal
➔ **IrDA**		Serial Port 2 mode is IrDA
➔ **ASK IR**		Serial Port 2 mode is ASK IR

➔ **Parallel Port Address [Disabled]**

Use the **Parallel Port Address** option to select the parallel port base address.

➔ **Disabled**	**DEFAULT**	No base address is assigned to the Parallel Port
➔ **378**		Parallel Port I/O port address is 378

- ➔ **278** Parallel Port I/O port address is 278
- ➔ **3BC** Parallel Port I/O port address is 3BC

➔ **Parallel Port Mode [Normal]**

Use the **Parallel Port Mode** option to select the mode the parallel port operates in.

- ➔ **Normal** **DEFAULT** The normal parallel port mode is the standard mode for parallel port operation.
- ➔ **EPP** The parallel port operates in the enhanced parallel port mode (EPP). The EPP mode supports bi-directional communication between the system and the parallel port device and the transmission rates between the two are much faster than the Normal mode.
- ➔ **ECP+EPP** The parallel port operates in the extended capabilities port (ECP) mode. The ECP mode supports bi-directional communication between the system and the parallel port device and the transmission rates between the two are much faster than the Normal mode

  The parallel port is also be compatible with EPP devices described above

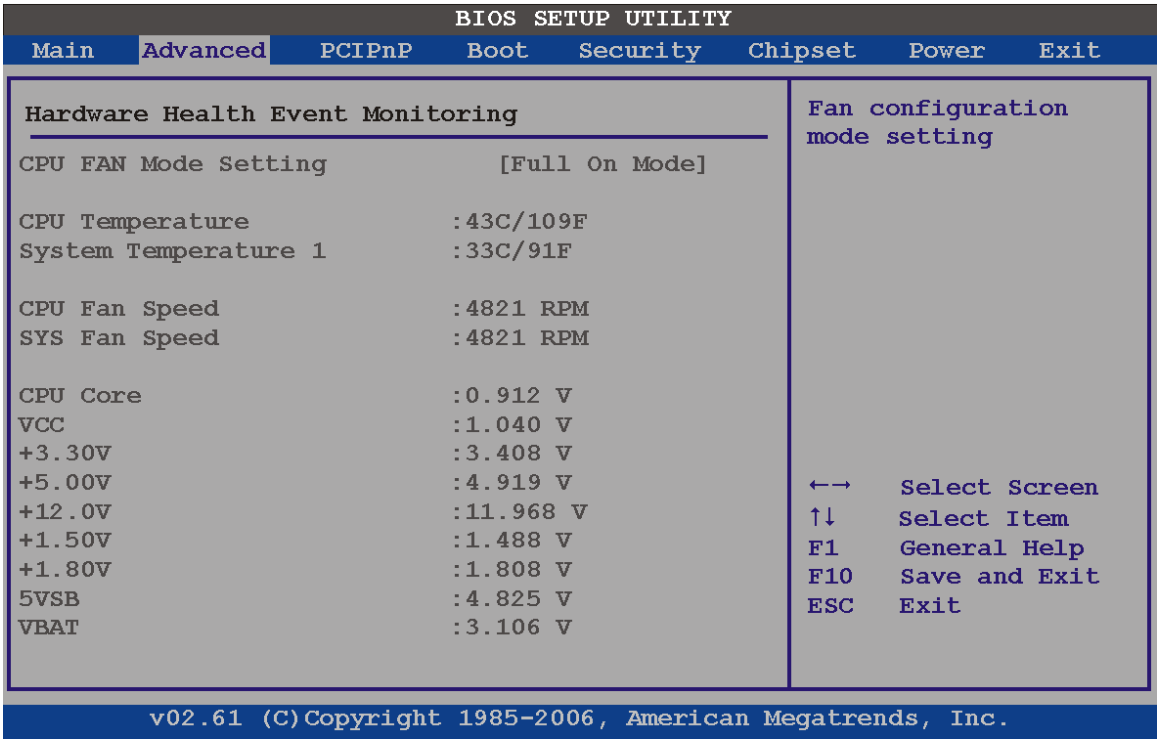
➔ **Parallel Port IRQ [IRQ7]**

Use the **Parallel Port IRQ** selection to set the parallel port interrupt address.

- ➔ **IRQ5** IRQ5 is assigned as the parallel port interrupt address
- ➔ **IRQ7** **DEFAULT** IRQ7 is assigned as the parallel port interrupt address

6.3.4 Hardware Health Configuration

The **Hardware Health Configuration** menu (**BIOS Menu 7**) shows the operating temperature, fan speeds and system voltages.



BIOS Menu 7: Hardware Health Configuration

➔ **CPU FAN Mode Setting [Full On Mode]**

Use the **CPU FAN Mode Setting** option to configure the second fan.

➔ **Full On Mode**	**DEFAULT**	Fan is on all the time
➔ **Automatic mode**		Fan is off when the temperature is low enough. Parameters must be set by the user.
➔ **PWM Manual mode**		Pulse width modulation set manually

When the **CPU FAN Mode Setting** option is in the **Automatic Mode**, the following parameters can be set.

- CPU Temp. Limit of OFF
- CPU Temp. Limit of Start
- CPU Fan Start PWM
- Slope PWM 1

When the **CPU FAN Mode Setting** option is in the **PWM Manual Mode**, the following parameters can be set.

- CPU Fan PWM control

➔ **CPU Temp. Limit of OFF [000]**

WARNING:

Setting this value too high may cause the fan to stop when the CPU is at a high temperature and therefore cause the system to be damaged.

The **CPU Temp. Limit of OFF** option can only be set if the **CPU FAN Mode Setting** option is set to **Automatic Mode**. Use the **CPU Temp. Limit of OFF** option to select the CPU temperature at which the cooling fan should automatically turn off. To select a value, select the **CPU Temp. Limit of OFF** option and enter a decimal number between 000 and 127. The temperature range is specified below.

- Minimum Value: 0°C
- Maximum Value: 127°C

➔ **CPU Temp. Limit of Start [020]**

WARNING:

Setting this value too high may cause the fan to start only when the CPU is at a high temperature and therefore cause the system to be damaged.

The **CPU Temp. Limit of Start** option can only be set if the **CPU FAN Mode Setting** option is set to **Automatic Mode**. Use the **CPU Temp. Limit of Start** option to select the CPU temperature at which the cooling fan should automatically turn on. When the fan starts, it rotates using the starting pulse width modulation (PWM) specified in the **Fan 3 Start PWM** option below. To select a value, select the **CPU Temp. Limit of Start** option and enter a decimal number between 000 and 127. The temperature range is specified below.

- Minimum Value: 0°C
- Maximum Value: 127°C

➔ **CPU Fan Start PWM [070]**

The **Fan 3 Start PWM** option can only be set if the **CPU FAN Mode Setting** option is set to **Automatic Mode**. Use the **Fan 3 Start PWM** option to select the PWM mode the fan starts to rotate with after the temperature specified in the **Temperature 3 Limit of Start** is exceeded. The Super I/O chipset supports 128 PWM modes. To select a value, select the **Fan 3 Start PWM** option and enter a decimal number between 000 and 127. The temperature range is specified below.

- PWM Minimum Mode: 0
- PWM Maximum Mode: 127

➔ **Slope PWM [0.5 PWM]**

The **Slope PWM 1** option can only be set if the **CPU FAN Mode Setting** option is set to **Automatic Mode**. Use the **Slope PWM 1** option to select the linear rate at which the PWM mode increases with respect to an increase in temperature. A list of available options is shown below:

- 0 PWM
- 1 PWM
- 2 PWM
- 4 PWM
- 8 PWM
- 16 PWM
- 32 PWM

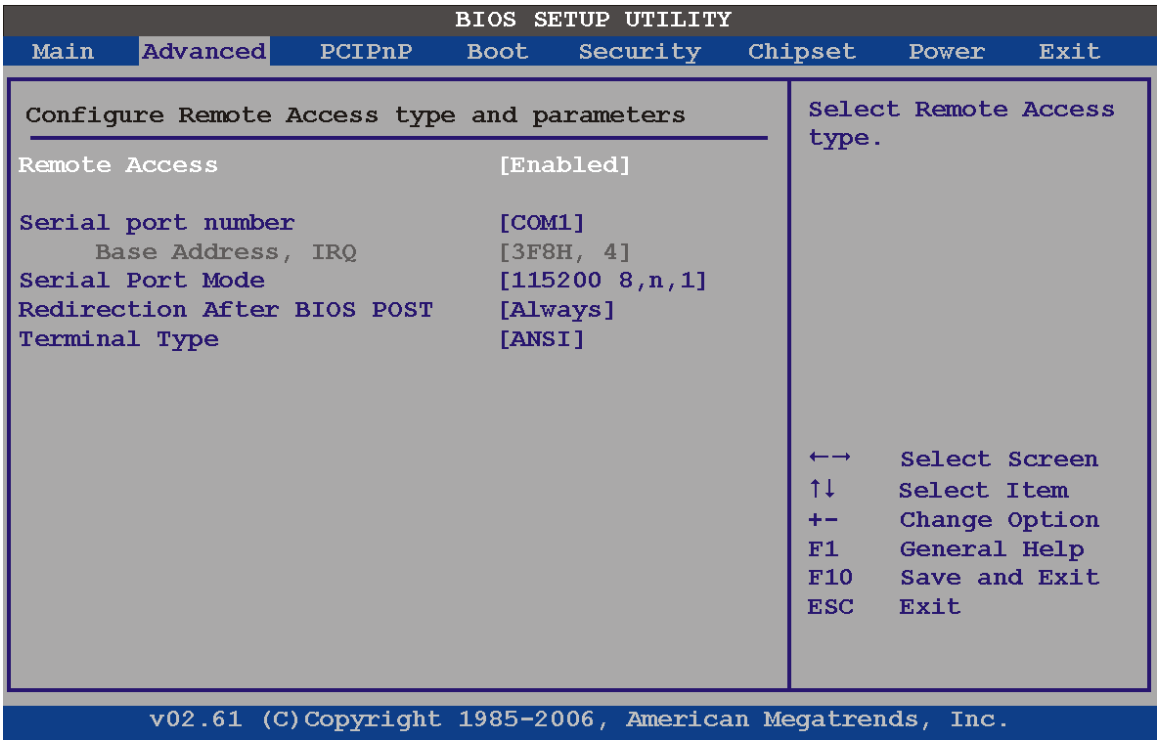
- 64 PWM

The following system parameters and values are shown. The system parameters that are monitored are:

- **System Temperatures**: The following system temperatures are monitored
  - CPU temperature
  - System temperature
- **Fan Speeds**: The CPU cooling fan speed is monitored.
  - CPU fan speed
  - System fan speed
- **Voltages**: The following system voltages are monitored
  - CPU Core
  - VCC
  - +3.30 V
  - +5.00 V
  - +12.0 V
  - +1.5 V
  - +1.8 V
  - 5 VSB
  - VBAT

6.3.5 Remote Configuration

Use the **Remote Access Configuration** menu (**BIOS Menu 8**) to configure remote access parameters. The **Remote Access Configuration** is an AMIBIOS feature and allows a remote host running a terminal program to display and configure the BIOS settings.



BIOS Menu 8: Remote Access Configuration

➔ **Remote Access [Disabled]**

Use the **Remote Access** option to enable or disable access to the remote functionalities of the system.

➔ **Disabled** **DEFAULT** Remote access is disabled.

➔	**Enabled**	Remote access configuration options shown below appear: Serial Port Number Serial Port Mode Flow Control Redirection after BIOS POST Terminal Type VT-UTF8 Combo Key Support These configuration options are discussed below.

➔ **Serial Port Number [COM1]**

Use the **Serial Port Number** option allows to select the serial port used for remote access.

➔	**COM1**	**DEFAULT**	System is remotely accessed through COM1
➔	**COM2**		System is remotely accessed through COM2

NOTE: Make sure the selected COM port is enabled through the Super I/O configuration menu.

➔ **Base Address, IRQ [2F8h,3]**

The **Base Address, IRQ** option cannot be configured and only shows the interrupt address of the serial port listed above.

➔ **Serial Port Mode [115200 8,n,1]**

Use the **Serial Port Mode** option to select baud rate through which the console redirection is made. The following configuration options are available

- 115200 8,n,1 DEFAULT
- 57600 8,n,1
- 38400 8,n,1
- 19200 8,n,1
- 09600 8,n,1

NOTE:

Identical baud rate setting musts be set on the host (a management computer running a terminal software) and the slave

➔ **Flow Control [None]**

Use the **Flow Control** option to report the flow control method for the console redirection application.

➔ **None**	**DEFAULT**	No control flow,
➔ **Hardware**		Hardware is set as the console redirection
➔ **Software**		Software is set as the console redirection

➔ **Redirection After BIOS POST [Always]**

Use the **Redirection After BIOS POST** option to specify when console redirection should occur.

➔ **Disabled**		The console is not redirected after POST
➔ **Boot Loader**		Redirection is active during POST and during Boot Loader
➔ **Always**	**DEFAULT**	Redirection is always active (Some OSes may not work if set to Always)

➔ **Terminal Type [ANSI]**

Use the **Terminal Type** BIOS option to specify the remote terminal type.

➔ **ANSI**	**DEFAULT**	The target terminal type is ANSI
➔ **VT100**		The target terminal type is VT100
➔ **VT-UTF8**		The target terminal type is VT-UTF8

➔ **VT-UTF8 Combo Key Support [Disabled]**

Use the **VT-UFT8 Combo Key Support** option to enable additional keys that are not provided by VT100 for the PC 101 keyboard.

The VT100 Terminal Definition is the standard convention used to configure and conduct emergency management tasks with UNIX-based servers. VT100 does not support all keys on the standard PC 101-key layout, however. The VT-UTF8 convention makes available additional keys that are not provided by VT100 for the PC 101 keyboard.

➔ **Disabled**	**DEFAULT**	Disables the VT-UTF8 terminal keys
➔ **Enabled**		Enables the VT-UTF8 combination key. Support for ANSI/VT100 terminals

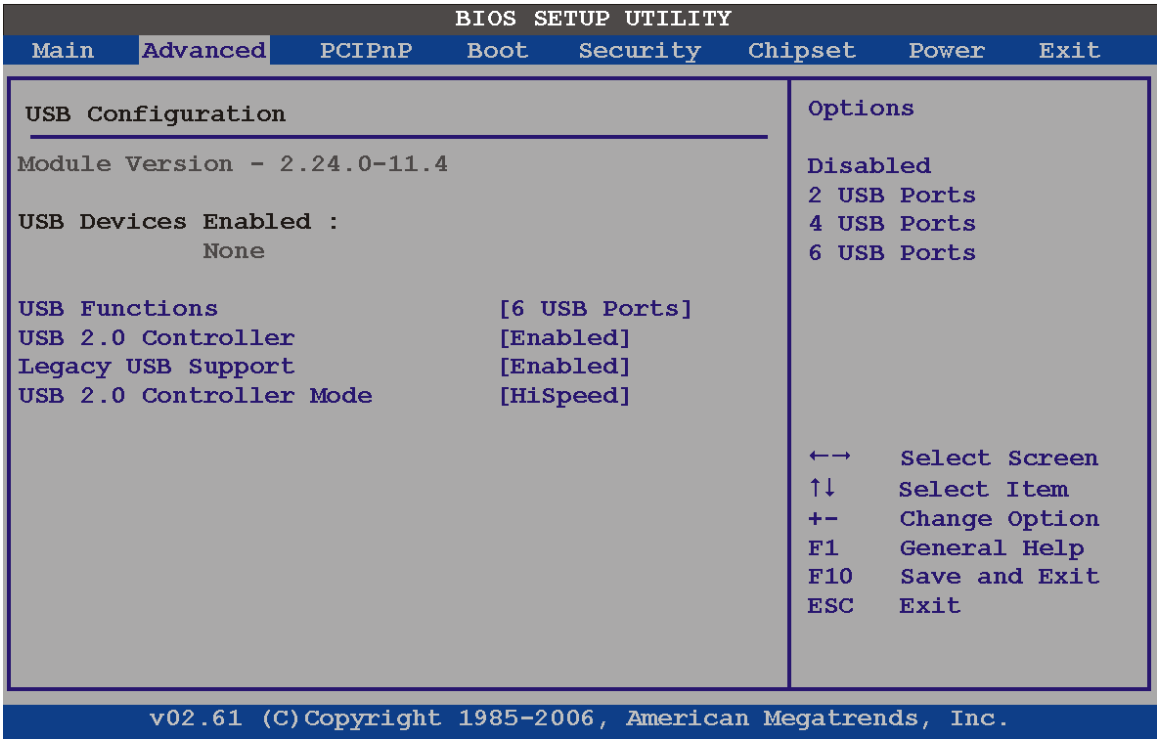
➔ **Sredir Memory Display Delay [Disabled]**

Use the **Sredir Memory Display Delay** option to select the delay before memory information is displayed. Configuration options are listed below

- No Delay DEFAULT
- Delay 1 sec
- Delay 2 sec
- Delay 4 sec

6.3.6 USB Configuration

Use the **USB Configuration** menu (**BIOS Menu 9**) to read USB configuration information and configure the USB settings.



BIOS Menu 9: USB Configuration

➔ **USB Functions [Enabled]**

Use the **USB Function** option to enable or disable the USB controllers.

➔ **Disabled** USB controllers are enabled

➔ **Enabled** **DEFAULT** USB controllers are disabled

➔ **USB 2.0 Controller [Enabled]**

The **USB 2.0 Controller** BIOS option enables or disables the USB 2.0 controller

➔ **Disabled** USB function disabled

➔ **Enabled** **DEFAULT** USB function enabled

➔ **USB2.0 Controller Mode [HiSpeed]**

The **USB2.0 Controller Mode** BIOS option sets the speed of the USB2.0 controller.

➔ **FullSpeed** The controller is capable of operating at full speed 12 Mb/s

➔ **HiSpeed** **DEFAULT** The controller is capable of operating at high speed 480 Mb/s

➔ **Legacy USB Support [Enabled]**

Use the **Legacy USB Support** BIOS option to enable USB mouse and USB keyboard support.

Normally if this option is not enabled, any attached USB mouse or USB keyboard does not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there is no USB driver loaded onto the system.

➔ **Disabled** Legacy USB support disabled

➔ **Enabled** **DEFAULT** Legacy USB support enabled

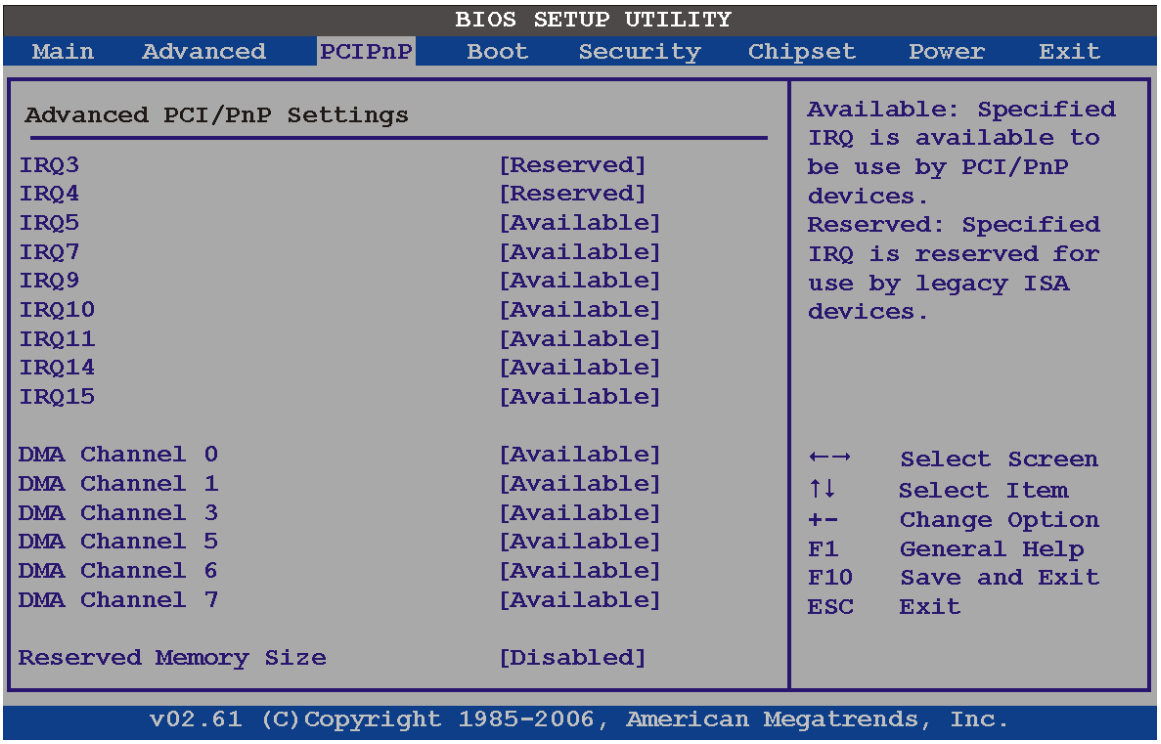
➔ **Auto** Legacy USB support disabled if no USB devices are connected

6.4 PCI/PnP

Use the PCI/PnP menu (**BIOS Menu 10**) to configure advanced PCI and PnP settings.

WARNING:

Setting wrong values for the BIOS selections in the PCIPnP BIOS menu may cause the system to malfunction.



BIOS Menu 10: PCI/PnP Configuration

➔ **IRQ# [Available]**

Use the **IRQ#** address to specify what IRQs can be assigned to a particular peripheral device.

➔ **Available** **DEFAULT** The specified IRQ is available to be used by PCI/PnP devices

➔ **Reserved** The specified IRQ is reserved for use by Legacy ISA devices

Available IRQ addresses are:

- IRQ3
- IRQ4
- IRQ5
- IRQ7
- IRQ9

- IRQ10
- IRQ 11
- IRQ 14
- IRQ 15

➔ **DMA Channel# [Available]**

Use the **DMA Channel#** option to assign a specific DMA channel to a particular PCI/PnP device.

➔ **Available**	**DEFAULT**	The specified DMA is available to be used by PCI/PnP devices
➔ **Reserved**		The specified DMA is reserved for use by Legacy ISA devices

Available DMA Channels are:

- DM Channel 0
- DM Channel 1
- DM Channel 3
- DM Channel 5
- DM Channel 6
- DM Channel 7

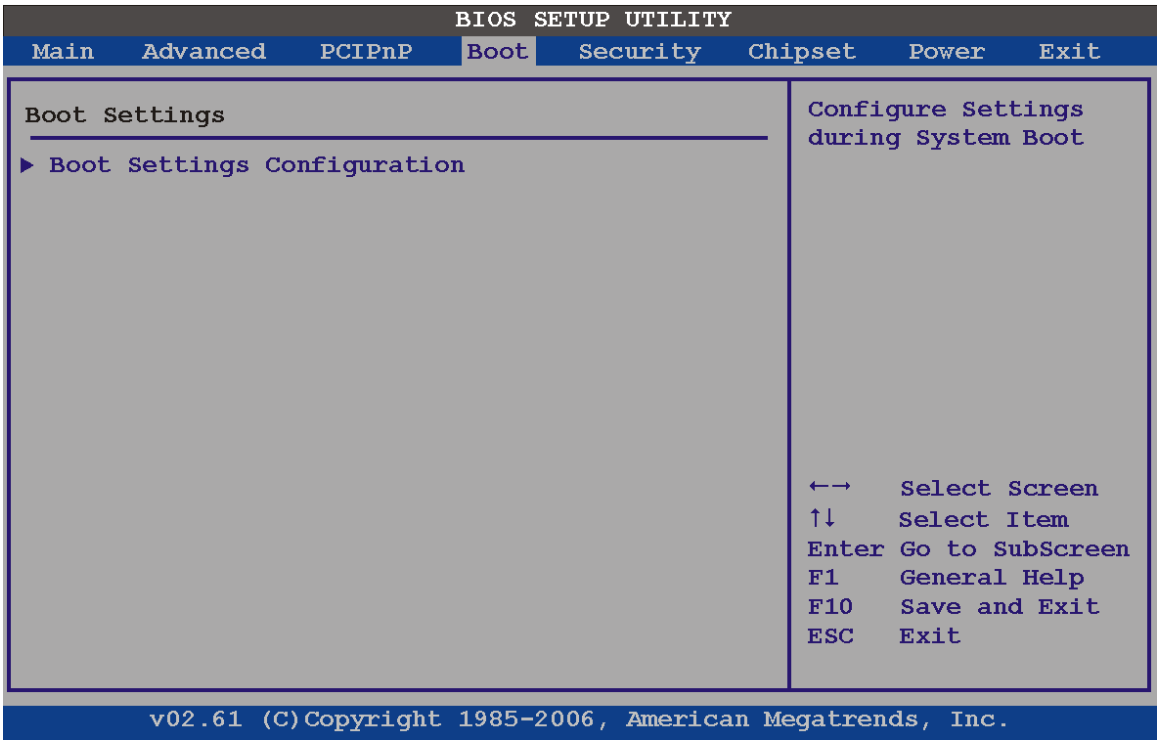
➔ **Reserved Memory Size [Disabled]**

Use the **Reserved Memory Size** BIOS option to specify the amount of memory that should be reserved for legacy ISA devices.

➔ **Disabled**	**DEFAULT**	No memory block reserved for legacy ISA devices
➔ **16K**		16 KB reserved for legacy ISA devices
➔ **32K**		32 KB reserved for legacy ISA devices
➔ **64K**		54 KB reserved for legacy ISA devices

6.5 Boot

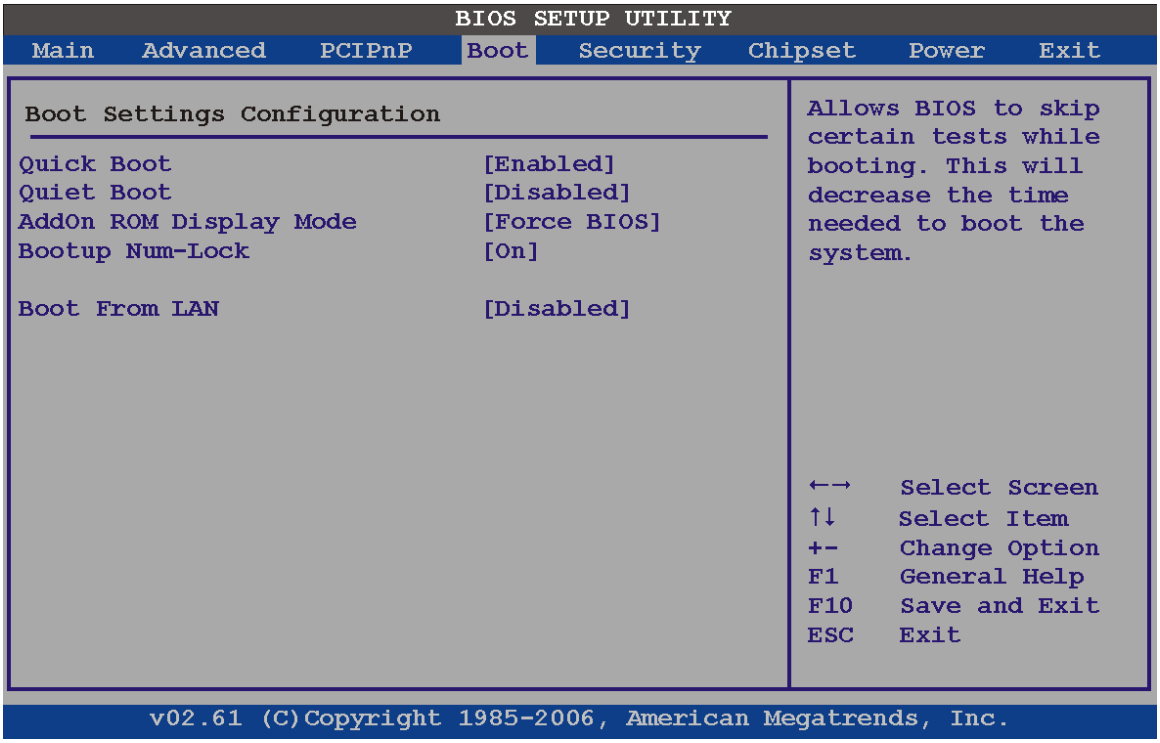
Use the Boot menu (**BIOS Menu 11**) to configure system boot options.



BIOS Menu 11: Boot

6.5.1 Boot Settings Configuration

Use the Boot Settings Configuration menu (**BIOS Menu 11**) to configure advanced system boot options.



BIOS Menu 12: Boot Settings Configuration

➔ **Quick Boot [Enabled]**

Use the **Quick Boot** BIOS option to make the computer speed up the boot process.

➔ **Disabled** No POST procedures are skipped

➔ **Enabled** **DEFAULT** Some POST procedures are skipped to decrease the system boot time

➔ **Quiet Boot [Disabled]**

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

➔ **Disabled** **DEFAULT** Normal POST messages displayed

➔ **Enabled** OEM Logo displayed instead of POST messages

➔ **AddOn ROM Display Mode [Force BIOS]**

The **AddOn ROM Display Mode** option allows add-on ROM (read-only memory) messages to be displayed.

➔ **Force BIOS** **DEFAULT** Allows the computer system to force a third party BIOS to display during system boot.

➔ **Keep Current** Allows the computer system to display the information during system boot.

➔ **Bootup Num-Lock [Off]**

The **Bootup Num-Lock** BIOS option allows the Number Lock setting to be modified during boot up.

➔ **Off** Does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard lights up when the Number Lock is engaged.

➔ **On** **DEFAULT** Allows the Number Lock on the keyboard to be enabled automatically when the computer system boots up. This allows the immediate use of the 10-key numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard is lit.

➔ **Boot From LAN Support [Disabled]**

The **BOOT From LAN Support** option enables the system to be booted from a remote system.

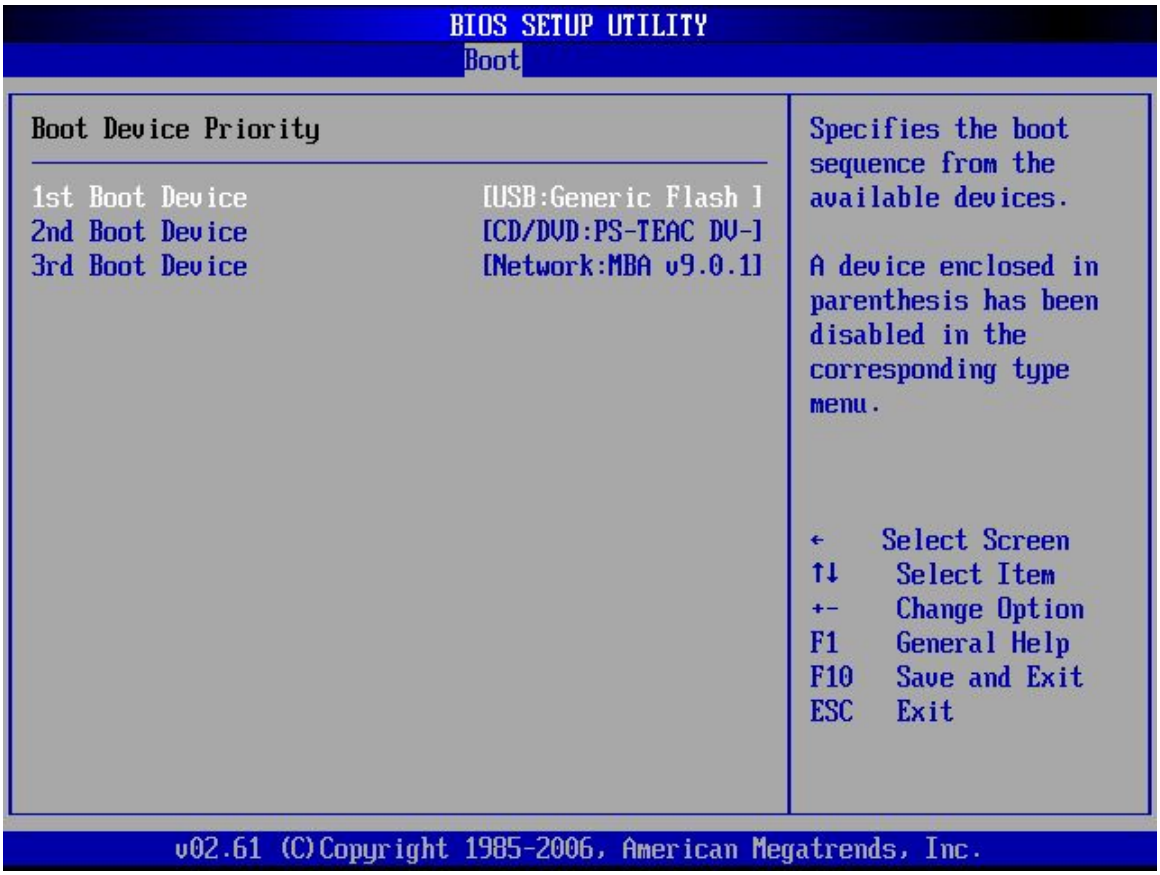
➔ **Disabled** **DEFAULT** Cannot be booted from a remote system through the LAN

➔ **Enabled** **DEFAULT** Can be booted from a remote system through the LAN

6.5.2 Boot Device Priority

Use the **Boot Device Priority** menu (**BIOS Menu 13**) to specify the boot sequence from the available devices. The following options are available:

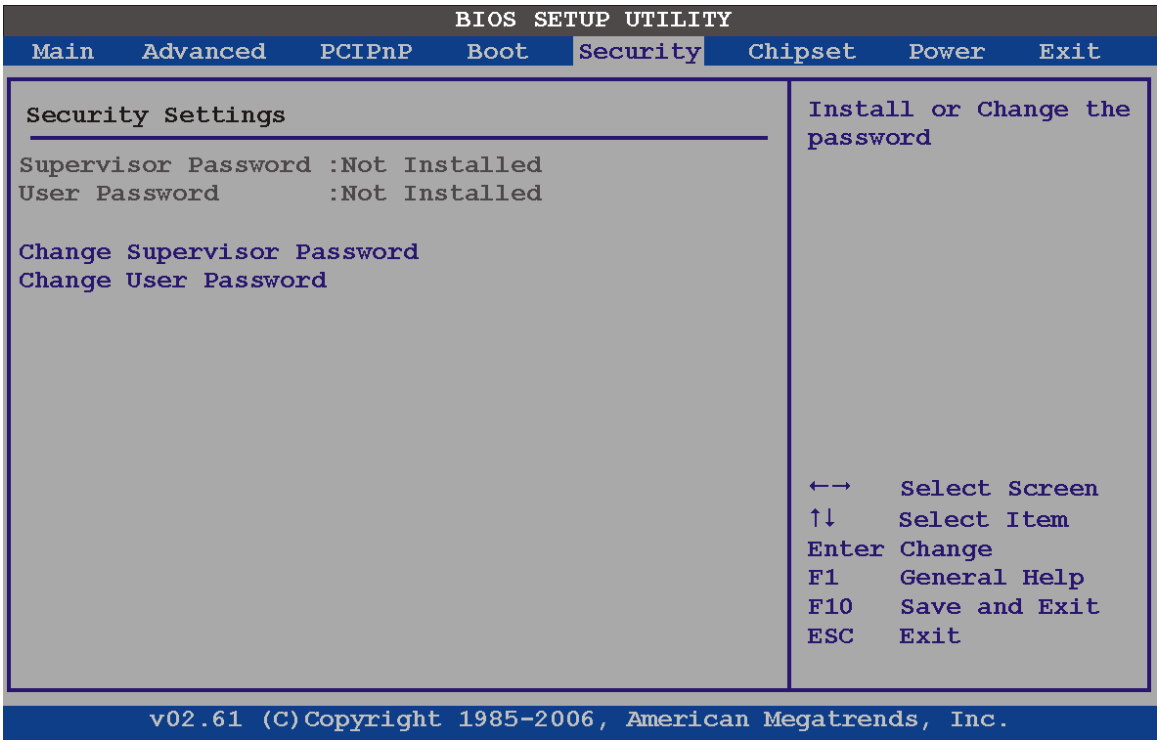
- 1st Boot Device
- 2nd Boot Device
- 3rd Boot Device



BIOS Menu 13: Boot Device Priority Settings

6.6 Security

Use the Security menu (**BIOS Menu 14**) to set system and user passwords.



BIOS Menu 14: Security

➔ **Change Supervisor Password**

Use the **Change Supervisor Password** to set or change a supervisor password. The default for this option is **Not Installed**. If a supervisor password must be installed, select this field and enter the password. After the password has been added, **Install** appears next to **Change Supervisor Password**.

➔ **Change User Password**

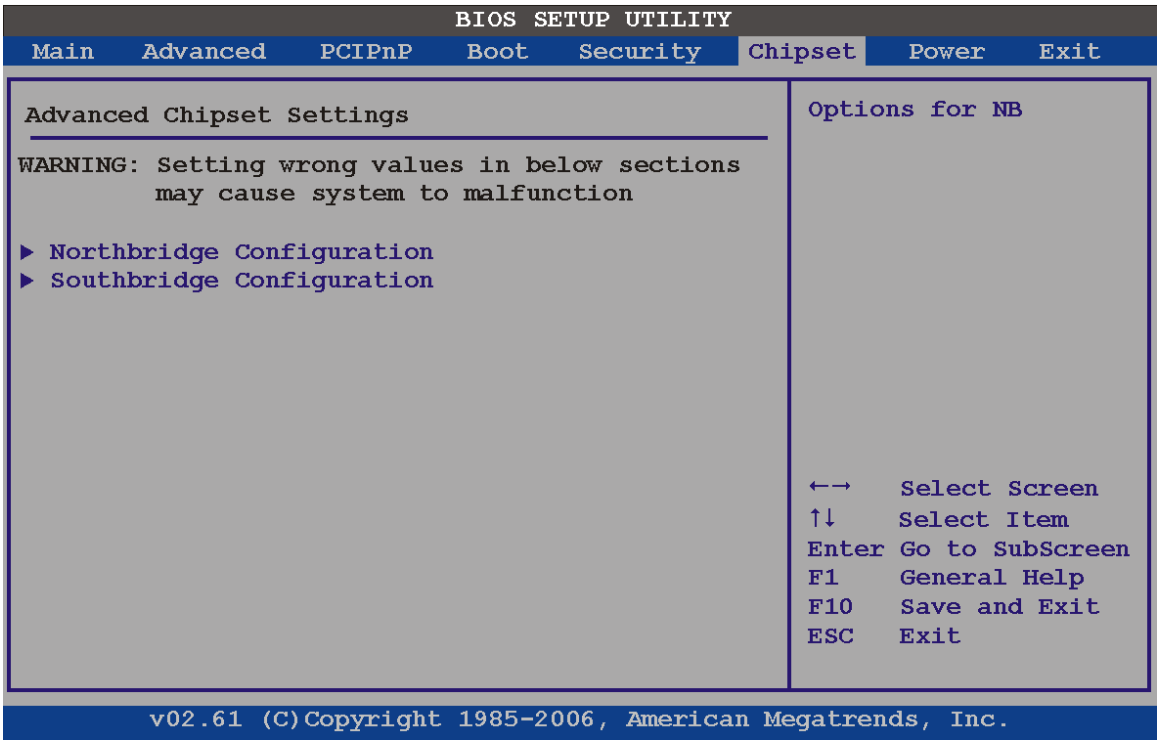
Use the **Change User Password** to set or change a user password. The default for this option is **Not Installed**. If a user password must be installed, select this field and enter the password. After the password has been added, **Install** appears next to **Change User Password**.

6.7 Chipset

Use the **Chipset** menu (**BIOS Menu 15**) to access the Northbridge and Southbridge configuration menus

WARNING!

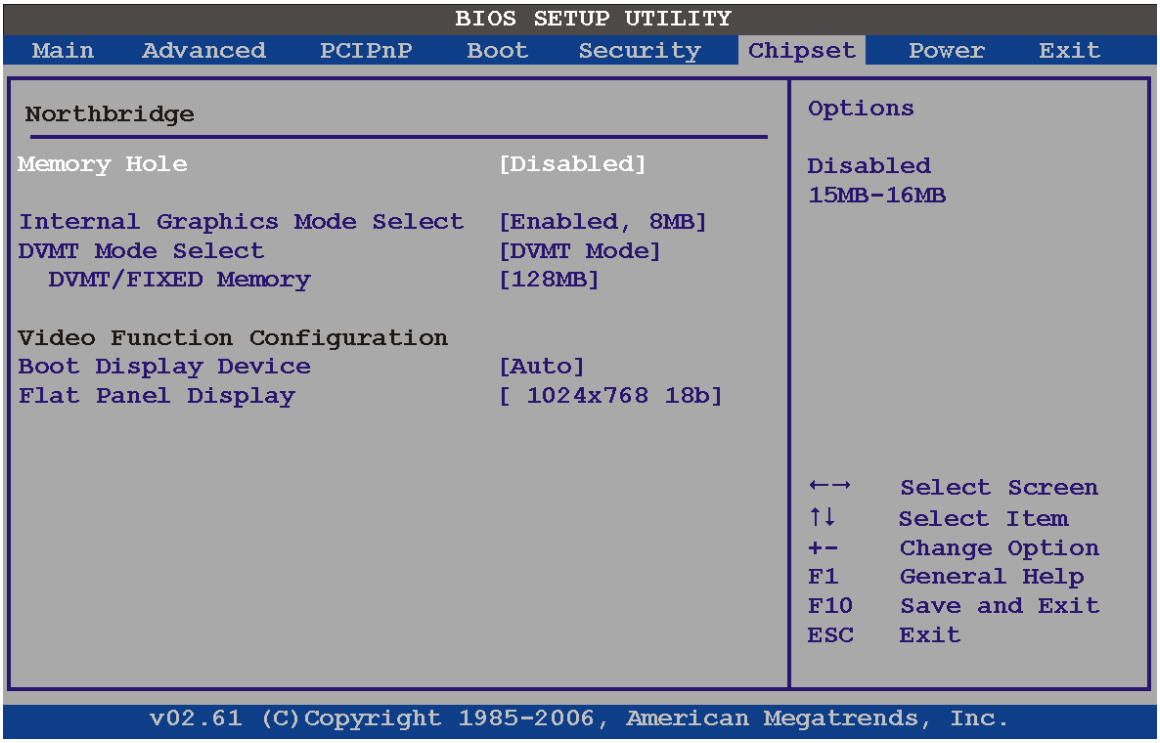
Setting the wrong values for the Chipset BIOS selections in the Chipset BIOS menu may cause the system to malfunction.



BIOS Menu 15: Chipset

6.7.1 Northbridge Chipset Configuration

Use the **Northbridge Chipset Configuration** menu (**BIOS Menu 15**) to configure the Northbridge chipset settings.



BIOS Menu 16: Northbridge Chipset Configuration

➔ **Memory Hole [Disabled]**

The **Memory Hole** reserves the memory space between 15 MB and 16 MB for ISA expansion cards that require a specified area of memory to work properly. If an older ISA expansion card is used, please refer to the documentation that came with the card to see if it is necessary to reserve the space.

➔ **Disabled** **DEFAULT** Memory is not reserved for ISA expansion cards

➔ **Enabled** Memory is reserved for ISA expansion cards

➔ **Internal Graphics Mode Select [Enable, 8 MB]**

The **Internal Graphic Mode Select** option determines the amount of system memory that can be used by the Internal graphics device.

➔ **Disable**		
➔ **Enable, 1 MB**		1 MB of memory used by internal graphics device
➔ **Enable, 8 MB**	**DEFAULT**	8 MB of memory used by internal graphics device

➔ **DVMT Mode Select [DVMT Mode]**

Use the **DVMT Mode Select** option to select the Intel Dynamic Video Memory Technology (DVMT) operating mode.

➔ **Fixed Mode**		A fixed portion of graphics memory is reserved as graphics memory.
➔ **DVMT Mode**	**DEFAULT**	Graphics memory is dynamically allocated according to the system and graphics needs.
➔ **Combo Mode**		A fixed portion of graphics memory is reserved as graphics memory. If more memory is needed, graphics memory is dynamically allocated according to the system and graphics needs.

➔ **DVMT/FIXED Memory**

Use the **DVMT/FIXED Memory** option to specify the maximum amount of memory that can be allocated as graphics memory. This option can only be configured for if **DVMT Mode** or **Fixed Mode** is selected in the **DVMT Mode Selec**t option. If **Combo Mode** is selected, the maximum amount of graphics memory is 128 MB. Configuration options are listed below.

- 64 MB
- 128 MB **DEFAULT**
- Maximum DVMT

➔ **Boot Display Device [Auto]**

The **Boot Display Device** selects the display device to use when the computer is booted up.

➔ **Auto**	**DEFAULT**	The display device is automatically selected from the connected display devices
➔ **CRT**		The device connected to the VGA port is selected
➔ **LFP**		The device connected to the LVDS port is selected

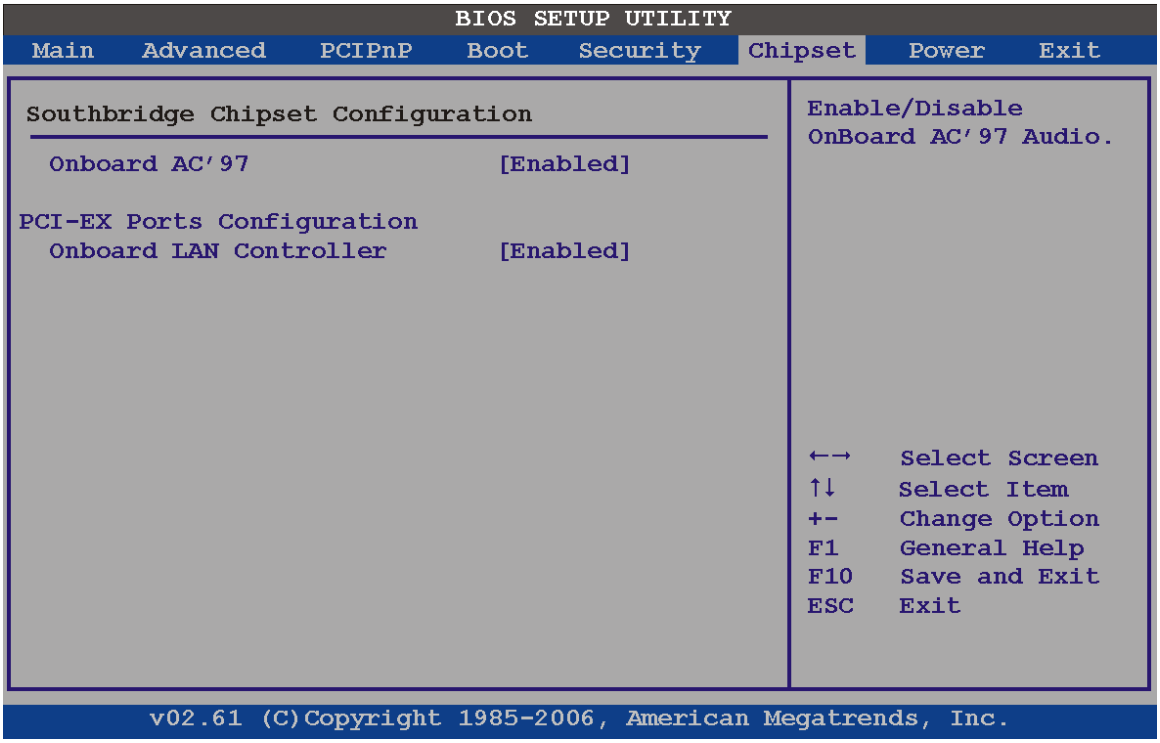
➔ **Flat Panel Type [1024x768 18b]**

The **Flat Panel Type** selection sets the resolution of the LVDS video output. The video output resolution options are shown below.

- 640 x 480, 18-bit
- 800 x 600, 18-bit
- 1024 x 768, 18-bit **DEFAULT**
- 1024 x 768, 24-bit
- 1280 x 1024, 48-bit
- 1600 x 1200, 48-bit
- 1280 x 768, 18-bit
- 1280 x 800, 18-bit
- 1366 x 768, 24-bit

6.7.2 Southbridge Configuration

The **Southbridge Configuration** menu (**BIOS Menu 17**) allows the Southbridge chipset to be configured.



BIOS Menu 17: Southbridge Chipset Configuration

➔ **Audio Controller [All Disabled]**

The **Audio Controller** option enables or disables the audio controller.

➔ **Enabled**	**DEFAULT**	The audio codec is turned on
➔ **Disabled**		The audio codec is turned off

➔ **Onboard LAN Controller [Enabled]**

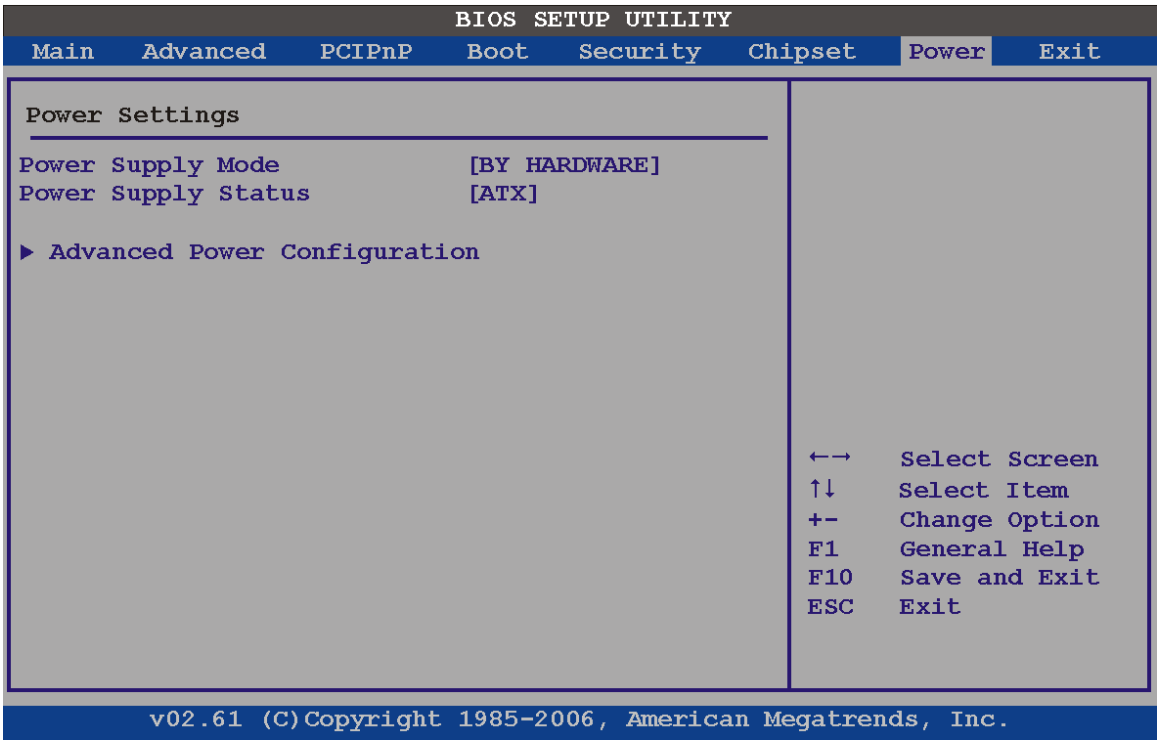
The **Onboard LAN Controller** option enables or disables the PCIe GbE connector.

➔ **Enabled**	**DEFAULT**	The Gigabit Ethernet controller is turned on

➔ **Disabled** The Gigabit Ethernet controller is turned off

6.8 Power Configuration

The **Power Configuration** menu (BIOS Menu 18) configures the Advanced Configuration and Power Interface (ACPI) and Power Management (APM) options.



BIOS Menu 18: Power Configuration

➔ **Power Supply Mode [BY HARDWARE]**

The **Power Supply Mode** option states that the power supply mode is determined by the hardware jumper setting.

➔ **BY HARDWARE** **DEFAULT** The power mode is set using the jumper setting on the board

➔ **AT** The power mode is set to AT, the system will always turn on when power is restored after a power loss

➔ **ATX** The power mode is set to ATX

➔ **Power Supply Status [ATX]**

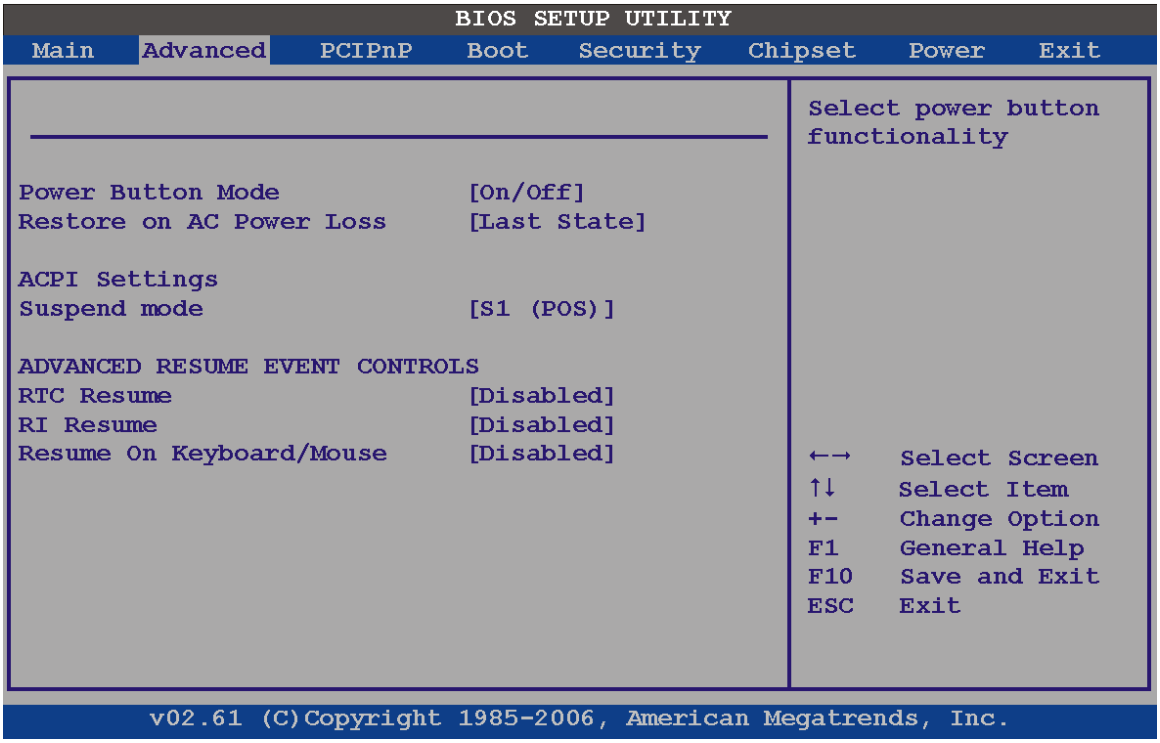
The **Power Supply Status** option shows the current setting of the power mode hardware jumper.

➔ **AT** The power mode is set to AT, the system will always turn on when power is restored after a power loss

➔ **ATX** **DEFAULT** The power mode is set to ATX

6.8.1 Advanced Power Configuration

The **Advanced Power Configuration** menu (**BIOS Menu 19**) configures the Advanced Configuration and Power Interface (ACPI).



BIOS Menu 19: Advanced Power Configuration

➔ **Power Button Mode [On/Off]**

Use the **Power Button Mode** BIOS to specify how the power button functions.

➔ **On/Off**	**DEFAULT**	When the power button is pressed the system is either turned on or off
➔ **Suspend**		When the power button is pressed the system goes into suspend mode

➔ **Restore on AC Power Loss [Last State]**

Use the **Restore on AC Power Loss** BIOS option to specify what state the system returns to if there is a sudden loss of power to the system.

➔ **Power Off**		The system remains turned off
➔ **Power On**		The system turns on
➔ **Last State**	**DEFAULT**	The system returns to its previous state. If it was on, it turns itself on. If it was off, it remains off.

➔ **Suspend Mode [S1(POS)]**

Use the **Suspend Mode** BIOS option to specify the sleep state the system enters when it is not being used.

➔ **S1 (POS)**	**DEFAULT**	System appears off. The CPU is stopped; RAM is refreshed; the system is running in a low power mode.
➔ **S3 (STR)**		System appears off. The CPU has no power; RAM is in slow refresh; the power supply is in a reduced power mode.

➔ **RTC Resume [Disabled]**

Use the **RTC Resume** option to specify the time the system should be roused from a suspended state.

➔ **Disabled**	**DEFAULT**	The real time clock (RTC) cannot generate a wake event
➔ **Enabled**		If selected, the following appears with values that can be selected: RTC Alarm Date (Days) System Time After setting the alarm, the computer turns itself on from a suspend state when the alarm goes off.

➔ **RI Resume [Disabled]**

Use the **RI Resume** BIOS option to enable activity on the RI (ring in) modem line to rouse the system from a suspend or standby state. That is, the system will be roused by an incoming call on a modem.

➔ **Disabled**	**DEFAULT**	Wake event not generated by an incoming call
➔ **Enabled**		Wake event generated by an incoming call

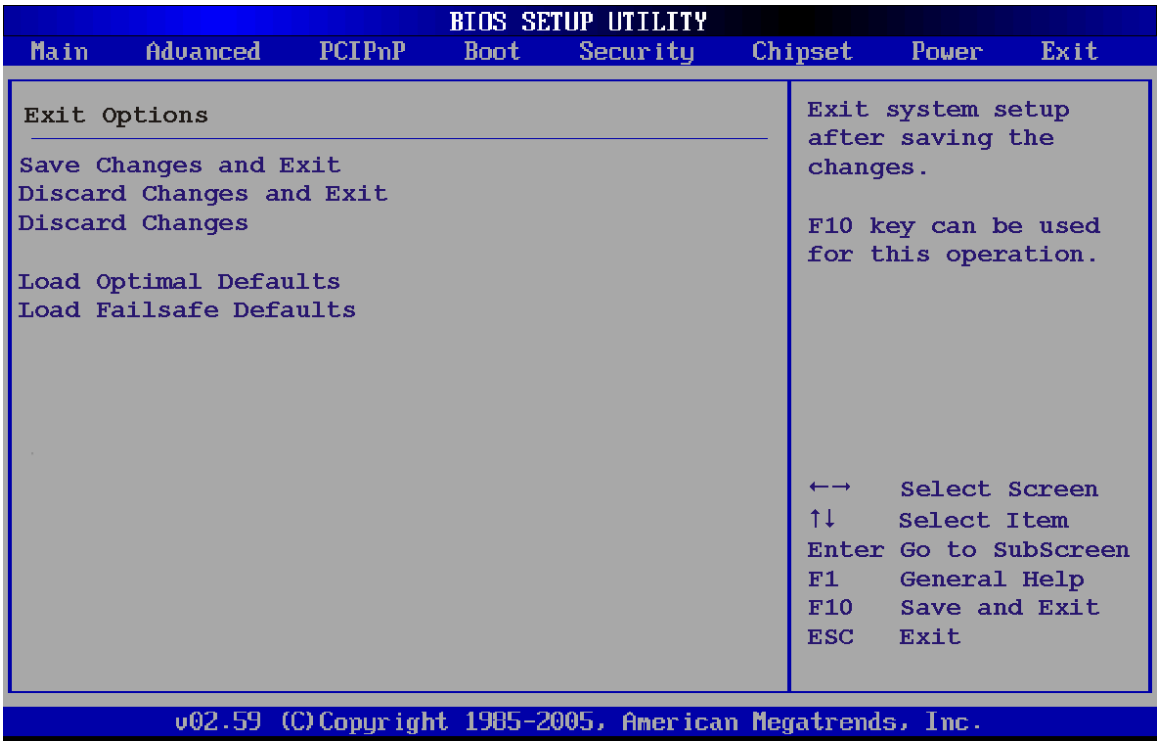
➔ **Resume on Keyboard/Mouse [Disabled]**

Use the **Resume on Keyboard/Mouse** BIOS option to enable activity on either the keyboard or mouse to rouse the system from a suspend or standby state. That is, the system is roused when the mouse is moved or a button on the keyboard is pressed.

➔ **Disabled**	**DEFAULT**	Wake event not generated by activity on the keyboard or mouse
➔ **Enabled**		Wake event generated by activity on the keyboard or mouse

6.9 Exit

Use the **Exit** menu (**BIOS Menu 20**) to load default BIOS values, optimal failsafe values and to save configuration changes.



BIOS Menu 20: Exit

➔ **Save Changes and Exit**

Use the **Save Changes and Exit** option to save the changes made to the BIOS options and to exit the BIOS configuration setup program.

➔ **Discard Changes and Exit**

Use the **Discard Changes and Exit** option to exit the BIOS configuration setup program without saving the changes made to the system.

➔ **Discard Changes**

Use the **Discard Changes** option to discard the changes and remain in the BIOS configuration setup program.

➔ **Load Optimal Defaults**

Use the **Load Optimal Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F9 key can be used for this operation.**

➔ **Load Failsafe Defaults**

Use the **Load Failsafe Defaults** option to load failsafe default values for each of the parameters on the Setup menus. **F8 key can be used for this operation.**

Chapter

7

Software Installation

7.1 Available Software Drivers

NOTE:

The content of the CD may vary throughout the life cycle of the product and is subject to change without prior notice. Visit the IEI website or contact technical support for the latest updates.

The following drivers can be installed on the system:

- Chipset
- VGA
- LAN
- Audio

Installation instructions are given below.

7.2 Starting the Driver Program

To access the driver installation programs, please do the following.

Step 1: Insert the CD-ROM that came with the system into a CD-ROM drive attached to the system.

Step 2: The screen in Figure 7-1 appears.

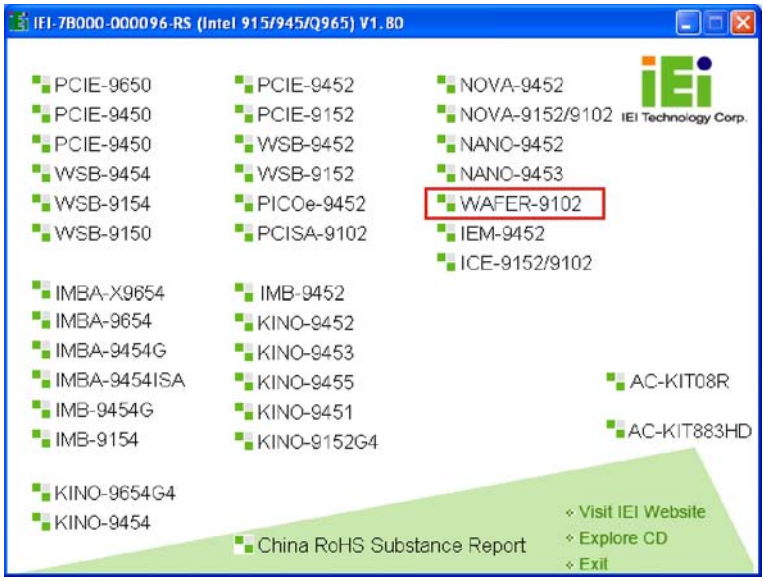


Figure 7-1: Start Up Screen

Step 3: Click WAFER-9102.

Step 4: The list of drivers in in Figure 7-2 appears.

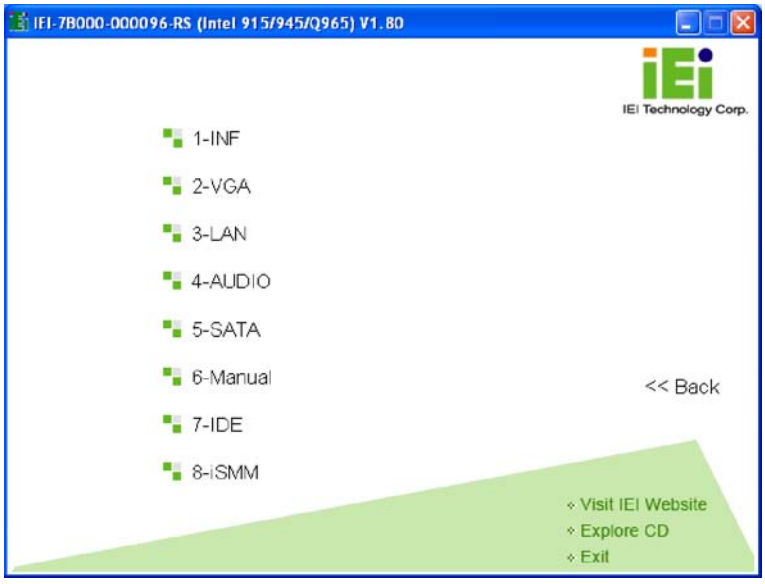


Figure 7-2: Select Operating System

Step 5: Select the driver as directed at the beginning of each subsection below.

7.3 Chipset Driver Installation

To install the chipset driver, please do the following.

Step 1: Access the driver list shown in Figure 7-2. (See **Section 7.2**)

Step 2: Click "**1-INF**"

Step 3: The file explorer window opens (Figure 7-3).

Figure 7-3: Chipset Driver Screen

Step 4: Browse to the "**1-INF\8.3.1.1009**" folder and double-click **infinst_autol**.

Step 5: When the setup files are completely extracted the **Welcome Screen** in Figure 7-4 appears.

Figure 7-4: Chipset Driver Welcome Screen

Step 6: Click NEXT to continue.

Step 7: The license agreement in Figure 7-5 appears.

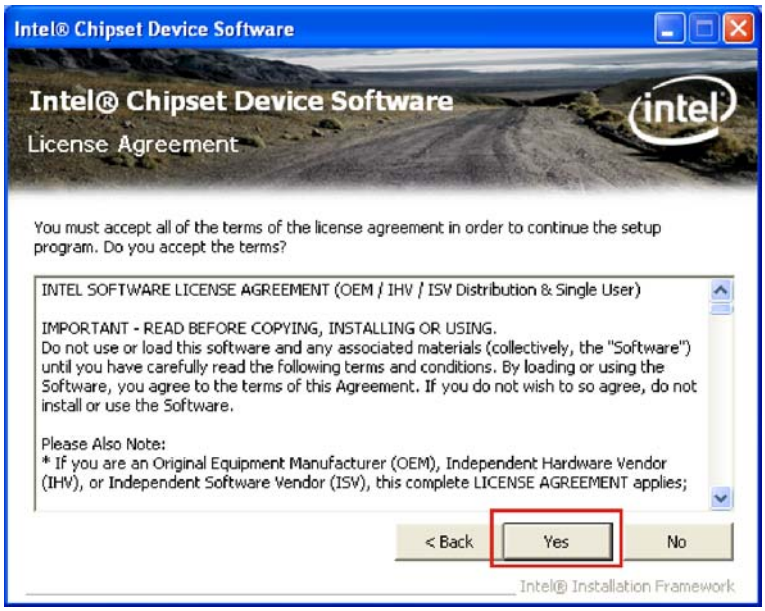


Figure 7-5: Chipset Driver License Agreement

Step 8: Read the **License Agreement**.

Step 9: Click the YES button to accept the agreement and continue.

Step 10: The Read Me file in Figure 7-6 appears.

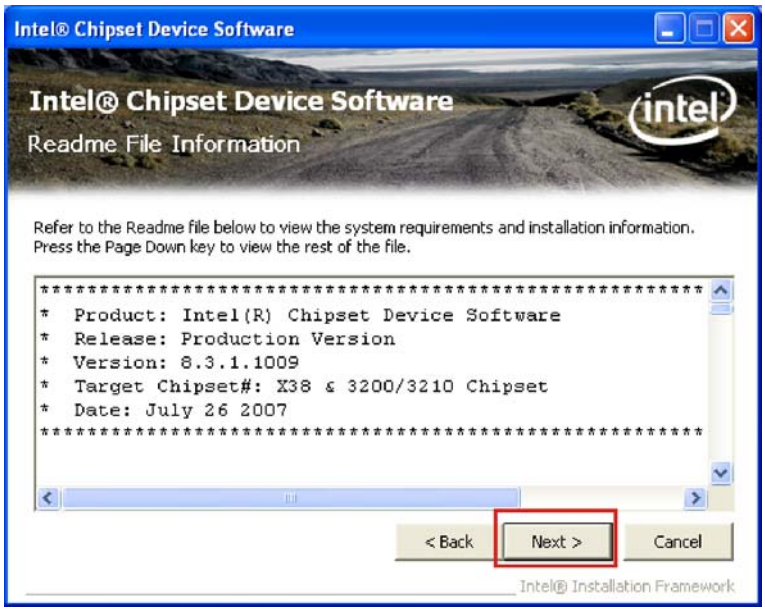


Figure 7-6: Chipset Driver Read Me File

Step 11: Click NEXT to continue.

Step 12: **Setup Operations** are performed as shown in Figure 7-7.

Figure 7-7: Chipset Driver Setup Operations

Step 13: Once the drivers are installed, click the **NEXT** button to continue.

Step 14: The **Setup is Complete** screen appears.

Figure 7-8: Chipset Driver Installation Finish Screen

Step 15: Click the **FINISH** button to exit.

7.4 VGA Driver Installation

To install the VGA driver, please do the following.

Step 1: Access the driver list shown in Figure 7-2. (See **Section 7.2**)

Step 2: Click "**2-VGA**"

Step 3: Browse to "**2-VGA\your-operating-system**" for Windows installations, select the folder shown in Figure 7-9 below.

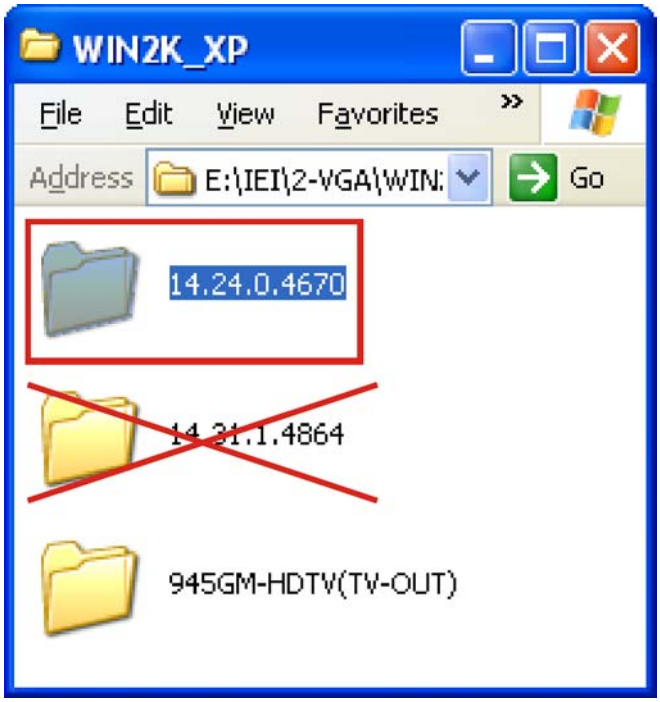


Figure 7-9: VGA Driver Directory

Step 4: Double-click the **win2k_xp1424** icon to begin the installation.

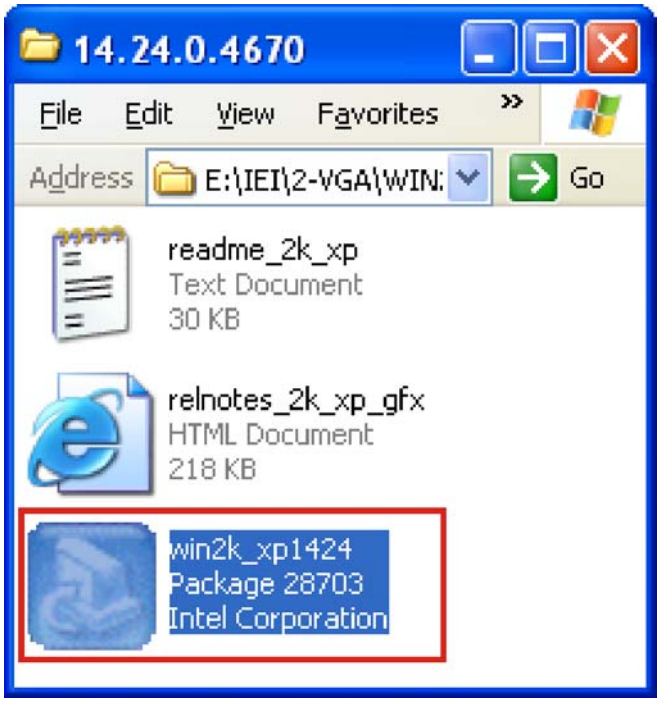


Figure 7-10: VGA Driver Installation File

Step 5: The VGA Read Me file in Figure 7-11 appears.

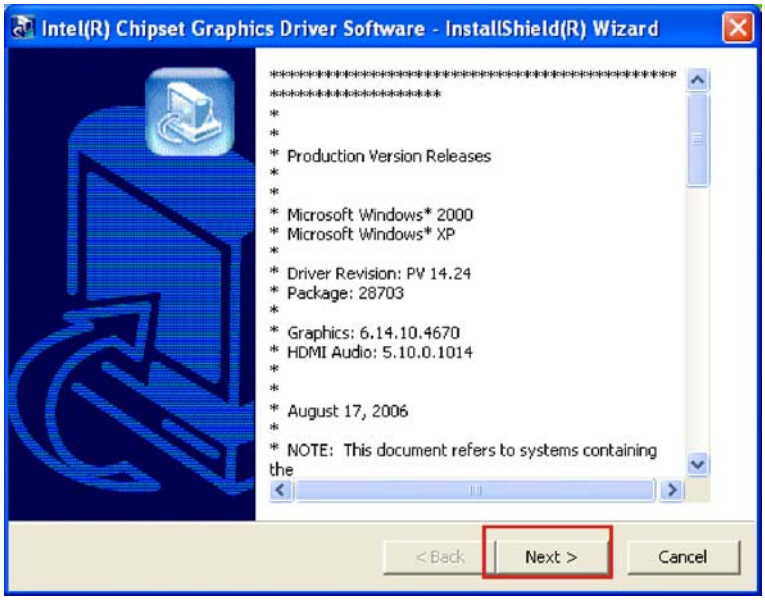


Figure 7-11: VGA Driver Read Me File

Step 6: Click NEXT to continue.

Step 7: The installation files are extracted. See Figure 7-12.

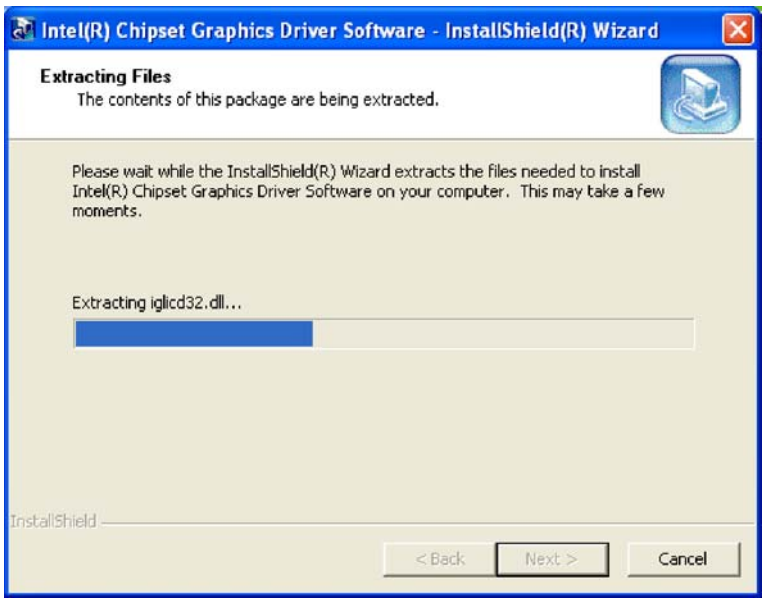


Figure 7-12: VGA Driver Setup Files Extracted

Step 8: The **Welcome Screen** in Figure 7-13 appears.

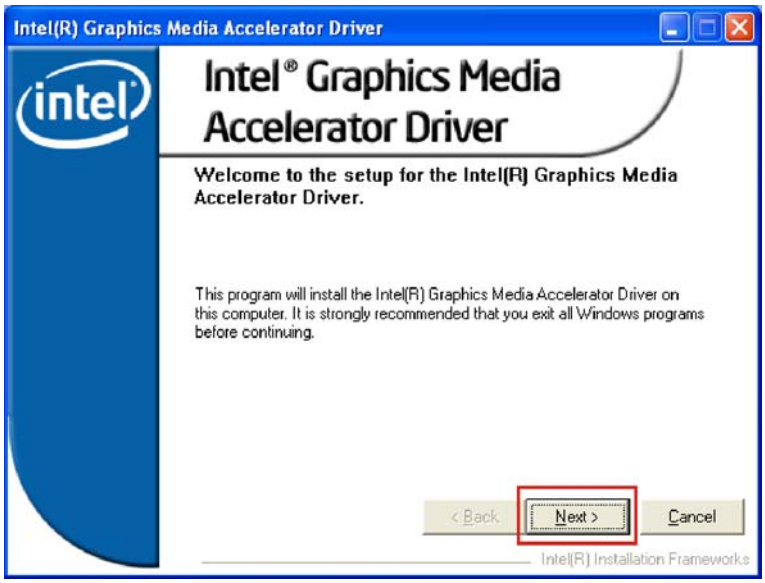


Figure 7-13: VGA Driver Welcome Screen

Step 9: Click NEXT to continue.

Step 10: The license agreement in Figure 7-14 appears.

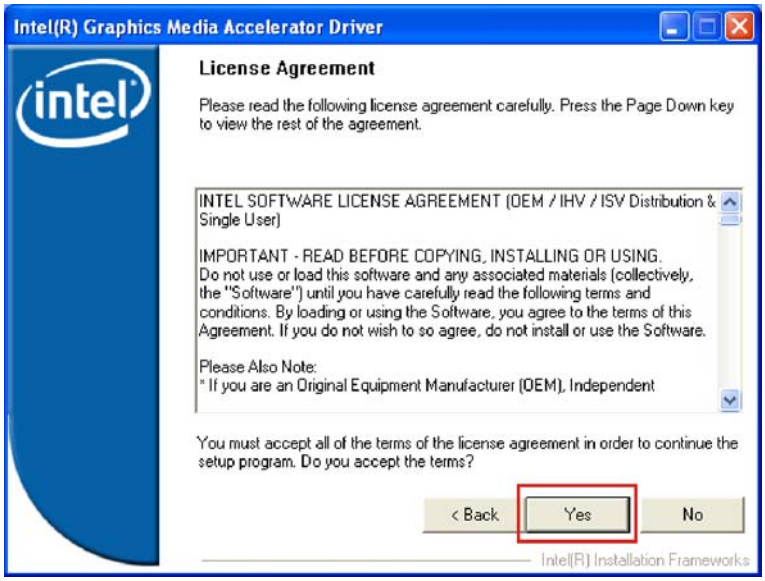


Figure 7-14: VGA Driver License Agreement

Step 11: Read the **License Agreement**.

Step 12: Click the **YES** button to continue.

Step 13: The Readme file in Figure 7-15 appears.

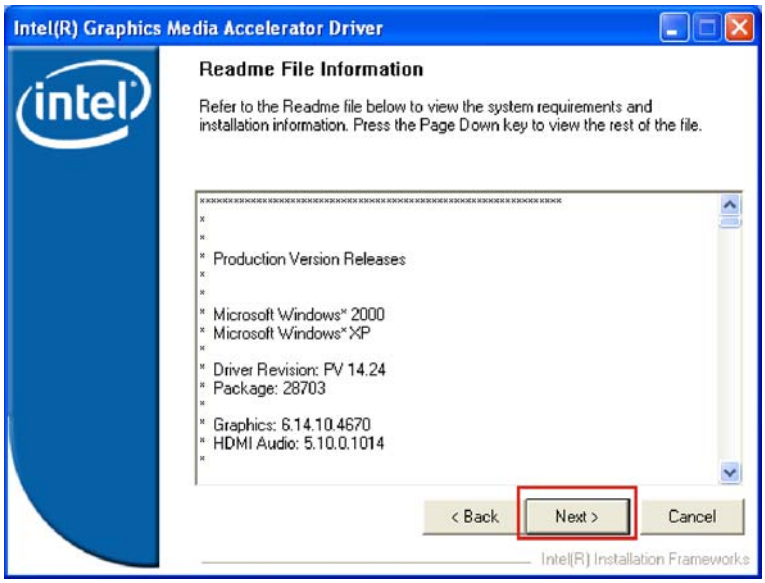


Figure 7-15: VGA Driver Read Me File

Step 14: Click NEXT to continue.

Step 15: **Setup Operations** are performed as shown in Figure 7-16.

NOTE:

The “Found New Hardware Wizard” will appear and then disappear during this step. Do not adjust any settings in the “Found New Hardware Wizard” window.

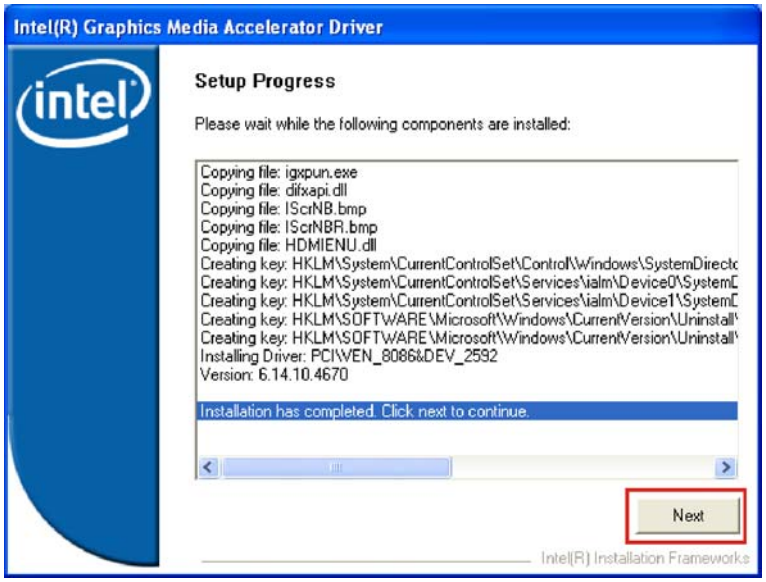


Figure 7-16: VGA Driver Setup Operations

Step 16: Once the **Setup Operations** are complete, click the NEXT button to continue.

Step 17: The **Finish** screen appears.

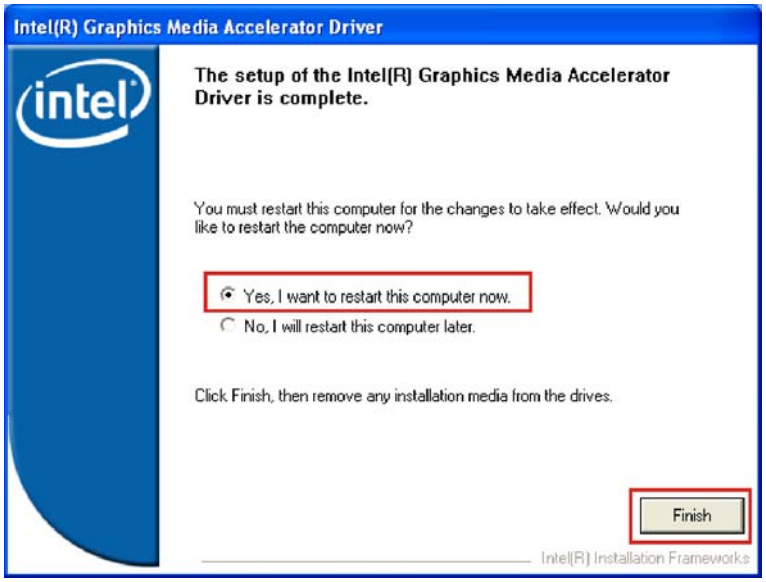


Figure 7-17: VGA Driver Installation Finish Screen

Step 18: Select "**Yes, I want to restart the computer now**" and click the FINISH button.

7.5 LAN Driver Installation

To install the chipset driver, please do the following.

Step 1: Access the driver list shown in Figure 7-2. (See **Section 7.2**)

Step 2: Click "**3-LAN**"

Step 3: Browse through the correct directories for the installed operating system.

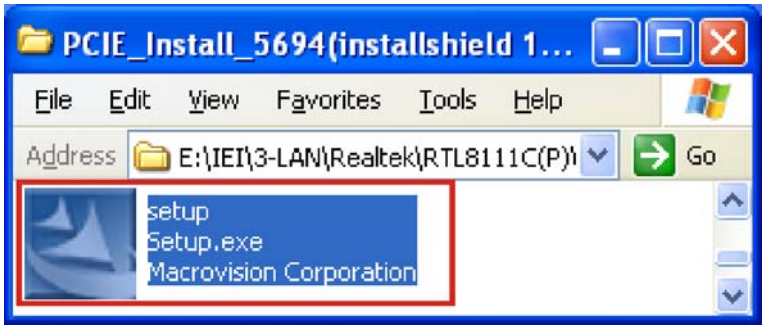


Figure 7-18: LAN Driver Welcome Screen

Step 4: Double-click the **setup** icon to begin the installation

Step 5: The **Welcome** screen in Figure 7-19 appears.

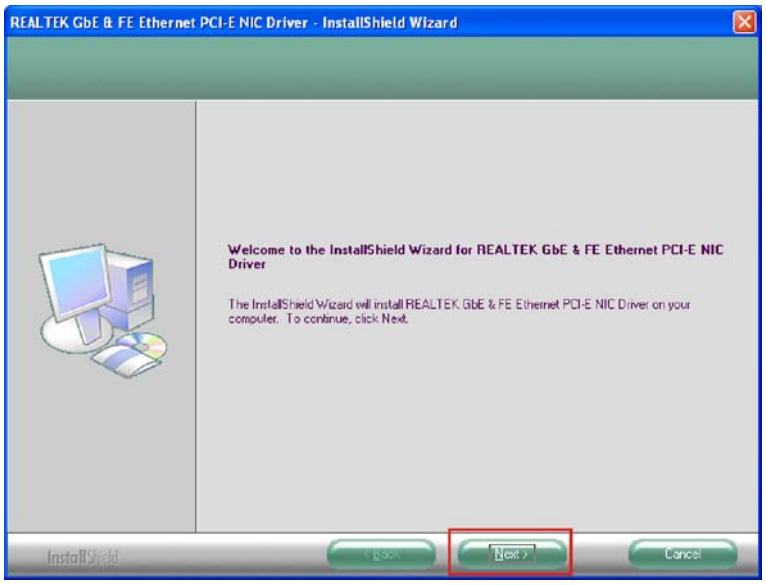


Figure 7-19: LAN Driver Welcome Screen

Step 6: Click NEXT to continue.

Step 7: The **Ready to Install** screen in Figure 7-20 appears.

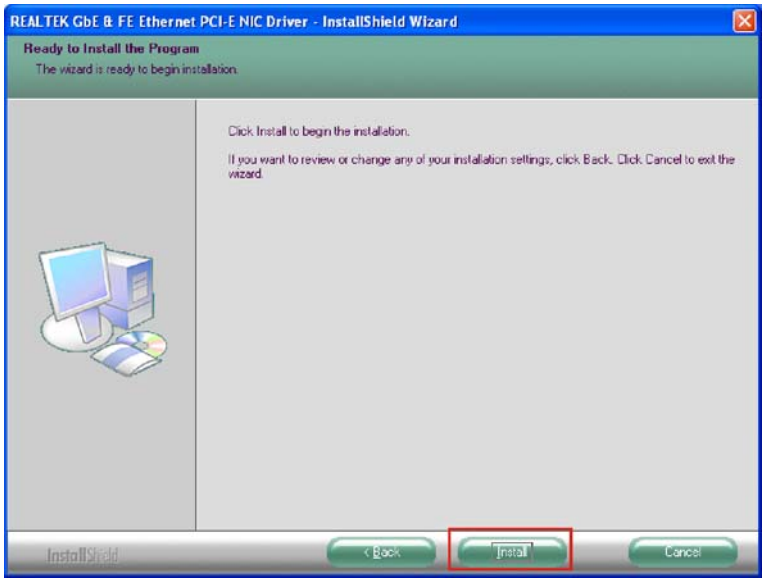


Figure 7-20: LAN Driver Welcome Screen

Step 8: Click NEXT to proceed with the installation.

Step 9: The installation program installs the LAN drivers.

Step 10: When the driver installation is complete, the screen in Figure 7-21 appears.

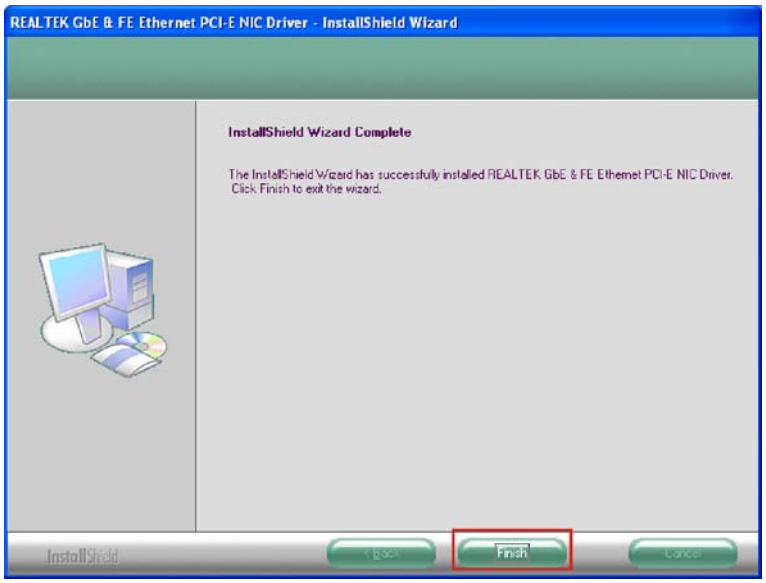


Figure 7-21: LAN Driver Installation Complete

Step 11: Click **FINISH** to exit the InstallShield Wizard (Figure 7-21).

7.6 AC'97 Driver Installation

To install the AC'97 audio driver, please do the following:

Step 1: Select "**4-AUDIO**" in Figure 7-2.

Step 2: Browse to the correct directory for the installed operating system.

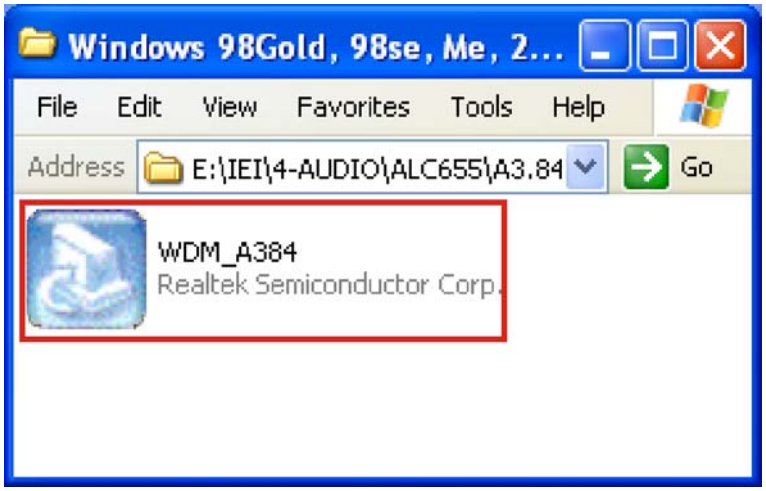


Figure 7-22: AC'97 Driver Installation Welcome Screen

Step 3: The installation files are extracted as shown in Figure 7-23.

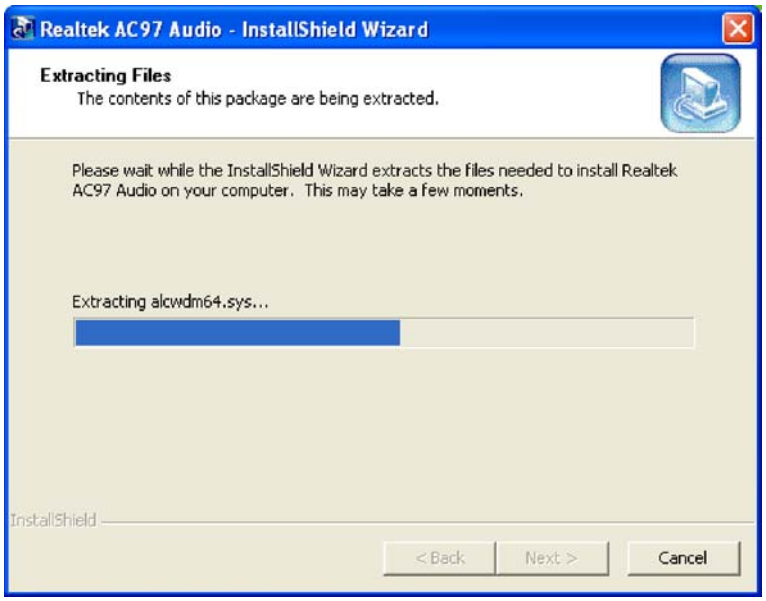


Figure 7-23: AC'97 Driver Installation File Extraction

Step 4: The AC'97 Driver Installation screen in Figure 7-24 appears.

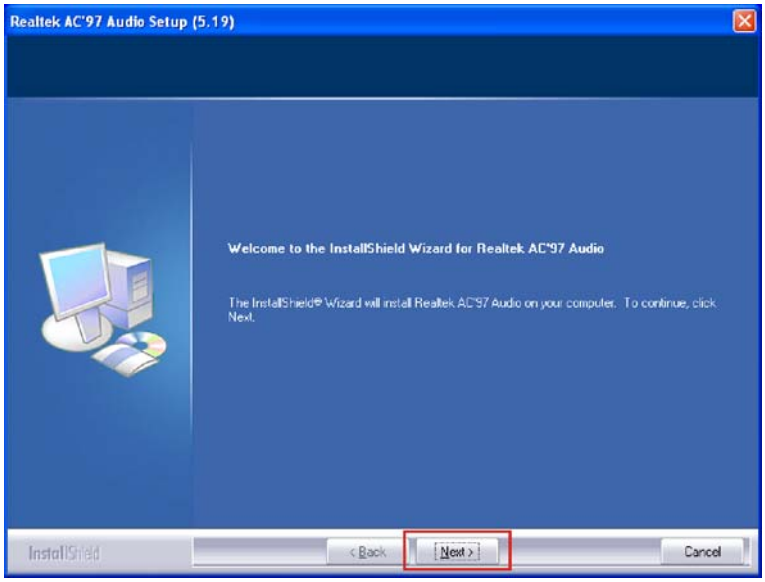


Figure 7-24: AC'97 Driver Installation Welcome Screen

Step 5: Click **NEXT** to continue.

Step 6: When the driver is installed, the driver installation finish screen in Figure 7-25 appears.

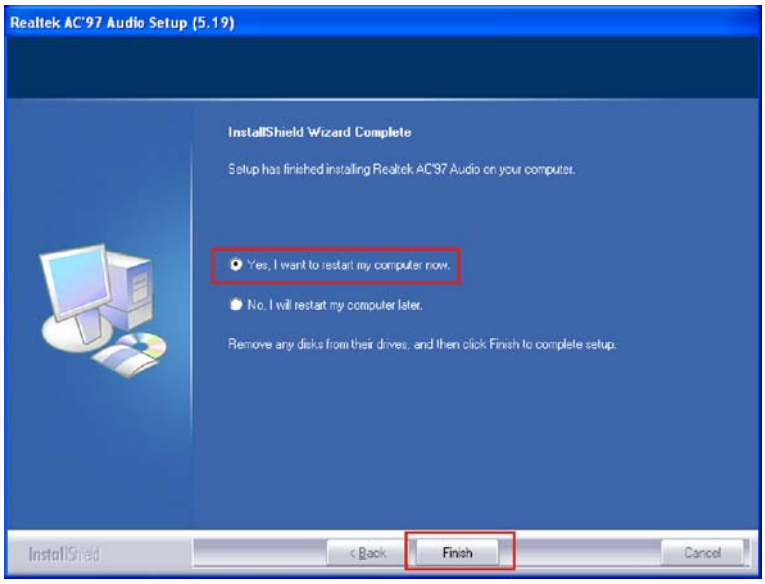


Figure 7-25: AC'97 Driver Installation Complete

Step 7: Select "**Yes, I wish to restart my computer now**" And click **FINISH** to exit the InstallShield Wizard and restart the computer.

Appendix

A

BIOS Options

Below is a list of BIOS configuration options in the BIOS chapter.

Appendix

B

Terminology

AC '97	Audio Codec 97 (AC'97) refers to a codec standard developed by Intel® in 1997.
ACPI	Advanced Configuration and Power Interface (ACPI) is an OS-directed configuration, power management, and thermal management interface.
AHCI	Advanced Host Controller Interface (AHCI) is a SATA Host controller register-level interface.
ATA	The Advanced Technology Attachment (ATA) interface connects storage devices including hard disks and CD-ROM drives to a computer.
ARMD	An ATAPI Removable Media Device (ARMD) is any ATAPI device that supports removable media, besides CD and DVD drives.
ASKIR	Amplitude Shift Keyed Infrared (ASKIR) is a form of modulation that represents a digital signal by varying the amplitude ("volume") of the signal. A low amplitude signal represents a binary 0, while a high amplitude signal represents a binary 1.
BIOS	The Basic Input/Output System (BIOS) is firmware that is first run when the computer is turned on and can be configured by the end user
CODEC	The Compressor-Decompressor (CODEC) encodes and decodes digital audio data on the system.
CompactFlash®	CompactFlash® is a solid-state storage device. CompactFlash® devices use flash memory in a standard size enclosure. Type II is thicker than Type I, but a Type II slot can support both types.
CMOS	Complimentary metal-oxide-conductor is an integrated circuit used in chips like static RAM and microprocessors.
COM	COM refers to serial ports. Serial ports offer serial communication to expansion devices. The serial port on a personal computer is usually a male DB-9 connector.
DAC	The Digital-to-Analog Converter (DAC) converts digital signals to analog signals.
DDR	Double Data Rate refers to a data bus transferring data on both the rising and falling edges of the clock signal.

DMA	Direct Memory Access (DMA) enables some peripheral devices to bypass the system processor and communicate directly with the system memory.
DIMM	Dual Inline Memory Modules are a type of RAM that offer a 64-bit data bus and have separate electrical contacts on each side of the module.
DIO	The digital inputs and digital outputs are general control signals that control the on/off circuit of external devices or TTL devices. Data can be read or written to the selected address to enable the DIO functions.
EHCI	The Enhanced Host Controller Interface (EHCI) specification is a register-level interface description for USB 2.0 Host Controllers.
EIDE	Enhanced IDE (EIDE) is a newer IDE interface standard that has data transfer rates between 4.0 MB/s and 16.6 MB/s.
EIST	Enhanced Intel® SpeedStep Technology (EIST) allows users to modify the power consumption levels and processor performance through application software. The application software changes the bus-to-core frequency ratio and the processor core voltage.
FSB	The Front Side Bus (FSB) is the bi-directional communication channel between the processor and the Northbridge chipset.
GbE	Gigabit Ethernet (GbE) is an Ethernet version that transfers data at 1.0 Gb/s and complies with the IEEE 802.3-2005 standard.
GPIO	General purpose input
HDD	Hard disk drive (HDD) is a type of magnetic, non-volatile computer storage device that stores digitally encoded data.
ICH	The Input/Ouput Controll Hub (ICH) is an Intel® Southbridge chipset.
IrDA	Infrared Data Association (IrDA) specify infrared data transmission protocols used to enable electronic devices to wirelessly communicate with each other.
L1 Cache	The Level 1 Cache (L1 Cache) is a small memory cache built into the system processor.
L2 Cache	The Level 2 Cache (L2 Cache) is an external processor memory cache.

LCD	Liquid crystal display (LCD) is a flat, low-power display device that consists of two polarizing plates with a liquid crystal panel in between.
LVDS	Low-voltage differential signaling (LVDS) is a dual-wire, high-speed differential electrical signaling system commonly used to connect LCD displays to a computer.
POST	The Power-on Self Test (POST) is the pre-boot actions the system performs when the system is turned-on.
RAM	Random Access Memory (RAM) is volatile memory that loses data when power is lost. RAM has very fast data transfer rates compared to other storage like hard drives.
SATA	Serial ATA (SATA) is a serial communications bus designed for data transfers between storage devices and the computer chipsets. The SATA bus has transfer speeds up to 1.5 Gb/s and the SATA II bus has data transfer speeds of up to 3.0 Gb/s.
S.M.A.R.T	Self Monitoring Analysis and Reporting Technology (S.M.A.R.T) refers to automatic status checking technology implemented on hard disk drives.
UART	Universal Asynchronous Receiver-transmitter (UART) is responsible for asynchronous communications on the system and manages the system's serial communication (COM) ports.
UHCI	The Universal Host Controller Interface (UHCI) specification is a register-level interface description for USB 1.1 Host Controllers.
USB	The Universal Serial Bus (USB) is an external bus standard for interfacing devices. USB 1.1 supports 12 Mb/s data transfer rates and USB 2.0 supports 480 Mb/s data transfer rates.
VGA	The Video Graphics Array (VGA) is a graphics display system developed by IBM.

Appendix

C

Digital I/O Interface

C.1 Introduction

The DIO connector on the WAFER-9102 is interfaced to GPIO ports on the Super I/O chipset. The DIO has both 4-bit digital inputs and 4-bit digital outputs. The digital inputs and digital outputs are generally control signals that control the on/off circuit of external devices or TTL devices. Data can be read or written to the selected address to enable the DIO functions.

NOTE:

For further information, please refer to the datasheet for the Super I/O chipset.

C.2 DIO Connector Pinouts

The following table describes how the DIO connector pins are connected to the Digital I/O port.

Pin	Description	Super I/O Pin	Super I/O Pin Description
1	Ground	N/A	N/A
2	VCC	N/A	N/A
3	Output 3	GP23	General Purpose I/O Port 2 Bit 3
4	Output 2	GP22	General Purpose I/O Port 2 Bit 2
5	Output 1	GP21	General Purpose I/O Port 2 Bit 1
6	Output 0	GP20	General Purpose I/O Port 2 Bit 0
7	Input 3	GP33	General Purpose I/O 33
8	Input 2	GP32	General Purpose I/O 32
9	Input 1	GP31	General Purpose I/O 31
10	Input 0	GP30	General Purpose I/O 30

Table C-1: Digital I/O Connector Pinouts

C.3 Assembly Language Samples

C.3.1 Enable the DIO Input Function

The BIOS interrupt call INT 15H controls the digital I/O. An assembly program to enable digital I/O input functions is listed below.

MOV	**AX, 6F08H**	Sets the digital port as input
INT	**15H**	Initiates the INT 15H BIOS call

C.3.2 Enable the DIO Output Function

The BIOS interrupt call INT 15H controls the digital I/O. An assembly program to enable digital I/O output functions is listed below.

MOV	**AX, 6F09H**	Sets the digital port as output
MOV	**BL, 09H**	
INT	**15H**	Initiates the INT 15H BIOS call

Appendix

D

Watchdog Timer

NOTE:

The following discussion applies to DOS environment. IEI support is contacted or the IEI website visited for specific drivers for more sophisticated operating systems, e.g., Windows and Linux.

The Watchdog Timer is provided to ensure that standalone systems can always recover from catastrophic conditions that cause the CPU to crash. This condition may have occurred by external EMIs or a software bug. When the CPU stops working correctly, Watchdog Timer either performs a hardware reset (cold boot) or a Non-Maskable Interrupt (NMI) to bring the system back to a known state.

A BIOS function call (INT 15H) is used to control the Watchdog Timer.

INT 15H:

AH – 6FH Sub-function:	
AL – 2:	Sets the Watchdog Timer's period.
BL:	Time-out value (Its unit-second is dependent on the item "Watchdog Timer unit select" in CMOS setup).

Table D-1: AH-6FH Sub-function

Call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. When the timer value reaches zero, the system resets. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the watchdog timer is disabled if the time-out value is set to zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.

NOTE:

When exiting a program it is necessary to disable the Watchdog Timer, otherwise the system resets.

EXAMPLE PROGRAM:

```
; INITIAL TIMER PERIOD COUNTER

;
W_LOOP:
;

        MOV     AX, 6F02H       ;setting the time-out value
        MOV     BL, 30          ;time-out value is 48 seconds
        INT     15H

;
; ADD THE APPLICATION PROGRAM HERE
;

        CMP     EXIT_AP, 1      ;is the application over?
        JNE     W_LOOP          ;No, restart the application

        MOV     AX, 6F02H       ;disable Watchdog Timer
        MOV     BL, 0           ;
        INT     15H

;
; EXIT ;
```

Appendix

E

Address Mapping

E.1 Direct Memory Access (DMA)

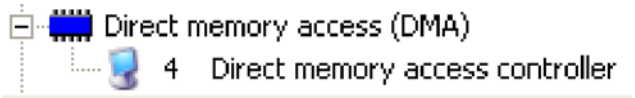


Figure E-1: Direct Memory Access (DMA)

E.2 Input/Output (IO)

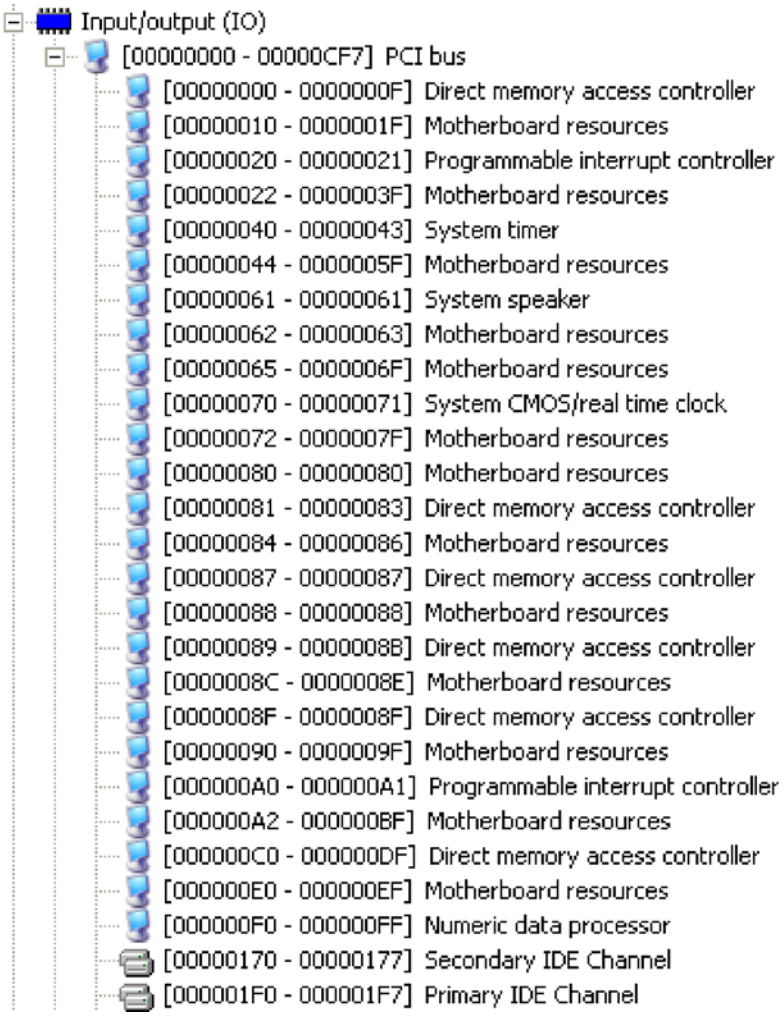


Figure E-2: Input/Output (1 of 2)

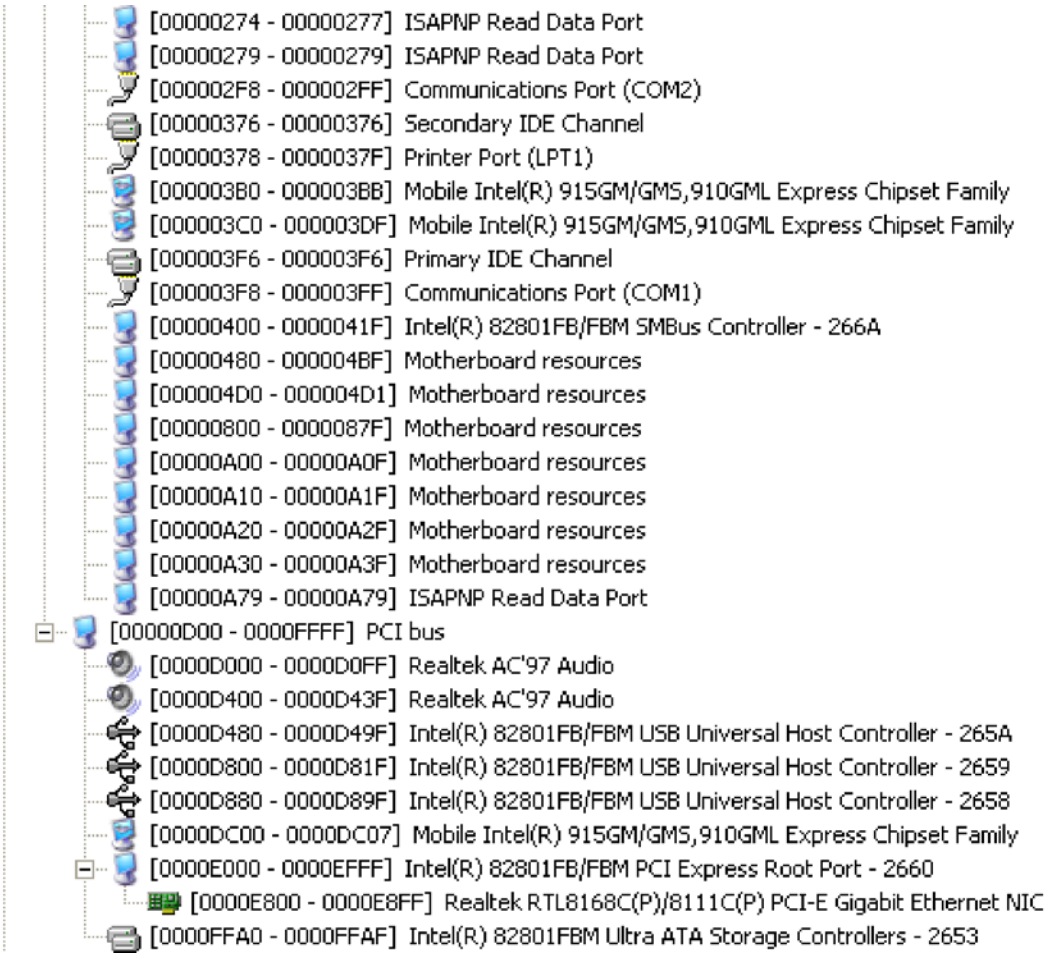


Figure E-3: Input/Output (2 of 2)

E.3 Interrupt Request (IRQ)

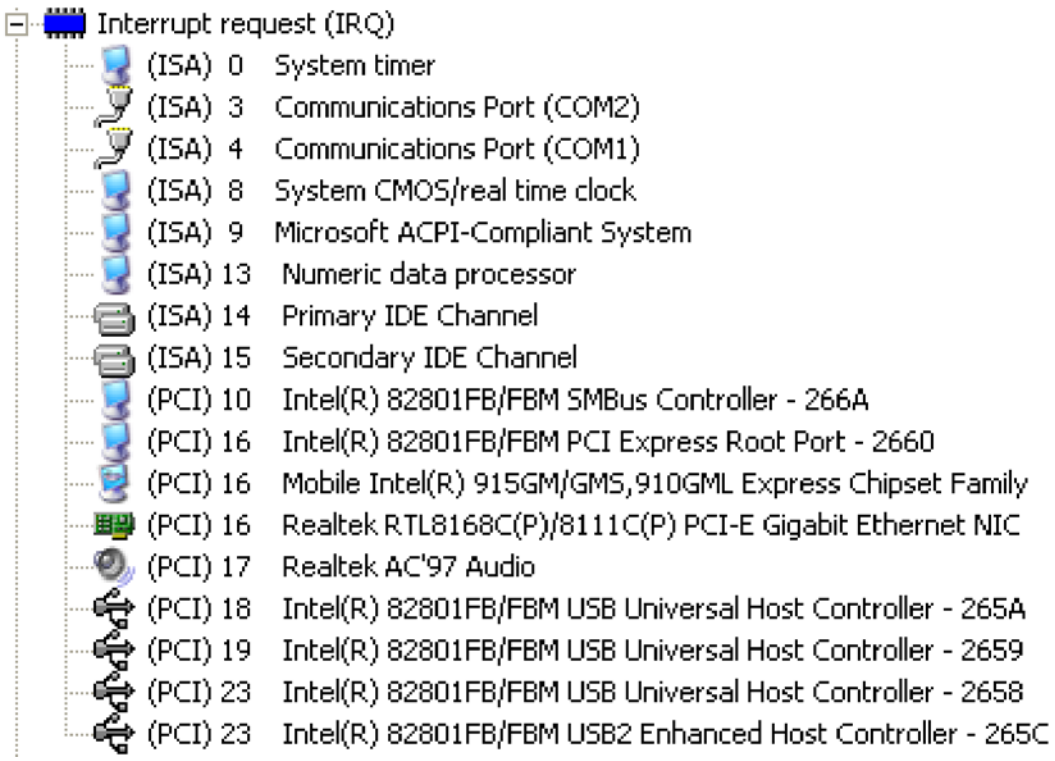


Figure E-4: Interrupt Request (IRQ)

E.4 Memory

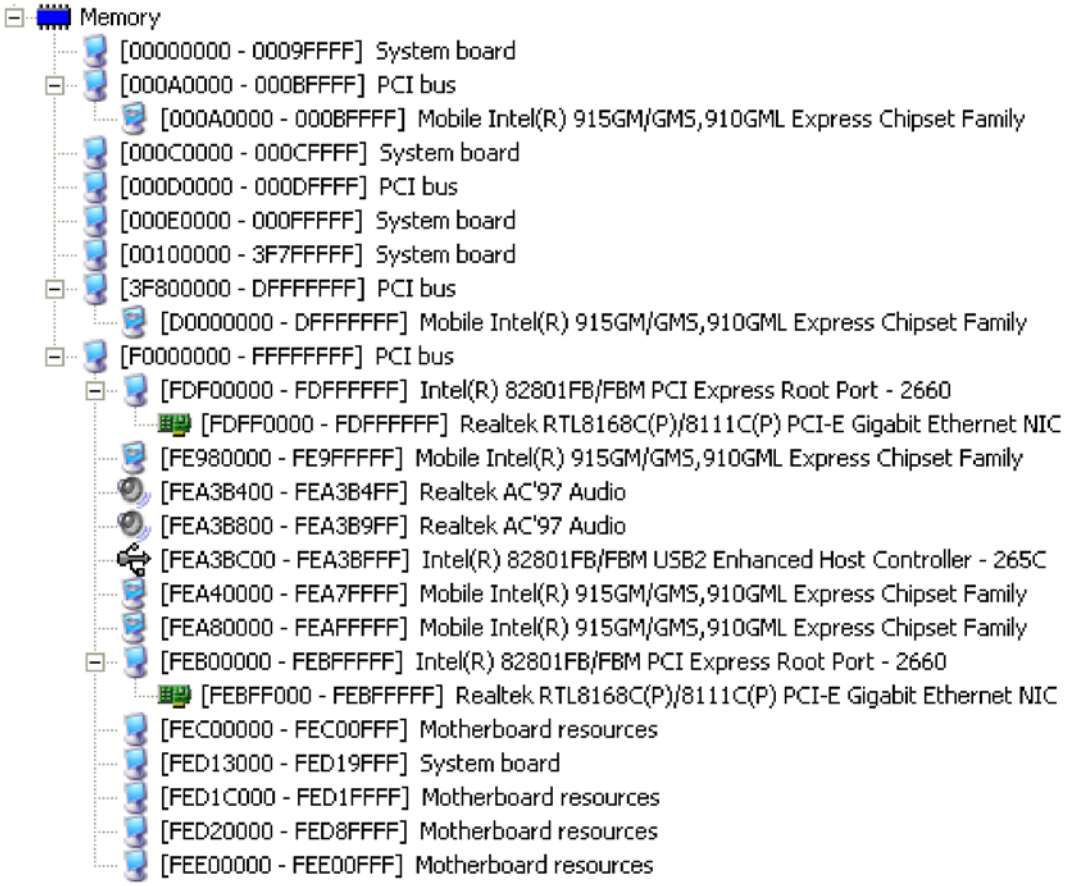


Figure E-5: Memory

Appendix

F

Hazardous Materials Disclosure

F.1 Hazardous Materials Disclosure Table for IPB Products Certified as RoHS Compliant Under 2002/95/EC Without Mercury

The details provided in this appendix are to ensure that the product is compliant with the Peoples Republic of China (China) RoHS standards. The table below acknowledges the presences of small quantities of certain materials in the product, and is applicable to China RoHS only.

A label will be placed on each product to indicate the estimated “Environmentally Friendly Use Period” (EFUP). This is an estimate of the number of years that these substances would “not leak out or undergo abrupt change.” This product may contain replaceable sub-assemblies/components which have a shorter EFUP such as batteries and lamps. These components will be separately marked.

Please refer to the table on the next page.

Part Name	Toxic or Hazardous Substances and Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (CR(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
Housing	X	O	O	O	O	X
Display	X	O	O	O	O	X
Printed Circuit Board	X	O	O	O	O	X
Metal Fasteners	X	O	O	O	O	O
Cable Assembly	X	O	O	O	O	X
Fan Assembly	X	O	O	O	O	X
Power Supply Assemblies	X	O	O	O	O	X
Battery	O	O	O	O	O	O

O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in SJ/T11363-2006

X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in SJ/T11363-2006

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有"环境友好使用期限"的标签，此期限是估算这些物质"不会有泄漏或突变"的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (CR(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
壳体	X	O	O	O	O	X
显示	X	O	O	O	O	X
印刷电路板	X	O	O	O	O	X
金属螺帽	X	O	O	O	O	O
电缆组装	X	O	O	O	O	X
风扇组装	X	O	O	O	O	X
电力供应组装	X	O	O	O	O	X
电池	O	O	O	O	O	O
O: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T11363-2006 标准规定的限量要求以下。 X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T11363-2006 标准规定的限量要求。						

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