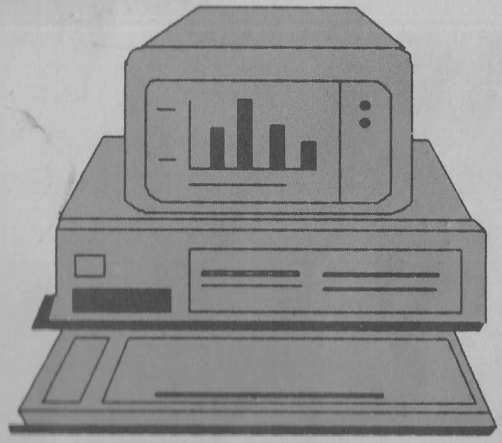
UMC 286 M/B

USER MANUAL



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SPECIFICATION & FEATURES

* 80286 10Mhz or 12Mhz CPU
* 12/16 MHz speed hardware and software selectable
* Up to 4 MB memory on board
* 16 MB expandable memory in the protect virtual address mode
* 2 sockets ROM BIOS
* 6 I/O expansion slots
* Socket for 80287 Math Processor
* CMOS clock and calendar with rechargeable battery
* 24-bit addressing and 16-bit data path capabilities
* 16-level interrupts
* 7-channel DMA (Direct Memory Access)
* 3-programmable timers
* Fully PC/AT compatible operation
* 4 Layers implementation for low noise operation

Jumpers Selection & Connector

JUMPER #	FUNCTION
SW1 [1]	Monitor Selection
JP1	Power Good Selection
JP2	Low Byte Memory Parity Check Selector
JP3	High Byte Memory Parity Check Selector
J17	Reset Jumper
J15	Turbo SW
J16	Turbo LED Connector
J18	Speaker Connector
J19	Key-lock & Power LED Connector
J1	External Battery Connector
SW1 [2,3,4]	Memory Configuration Switch

Power Supply Connector

PIN	ASSIGNMENT	WIRE COLOR
1	Power Good	Orange
2	+ 5V	Red
3	+ 12V	Yellow
4	- 12V	Blue
5	Ground	Black
6	Ground	Black
7	Ground	Black
8	Ground	Black
9	- 5V	White
10	+ 5V	Red
11	+ 5V	Red
12	+ 5V	Red

External Battery Connector [J1]	
PIN	ASSIGNMENT
1	6V DC
2	Not used
3	Ground
4	Ground

[J19] Keylock/Power LED	
PIN	ASSIGNMENT
1	Power LED
2	Not used
3	Ground
4	Keyboard inhibit
5	Ground

Speaker Connector [J18]	
PIN	ASSIGNMENT
1	Data out
2	Not used
3	Ground
4	+ 5V

Low & High Memory Parity Check Selector	
DRAM PARITY ENABLE	DRAM PARITY DISABLE
1 ⊠⊠□ 3 JP2 1 ⊠⊠□ 3 JP3	1 □⊠⊠ 3 JP2 1 □⊠⊠ 3 JP3
When parity disable,the parity DRAM is not necessary (U25, U26, U15, U16)	

[JP1] Power Good Selector	
External	Internal
1 ⊠⊠ 2 PS PG	1 □□ 2 PG O.B.P

TURBO LED Connector [J16] -LED light connector for TURBO SW.

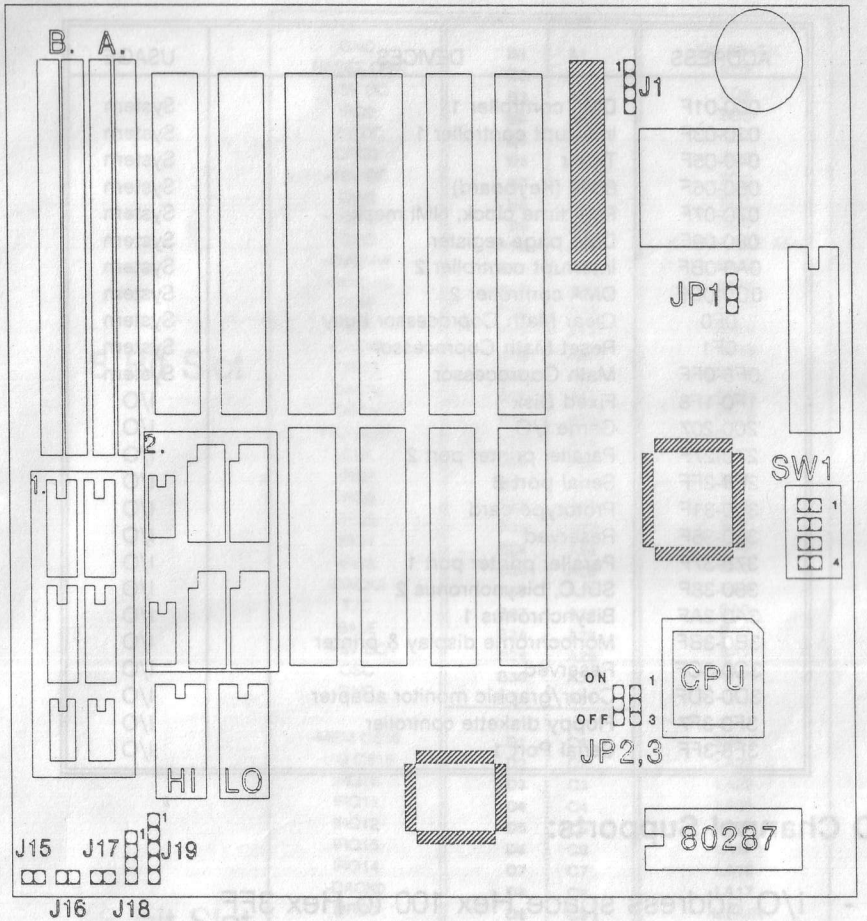
Reset Jumper [J17] -The system will be reset,if the jumper is on.

Monitor Selection [SW1 {1}] -Select OFF for MONO display, ON for COLOR display.

System Memory Map

ADDRESS	FUNCTION
000000-07FFFF	System memory (512K)
080000-09FFFF	System memory (128K)
0AFFFF-08FFFF	Display card buffer (128K)
0C0000-0DFFFF	Expansion ROM (128K)
0E0000-0EFFFF	System usage (64K)
0F0000-0FFFFF	BIOS (64K)
100000-11FFFF	System memory (128K)
120000-15FFFF	System memory (128K)
160000-FDFFFF	Expansion RAM (14870K)
FE0000-FEFFFF	System usage (64K)
FF0000-FFFFFF	BIOS

DRAM TYPE/SIZE CONFIGURATION					
SW1[2]	SW1[3]	SW1[4]	BANK0	BANK1	TOTAL
ON	ON	ON	256K	-	512K
OFF	ON	ON	256K	64K	640K
ON	OFF	ON	256K	256K	1MEG
OFF	OFF	ON	1MEGA	-	2MEG
ON	ON	OFF	1MEGA	1MEGA	4MEG



* BANK0 [1.,A.]
BANK1 [2.,B.]

Jumpers & Connectors Location Diagram

I/O Address Map

ADDRESS	DEVICES	USAGE
000-01F	DMA controller 1	System
020-03F	Interrupt controller 1	System
040-05F	Timer	System
060-06F	8042 (Keyboard)	System
070-07F	Real time clock, NMI mask	System
080-09F	DMA page register	System
0A0-0BF	Interrupt controller 2	System
0C0-0DF	DMA controller 2	System
0F0	Clear Math Coprocessor busy	System
0F1	Reset Math Coprocessor	System
0F8-0FF	Math Coprocessor	System
1F0-1F8	Fixed Disk	I/O
200-207	Game I/O	I/O
278-27F	Parallel printer port 2	I/O
2F8-2FF	Serial port 2	I/O
300-31F	Prototype card	I/O
360-36F	Reserved	I/O
378-37F	Parallel printer port 1	I/O
380-38F	SDLC, bisynchronus 2	I/O
3A0-3AF	Bisynchronus 1	I/O
3B0-3BF	Monochrome display & printer	I/O
3C0-3CF	Reserved	I/O
3D0-3DF	Color/graphic monitor adapter	I/O
3F0-3F7	Floppy diskette controller	I/O
3F8-3FF	Serial Port 1	I/O

I/O Channel Supports:

- I/O address space Hex 100 to Hex 3FF
- 24-bit memory address (16MB)
- Refresh of system memory from channel microprocessors
- Selection of data accesses (either 8 bit or 16 bit)
- Interrupt
- DMA channels
- I/O wait-state generation
- Open-bus structure (allowing multiple microprocessors to share the system's resources, including memory)

I/O Slots Pin Assignment:

	GND	B1	A1	-I/O CH CK
	RESET DRV	B2	A2	SD7
	+5V DC	B3	A3	SD6
	IRQ2	B4	A4	SD5
	-5V DC	B5	A5	SD4
	DRQ2	B6	A6	SD3
	-12V DC	B7	A7	SD2
	OWS	B8	A8	SD1
	+12V DC	B9	A9	SD0
	GND	B10	A10	-I/O CH RDY AEN
	-SMEMW	B11	A11	SA19
	-SMEMR	B12	A12	SA18
	-IOW	B13	A13	SA17
	-IOR	B14	A14	SA16
	-DACK3	B15	A15	SA15
8 Bit Slot	DRQ3	B16	A16	SA14
	-DACK1	B17	A17	SA13
	DRQ1	B18	A18	SA12
	-REFRESH	B19	A19	SA11
	CLK	B20	A20	SA10
	IRQ7	B21	A21	SA9
	IRQ6	B22	A22	SA8
	IRQ5	B23	A23	SA7
	IRQ4	B24	A24	SA6
	IRQ3	B25	A25	SA5
	-DACK2	B26	A26	SA4
	T/C	B27	A27	SA3
	BALE	B28	A28	SA2
	+5V DC	B29	A29	SA1
	OSC	B30	A30	SA0
	GND	B31	A31	
	-MEM CS16	D1	C1	SBHE
	-I/O CS16	D2	C2	LA23
	IRQ16	D3	C3	LA22
	IRQ11	D4	C4	LA21
	IRQ12	D5	C5	LA20
	IRQ15	D6	C6	LA19
	IRQ14	D7	C7	LA18
	-DACK0	D8	C8	LA17
16 bit Slot	DRQ0	D9	C9	-MEMR
	-DACK5	D10	C10	-MEMW
	DRQ5	D11	C11	SD08
	-DACK6	D12	C12	SD09
	DRQ6	D13	C13	SD10
	-DACK7	D14	C14	SD11
	DRQ7	D15	C15	SD12
	+5V DC	D16	C16	SD13
	-MASTER	D17	C17	SD14
	GND	D18	C18	SD15

System Timers The system has 3 programmable timer/counters controlled by 8254 timer/counter. These are channels 0 through 2, defined as follows:

Channel 0	System timer
GATE 0 CLK IN 0 CLK OUT 0	Tied on 1.190 MHz OSC 8259A IRQ

Channel 1	Refresh Request Generator
GATE 1 CLK IN1 CLK OUT 1	Tied on 1.190 MHz OSC Request Refresh Cycle

Channel 2	Tone Generation for Speaker
Gate 2 CLK IN 2 CLK OUT 2	Controlled by bit 0 of port HEX 61 PPI bit 1.190 MHz OSC Used to drive the speaker

System Interrupts 16 levels of system interrupts are proved by the 80286 NMI and two 8259A Interrupt Controller. The following shows the interrupt-level assignments in decreasing Priority:

LEVEL		FUNCTION
Microprocessor NMI Interrupt controllers		Parity or I/O channel check
Ctrl 1	**Ctrl 2**	
IRQ 0		Timer output 0
IRQ 1		Keyboard (output buffer full)
IRQ 2		Interrupt from CTLR 2
	IRQ 8	Realtime clock interrupt
	IRQ 9	Software redirected to INT OAH
	IRQ 10	Reserved
	IRQ 11	Reserved
	IRQ 12	Reserved
	IRQ 13	Coprocessor
	IRQ 14	Fixed disk controller
	IRQ 15	Reserved
IRQ 3		Serial port 2
IRQ 4		Serial port 1
IRQ 5		Parallel port 2
IRQ 6		Diskette controller
IRQ 7		Parallel port 1

Direct Memory Access 8 DMA channels are supported by the system. Two 8237 DMA controller (four channels in each) are used. DMA channels are assigned as follows:

CTRL 1	CTRL 2
Ch 0 - Space	Ch 4 - Cascade for CTRL 1
Ch 1 - SDLC	Ch 5 - Space
Ch 2 - Diskette	Ch 6 - Space
Ch 3 - Space	Ch 7 - Space

Channel 0 through 3 are contained in DMA controller 1. Transfers of 8-bit data, 8-bit I/O adapters and 8-bit or 16-bit system memory are supported by these channels. Each of these channels will transfer data in 64KB blocks throughout the 16-megabyte system address space.

Channel 4 through 7 are contained in DMA controller 2. To cascade channels 0 through 3 to the microprocessor, use channel 4. Transfers of 16-bit data between 16-bit adapters and 16-bit system memory are supported by channels 5,6,7. DMA channels 5 through 7 will transfer data in 128KB blocks throughout the 16-megabyte system address space. These channels will not transfer data on odd-byte boundaries.

The address for the page register are as follows:

PAGE REGISTER	I/O HEX ADDRESS
DMA channel 0	0087
DMA channel 1	0083
DMA channel 2	0081
DMA channel 3	0082
DMA channel 5	008B
DMA channel 6	0089
DMA channel 7	008A
Refresh	008F

Address generation for the DMA channels is as follows:

For DMA channels 3 through 0

SOURCE	DMA PAGE REGISTERS	8237A
Address	A23--------A16	A15--A0

Note To generate the addressing signal "byte high enable"(BHE) invert address line A0.

For DMA channels 7 through 5

SOURCE	DMA PAGE REGISTERS	8237A
Address	A23--------A17	A16--A1

Note The BHE and A0 addressing signals are forced to a logic 0. DMA channel addresses do not increase or decrease through page boundaries (64KB for channels 0 through 3 and 128KB for channels 5 through 7).

Real Time Clock And Nonvolatile Ram - The real time clock 146818 and its 64 bytes of RAM information are backed up by 6V DC battery. The internal clock circuitry uses 14 bytes while the rest is allocated to system configuration.

ADDRESS	Real Time Clock & NV Ram Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status Register A
0B	Status Register B
0C	Status Register C
0D	Status Register D
0E	Diagnostic status byte
0F	Shutdown
10	Diskette driver type, A and B
11	Reserved
12	Fixed disk type, C and D
13	Reserved
14	Equipment byte
15	Low base memory
16	High base memory
17	Low expansion memory byte
618	High expansion memory byte
19-2D	Reserved
2E-2F	2 byte CMOS Checksum
30	Low expansion memory byte
31	High expansion memory byte
32	Data century byte
33	Information flags (set during power on)
34-3F	reserved