Thank you for purchasing the 54TDP system board. This document will aid you in configuring and installing this system board properly. The document is prepared with our best knowledge; however, we make no representation or warranty concerning the contents or use of this manual, and specifically disclaim any expressly implied warranties or merchant liability or fitness of any particular purpose. The information in this document is subject to change without notice.

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# **Technical References**

- . Pentium<sup>tm</sup> Microprocessor Family User's Manual.
- . (Intel Order No: 241428,241429,241430)
- . Intel 82430HX PCISet
- . Intel 82375SB/82374SB PCISet
- . (Intel Order No: 290478-003, 290476-003)
- . The Adaptec AIC-7880 PCI SCSI Controller Data Book.
- . The SMC FDC37C669 Super I/O Controller Data Book
- . The Peripheral Component Interconnect (PCI) Specification
- . The EISA Specification is published by BCPR Services, Incorporated

# **TABLE OF CONTENTS**

PREFACE
Trademarks
Technical References
TABLE OF CONTENTS
TABLE OF CONTENTS
CHAPTER 1: INTRODUCTION
PRODUCT OVERVIEW
Features
Product Specifications
TECHNICAL OVERVIEW
Dual Pentium <sup>tm</sup> Microprocessor
Cache Memory
Main System Memory (DRAM)
DRAM control Logic
Shadow DRAM Feature
PCI/EISA/ISA Compatible Expansion Bus
CHAPTER 2: SYSTEM BOARD HARDWARE SETUP
HIMPED DESCRIPTIONS
JUMPER DESCRIPTIONS
PC/AT Standard Connectors.
Peripheral ConnectorsBuilding a high performance system
CPU Installation
Cooling fan installation
Installing DRAM SIMMs
Peripheral Device Connection
Peripheral Add-on Card installation
CHAPTER 3: SYSTEM BOARD SOFTWARE SETUP
SETUP SYSTEM CMOS:
Entering CMOS Setup
Setup Windows:
Standard Setup
Advanced Setup
Advanced Chipset Setup
Power Management Setup
PCI/PnP Setup
Peripheral Setup
Security Setup Window
Utility Window
IDE Detect

Default Setup Window
PROGRAMMING FLASH BIOS
APPENDIX A-AMIBIOS ERROR MESSAGES AND BEEP CODES
APPENDIX B: AMI BIOS HARD DISK TYPE
APPENDIX C: ISA I/O ADDRESS MAP
APPENDIX D: EISA I/O ADDRESS SPACE
APPENDIX E: INTERRUPT LEVEL ASSIGNMENTS
APPENDIX F: MEMORY MAP
PRODUCT INFORMATION RECORD
System Board PCI Add-on Cards: ISA Add-on Cards: For More Information

### PRODUCT OVERVIEW

The 54TDP system board is designed to address the needs of today's high performance systems by combining powerful performance, quality and innovative system board design. The 54TDP utilizes dual 64-bit Pentium processors running at 75/90/100/120/133/150/166/180/200Mhz Symmetrical in a Multi-processor (SMP) architecture. The Pentium processor incorporates 16KB of very high speed cache memory. The optional 256K/512K Pipeline Burst Level 2 Cache Memory effectively couples the pentium processor to the 64-bit DRAM memory. The 54TDP brings exceptional processing power to the personal computer (PC) that could only be achieved by High-end workstations just a few years ago. To speed up I/O throughput, the board incorporates the new emerging 32-bit Peripheral Component Interconnect (PCI) Local Bus, and the 32-bit Extended Industry Standards Architecture (EISA) expansion bus. The built-in PCI to Ultra Fast and Wide SCSI ports, and high performance I/O ports help dramatically boosts system throughput and expandability for even the most demanding applications in today's market.

#### Features

## **CPU Support**

 Two socket for Dual Intel Pentium 75/90/100/120/133/ 150/166/180/200MHz and Pentium Overdrives. Built-in 16KB or fast Cache Memory per CPU and Advanced Peripheral Interrupt Controller (APIC) for Symmetrical Multi-Processor support.

# **Cache Memory**

• Supports 256K or 512K Pipe line burst Cache memory.

### **System Memory DRAM**

- 6 Banks of Memory that support 1Mx36, 2Mx36, 4Mx36, 8Mx36, 16Mx36, 32Mx36 72-pin SIMMs.
- Up to 768MBytes on-board memory.

### System BIOS

 1024KB of AMI BIOS with Built-in Window CMOS Setup, Configuration Utilities, and firmware for Built-in PCIto-SCSI Controller.

## **System Chipset**

- Intel 82430HX Host to PCI Bridge and Memory Controller
- Intel 82374/82375SB PCI to EISA Bridge and EISA Peripheral Controller

### **PCI/EISA Bus**

- Four 32-bit PCI bus mastering slots. Fast, Wide SCSI, and Ultra Wide Ports also interface to PCI bus.
- Four EISA slots. All four slots support EISA bus mastering.

#### **SCSI Ports**

- Supports 8-bit Fast SCSI-2 Port for data transfer rate up to 10MB/s (Single Ended Active Termination).
- 16-bit Ultra Wide SCSI Port for data transfer rate up to 20MB/s (Single Ended Active Termination).
- Ultra Wide SCSI Port for data transfer rate up to 40MB/s.
- 32-bit PCI Local Bus interface with 128-byte data buffer for performance improvement.
- Based on Adaptec AIC-7880 PCI-to-SCSI controller chip that provide extensive drives supports for most of Operating System such as DOS, WINDOWS, WINDOWS NT,WINDOWS 95, IBM OS/2, Novell

Netware, SCO UNIX, UNIXWARE and other major operating systems.

- Supports Processor Programmed I/O.
- Multitasking ASPI manager for DOS.
- On-board BIOS supports boot capability, and 2 hard disk drives under DOS without a software driver.
- Supports wide range of both synchronous and asynchronous devices: Hard disks, Tape, CD-ROMs, WORMs, DATs, and other SCSI peripherals.

## **Floppy Disk Controller Port:**

- Fully IBM register set compatible.
- Supports up to two 3.5-inch or 5.25-inch floppy disk drives.
- Support Enhanced mode
- Supports 360KB / 720KB / 1.2MB / 1.44MB / 2.88M densities.
- Floppy Disk Controller can be disabled via BIOS setup.

## I/O Peripheral Ports:

- Supports two high speed Serial Ports with 16-bytes high performance FIFO buffers (16550-compatible) and one Parallel Port (EPP and ECP mode compatible).
- I/O ports can be selectively disabled via BIOS setup.

# Real Time Clock and EISA Configuration RAM:

• BQ4287 or Dallas 14287 and a 8Kx8 low stand-by power consumption SRAM for EISA configuration CMOS.

#### **Board Form Factor**

• Standard XT (AT) form factor and mounting holes.

# **Product Specifications**

#### **Electrical**

Power (System board only): +5VDC +- 5%

10 Amps, max.

### **Environmental**

Operating temperature (ambient): O<sup>0</sup>C/32<sup>0</sup>F to 55<sup>0</sup>C/131<sup>0</sup>F

Storage temperature -20°C/-4°F to 70°C/158°F

Operating Humidity: 10% to 90%

(non-condensing)

Storage Humidity: 5% to 95%

(non-condensing)

#### **Dimensions**

Width:

8.7 inches (221.0 mm)

Length:

13.07 inches (332.0 mm)

#### **Interface Connections**

Fast SCSI-2 Port 50-pin double-row connector

Fast and Wide SCSI-2 Port 68-pin micro-connector

Floppy Port 34-pin double-row connector

Two Serial Ports 10-pin double-row connectors

One Parallel Ports 26-pin double-row connectors

# **Dual Pentium<sup>tm</sup> Microprocessor**

The 54TDP supports Symmetrical Multi-Processor (SMP) Architecture when two Intel Pentium Microprocessors are used. Symmetrical Dual-Processor CPUs provide processing power that almost double that of a single CPU. In a Dual Processor system, the tasks of the application will be distributed to each CPU, and from there, each CPU will execute the tasks concurrently. A symmetrical Architecture ensures that system and application software execute the same regardless of the number of processors or the configuration of the I/O subsystem. In a symmetrical Architecture, the system DRAM memory is shared by all processors, thus, all processors can execute a single copy of the OS kernel- which makes a multiprocessor system appear totally identical to a uniprocessor systems from the end-user's point of view. A symmetrical Architecture also provide symmetrical I/O operations which eliminates the bottleneck that is normally seen on asymmetrical architecture systems.

The Intel pentium processor with its built in APIC and large on-chip cache, provides an inexpensive yet high performance symmetrical multi-processor system on a PC system board. The pentium processor incorporates the following features:

- 16KB Internal Cache Memory in a 2-way set associative 32-Byte Line Size. The Cache Memory is separated into two 8KB segments, one for Data and another for code.
- 32-bit Address and 64-bit Data interfaces
- 4 Gigabytes (Giga = 1,073,741,824) of physical address space
- 64 Terabytes (Tera = 2 to the power of 40) of virtual address space
- Binary Compatible with Large Software Base such as DOS, OS/2, UNIX, Windows, Windows 95 Netware, etc.,
- Advanced Design Features such as Branch Prediction, Virtual Mode Extensions

 Built-in 80387 Compatible high performance Floating-point Instruction Execution Unit.

## Cache Memory

The increase in DRAM speed over the last few years has not kept pace with the increase in microprocessor speeds. This has required very fast and unavailable DRAMs or many additional wait states in the CPU memory cycles. System performance decreases as the number of wait states increases.

Cache memory is small, but can be accessed very fast. The code and data frequently accessed by the CPU is normally stored here. The Pentium Microprocessor has a built-in 16KB cache that is separated into two 8KB segments for Code and Data Cache. When the Pentium processor accesses memory, it checks to see if the data is in the cache memory and, if the data is there, data will be read from cache instead of going to much slower main system memory. This is a cache hit situation. It is possible that 95 to 99 percent of all memory accesses are cache hits, depending on the application software.

To achieve higher performance, an optional 256KB or 512 KB external write-back cache is provided on the 54TDP.

## Main System Memory (DRAM)

The main memory subsystem of the 54TDP consists of 640K of DRAM memory below 1 Mega Byte address space, 256K of I/O ROM BIOS, 128KB of system BIOS ROM, and up to 768MB of extended system memory.

## System ROM

The BIOS ROM is provided in a single 8-bit EPROM, which can hold up to 128KB of code and data. It is accessible at the top of the system's 4 GB memory address space and at the top of the first Megabyte of memory. The BIOS ROM supports all PCI/EISA/ISA compatible features. In addition, Shadow RAM

feature is provided to allow the BIOS code and VIDEO BIOS to be executed from 32-bit system DRAM resident at the same physical address. This feature significantly improves the performance in BIOS-call intensive applications.

The processor resets automatically when power is turned on or when the RESET switch is used. After RESET, the Pentium CPU is initialized to a known internal state and begins fetching instructions, out of the BIOS ROM, from the reset address FFFFFFFO. This address leads to the entry point of the power-on system initialization procedure stored in BIOS ROM. The BIOS system initialization procedure consists of the following functions:

- Power-on self-tests such as BIOS Check Sum Test, system DRAM Test, Battery- Backed CMOS RAM Test.
- Initialize all the standard compatible I/O components such as Interrupt Controllers (APIC and Intel 8259A register compatible), DMA Controllers (Intel 8237A register compatible), Keyboard Controller (Intel 8742 register compatible), Video Controller (CGA, EGA, VGA, etc..), System Timers (Intel 8254 register compatible).
- Initializing all the PCI/EISA/ISA add-on cards based on the information stored in the EISA CMOS, if the system has previously been configured.
- Built-in SETUP program, if allowed, is used for system configuration such as:
  - . Day/Time setting
  - . Selection for floppy disk and hard disk types
  - . Shadow RAM and Cache Memory Enable/Disable .
  - . Auto Detect IDE Hard Drives
  - . Virus Protection and Password for Security

Besides initializing the system, the BIOS ROM also provides BIOS interrupt calls for such functions as video access, floppy disk access, printer access, etc...

# DRAM control Logic

The DRAM control logic on the 54TDP system board is designed and optimized for the Pentium CPU. Unlike most other systems with a separate cache controller, the DRAM control logic is tightly coupled with the on-chip cache controller. When address for a new memory cycle becomes available, both controllers operate in parallel. If the cycle is a read hit or a write hit, the cache controller will take control of the cycle while the DRAM controller stays in idle. If the cycle is a read miss, the DRAM controller will cooperate with the cache controller to generate appropriate cycles to write the data from the cache memory back to the system memory. If the cache data line is dirty, then data is read from the system memory to the CPU and cache memory. If the cycle is a write miss, the DRAM controller simply takes control to write the data to the system memory while the cache controller stays in idle. The DRAM controller and the cache memory controller both support the Pentium's burst memory read cycles of 128 Bytes.

The 54TDP on-board DRAM is configured in a 72-bit-wide arrangement consisting of 64 bits of data and 8 bits of parity. Each parity bit is directly associated with one of the 8 bytes in the 64-bit data path.

The 54TDP system board supports 4 banks of by-36 SIMM DRAM memory on the system board. At least two SIMMs are required to make up the 64-bit data path.

### **Shadow DRAM Feature**

The 54TDP supports the Shadow DRAM feature that allows the executed from the system DRAM which resides at the same physical address space. The shadow DRAM feature significantly improves the system performance in BIOS-call intensive applications because executing code out of 64-bit DRAM is much faster than from the 8-bit EPROMs.

## **PCI/EISA/ISA Compatible Expansion Bus**

The 54TDP system board has 4 32-bit PCI Expansion Bus connectors and 4 32-bit EISA/ISA Expansion Bus connectors for interfacing with all PCI and ISA/EISA compatible adapters.

#### **Introduction to PCI Local Bus**

PCI is an electrical specification and logic requirement for a local bus standard. PCI is a multiplexed extension of the CPU bus. PCI defines a standard I/O component level interface that permits all PCI Local Bus products to be totally interchangeable and directly connected without using any glue logic.

## What PCI accomplishes

PCI is a way to physically interconnect highly integrated peripheral components and processor/memory systems.

#### **PCI Features**

- Up to 4 PCI devices can be used in the same system on the PCI expansion slots, not including the PCI Controller and an expansion bus controller for EISA, ISA, or MCA. PCI de-couples the CPU from the expansion bus and works at 33 MHz using either a 32-bit or a 64-bit data connection path to the CPU.
- Has a multiplexed address, command, and data bus. It supports burst mode operation on reads and writes.
- Runs synchronous with the CPU at speeds up to 33 MHz, has a maximum data transfer rate of 120 MBs (with a peak rate of 132 MBs on a 32-bit data path).
- Has low latency random accesses (about 60 ns write access latency) to slave registers from a PCI bus master on the PCI bus.
- Is capable of full concurrence with the processor and PCI bus masters.
- Has full multi-master capability, allowing any PCI Master peer-to-peer access to any PCI slave.
- Has hidden and overlapped central arbitration.

- Has a low pin count: master 47; slave 45 (32-bit data path)
- Has address and data parity, and uses three physical address spaces: 32-bit memory, 32-bit I/0, and a 256 byte-peragent configuration space.
- The PCI Controller buffer reads and writes between the memory/CPU and PCI peripheral devices.
- The CPU in a PCI system runs concurrently with PCI bus mastering peripherals. Although bus mastering peripheral devices are arbitrated, significant data transfer rate improvements can be achieved without splitting resources utilization between the CPU and a bus mastering device. Peripheral devices can operate up to 33 MHz in a PCI environment.
- PCI devices can be bus masters, slaves, or a combination of bus master and slave.
- The PCI specification also provides for burst mode of any length for both reads and writes.
- PCI is a multiplexed bus which is capable of sending more than one signal on the same electrical path. The control mechanisms have been modified and extended to optimize I/O support.
- PCI components must be one of three classes: Bus master, Slave, or Master/slave combination.

### **Introduction to EISA BUS**

The Extended Industry Standard Architecture(EISA) is a joint development effort by leading computer manufacturers to add 32-bit data transfer, 32-bit addressing and intelligent bus mastering capabilities to the original IBM PC AT Bus called Industry Standard Architecture(ISA) bus. ISA bus cards are fully compatible with the EISA bus. All ISA cards can go into EISA slots.

#### **EISA Features**

• 32-bit addressing and data transfers

- Data transfer rates up to 33 MB/s.
- Intelligent Bus master support with multiple bus master arbitration.
- Interrupt sharing
- Automatic system configuration

The EISA connector has been specially designed to accommodate both ISA and EISA cards. The connector has 192 pins in a two-level arrangement. The upper level of contacts are ISA compatible. The lower-level contacts are for EISA signals. The connector is keyed so that only EISA cards can touch both levels of contacts.

For ease of use, EISA provides an automatic configuration facility. Each EISA adapter manufacturer has a designated ID code. The ID code identifies the card type, and it allow the set-up program to access a corresponding configuration file. Setup information is then written to the system board battery backed CMOS RAM and to special I/O ports that can be addressed by physical slot numbers.

## **ISA Compatible Peripherals**

The 54TDP system board provides the following standard peripherals:

- Enhanced DMA functions with seven independently programmable channels (Super set of Intel 8237A compatible DMA controller).
- Two 82C59A compatible Interrupt Controllers
- Five 82C54 compatible programmable interval timers
- One keyboard controller

### **CHAPTER 2: SYSTEM BOARD HARDWARE SETUP**



When working with the 54TDP, it is extremely important that you avoid Electrical Static Discharge (ESD).

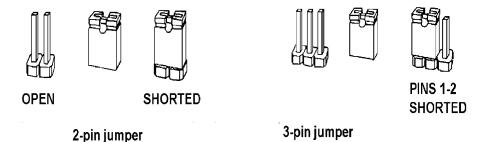
Always ground yourself by wearing a grounded wristband or ankle strap.

Figure 1 on the next page shows the component layout of the 54TDP system board with locations of the system board jumpers and connectors. Note that most jumpers and connectors on the system board are labeled with proper names with pin 1 marked as '1'. To avoid damaging the board and to have proper operation, caution should be taken when connecting these jumpers and connectors.

# **JUMPER DESCRIPTIONS**

Jumpers are used to select between various operating modes. A jumper switch consists of two, three, or four gold pins projecting from the system board. Placing the plastic jumper cap over two pins connects those pins and makes a particular selection. Using the jumper cap to cover two pins in this way is referred to as shorting those pins. If the cap is not placed on any pins at all or placed on only one pin, this is referred to as leaving the pins open.

Note: When you open a jumper, leave the plastic jumper cap attached to one of the pins so you don't lose it.



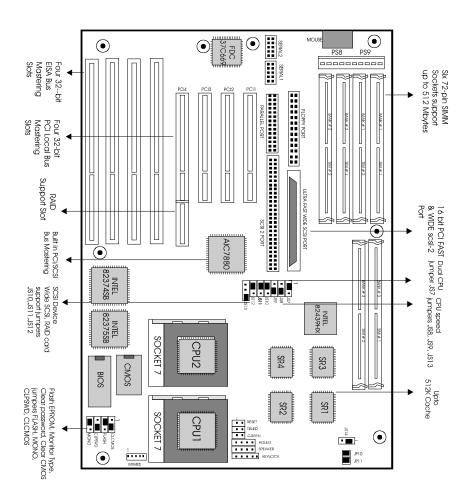


Figure 1: 54TDP Component Layout

**Remark:** The sample jumper setting shown above is set at Pentium-133MHz.

### **Dual CPU Selection Jumpers**

The 54TDP can be used with a single Intel Pentium 75/90/100/120/133/166/180/200mhz microprocessor or with Dual Intel Pentium microprocessors. The jumper is set according to the number of CPU installed.

Number of CPU installed	JS7
Single	1-2
Dual	2-3

## **CPU Clock Frequency Jumpers**

The54TDP supports Pentium 75, 90, 100, 120, 133, 150, 167, 180, 200MHz. The jumper should be set to correspond to CPU speed.

CPU Speed	JS8	JS9	JS13(pin 1-2)	JS13(pin 2-3)
75 Mhz	2-3	1-2	Open	Open
90 Mhz	1-2	1-2	Open	Open
100 Mhz	2-3	2-3	Open	Open
120 Mhz	1-2	1-2	Open	Short
133 Mhz	2-3	2-3	Open	Short
150 Mhz	1-2	1-2	Short	Short
167 Mhz	2-3	2-3	Short	Short
180 Mhz	1-2	1-2	Short	Open
200 Mhz	2-3	2-3	Short	Open

## RAID card Support (to support Adaptec ARO-1130)

The 54TDP has one RAID Support Slot that can be used with Adaptec ARO-1130. The setting should be according.

RAID Support Add-on card	JS10
Not Installed	1-2
Installed	2-3

## **SCSI Device Type**

Set to position 2-3 if at least one 16-bit SCSI device connect to the system board. Otherwise, set at position 1-2.

Device Type	JS11
16-bit	2-3
8-bit	1-2

### Wide SCSI termination

Please see SCSI Setup for more detail information about setting up this jumper.

Termination high Byte	JS12
Together with low Byte	1-2
Always	2-3

#### Clear CLCMOS

This jumper is to override the content of the EISA CMOS. Install at position 1-2 will allow the system to ignore EISA CMOS content during boot up. Return to postion 2-3 allow normal read and write to the EISA CMOS.

Operation	CLCMOS
Normal	2-3
Clear	1-2

## Flash BIOS Type Select Jumper

This jumper is used to select the appropriate voltage supplied to the FLASH EPROM. Please refer to Programming the Flash BIOS instruction section for more detailed information. Manufacturing jumper only.

Flash EPROM Type	FLASH
12V	1-2
5V	2-3

#### **Clear Password**

Once install at position 2-3, during boot up, even with password setup, the system will ignore the set up password and allow user to enter into CMOS setup to change to new password. Return to position 1-2 for normal operation.

Operation	CLPSWD
Normal	1-2
Clear	2-3

## **Monitor Type**

Туре	MONO
Color	1-2
Mono	2-3

### Support P55 CPU

CPU Type Selection	JP11	JP10	JS14
P55 CPU	Open	Open	2-3
P54 CPU	Short	Short	1-2

## **CONNECTOR Descriptions**

Following is the list of 54TDP system board connectors. For more detailed descriptions of these components, please refer to the next section. To avoid damaging the board and to have proper operation, caution should be taken when connecting these components.

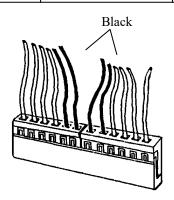
- Power supply connectors (PS8 and PS9)
- Reset connector (RESET)
- Power LED and keyboard lock connector (KEYLOCK)
- Speaker connector (SPEAKER)
- Turbo LED connector (TBLED)
- SCSI Harddisk Activity LED connector (HDLED)
- Support Infrared (INFRARED PORT)
- Keyboard connector (KBCN1)
- Parallel Port connector (PARALLEL PORT)
- Serial Port 1 & 2 connector (SERIAL1) (SERIAL2)
- Floppy Interface connector (FLOPPY PORT)
- SCSI Interface connectors
- (SCSI2 PORT & ULTRA FAST WIDE SCSI PORT)

## **PC/AT Standard Connectors**

## Power Supply Connectors (PS8 and PS9)

The two Power Supply connectors (PS8 and PS9) are 6-pin AT standard power connectors. Most power supplies have two sixwire connectors, two of the wires on each connector are black. Align the two six-wire connectors so that the two black wires on each connector are in the middle as shown below.

Pin	Connector PS9	Connector PS8
1	Power Good	Ground
2	+5 VDC	Ground
3	+12 VDC	-5 VDC
4	-12 VDC	+5 VDC
5	Ground	+5 VDC
6	Ground	+5 VDC



## **Keyboard Connector**

The keyboard connector (KBCN1) is a 5-pin, circular-type DIN socket. It is used to connect the system board keyboard interface to any standard AT-compatible keyboard. (84 or 101 - key type keyboards). The pin assignments are listed below:

Pin	Description	
1	Keyboard Clock Signal	
2	Keyboard Data Signal	
3	Not Used	
4	Ground	
5	+5V Fused VDC	

#### **Reset Connector**

The system RESET is a 2-pin Berg strip. It is used to connect the push button reset switch located on the front panel to the system board. System reset can be done by shorting pin 1 to pin 2 with the same effect as turning the power off and then on again.

Pin	Description	
1	Reset Input	
2	Ground	

### **Power LED and Keyboard Lock Connector**

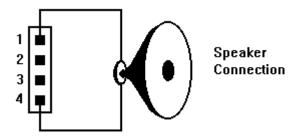
The Power LED and Keyboard Lock (KEYLOCK) is a 5-pin keyed Berg strip. It is used to connect +5 VDC power to the power indicator LED at the front panel and connect the security keyboard lock to the keyboard controller. This allows you to switch off the keyboard and to provide limited security against casual intruders. The pin assignments are indicated below:

Pin	Description	
1	LED Power	
2	Key (No Connection)	
3	Ground	
4	Keyboard Lock	
5	Ground	

## **Speaker Connector**

The Speaker is a 4-pin keyed (SPEAKER) Berg strip. It is used to connect an external 2-inch, 8-ohm speaker to the system board to provide sound capability. The pin assignments are defined below:

Pin	Description	
1	Speaker Data Out	
2	Key (No Connection)	
3	Ground	
4	+5 VDC	



#### **Turbo LED Connector**

The Turbo LED connector (TBLED), marked as 'TB/LED', is a 2-pin Berg strip. It is used to connect a CPU operating frequency indicator LED from the front panel to the system board. The pin assignments are indicated below:

Pin	Description	
1	LED Anode(+)	
2	LED Cathode(-)	

# **Hard Disk Activity LED Connector**

The hard disk activity LED connector (HDLED) is a 4-pin keyed Berg strip. The LED will be on whenever data is transferred on the SCSI bus. The connector should be connected to the case's front panel hard disk LED.

Pin	Description	
1	LED Anode (+)	
2	Key (N/C)	
3	LED Cathode(-)	

Pin	Description	
4	LED Anode(+)	

## **Peripheral Connectors**

#### Parallel Port Connector

The on-board parallel port (PARALLEL PORT) connector is a 2x13-pin male header connector. The On-board Parallel Port can be disabled through the BIOS Setup. Please refer to Chapter 3 "Peripheral Management Setup" section for more detailed information. The pin assignment is shown below:

Pin	Description	Pin	Description
1	STROBE	2	AUTO FEED XT
3	Data Bit 0	4	ERROR
5	Data Bit 1	6	INIT
7	Data Bit 2	8	SLCT IN
9	Data Bit 3	10	Ground
11	Data Bit 4	12	Ground
13	Data Bit 5	14	Ground
15	Data Bit 6	16	Ground
17	Data Bit 7	18	Ground
19	ACK	20	Ground
21	BUSY	22	Ground
23	PE	24	Ground
25	SLCT	26	No Connection

The 54TDP's Integrated Parallel Port supports Extended Capabilities Port protocol (ECP) to provide a number of advantages for the parallel port as listed below:

• Uses DMA channel 1 or 3 to transfer data across the Parallel port in both forward and reverse directions; therefore, processor time is saved for other tasks. This is especially important in multi-tasking operating systems.

Peer-to-peer capability for networking.

Single byte run length encoded (RLE) compression for improved throughput (64:1.)

### **Serial Port 1 & 2 Connectors**

The Serial Port 1 and 2 connectors are the 2x5-pin male headers SERIAL1 & SERIAL2. Users should use a flex cable with a 9 or 25 -pin male D-subminiature receptacle at one end and a 2x5-pin female header at the other end to provide RS-232 serial interface. The On-board Serial Ports can be disabled through BIOS setup. Please refer to Chapter 3 "Peripheral Management Setup" section for more detailed information. The pin assignment for COM1/COM2 is defined below:

Pin	Description	Pin	Description
1	Carrier Detect (RLSD)	2	Receive Data (RXD)
3	Transmit Data (TXD)	4	Data Terminal Ready (DTR)
5	Signal Ground	6	Data Set Ready (DSR)
7	Request To Send (RTS)	8	Clear To Send (CTS)
9	Ring Indicator (RI)	10	No Connection

# **Floppy Interface Connector**

The On-board Floppy Interface connector (FLOPPY PORT) is a 2x17-pin male header. This interface supports two 5.25" or 3.5" floppy drives in any combination and also can be disabled if no floppy drives are present on the system. The On-board Floppy Port can be disabled through the BIOS setup. Please refer to Chapter 3 "Peripheral Management Setup" section for more detail information. The pin assignment is as follows:

Pin	Description	Pin	Description
2	RPM	1	Ground

Pin	Description	Pin	Description
4	No Connection	3	Ground
6	No Connection	5	Ground
8	Index	7	Ground
10	Motor 1	9	Ground
12	Drive 2	11	Ground
14	Drive 1	13	Ground
16	Motor 2	15	Ground
18	Direction	17	Ground
20	Step	19	Ground
22	Write Data	21	Ground
24	Write Enable	23	Ground
26	Track0	25	Ground
28	Write Protect	27	Ground
30	Read Data	29	Ground
32	Head Select	31	Ground
34	Disk Change	33	Ground

#### **SCSI Interface Connectors**

The 54TDP supports two SCSI Port connectors. The 2x25 pin header SCSI1 port is 8-bit SCSI1 port interface. The 68-pin Female Miniature receptacle header SCSI2 port is 16-bit and Ultra Fast Wide SCSI2 Port interface. The SCSI Ports can be disabled through BIOS setup. Please refer to Chapter 4 "Peripheral Management Setup" section for more detailed information. The pin assignment of SCSI2 Port is as follows:

Pin	Description	Pin	Description	
2	Data 0	1	Ground	
4	Data 1	3	Ground	
6	Data 2	5	Ground	
8	Data 3	7	Ground	
10	Data 4	9	Ground	

Pin	Description	Pin	Description	
12	Data 5	11	Ground	
14	Data 6	13	Ground	
16	Data 7	15	Ground	
18	Data Parity	17	Ground	
20	Ground	19	Ground	
22	Ground	21	Ground	
24	Ground	23	Ground	
26	Terminator Power	25	Ground	
28	Ground	27	Ground	
30	Ground	29	Ground	
32	Attention	31	Ground	
34	Ground	33	Ground	
36	Busy	35	Ground	
38	Acknowledge	37	Ground	
40	Reset	39	Ground	
42	Message	41	Ground	
44	Select	43	Ground	
46	Command/Data	45	Ground	
48	Request	47	Ground	
50	In/Out	49	Ground	

The pin assignment for 68-pin receptacle header SCSI2 is as follows:

Pin	Description	Pin	Description
35	Data12	1	Ground
36	Data13	2	Ground
37	Data14	3	Ground
38	Data15	4	Ground
39	Data Parity(8-15)	5	Ground
40	Data0	6	Ground
41	Data 1	7	Ground
42	Data 2	8	Ground

Pin	Description	Pin	Description	
43	Data 3	9	Ground	
44	Data 4	10	Ground	
45	Data 5	11	Ground	
46	Data 6	12	Ground	
47	Data 7	13	Open	
48	Data Parity(0-7)	14	Ground	
49	Ground	15	Ground	
50	Ground	16	Ground	
51	Terminator Power	17	Terminator Power	
52	Terminator Power	18	Terminator Power	
53	Reserved	19	Reserved	
54	Ground	20	Ground	
55	Attention	21	Ground	
56	Ground	22	Ground	
57	Busy	23	Ground	
58	Acknowledge	24	Ground	
59	Reset	25	Ground	
60	Message	26	Ground	
61	Select	27	Ground	
62	Command/Data	28	Ground	
63	Request	29	Ground	
64	In/Out	30	Ground	
65	Data8	31	Ground	
66	Data9	32	Ground	
67	Data10	33	Ground	
68	Data11	34	Ground	

# **Building a high performance system**

The dimensions of the 54TDP system boards are designed to fit perfectly in a PC/XT (or PC/AT) standard case. To build a complete high performance system based on the 54TDP system board, the following equipment is needed:

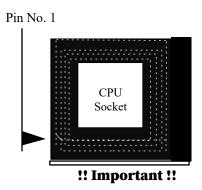
1. A chassis (Case) with dimensions similar to PC/XT/AT standard chassis. The chassis should have a front Panel with connectors for Reset, Power, Keylock, Turbo LED, Speaker,

and Hard drive LED. The standard AT 230W power supply should be capable of providing a continuous power within a +4.75 VDC to +5.25 VDC range. A power line filter may be needed for areas with noisy transmission.

- 2. One or two floppy drives (360K/1.2M/1.44M/2.88M).
- 3. SCSI Hard disk drive to use with onboard SCSI controller or IDE hard disk drive with hard IDE disk controller.
- 4. Video card (Monochrome, CGA, EGA, VGA).
- 5. A video display monitor.
- 6. An AT-compatible keyboard (84 or 101 Keyboard).
- 7. The following additional peripherals will be useful in enhancing the system:
  - A bus or serial mouse.
  - A tape back up drive.
  - A CD-ROM drive.
- 8. Cables
  - A set of flat cables for floppy drive and hard disk drive.
  - AC Power cable (Usually Comes with power supply in case)
- 9. Tools
  - Set of Screw drivers, Cutter, Pliers

### CPU Installation

Care should be taken when installing the CPU into the Zero Insertion Force (ZIF) socket on the system board. Lift the handle of ZIF socket up. Place the Pentium processor into the ZIF socket. No force should be required to insert the CPU. On Pentium processors, pin 1 has a square base and it goes into a particular hole on the socket. Match the hole and pin one first and then easily insert the processor into the socket. Press the handle gently down. Pin 1 can also be identified by the non rectangular corner.



## **Cooling fan installation**

Mount the cooling kit with fan on top of the CPU. Connect power to fan from power supply. Make sure the cooling kit's bottom surface makes proper contact with top surface of CPU.

# !! Warning !!

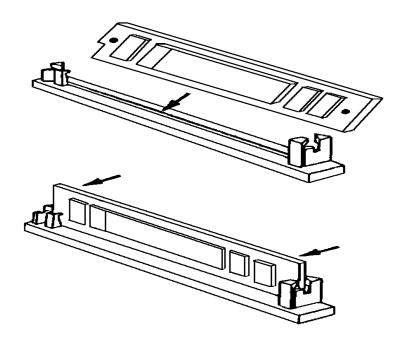
The manufacturer of the board or CPU is not responsible for any damage to CPU because of improper handling during installation or if a cooling kit with fan is not used.

# **Installing DRAM SIMMs**



When working with DRAM SIMMs, it is extremely important that you avoid Electrical Static Discharge (ESD). Always ground yourself by wearing a grounded wristband or ankle strap.

- 1. Power must be off while installing SIMMs.
- 2. The SIMM module should face to the right with pin 72 next to the power supply connectors.
- 3. Insert the SIMM at a 45 degree angle, tilted towards ISA slots.
- 4. Gently push the SIMM to an upright position until it "snaps" into place.
- 5. Repeat above steps until the entire bank is filled.



## **DRAM SIMMs Configuration**

The on-board DRAM memory sub-system has six module mounting sockets which are divided into "banks" of two sockets each. Sockets labeled SIM1 & SIM2 constitute bank 1. Sockets labeled SIM3 & SIM4 constitute bank 2. Socket label SIM5 & SIM6 constitute bank 3. They support EDO, Fast Page Mode, None Parity, and Parity of 256Kx36,512Kx36, 1Mx36, 2Mx36, 4Mx36, 8Mx36, 16Mx36 and 32Mx36 DRAM SIMMs and support up to 768MB. DRAM speed must be 70ns or faster and must be two SIMMs for each bank. You can configure the memory of the 54TDP in a variety of ways as follows.

Bank # 1	Bank # 2	Bank # 3	Total
SIM#1&SIM#2	SIM#3&SIM#4	SIM#5&SIM#6	DRAM
256Kx36	None	None	2MB
256Kx36	256Kx36	None	4MB
256Kx36	256Kx36	256Kx36	6MB
512Kx36	None	None	4MB
512Kx36	512Kx36	None	8MB
512Kx36	512Kx36	512Kx36	12MB
1Mx36	None	None	8MB
1Mx36	1Mx36	None	16MB
1Mx36	1Mx36	1Mx36	24MB
2Mx36	None	None	16MB
2Mx36	2Mx36	None	32MB
2Mx36	2Mx36	2Mx36	40MB
4Mx36	None	None	32MB
4Mx36	4Mx36	None	64MB
4Mx36	4Mx36	4Mx36	96MB
8Mx36	None	None	64MB
8Mx36	8Mx36	None	128MB
8Mx36	8Mx36	8Mx36	192MB
16Mx36	None	None	128MB
16Mx36	16Mx36	None	256MB
16Mx36	16Mx36	16Mx36	384MB
32Mx36	None	None	256MB
32Mx36	32Mx36	None	512MB
32Mx36	36Mx36	36Mx36	768MB

#### **SCSI Device Connection**

The 54TDP supports both 8-bit and 16-bit SCSI ports. If the SCSI devices of the system are regular 8-bit type, use the provided 50-pin cable to connect the SCSI devices such as hard drives, CD-ROM, etc.,. to the 50-pin double row connector SCSI-2 port on the board. Make sure the colored stripe on the cable (indicating the location of pin 1) matches Pin 1 of the connector on the mother board as well as Pin 1 of the SCSI devices' connectors.

If the SCSI devices of the system are 16-bit type, the optional Fast and Wide SCSI cable must be purchased to connect the devices to the Miniature receptacle connector Ultra Fast & Wide port on the board. Note that to hook up regular 8-bit external SCSI devices, a special extension connector card named QAX must be used. Contact your dealer or distributor to purchase this card. For 16-bit Fast and Wide external SCSI devices, the cable already has a built-in external connector.

# Terminate the endpoints of the SCSI bus.

The SCSI bus must be terminated correctly to ensure proper operation. The first and last physical SCSI devices on the SCSI cable must have terminators installed or enabled. All other SCSI devices in middle must have terminators removed or disabled.

Terminators on the motherboard are active type and are enabled by default. To disable the onboard SCSI termination, use the SCSI Select Utility that is built-in to the SCSI firmware.

# **Floppy Disk Drives Connection**

The 54TDP supports to 2 floppy drives. The floppy ribboncable is provided with the system board. Use the cable to connect the floppy drives into 34-pin double-row connector Floppy port on the board. Make sure the colored stripe on the cable (indicating the location of pin 1) matches Pin 1 of the connector on the mother board as well as Pin 1 on the floppy drives.

### **Serial Port and Parallel Port connection**

The 54TDP motherboard is shipped with a set of ribbon-cable and mounting bracket for two Serial Ports and one Parallel Port. Connect the 10-pin double-row connectors of the ribbon cable to the 10-pin double row headers SERIAL1 & SERIAL2 on the motherboard. You can optional select the 9-pin external connector or the 25-pin external connector. The parallel Port connection should be done through the 26-pin double row header parallel port on the motherboard. The external connector bracket can be either mounted into a regular I/O slot brackets or to the system case by removing the bracket.

## Peripheral Add-on Card installation

The 54TDP supports both PCI slots and EISA add-on cards. You can install the corresponding add-on cards into any of these slots. Make sure the add-on cards' interrupts or DMA channels do not conflict with each other. The best way to remember is to write down the information of all the installed cards into the back of this manual for later reference.

- . Normally PCI Add-on cards can be automatically configured by system BIOS during boot up. However, some PCI add-on cards do have jumper settings for INTA or INTB. Write down the information if it is available for later reference.
- . EISA Add-on cards can be configured automatically by EISA Configuration Utility (ECU); thus, you only need to write down the slot number that the card installed into.
- . ISA Add-on cards' memory mapping, interrupt level, or DMA channels are normally configured by jumper settings or switches and they cannot be detected by running the ECU. You should write down the information of the cards in detail for later reference.

Please refer to the manuals shipped with the add-on cards for more information. Care should be taken when inserting the cards into the slots to make sure the connectors slots are not damaged.

### CHAPTER 3: SYSTEM BOARD SOFTWARE SETUP

### **SETUP SYSTEM CMOS:**

You need to setup the system CMOS every time:

- \* You start a new and un-configured system
- \* You receive at start-up time an error message indicating the configuration information stored in the non Volatile CMOS RAM has somehow become corrupted.
- \* You add, remove, or change peripherals from your system.
- \* You add, remove, or change DRAM from your system.

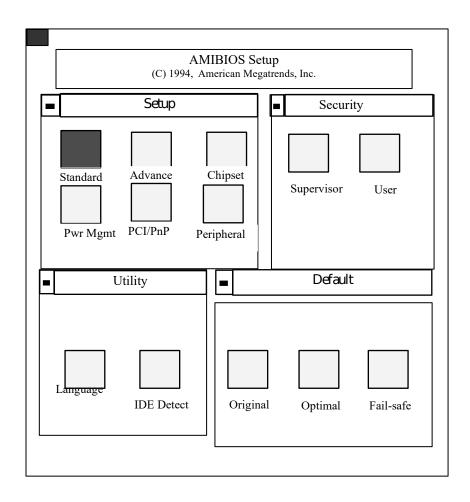
The first time you power up the system, the configuration information stored in the battery-backed CMOS RAM may not be correct. The BIOS detects this condition and prompts the user to go through the CMOS SETUP section. This chapter explains how to use the BIOS SETUP program and make the appropriate entries.



Some of the parameters are already factory preset and do not need to be changed. Please read the instructions carefully and only change the settings if necessary.

## **Entering CMOS Setup**

The System BIOS provides a Built-in Setup Utility that can be accessed by pressing < Del > key at the appropriate time during system boot up. Setup configuration data is stored in the system CMOS RAM. The Following window will appear in the AMIBIOS Setup main screen. Details of setup options in each window is given in the following section:



## **Setup Windows:**

Types of Setup	Description
Standard Setup	Sets date & time, hard disk type, floppy drive
	types.
Advanced Setup	Features for a high performance motherboard such as Quick Boot ,BootUp Sequence ,BootUp Num-Lock, Floppy Drive Swap, Mouse Support, Primary Display, Password Check, OS/2 Compatible Mode, Internal Cache, External Cache, System BIOS Cacheable, C000 to DC00 Shadow, etc.,.
Chipset Setup	Sets chipset-specific options and features.
Power Mgmt	Power Management control options.
PCI/PnP Setup	Sets options related to the PCI bus and Plug and Play features.
Peripheral Setup	Controls I/O Peripheral Controller-related options.

## Standard Setup

Standard Setup options are displayed by choosing the Standard icon from the WINBIOS Setup menu. All Standard Setup options are described below.

#### **Pri Master**

Pri Slave Sec Master Sec Slave

For each icon above, once select, you can either enter the type of drive installed, if known, or select **Auto** to have system BIOS detect the drive type for you.

## Date/Time

Select the Date/Time option to change the date or time. The current date and time are displayed. Enter new values through the displayed window.

## Floppy Drive A, B

Choose the Floppy Drive A or B icon to specify the floppy drive type. The settings are  $360 \text{ KB } 5\frac{1}{4}$ ",  $1.2 \text{ MB } 5\frac{1}{4}$ ",  $720 \text{ KB } 3\frac{1}{2}$ ",  $1.44 \text{ MB } 3\frac{1}{2}$ ", or  $2.88 \text{ MB } 3\frac{1}{2}$ ".

## **Advanced Setup**

Advanced Setup options are displayed by choosing the Advanced icon from the WINBIOS Setup main menu. All Advanced Setup options are described in this section.

## **Quick Boot**

Set this option to *Enabled* to instruct BIOS to boot quickly when the computer is powered on.

Setting	Description
Disabled	BIOS test all system memory. BIOS waits up to 40
	seconds during detecting disk drive attached to the
	system. This is very important for some hard drives that
	have very long initialization time after being reset.
Enabled	BIOS does not test system memory above 1 MB.
	BIOS will only quickly scan the bus to detect if hard
	drives present and will not wait if device is slow to
	response.

The Optimal and Fail-Safe default settings are *Enabled*.

## **BootUp Sequence**

This option sets the sequence of boot drives (floppy drive A:, hard disk drive C:, or a CD-ROM drive) that the AMIBIOS attempts to boot from after AMIBIOS POST completes. The settings are *C:,A:,CDROM, CDROM,C:,A:*, or *A:,C:, CDROM*. The default settings are *C:,A:,CDROM*.

## **BootUp NumLock**

Set this option to *Off* to turn the Num Lock key off when the computer is booted so you can use the arrow keys on both the numeric keypad and the keyboard. The settings are *On* or *Off*. The default setting is *On*.

## **Floppy Drive Swap**

Set this option to *Enabled* to permit drives A: and B: to be swapped. This option allows system to boot up either from floppy drive A: or B:, specially for the system with two different types of floppy drives. The settings are *Enabled* or *Disabled*. The default setting is *Disabled*.

## **Mouse Support**

When this option is set to *Enabled*, the PS/2-type mouse port will be enabled. Note that this is not applied for Serial Mouse that typically connected to Serial port. The settings are *Enabled* or *Disabled*. The default setting is *Disabled*.

## **Primary Display**

This option specifies the type of display monitor and adapter in the computer. The settings are *Mono*, *CGA40*, *CGA80*, *EGA/VGA*, or *Absent*. The Optimal and Fail-Safe default settings are EGA/VGA.

#### Password Check

This option enables password checking every time the computer is powered if password been setup previously. If *Always* is chosen, a user password request prompt appears every time the computer is turned on. If *Setup* is selected, a user password request prompt appears every time user wants to get into CMOS setup screen (by pressing "DEL" key right after power on. The Optimal and Power-On defaults are *Setup*.

## **Parity Check**

This option is to check the parity DRAM. This option should be only enabled if you are sure that the memory installed in the system support parity bit (By 36, not by 32 type), if this option is Enabled and DRAM is none parity than the BIOS will report the error message during boot up. The Default setting is *Disabled*.

## **OS/2 Compatible Mode**

Set this option to *Enabled* to permit the system run properly with IBM OS/2 (if IBM OS/2 operating system is installed). The settings are *Enabled* or *Disabled*. The default setting is *Disabled*.

#### **Internal Cache**

This option specifies the caching algorithm used for the Cache Memory built-in the microprocessor. The Cache Memory can be disabled, enabled as Write Back or Write Through. Write back provide better performance. However, very few applications may required Write Through. Default setting is *Write Back*.

#### **External Cache**

This option specifies the caching algorithm used for the External Cache Memory (or called Level 2 Cache. Level 1 Cache is the one built-in the microprocessor) built-in the system board. The Cache Memory can be disabled, enabled as Write Back or Write Through. Write back provide better performance. However, very few applications may required Write Through. Default setting is *Write Back*.

## **System BIOS Cacheable**

When this option is set to *Enabled*, the BIOS code, beside be shadowed into system Memory, also be cached into the Cache Memory. If Disabled is select, the BIOS code only be shadowed into system memory. The settings are *Enabled* or

*Disabled.* The Optimal default setting is *Enabled.* The Fail-Safe default setting is *Disabled.* 

## C000,16K Shadow

C400,16K Shadow C800,16K Shadow CC00,16K Shadow D000,16K Shadow D400,16K Shadow D800,16K Shadow C000,16K Shadow

These options allow the I/O ROM (most of the time is 8-bit device) at the specific region of I/O memory address space, if present, to be *Enabled* (or *Shadowed*), in the 64-bit system memory DRAM, or aslo be Cached into the Cache memory for faster execution. The 16KB at C000 and 16KB at C400, which are used for display ROM address space, is set as Enabled as default to improve display performance.

## **Advanced Chipset Setup**

## **Memory Hole**

This option allows the enabling of a memory hole at either address 512K-640K or at address 15M-16M. This is to support some special adapters that require linear frame buffer memory space. Select this option only when you know very well about the adapters installed in the system and whether they need this memory hole. The Default setting is *Disabled*.

## 8Bit I/O Recovery Time (BCLK)

This setup allows to insert wait states for I/O cycles on the ISA bus for some old 8-bit ISA adapter cards is too slow for the new advanced system board with very high performance CPU speed. This is reserved for advanced users. The higher number, the more wait states will be added. The Default setting is 2.

## 16Bit I/O Recovery Time (BCLK)

This setup allows to insert wait states for I/O cycles on the ISA bus for some old 16-bit ISA adapter cards is too slow for the new advanced system board with very high performance CPU speed. This is reserved for advanced users. The higher number, the more wait states will be added. The Default setting is 1.

## **DRAM Timings**

This setup should be set according to the speed of DRAM memory installed in the system. The optimal setting is 60ns for the best performance. However, care should be taken to make sure the memory speed is also 60ns or faster. If you do not know for sure the memory speed, select 70ns. The default setting is 70ns.

#### **Refresh Rate**

Allows the refresh rate to be set according to the memory bus clock (50mhz, 60mhz or 66mhz).

## **Read Burst Timing**

This option is to optimize system memory timing.

## **Write Burst Timing**

This option is to optimize system memory timing.

## **Fast RAS to CAS Delay (Clocks)**

This is to control DRAM memory timing. It is reserved for advanced users. Default setting is 2.

## LeadOff Timing

This option should be set accordingly to the type of memory use in the system. Default setting is 7/6/3/4.

## **Power Management Setup**

Power Management Setup options are displayed by choosing the Power Mgmt icon from the WINBIOS Setup main menu. All Power Management Setup options are described in this section.

## **Power Management/APM**

Set this option to *Enabled* to enable the power management and APM (Advanced Power Management) features. The settings are *Enabled* or *Disabled*. The default setting is *Disabled*.

## **Instant On Support**

Set this option to *Enabled* to allow the computer to go to full power on mode when leaving a power-conserving state. *This option is only available if supported by the computer hardware*. AMIBIOS uses the RTC Alarm function to wake the computer at a prespecified time. The settings are *Enabled* or *Disabled*. The default setting is *Disabled*.

#### **Green PC Monitor Power State**

This option specifies the power management state that the Green PC-compliant video monitor enters after the specified period of display inactivity has expired. The settings are *Disabled*, *Off*, *Standby*, or *Suspend*. The default setting is Standby.

#### Video Power Down Mode

This option specifies the power management state that the video subsystem enters after the specified period of display inactivity has expired. The settings are *Disabled*, *Standby*, or *Suspend*. The default setting is *Disabled*.

#### **Hard Disk Power Down Mode**

This option specifies the power management state that the hard disk drive enters after the specified period of display inactivity has expired. The settings are *Disabled*, *Standby*, or *Suspend*. The default setting is *Disabled*.

## Hard Disk Time-out (Min.)

This option specifies the length of a period of hard disk inactivity. When this period expires, the hard disk drive enters the power-conserving mode specified in the **Hard Disk Power Down Mode** option described on the previous page. The settings are *Disabled*, *1 Min (minutes)*, and all one minute intervals up to and including 15 *Min*. The default setting is *Disabled*.

## **Standby Time-out**

This option specifies the length of the period of system inactivity when the computer is in Full-On mode before the computer is placed in Standby mode. In Standby mode, some power use is curtailed. The settings are *Disabled*, *1 Min*, *2 Min*., and all one minute intervals up to and including 15 *Min*. The default setting is *Disabled*.

## Suspend Time-out

This option specifies the length of the period of system inactivity when the computer is already in Standby mode before the computer is placed in Suspend mode. In Suspend mode, nearly all power use is curtailed. The settings are *Disabled*, *1 Min.*, *2 Min.*, and all one minute intervals up to and including 15 *Min.* The default setting is *Disabled*.

#### Slow Clock Ratio

This option specifies the speed at which the system clock runs in power saving modes. The settings are expressed as a ratio between the normal clock speed and the power down clock speed. The settings are 1:1, 1:2 (half as fast as normal), 1:4 ((the normal clock speed), 1:8, 1:16, 1:32, 1:64, or 1:128. The default setting is 1:8.

## **Display Activity**

This option specifies if AMIBIOS is to monitor activity on the display monitor for power conservation purposes. When this options set to *Monitor* and there is no display activity for the length of time specified in the value in **the Full-On to Standby (Min)** option, the computer enters a power saving state. The settings are *Monitor* or *Ignore*. The default setting is *Ignore*.

IRQ 3..... IRQ 15

These options enable event monitoring. When the computer is in a power saving mode, activity on the named interrupt request line is monitored by AMIBIOS. When any activity occurs, the computer enters Full On mode. Each of these options can be set to *Monitor* or *Ignore*. The default setting for all options are *monitor* except IRQ13.

## PCI/PnP Setup

PCI/PnP Setup options are displayed by choosing the PCI/PnP Setup icon from the WINBIOS Setup main menu. All PCI/PnP Setup options are described in this section

## **Plug and Play Aware OS**

Set this option to *Yes* if the operating system installed in the computer is Plug and Play-aware. AMIBIOS only detects and enables PnP ISA adapter cards that are required for system boot. The Windows 95 operating system detects and enables all other PnP-aware adapter cards. Windows 95 is PnP-aware. Set this option to *No* if the operating system (such as DOS, OS/2, Windows 3.x) does not use PnP. *You must set this option correctly or PnP-aware adapter cards installed in your computer will not be configured properly*. The settings are *No* or *Yes*. The Optimal and Fail-Safe default settings are *No*.

## **PCI Latency Timer (in PCI Clocks)**

This option sets latency of all PCI devices on the PCI bus. The settings are in units equal to PCI clocks. The settings are 32, 64, 96, 128, 160, 192, 224, or 248. The Optimal and Fail-Safe default settings are 32.

## **PCI VGA Palette Snoop**

This option must be set to *Enabled* if any ISA adapter card installed in the computer requires VGA palette snooping. The settings are *Disabled* or *Enabled*. The Optimal and Fail-Safe default settings are *Disabled*.

#### **PCI IDE Bus Master**

Set this option to *Enabled* to specify that the IDE controller on the system board or add-on card has bus mastering capability. The settings are *Disabled* or *Enabled*. The Optimal default settings are *Enabled*.

#### Offboard PCI IDE Card

This option specifies if an offboard PCI IDE controller adapter card is used in the computer. You must also specify the PCI expansion slot on the motherboard where the offboard PCI IDE controller card is installed. This requires because mode of PCI IDE add-on card do not have built-in configuration EPROM as

required by PCI specification. If an offboard PCI IDE controller is used, the onboard IDE controller on the motherboard is automatically disabled. The settings are *Disabled*, *Auto*, *Slot1*, *Slot2*, *Slot3*, or *Slot4*.

If *Auto* is selected, AMIBIOS automatically determines the correct setting for this option. The Optimal and Fail-Safe default settings are *Auto*.

## **Offboard PCI IDE Primary IRQ**

This option specifies the PCI interrupt used by the primary IDE channel on the offboard PCI IDE controller. The settings are *Disabled, INTA, INTB, INTC,* or *INTD*. The Optimal and Fail-Safe default settings are *Disabled*.

## Offboard PCI IDE Secondary IRQ

This option specifies the PCI interrupt used by the secondary IDE channel on the offboard PCI IDE controller. The settings are *Disabled*, *INTA*, *INTB*, *INTC*, or *INTD*. The Optimal and Fail-Safe default settings are *Disabled*.

## PCI Slot 1 IRQ Priority...

These options allow user to selectively specify the required interrupt for some special PCI adapter cards. Normally, the system BIOS will assign whatever interrupt available to the PCI adapters installed. However, some PCI adapters required the interrupt assigned to be specific. These options should be set only when you know very well about the PCI adapters installed. Otherwise, they should be set to *Auto*.

#### DMA Channel 0....

These options allow user to selectively assign DMA channel. The options are reserved for advanced user setup. Default setting is PnP.

## IRQ3.....

These options specify the bus that the named interrupt request lines (IRQs) are used on. These options allow you to specify IRQs for use by legacy ISA adapter cards.

These options determine if AMIBIOS should remove an IRQ from the pool of available IRQs passed to BIOS configurable devices. The available IRQ pool is determined by reading the ESCD NVRAM. If more IRQs must be removed from the pool, the end user can use these PCI/PnP Setup options to remove the IRQ by assigning the option to the *ISA/EISA* setting. Onboard I/O are configurable by AMIBIOS. The IRQs used by onboard I/O are configured as *PCI/PnP*. The settings are *PCI/PnP* or *ISA/EISA*. The Optimal and Fail-Safe default settings are *PCI/PnP*.

## **Peripheral Setup**

Peripheral Setup options are displayed by choosing the Peripheral Setup icon from the WINBIOS Setup main menu. All Peripheral Setup options are described in this section. Note that *Auto* selection means the BIOS will detect all the resources available in the system and will setup each peripheral automatically.

#### **On-Board PCI SCSI**

This option specifies the onboard SCSI Controller. The settings are *Enabled* & *Disabled*. The Default setting is *Enabled*.

(This option is only for the system board with Built-in SCSI)

#### Onboard FDC

This option enables the floppy drive controller on the motherboard. Note that if there is another floppy controller exist on the I/O bus, such as from adapter card, then the onboard FDC

will be automatically disabled. The settings are Auto, *Enabled* or *Disabled*. The Optimal default setting is *Auto*.

#### **Onboard Serial Port1**

This option enables serial port 1 on the motherboard and specifies the base I/O port address for serial port 1.

The settings are 2F8h, 2E8h, 3F8h, 3E8h, Auto or *Disabled*. The Optimal default setting *Auto*.

#### **Onboard Serial Port2**

This option enables serial port 2 on the motherboard and specifies the base I/O port address for serial port 2.

The settings are *2F8h*, *2E8h*, *3F8h*, *3E8h*, *Auto* or *Disabled*. The Optimal default setting is *3F8h*. The Fail-Safe default setting is *Auto*.

#### **Onboard Parallel Port**

This option enables the parallel port on the motherboard and specifies the parallel port base I/O port address. The settings are *378h*, *278h*, *3BCh*, *Auto* or *Disabled*. The Optimal default setting is *Auto*.

#### **Parallel Port Mode**

This option specifies the parallel port mode. ECP and EPP are both bi-directional data transfer schemes that adhere to the IEEE P1284 specifications. The settings are:

Setting	Description
Normal	The normal parallel port mode is used. This is the
	default setting.
EPP	The parallel port can be used with devices that adhere
	to the Enhanced Parallel Port (EPP) specification. EPP
	uses the existing parallel port signals to provide
	asymmetric bi-directional data transfer driven by the

Setting	Description
	host device.
ECP	The parallel port can be used with devices that adhere
	to the Extended Capabilities Port (ECP) specification.
	ECP uses the DMA protocol to achieve transfer rates
	of approximately 2.5 Mbs. ECP provides symmetric
	bi-directional communications.

#### **EPP version**

This option is reserved for some of old version EPP devices that were designed based on early version of the EPP specification. The function is only for debugging purpose.

## **Parallel Port IRQ**

Normally parallel port uses interrupt 7 (if mapped at primary address 378h). However, it also can use interrupt 5 (if mapped as secondary address 278h). Default setting is Auto.

## **Security Setup Window**

## **Supervisor**

Select this option to set the password at supervisor level. Note that user level can not change supervisor password.

#### User

Select this option to set the password at user level.

## **Utility Window**

## Language

#### **IDE Detect**

Select this option to let the system detect all IDE devices installed in the system.

## **Default Setup Window**

The Default Setup windows has following options. Every option in BIOS Setup contains two default values: a Fail-Safe default and the Optimal default value.

## **Original Defaults**

Restores old values of setup if the user decides to abandon changes.

## **Optimal Defaults**

The Optimal default values provide optimum performance settings for all devices and system features. If the onboard SCSI, floppy and I/O controller are used in the system, Optimal default setting should be loaded to simplify the CMOS setup process.

#### **Fail-Safe Defaults**

The Fail-Safe default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance characteristics. Once this option is loaded, user should go back to the first selection setup menu to manually select other options.

#### PROGRAMMING FLASH BIOS

You can reprogram the BIOS when there is BIOS update instead of the need to replacing the BIOS EPROM. There are two ways to re-program the Flash BIOS. The first way can be done during boot up time. The second way can be done with utility included in the Utility floppy diskette shipped with the board.

## Flash from boot up time:

- a. Prepare a diskette for BIOS ROM file with the file name should be 54TDP.ROM. This file comes from our technical support HomePage or from our BBS. Once you down load the file, you should rename it to the name above.
- b. Insert a diskette into drive A.
- c. Press the keys CTRL + HOME down and turn the system power on. Release the keys once the systems start to search for the floppy drive. The system will take the file from the floppy diskette and reprogram the onboard FLASH BIOS.

#### Note:

- . If the system beeps two times, it indicates the update ROM file name is not match.
- . If the system beeps continuously, it indicates no diskette in floppy drive.
- . If there is no beep during drive A searching, it indicates the system gets the right file and flashing the FLASH ERPOM. The system will give four beeps when the flashing process completes and then reboots the system with the new BIOS.
- 4. Now you can enter into the CMOS setup by following the CMOS setup procedure in the CMOS setup section.
- If the system crash during flash or corruption caused by BIOS. Just recopy the new BIOS ROM file into floppy diskette and repeat the steps above. The system will automatically flashes BIOS ROM file into EPROM as normal.

# APPENDIX A-AMIBIOS ERROR MESSAGES AND BEEP CODES

Errors can occur during POST (Power On Self Test) which is performed every time the system is powered on. Fatal errors, which prevent the system from continuing the boot process, are communicated through a series of audible beeps. Other errors are displayed in the following format:

ERROR Message Line I ERROR Message Line 2

For most displayed error messages, there is only one message. If a second message appears, it is "RUN SETUP". If this message occurs, press <Fl> to run AMIBIOS Setup.

#### **BEEP CODES**

Beeps	Error Message	Description
1	Refresh Failure	The memory refresh circuitry on the baseboard is faulty.
2	Paity Error	Parity is not support on this product, will not occur
3	Base 64KB Memory Failure	Memory failure in the first 64KB.
4	Timer Not Operational	Memory failure in the first 64KB of memory, or Timer 1 on the baseboard is not functioning.
5	Processor Error	The CPU on the baseboard generated an error.
6	8042-Gate A20 Failure	The keyboard controller(8041) may be bad. The BIOS can not switch to protectd mode.
7	Processor Exception	The CPU generated an exception interrupt.
8	Display Memory Read/Write error	The system video adapter is either missing or its memory is faulty. This is not a fatal erroe.
9	ROM Checksum Error	ROM checksum value does not match the value enclosed in BIOS.
10	CMOS Shut down Register Read/Write Error	The shutdown register for CMOS RAM failed.
11	Cache Error External Bad	The external cache is faulty.

#### ERROR MESSAGES

	E14'
0042 G + 120 F	Explanation (2012)
8042 Gate-A20 Error	Gate A20 on the keyboard controller (8042) is not
Address Line Short!	working. Replace the 8042.  Error in the address decoding circuitry on the
Address Line Short!	baseboard.
Casha Managan Dad	
Cache Memory Bad, Do Not Enable Cache!	Cache memory is defective. Replace it.
CH-2 Timer Error	Most AT systems include two times. There is an
	Most AT systems include two timers. There is an error in timer 2.
CMOS Battery State	CMOS RAM is powered by a battery. The battery
Low	power is low. Replace the battery.
CMOS Checksum	After CMOS RAM values are saved, a checksum
Failure	value is generated for error checking. The previous
	value is different from the current value. Run
	AMIBIOS Setup.
CMOS System	The values stored in CMOS RAM are either corrupt
Options Not Set	or nonexistent. Run setup.
CMOS Display Type	The video type in CMOS RAM does not match the
Mismatch	type detected by the BIOS. Run AMIBIOS Setup.
CMOS Memory Size Mismatch	The amount of memory on the baseboard is
Mismatch	different than the amount in CMOS RAM. Run AMIBIOS Setup.
CMOS Time and Date	Run Standard CMOS Setup to set the date and time
Not Set	in CMOS RAM.
Diskette Boot Failure	The boot disk in floppy drive A: is corrupt. It
	cannot be used to boot the system. Use another
	boot disk and follow the screen instructions.
Display Switch Not	The display jumper is not implemented on this
Proper	product, this error will not occur.
DMA Error	Error in the DMA controller.
DMA #1 Error	Error in the first DMA channel.
DMA #2 Error	Error in the second DMA channel.
FDD Controller	The BIOS cannot communicate with the floppy disk
Failure	drive controller. Check all appropriate connections
	after the system is powered down.
HDD Controller	The BIOS cannot communicate with the hard disk
Failure	drive controller. Check all appropriate connections
DIED //1 E	after the system is powered down.
INTR #1 Error	Interrupt channel 1 failed POST.
INTR #2 Error	Interrupt channel 2 failed POST.
Invalid Boot Diskette	The BIOS can read the disk in floppy drive A:, but
TZ 1 1'	cannot boot the system. Use another boot disk.
Keyboard is	The keyboard lock on the system is engaged. The
LockedUnlock it	system must be unlocked to continue.

	Explanation		
Keyboard Error	There is a timing problem with the keyboard. Set		
	the keyboard option in standard CMOS Setup to		
	Not installed to skip the keyboard POST routines.		
KB/Interface Error	There is an error in the keyboard connector.		
Off Board Parity Error	Parity error in memory installed in an expansion		
	slot. The format is:		
	OFF BOARD PARITY ERROR ADDR (HEX) =		
	(XXXX)		
	XXXX is the hex address where the error occurred.		
On Board Parity Error	Parity is not supported on this product, this error		
	will not occur.		
Parity Error ????	Parity error in system memory at an unknown		
	address.		

## ISA NMI MESSAGES

ISA NMI Message	Explanation
Memory Parity Error	Memory failed. If the memory location can be
at xxxxx	determined, it is displayed as xxxxx. If not, the
	message is Memory Parity Error ????.
I/O Card Parity Error	An expansion card failed. If the address can be
at xxxxx	determined, it is displayed as xxxxx. If not, the
	message is I/O Card Parity Error ????.
DMA Bus Time-out	A device has driven the bus signal for more than 7.8
	microseconds.

## APPENDIX B: AMI BIOS HARD DISK TYPE

Туре	Cylinder	Heads	Write Precomp	Landing Zone	Sectors	Size
1	306	4	128	305	17	10MB
2	615	4	300	615	17	20MB
3	615	6	300	615	17	31MB
4	940	8	512	940	17	62MB
5	940	6	512	940	17	47MB
6	615	4	65535	615	17	20MB
7	462	8	256	511	17	31MB
8	733	5	65535	733	17	30MB
9	900	15	65535	901	17	112MB
10	820	3	65535	820	17	20MB
11	855	5	65535	855	17	35MB
12	855	7	65535	855	17	50MB
13	306	8	128	319	17	20MB
14	733	7	65535	733	17	43MB
16	612	4	0	663	17	20MB
17	977	5	300	977	17	41MB
18	977	7	65535	977	17	57MB
19	1024	7	512	1023	17	60MB
20	733	5	300	732	17	30MB
21	733	7	300	732	17	43MB
22	733	5	300	733	17	30MB
23	306	4	0	336	17	10MB
24	925	7	0	925	17	54MB
25	925	9	65535	925	17	69MB
26	754	7	754	754	17	44MB
27	754	11	65535	754	17	69MB
28	699	7	256	699	17	41MB
29	823	10	65535	823	17	68MB
30	918	7	918	918	17	53MB

Туре	Cylinder	Heads	Write Precomp	Landing Zone	Sectors	Size
31	1024	11	65535	1024	17	94MB
32	1024	15	65535	1024	17	128MB
33	1024	5	1024	1024	17	43MB
34	612	2	128	612	17	10MB
35	1024	9	65535	1024	17	77MB
36	1024	8	512	1024	17	68MB
37	615	8	128	615	17	41MB
38	987	3	987	987	17	25MB
39	987	7	987	987	17	57MB
40	820	6	820	820	17	41MB
41	977	5	977	977	17	41MB
42	981	5	981	981	17	41MB
43	830	7	512	830	17	48MB
44	830	10	65535	830	17	69MB
45	917	15	65535	918	17	114MB
46	1224	15	65535	1223	17	152MB
47	USER'S	TYPE				

# APPENDIX C: ISA I/O ADDRESS MAP

I/O ADDRESS (HEX)	I/O DEVICE	
000 - 01F	DMA Controller 1, 8237A-5	
020 - 03F	Interrupt Controller 1, 8259A	
040 - 05F	System Timer, 8254-2	
060 - 06F	8742 Keyboard Controller	
070 - 07F	real-time Clock/CMOS and NMI Mask	
080 - 09F	DMA Page Register, 74LS612	
0A0 - 0BF	Interrupt Controller 2, 8259A	
0C0 - 0DF	DMA Controller 2, 8237A-5	
0F0 - 0FF	i486 Math Coprocessor	
1F0 - 1F8	Fixed Disk Drive Adapter	
200 - 207	Game I/O	
20C - 20D	Reserved	
21F	Reserved	
278 - 27F	Parallel Printer Port 2	
2B0 - 2DF	Alternate Enhanced Graphic Adapter	
2E1	GPIB Adapter 0	
2E2 - 2E3	Data Acquisition Adapter 0	
2F8 - 2FF	Serial Port 2 (RS-232-C)	
300 - 31F	Prototype Card	
360 - 363	PC Network (Low Address)	
364 - 367	Reserved	
368 - 36B	PC Network (High Address)	
36C - 36F	Reserved	
378 - 37F	Parallel Printer Port 1	
380 - 38F	SDLC, Bisynchronous 2	
390 - 393	Cluster	
3A0 - 3AF	Bisynchronous 1	
3B0 - 3BF	Monochrome Display and Printer Adapter	
3C0 - 3CF	Enhanced Graphics Adapter	
3D0 - 3DF	Color/Graphics Monitor Adapter	

I/O ADDRESS (HEX)	I/O DEVICE
3F0 - 3F7	Diskette Drive Controller
3F8 - 3FF	Serial Port 1 (RS-232-C)
6E2 - 6E3	Data Acquisition Adapter 1
790 - 793	Cluster Adapter 1
AE2 - AE3	Data Acquisition Adapter 2
B90 - B93	Cluster Adapter 2
EE2 - EE3	Data Acquisition Adapter 3
1390 - 1393	Cluster Adapter 3
22E1	GPIB Adapter 1
2390 - 2393	Cluster Adapter 4
42E1	GPIB Adapter 2
62E1	GPIB Adapter 3
82E1	GPIB Adapter 4
A2E1	GPIB Adapter 5
C2E1	GPIB Adapter 6
E2E1	GPIB Adapter 7

# APPENDIX D: EISA I/O ADDRESS SPACE

ADDRESS (Hex)	DESCRIPTION	COMMENTS	
0000 - 00FF	ISA System Board I/O		
0100 - 03FF	ISA Expansion Adapter	EISA System Board	
0400 - 04FF	EISA System Board Controller	ISA I/O Space	
0500 - 07FF	Alias of 0100 - 03FF	(0 to 4KB Range)	
0800 - 08FF	EISA System Board I/O		
0900 - 0BFF	Alias of 0100 - 03FF		
0C00- 0CFF	EISA System Board I/O		
0D00- 0FFF	Alias of 0100 - 03FF		
1000 - 10FF	Slot 1 I/O		
1100 - 13FF	Alias of 0100 - 03FF		
1400 - 14FF	Slot 1 I/O		
1500 - 17FF	Alias of 0100 - 03FF	EISA Slot 1 I/O Space	
1800 - 18FF	Slot 1 I/O		
1900 -1BFF	Alias of 0100 - 03FF		
1C00 -1CFF	Slot 1 I/O		
1D00 -1FFF	Alias of 0100 - 03FF		
z100 - z3FF	Alias of 0100 - 03FF		
z400 - z4FF	Slot "z" I/O		
z500 - z7FF	Alias of 0100 - 03FF	EISA Slot "z" I/O Space	
z800 - z8FF	Slot "z" I/O	z = 2, 3, 4, 5, 6, 7, 8, 9	
z900 - zBFF	Alias of 0100 - 03FF	A, B , C, D, E, or F	
zC00 - zCFF	Slot "z" I/O		
zD00 - zFFF	Alias of 0100 - 03FF		

## APPENDIX E: INTERRUPT LEVEL ASSIGNMENTS

LEVEL	LEVEL	TYPICAL INTERRUPT SOURCE
on SYSTEM	on IO BUS	
NMI	None	Parity, ISA/EISA Channel Check,
		Bus Time Out, Fail Safe Timer Time-out
IRQ0	None	Interval Timer 1, Counter 0 Out
IRQ1	None	Keyboard Controller
IRQ2	None	Cascade Interrupts from IRQ8 to IRQ15
IRQ3	IRQ3	Serial Port 2
IRQ4	IRQ4	Serial Port 1
IRQ5	IRQ5	Parallel Port 2
IRQ6	IRQ6	Diskette Controller
IRQ7	IRQ7	Parallel Port 1
IRQ8	None	Real Time Clock
IRQ9	IRQ2	Expansion Bus Pin
IRQ10	IRQ10	Expansion Bus Pin
IRQ11	IRQ11	Expansion Bus Pin
IRQ12	IRQ12	Expansion Bus Pin
IRQ13	None	Coprocessor Error, DMA Chaining
IRQ14	IRQ14	Fixed Disk Drive Controller
		Expansion Bus Pin
IRQ15	IRQ15	Expansion Bus Pin

## APPENDIX F: MEMORY MAP

Address	Function	Comments	
(hex)			
00000000-0007FFFF	512K System RAM	Cached	
00080000-0009FFFF	128K System RAM	Cached	
000A0000-000BFFFF	128K Video RAM	Not Cached	
000C0000-000C7FFF	32K Video BIOS	Cached	
000C8000-000CFFFF	32K I/O ROM	Not Cached	
000D0000-000DFFFF	64K I/O ROM	Not Cached	
000E0000-000EFFFF	64K Extended BIOS	Not Cached	
000F0000-000FFFFF	64K On-Board BIOS ROM	Cached	
00100000-00BFFFFF	System Memory (RAM)	Cached	
00C00000-00FFFFF	System Memory (RAM)	Cached	
01000000-BFFFFFF	System Memory (RAM)	Cached	
C0000000-C1FFFFF	System Memory (RAM)	Cached	
C2000000-FFFDFFFF	System Memory	Cached	
FFFE0000-FFFFFFF	128K On-Board BIOS ROM	Not cached	

## PRODUCT INFORMATION RECORD

System Roard

Record all the information as you receive the product and provide to your supplier in writing in the event that you should need technical support assistance. This will help to speed up the response and get your problem solved.

Date Purchased or R	eceived:		
Purchased From:			
Product Name:		PCB Ver:	Rev:
Serial Number:			
CPU Processor Spee	ed:	Memory Size	e:
BIOS Version:	Software Driver	r Rel #:	
PCI Add-on Card	ls:		
Model #	Interrupt	:	_ Slot #:
Model #	Interrupt	:	_ Slot #:
Model #	Interrupt	•	_ Slot #:
ISA Add-on Carc	ls:		
Model #	Interrupt:	_ DMA:	_ Slot #:
Model #	Interrupt:	_ DMA:	_ Slot #:
Model #	Interrupt:	_ DMA:	_ Slot #:
	Interrupt:	DM	C1 //

For More In	formatic	on .	 	 