

# SI54P AIO

(FOR PHOENIX BIOS)





## SI54P AIO User's Manual (for Phoenix BIOS)

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## Contents 🖉

Introduction	
General Specifications	1
System Chipset	2
-,	
System Memory	
Casha Mamara Subaratawa	-
Cache Memory Subsystems	
lumper Settings and Connectors	
	~
Setting the Jumpers	S
Connectors	7
Board Layouts	8
Built-in BIOS SETUP Program	
SETUP Program	9
System Setup	10
Fixed Disk Setup	11
Advanced System Setup	13
Integrated Peripherals	14
Memory Cache	15
Memory Shadow	18
Advanced Chipset Control	19
PCI Devices	23
Boot Options	26
Security Setup	27
Green PC Feature	28
Load ROM Default Values	31
Load Values from CMOS	32
Save Values to CMOS	33
On it is a factor	21

## **1** Introduction

The SI54P AIO is a Pentium<sup>™</sup> PCI Bus mainboard. It uses the SiS 85C501, 85C502, 85C503 system chipset, CMD PCI0640B PCI Bus IDE Controller, and SMC 37C665 Super I/O Controller. Other on-board specifications include 4 AT Bus slots and 4 PCI slots, 2 memory banks with memory sizes of up to 128MB, and cache sizes from 256KB to 1MB.

## 1.1 General Specifications

Processor:	Intel Pentium™ 75/90/100
Chipset:	SiS 85C501 (PCI/ISA Cache Memory Controller) SiS 85C502 (PCI Local Data Buffer) SiS 85C503 (PCI System I/O) CMD PCI0640B (PCI Bus IDE Controller) SMC 37C665 (Super I/O Controller) UMC 82C865 (I/O TTL Integration)
External Cache:	256/512 KB or 1MB cache supporting write back or write-through policies
Memory Size:	2 banks of DRAM with memory size capacity of up to 128MB, all supporting double-sided SIMMs
BIOS:	Phoenix
Slots :	Four 16-bit ISA slots Four PCI slots
Connectors:	Power Keylock & Power LED Hardware Reset Speaker Turbo LED Turbo Switch Suspend HDD LED
Form Factor:	Baby-AT
PCB :	4 layers

1

#### System Chipset

#### SIS 85C501

- Supports Pentium<sup>™</sup> processor at 50/60/66 MHz bus speed
- Integrated second level (L2) cache modes
- write-through and write-back cache modes
- direct mapped organization
- supports standard and burst SRAMs
- supports 128KB to 2MB cache sizes
- cache read/write cycle of 3-2-2-2 or 4-3-3-3 using standard SRAM at 66MHz
- Integrated DRAM controller
- supports 2MB to 128MB of cacheable main memory
- 1 level posted write buffer of 4 Qwords deep
- concurrent write back
- CAS#-before-RAS# transparent DRAM refresh
- 256K/1M/4M/16M\*N 70ns fast page mode DRAM support
- programmable DRAM speed

#### SIS 85C502

- Three integrated posted write buffers and two read buffers increase system performance
- 1 level CPU-to-Mem posted write buffer with 4 Qwords deep
- 4 levels CPU-to-PCI posted write buffer with 4 Dwords deep
- 1 level PCI-to-Mem posted write buffer with 1 Qword deep
- 1 level Mem-to-CPU read buffer with 1 Qword deep
- 1 level Mem-to-PCI read buffer with 1 Qword deep
- Provides a 64-bit Pentium<sup>™</sup>, DRAM data bus and 32-bit PCI data bus
- Operates synchronously to the 66.7MHz CPU and 33.3MHz PCI clocks
- Provides parity generation for memory writes

#### SIS 85C503

- Integrated bridge between PCI Bus and ISA Bus
- translates PCI Bus cycles into ISA Bus cycles
- translates ISA master or DMA cycles into PCI Bus cycles
- provides PCI-to-ISA memory one Dword posted write buffer
- Integrated ISA Bus compatible logic
- Supports reroutability of four PCI interrupts to any unused IRQ interrupt
- Supports Flash ROM

#### CMD PCI0640B

- Fully compatible with the latest PCI IDE and ATAPI specifications
- The most complete 32-bit driver support in the industry (DOS, Windows 3.1 Past Disk, Windows NT, OS/2, Novell & SCO Unix 32-bit driver support)
- Programmable data transfer timing supports customized setting for 4 IDE devices
- Read-ahead and write-back buffers enhance transfer rates and allow concurrent operations
- Suitable for PCI motherboard or PCI expansion card applications
- Fully supports and surpasses enhance IDE Mode-3
- Supports program I/O function

#### SMC 37C665

- Super I/O controller
- Two 16C550 compatible UARTs
- One multi-mode parallel port which include EPP and ECP support

## 2 System Memory

SI54P AIO accepts a minimum of 2MB and a maximum of 128MB onboard. There are two memory banks which support 256/512 KB or 1/2/4/8/16 MB 72-pin type, single- and/or double-density modules.

Important: DRAM insertion on every bank should come in pair and of the same type. For instance, if you only have two DRAM modules, you cannot install one DRAM module in socket SIM1 and another DRAM module of the same type on SIM3. Likewise, memory type mixing is NOT allowed within a bank.

The following table lists all the possible DRAM module combinations and the total memory amount for each option.

Bank 0		Ban	k1	Total
SIM3	SIM4	SIM1	SIM2	Memory Size
256K x 36	256K x 36	None	None	2MB
256K x 36	256K x 36	256K x 36	256K x 36	4MB
512K x 36	512K x 36	None	None	4MB
512K x 36	512K x 36	512K x 36	512K x 36	8MB
512K x 36	512K x 36	4M x 36	4M x 36	36MB
1M x 36	1M x 36	None	None	8MB
1M x 36	1M x 36	1M x 36	1M x 36	16MB
1M x 36	1M x 36	4M x 36	4M x 36	36MB
2M x 36	2M x 36	None	None	16MB
2M x 36	2M x 36	2M x 36	2M x 36	32MB
2M x 36	2M x 36	4M x 36	4M x 36	48MB
4M x 36	4M x 36	4M x 36	4M x 36	64MB
8M x 36	8M x 36	None	None	64MB
8M x 36	8M x 36	8M x 36	8M x 36	128MB

Table 2-1. Memory Configurations and Requirements

Cache Size	Dirty RAM (U28)	TAG RAM (U27)	Data (U23-26) (U34 - U37)
256KB	32Kx8 (5V)	32Kx8 (5V)	32Kx8 (3.3V)
512KB	32Kx8 (5V)	32Kx8 (5V)	64Kx8 (3.3V)
1MB	32Kx8 (5V)	32Kx8 (5V)	128Kx8 (3.3V)

## **Cache Memory Subsystems**

Table 2-2. Second Level Cache Memory Configurations

## **3 Jumper Settings and Connectors**

## 3.1 Setting the Jumpers

The table below summarizes the functions and jumper settings on the SI54P AIO.

F	Jumper Settings	
	50MHz (for 75MHz CPU)	JP7 short 2-3, 5-6, 7-8
CPU Clock Select	60MHz (for 90MHz CPU)	JP7 short 2-3, 4-5, 8-9
1 m 6 m 1	66MHz (for 100MHz CPU)	JP7 short 1-2, 5-6, 7-8
	Internal Cache Write-back	JP12 short 1-2
CPU Signal Select	Internal Cache Write- through	JP12 short 2-3
	Always invalidated	JP14 short 1-2
1 î.h.	Write to invalidated	JP14 short 2-3
n Alexandra ang Managangangangangangangangangangangangang	256KB (with 32Kx8 SRAMs)	JP11 open JP10 open
External Cache Memory Settings	512KB (with 64Kx8 SRAMs)	JP11 short JP10 open
Million and States	1MB (with 128Kx8 SRAMs)	JP11 short JP10 short

Table 4-1. Jumper Settings (Continued . . . . )

	Function	Jumper Settings
Sec. 2. 20	For Programming Flash ROM (+5V) used	JP8 short 1-2
ROM BIOSSelection	For Programming Flash ROM (+12V) used	JP8 short 2-3
	EPROM.	JP8 open
. Second States of Second	Enable IDE	JP4 open
On-board PCI IDE	Disable IDE	JP4 short
	Enabled	JP3 short 1-2
On-board I/O	Disabled	JP3 short 2-3
State and a state of the state	ECP Mode Parallel Port DRQ1 DACK1 Selection	JP1 short 1-2 JP2 short 2-3
ECP Mode	ECP Mode Parallel Port DRQ3 DACK3 Selection	JP1 short 2-3 JP2 short 1-2
Sec. State of the state	Enabled	JP9 short
DRAM Parity Check	Disabled	JP9 open
n Bolaich ang Staite an Staite an Staite	All SIMMs are single density modules	JP5 short 2-3
Memory Select	All SIMMs are double density modules or SIMMs 3/4 are double density and SIMMs 1/2 are single density	JP5 short 1-2, 3-4

Table 4-1. Jumper Settings

Note1: If a flash ROM is installed on the mainboard, please refer to the README.DOC file in the Flash Utility diskette before programming the Flash ROM BIOS.

Note2: Before installing the driver for on-board PCI IDE (CMD PCI0640B), consult the readme file in the CMD Driver Diskette.

Note3: 1. JP8 open for EPROM and Flash ROM normal use.

- 2. When you update your system BIOS with Flash ROM utility, please set the JP8 to short 1-2 for +5V Flash ROM or JP8 to short 2-3 for +12V Flash ROM.
- 3. After updated the system BIOS, you should remove the jumper JP8.

6

## 3.2 Connectors

There are several connectors located on the SI54P AIO. Their functions are listed below.

Connector	Function
J2	AT Keyboard Connector
J4	Power Connector
J5	Floppy Connector
J6	COM1 Port Connector
J7	COM2 Port Connector
J8	Printer Port Connector
J9	IDE Primary Connector
J10	IDE Secondary Connector
J11	Power Connector (For 3.3V)
J12	HDD LED Connector
J13	2X10 JUMPER BLOCK



pin 2-3: Turbo LED pin 4-5: Suspend Push Button (SMI) PIN 6-7: Turbo Switch pin 9-10: Hardware Reset pin11-13: System Power LED & pin 14-15 Keylock pin 17-20: Speaker

Note:

J13 (pin6-7), Turbo Switch Function Procedure: a. Short 2-3 for the jumper setting of JP12. b. Set the L1 Cache Update Mode into (WT) Write

- Through within the BIOS Chipset Features SETUP. c. After finishing Steps a & b, the H/W turbo switch will
- function normal and the Turbo LED will turn on/off when system in the Turbo/De-turbo mode.



## 3.3 Board Layouts

Figure 4-1. SI54P AIO Mainboard Layout

## 4 Built-in BIOS SETUP Program

## 4.1 SETUP Program



Figure 4-1. SETUP Main Menu

It is highly recommended that you list down all the values of the SETUP program before making any changes. Doing so will save a lot of time restoring the system back in the event of a configuration memory loss.

Note: On-screen instructions at the bottom of each screen explain how to use the program.

**System Setup** - allows checking or modification of general configuration information.

**Fixed Disk Solup** - allows for automatic detection of the hard disk drive type(s) including the number of cylinders and heads, write pre-compensation time, read/write head landing zone, and number of sectors per track. Also switches the LBA Mode feature of the hard disk to on or off.

Advanced System Setup - sets the various system options for the user, including the Integrated Peripherals, Memory Cache, Memory Shadow, Advanced Chipset Control, and PCI Devices.

**Boot Options -** determines the sequence with which the system will proceed when booting the operating system.

**Socurity Setup** - provides special access for the user to enter the operating system and Setup program, and restricts unauthorized access to the floppy disk drives.

**Green PC Features -** allows the timer settings for the DOZE, STANDBY and RESUME modes. It also lists the SMI events by which the system wakes up from STANDBY or SUSPEND modes. If the device is not active, Power Management Function will slow down the CPU speed and bothe IDE and monitor will be put into doze, standby, or suspend mode.

Load ROM Default Values - allows for automatic configuration of all the above options using the values stored in the ROM BIOS table.

Load Values from CMOS - allows for automatic configuration of all the above options using the previous values stored in the CMOS SRAM.

Save Values to GMOS - saves the changes you have made in the SETUP program, then exits and reboots the system.

To choose an item from the SETUP main menu, move the cursor using the <Up> and <Down> arrow keys and press <Enter>.

## 4.2 System Setup



Figure 4-2. System Setup Screen

System Time - sets the system's internal clock which includes hour, minutes, and seconds.

Systom Date - allows manual setting of the electronic calendar on the mainboard.

Wideo System - specifies the display adapter installed.

**System/Extended Memory** - displays important information about your system configuration which includes the system and extended memory sizes. They are updated automatically by the SETUP program according to the status detected by the BIOS self-test. This section of the System Setup screen is for viewing purpose only and manual modifications are not allowed.

**Diskette Drive A:/B**: - specify the capacity and format of the floppy drives installed in your system.

Koyboard - selects Install/ Not Installed for keyboard device setting.

### 4.3 Fixed Disk Setup

The Fixed Disk Setup provides auto configuration of the hard drive installed in the system. After pressing the <Enter> key on this item in the main menu, the following screen is displayed.



Figure 4-3. Fixed Disk Setup Screen 1

Once the program detects the type of hard disk 0 and/or 1 installed, it will display the relative information such as the type, cylinder, heads, write precompensation, landing zone, number of sectors per track, and the LBA mode control.

If the program fails to detect the hard disk type(s) or the <Enter> key was not pressed in the Autotype Fixed Disk option, manual setting of the values is recommended.

Fixed Disk 0 Cont	trol (Boot Drive)	
Autotype Fixed Disk:	[Press Enter]	
Tume:	[User]	100
Culinders:	[ 667]	
Heads:	[ 8]	
Sectors/Track:	[ 33]	
Write precomp:	[None]	1.0
Multi-Sector Transfers:	[Disabled]	
LBA Node, Control:	[Disabled]	
32 Dit 1/0:	[Disabled]	1. 1. 1. 1.

Figure 4-4. Fixed Disk Setup Screen 2

**Autotype Fixed Disk** - detects the type of fixed disk 0 and/or 1 installed. If successful, it fills the remaining fields on this menu.

Type - 1 to 45 fill the remaining fields with values for predefined disk drives. "User" allows the user to fill in the remaining fields. "Auto" allows the system auto detect IDE HDD Function, if you already install IDE HDD.

**Cylinders** - specifies the number of cylinders of the hard disk drive.

**Hoads** ~ specifies the number of read/write heads of the hard disk drive.

**Sociors/Track** - provides the number of sectors per track defined for the hard disk drive.

**Landing Zono** - refers to the cylinder number where the disk drive heads (read/write) are positioned to when the disk drive is parked.

Write Procomp - refers to the cylinder number, above which, disk drive operations require reduced write current. Also specifies the number of cylinders at which to change the write timing.

**Largo Disk Access Mode** - for Large Hard Disk Compatibility (larger than 528MB) issues, you must enable this item except when running the system under UNIX. The default setting of this option is "Disabled."

**Multi-Sector Transfors** - determines the number of sectors per block for multiple sector transfers. The available options are 2/4/8/16 sectors, "Auto" which refers to the size the disk returns when queried, and "Dis-abled" (default).

**LBA Mode Control** - turns on or off the hard disk drive's LBA Mode support. Some HDD sizes support more than 540MB and the LBA mode for data transfer. If your hard disk supports LBA mode, you should enable (on) this option otherwise disable (off) it.

**32 BR1/0** - it is only for PCI IDE card, if you want to use the ISA IDE card, you have to disable it.

## 4.4 Advanced System Setup

The Advanced System Setup allows the user to program five main groups of parameters namely the Integrated Peripherals, Memory Cache, Memory Shadow, Advanced Chipset Control, and PCI Devices. This BIOS Setup parameter is designed for programmers who wish to fine tune the on-board chipset.



Figure 4-5. Advanced System Setup Screen

#### Integrated Peripherals

Selecting Integrated Peripherals from the Advanced System Setup main menu displays the following screen. The actual features displayed depend on the capabilities of your system's hardware.

Integrated Pe	ripherals	
COM1 Port: COM2 Port: LFT Port: Diskette Controllor: LFT Extended Mode: CMD Enhanced Mode:	(1080, 180, 41) (288, 180, 31) (370, 180, 71) (Enabled) (Standard) (Disabled)	ن ہے۔ 12 کے کار 12 کار کار

Figure 4-6. Integrated Peripherals Screen

**GOM1/2 Port** - assign the addresses of the primary and secondary serial ports on-board. The available options are:

Enabled (default)

**LPT Port** - assigns the address of the parallel port on-board. This option also prevents the system from encountering any conflict when an add-on card with parallel port is installed in the future. The available options are:

Enabled (default) Disabled

**Diskette controller** - sets the diskette controller mode of the SMC 37C665 I/O chip to either on or off. The available options are:

Enabled (default)

**LPT Extended Mode** - In "ECP & EPP" mode, EPP can select through the ECR register of ECP mode 100. "Standard" mode can be selected through the ECR register as mode 000. The available options are:



**GMD Enhanced Mode** - enables 32 Bit I/O and CMD Enhanced Mode to support CMD DOS driver.

#### Memory Cache

Selecting the Memory Cache from the Advanced System Setup main menu displays the following screens. The actual features displayed depend on the capabilities of your system's hardware.

	Mon	ory Cache	
Exte	arnal cache:	(Engl)ed)	
L1 (	ache write back:	[Enabled]	
LZ (	ache write back:	[Enabed]	
Sust	ten BIOS cacheable:	[Disabled]	
Cacl	ne speed:	[Slower]	
Cacl	e burst r/w cantle:	[37]	
Refi	resh RAS active time:	[6]]	UI.
Non-	cacheable area#1:	[Disabled]	н
Allo	cation of non-cacheable	area#1: [Local DRAM]	
	Region 1, start addr:	E 0 KB1	
	Region 1, size:	[ 61 KB]	
10.00			-
-	and a second second second second		_

Figure 4-7. Memory Cache Screen 1

Menory Cache	
Non-cacheable area#1: Allocation of non-cacheable area#1: Region 1, start addr: Region 1, size:	(DIGRATICA) Lacal DRANJ L 0 KBJ L 64 KBJ
k 's amhil 's churse 's l	ione 122 <sup>1</sup> 220 757 132

Figure 4-8. Memory Cache Screen 2

External cache - turns on or off the function of the external (L2) cache memory.

Enabled (default) Disabled

LI cache write back - switches the write-back feature of the (L1) internal cache of the Pentium<sup>™</sup> CPU to either on or off. "Disabled" sets the L1 cache into write through mode. The available options are:



Disabled

L2 cacho write back ~ switches the write-back feature of the (L2) external cache on-board to either on or off. "Disabled" sets the L2 cache into write through mode. The available options are:

Concession in which the	-
	E
=	_
	D

nabled (default) Disabled

System BIOS cacheable - controls the caching of the system BIOS area.

Enabled

Disabled (default)

**Cacho spood** - specifies the speed of the standard SRAM cache during normal read/write operations. The available option are:

Slower Faster Fastest **Cacho burst r/w cyclo** - defines the speed of the cache SRAM burst read/write cycles. The available options are:



**Refresh RAS active time** - defines the amount of active time needed for the row address strobe (RAS), during DRAM refresh time, to be refreshed.

5T 6T (default)

**Non-cacheable area#1/#2** - allow a certain block of the local DRAM to be classified as non-cacheable. The available options are:

Enabled
 Disabled (default)

**Allocation of non-cacheable area#1/#2** - define the location of the non-cacheable blocks. The available options are:

Local DRAM (default)

AT Bus

**Rogion 1/2 start addr** - accommodates ISA devices that have their memory mapped into the 1MB to 15.5MB range (i.e., an ISA LAN card or an ISA frame buffer), and defines a hole in main memory that transfers the cycles in this address space to the PCI Bus instead of main memory. This area is not cacheable and its default is 0 KB.

**Region 1/2, Size** - defines the size or Region 1/2. If the frame buffer range is programmed below 16MB and within main memory space, this option must include the frame buffer range. The amount of main memory specified in the following options is remapped to the top of main memory. The options are:



#### Memory Shadow

Selecting the Memory Shadow from the Advanced System Setup main menu displays the following screen. The actual features displayed depend on the capabilities of your system's hardware.

	Nenor	y Shadou	State of the second second
System 1	010S shadow:	Enabled	 
Video B.	IOS shadow:	[Enabled]	a 15 kilo 58
Shadow (	Option ROM'S		20 52
C800	) - CFFF:	[Disabled]	- 20g -
DBOO	) - DFFF:	[Disabled]	at the state

Figure 4-9. Memory Shadow Screen

System BIOS shadow ~ allows shadowing of the system BIOS which improves the system performance. This option is always set as "Enabled."

**Video BIOS shadow** - sets the mode of the system's video BIOS shadowing mode. The available options are "Enabled" (default) and "Disabled."

**Shadow Option ROM's** - shadows the memory regions located in the specified blocks of memory, which can likewise improve the system performance.

Note: Some option ROMs do not work properly when shadowed.

### Advanced Chipset Control

Selecting the Advanced Chipset Control from the Advanced System Setup main menu displays the following screens. The actual features displayed depend on the capabilities of your system's hardware.

Advanced Chips	et Control
DRAM read CAS pulse width:	[41]
DRAM write CAS pulse width:	[37]
DRAM CAS precharge time:	[27]
DRAM RAS precharge time:	[ST]
RAS to CAS delay Time:	[4T]
DRAM write push to CAS delay:	[27]
PCI master access shadow RAM:	[Disabled]
GateA20 enulation:	[Enabled]
Fast reset enulation:	[Enabled]
Fast reset latency:	[2 us]
16-hit I/O recovery time:	[5 BusClk]
8-bit I/O recovery time:	LB BusClk]
16-bit mem, I/O wait state:	[1 Ws]
81	v

Figure 4-10. Advanced Chipset Control Screen 1





**DRAM read CAS pulse width** ~ determines the pulse width length of the CAS during DRAM read cycles. The available options are:



4T (default)

**DRAM write CAS pulse width** - determines the pulse width length of the CAS during DRAM write cycles. The available options are:

2T

3T (default)

**DRAM CAS precharge time** - sets the amount of time for DRAM CAS recovery. The available options are:

1T 2T (default)

**DRAM RAS procharge lime** - sets the amount of time for DRAM RAS recovery. The available options are:

**4**T

5T (default)

**RAS to CAS delay time** - defines the amount of time required after which a CAS# will be succeeded by RAS# signal. The available options are:

3T 4T (default)

**DRAM write push to CAS delay** - pertains to the number of cycles needed by DRAM to force the CAS to delay thereby matching the DRAM timing specifications. The available options are:

1T 2T (default)

**PCI master accesses shadow RAM** - enables the PCI master shadowing for improved performance. The available options are:

Enabled
 Disabled (default)

GalcA20 emulation - allows access and increases the speed of the Gate A20 feature incorporated in the on-board chipset. When enabled, the SiS85C501 responds the cycle by asserting DEVSEL# in slowest timing. Otherwise, the cycle is subtractively decoded by SiS85C503, and then is passed to 8042 on the ISA Bus. The available options are:



Disabled

Fast reset emulation - enhances the speed of the software reset by delaying the assertion of INIT or CPURST by 2µs or 6µs, and holding them for 25 CPUCLK. The available options are:



Disabled

Fast reset latency - defines the time (in microseconds) required for soft-State State - State ware reset. The available options are:

2 μs (default) 6 us

16-bit I/O recovery time - used to specify the 16-bit I/O command recovery time except for some add-on cards that cannot work properly. It is recommended to set this option at a "low" value to enhance the I/O performance. The available options are:

2 BusClk			
3 BusClk			
4 BusClk			
5 BusClk (default)			

8-bit 1/0 recovery time - used to specify the 8-bit I/O command recovery time except for some add-on cards that cannot work properly. It is recommended to set this option at a "low" value to enhance the I/O performance.

1	3 BusClk
	4 BusClk
	5 BusClk
	8 BusClk (default)

16-bit mem, I/O wait state - determines the number of wait states to be inserted to the 16-bit ISA I/O command. The available options are:

0 W/s

1 Ws (default)

**Slow refresh** - allows you to turn the DRAM's slow refresh feature to on or off. The available options are:

Enabled

Disabled (default)

De-lumo switch - controls the software's turbo and de-turbo features.

Always turbo (default)

Enabled

AT hus clock frequency - specifies the speed of the AT Bus clock of the system. The available options are:

PCICLK/3

PCICLK/4 (default)

7.159MHz

PCI clock frequency - selects the timing of the PCI Bus clock.

CPUCLK/1.5

CPUCLK/2 (default)

14MHz

**CAS#width to PCI master willo** ~ defines the pulse width of CAS# when the PCI master writes to DRAM. The available options are:

1T (default) 2T

**Latency for CPU to PCI write** - pertains to the delay time before the CPU writes data into the PCI Bus. The available options are:



**CPU to PCI burst memory write** - If enabled, back-to-back sequential CPU memory write cycles to PCI are translated to PCI burst memory write cycles. If disabled, each single write to PCI will have an associated FRAME# sequence. The available options are:

Enabled Disabled (default)

22

**CPU to PCI post momory write** - enabling allows up to 4 Dwords of data to be posted to PCI. Disabling this option not only disables the buffering but also limits the completion of CPU write (CPU write does not complete until the PCI transaction completes). In general, this option enhances the performance of the PCI slots when "Enabled" (default).

Enabled



**Latencyfrom ADS# to local mem -** determines the CPU to PCI Post write speed. When this is set to "3T" (default), the Post write rate is 5T for each double word. When this option is set to "2T", the rate is 4T per double word. For a Qword PCI memory write, the post write rate is 7T (2T) or 8T (3T).



**Refresh GPU in hold** - enables the refresh cycle when the CPU is in HOLD state. The available options are:



### **PCI** Devices

Selecting the Advanced Chipset Control from the Advanced System Setup main menu displays the following screens. The actual features displayed depend on the capabilities of your system's hardware.

PCI De	vices
Base I/O Address:	[3000]
Base Memory Address:	10000000001
Multimedia node:	[Disabled]
Parity: (Which)	[Disabled]
PCI Interrupt 1 set to:	[None]
Edge/Level Select:	[LEVEL]
PCI Interrupt 2 set to:	[None]
Edge/Level Select:	[Level]
PCI Interrupt 3 set to:	[None]
Edge/Level Select:	[Level]
	▼

Figure 4-12. PCI Devices Screen 1



Figure 4-13. PCI Devices Screen 2

		나는 것 같아요. 이 것 같아.
	PCI Deuice Slot #3'	Ê
	Enable Device:	(Enabled)
	Enable Master:	[Enabled]
	Use Default Latency Timer Value:	[Yes]
12.00	Latency Timer Value:	100403
10.00	PCI Device, Slot #4:	والمراجع والمتجري فليتها مراجع
	Enable Device:	[Enabled]
	Enable Master:	[Enabled]
	Use Default Latency Timer Value:	[Yes]
	Latency Timer Value:	[0040]

Figure 4-14. PCI Devices Screen 3

**Base I/O Address** ~ refers to the base of I/O address ranges from which the PCI device resource requests are satisfied.

**Base Memory Address** - pertains to the base of 32-bit memory address range from which the PCI device resource requests are satisfied.

Multimedia mode - enables or disables palette snooping for multimedia card.

Parity ~ enables or disables the parity checking.

**PCI Interrupt 1/2/3/4 set to** ~ program the IRQ associated with PCI Interrupt 1, 2, 3 and 4. The available IRQs are 3/5/7/9/10/11/ 14/15 and None (default)

**Edgo/Lovel Soloct** - programs the PCI IRQ to single edge or logic level. Level/Edge sensitivity is programmed per controller. Every IRQ input for a given bank is either "EDGE" or "LEVEL" (default) triggered.

Note: When a PCI IDE add-on card is installed onto the mainboard, it will require the user to plug the card onto a daughter board and to set this option to "EDGE" triggered.

#### PCI Device, Slot #1/#2/#3/4#:

Enable Device ~ enables the I/O and memory cycle decoding.

- Disabled (default)
- Enabled

**Enable Master** ~ enables selected device as a PCI bus master and checks whether the PCI card is a master or not.

- Disabled (default)
- Enabled

**Use Default Latency Timer Value** - determines whether or not the default value for the Latency Timer will be loaded or the succeeding Latency Timer Value will be used. If set to "Yes", no further programming is needed in the Latency Timer Value option.

Yes (default)

No

**Latency Timer Value** - pertains to the maximum number of PCI bus clocks that the master may burst. The available options are:

0040 (default)

## 4.5 Boot Options

	Boot Options	*	
Boot se SETUP p POST Er Floppy Sunnary	quence: [A: then C prompt: [Enabled] rors: [Enabled] check: [Enabled] screen:[Enabled]	:]	

Figure 4-15. Boot Options Screen

**Bool Sequence** - selects the drive where the system would search for the operating system to run with. The available options are:

A: then C: (default) C: then A:

**SETUP prompt** - displays the message during boot-up that gives you the chance to load the SETUP program. The available options are:

Enabled	(default)
Disabled	

**POST ENTOTS** - activates the Power-On-Self-Test error messages to be displayed on the screen when detected. The available options are:

Enabled	(defa	ault)
Disabled		63

**Boot Up Floppy Sock** - checks whether the floppy drives installed on the system are correct or not. This option's operation usually occurs when the magnetic heads of the floppy drives produce a sound during power on self test. The available options are:

Enabled (default)

**Summary SCHOON** - enables (default) or disables the Summary Screen display. The Summary Screen descripts the system H/W configuration.

### 4.6 Security Setup

Figure 4-16. Security and Anti-Virus Screen

Security Setup	
Supervisor Password is Disabled	
User Password is Disabled	
Set Supervisor Password [Press Enter]	
Set User Password Press Enter	
Password on boot: [Disabled]	
Diskette access: [Supervisor]	
Fixed disk boot sector: [Normal]	
Diskette access: [Supervisor] Fixed disk boot sector: [Normal]	

**Supervisor Password is** - shows whether the supervisor password is enabled or disabled (default).

**User Password is** - shows whether the user password is enabled or disabled (default).

**Sot Supervisor Password** ~ requires a password when entering Setup. the passwords are not case sensitive. Pressing the <Enter> key will display a message requiring for the supervisor password which can be up to seven al-phanumeric characters. This option also gives full access to the Setup menus.

**Sot User Password** - Pressing the <Enter> key will display a message requiring for the user password which can be up to seven alphanumeric characters. This option also gives restricted access to the Setup menus and requires the setting of the Supervisor Password first.

**Password on boot** - determines whether the password is required on boot. The option needs the setting of the Supervisor Password. If Supervisor Password is set and this option is disabled (default), BIOS assumes that the user is booting.

**Disketto access** - restricts the use of floppy drives only to the supervisor when set as Supervisor (default). Also, choosing Supervisor for this option will require the setting of the Supervisor Password. Setting it as User allows access to the floppy drives at any time.

## 4.7 Green PC Feature

Green PC F	eatures
Power Saving Mode:	Disabled]
System Doze Timer:	[20 sec]
System Standby Timer:	[5 min]
System Suspend Timer:	[10 min]
Hard Disk Standby Timer:	(Disabled)
UGA with Power Down feature:	[None]
Power Saving in Doze Node:	[Save 1/Z]
Power Saving in Standby Node:	[Save 2/3]
Advanced Power Managemen	t Setup
Systemt timer reload or stop	clock break select
Suspend Switch Select:	[Enabled]

Figure 4-17. Green PC Features Screen 1

Green	PC Features
APM SWI Function Support:	(Enabled)
VGA Access Detection:	[Disabled]
PN monitor IR01-IR015 Activity	A CONTRACTOR OF A CONTRACT OF
IRD3 (CONZ);	[On]
IRD4 (CON1):	[On]
IROS (Alt. printer);	[On]
IRO6 (Diskette):	[0n]
IRO7 (Printer);	[On]
IRO9 (IRO2 Redir):	[On]
IR010 (User defined):	[On]
IB011 (User defined):	[On]

Figure 4-18. Green PC Features Screen 2



Figure 4-19. Green PC Features Screen 3

Power Saving Mote - enables or disables (default) the power saving mode fewature of the chipset. Once enabled, the values of the following options can be set.

System Dozo Timer - sets the time interval after system inactivity when the system enters DOZE mode. The avaiable options are:

- 20 sec (default)
- . 40 sec

• 1 min 3 min

90 sec

Disabled

System Standby Timer - sets the time interval after system inactivity when the system events enters STANDBY mode. The options are:

20 sec

0

- 5 min (default)
- . 1 min 10 min a.
- 20 min .
- 15 min 30 min
- Disabled •

System Suspend Timer - sets the time interval after system inactivity when the system enters SUSPEND mode. The available options are:

- 20 sec
- 5 min
- 15 min
- 30 min

- 1 min 10 min (default)
- 20 min .
- Disabled

Hard Disk Standby Timor - sets the time interval after HDD inactivity when the HDD enter standby mode. The options are:

- Disabled (default)
- 1-15 min

**VGA with Power Down feature** - sets the method by which the VGA chip enters SLEEP mode. The options are:

- None (default)
  Standard
- VESA DPMS

**Power Saving in Doze Mode** - sets the CPU power Saving rate when system enters DOZE mode. The options are:

- Save 1/2 (default)
  Save 2/3
- Save 3/4

**Power Saving in Standby Mode** ~ sets the CPU Power Saving rate when system enters STANDBY mode. The options are:

- Save 1/2
  Save 2/3 (default)
- Save 3/4

**Suspend Switch Select** - enables or disables the function of Suspend Switch.

Enabled (default)
 Disabled

**APM SMI Function Support** - enables APM Function control from Operating System(OS) APM Function.

Enabled (default)
 Disabled

**VGA Access Detection** ~ The available options are:

Enabled
 Disabled (default)

**PM monitoriRQ1-IRQ15 Activity.** (Switch the following parameters to on or off)

- IRQ3 (COM2)
- IRQ5 (Alt. printer)
- IRQ7 (Printer)
- IRQ10 (User defined)
- IRQ14 (Fixed Disk)
- IRQ4 (COM1)
- IRQ6 (Diskette)
- IRQ9 (IRQ2 Redir)
- IRQ11 (User defined)
- IRQ15 (User defined)

### 4.8 Load ROM Default Values

If, during bootup, the BIOS program detects a problem in the integrity of the CMOS, it will display a message asking you to either press the  $\langle DEL \rangle$  key to run Setup or the  $\langle F1 \rangle$  key to resume booting. This probably means that the CMOS values have been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS.

Press the <F1> key to resume the boot or <DEL> to run Setup with the ROM default values already loaded in the menus. You can make other changes before saving the values to CMOS.



Figure 4-20. Load ROM Default Values Screen

## 4.9 Load Values from CMOS

If, during a Setup session, you change your mind about your selections and have not yet saved the values to CMOS, you can restore the values you previously saved to CMOS.

Select Load Values from CMOS on the Main Menu and the program will display the following screen.



Figure 4-21. Load Values from CMOS Screen

## 4.10 Save Values to CMOS

After making your selections on the Setup menus, always select Save Values to CMOS in order to make them operative. Unlike standard RAM memory, CMOS RAM is sustained by an on-board battery and stays on after you turn your system off.

After you save your selections, the program will display the following screen.



Figure 4-22. Save Values to CMOS Screen

If you attempt to exit without saving, the program will ask you if you would like to save the changes made before exiting.

During bootup, BIOS for the chipset attempts to load the values you saved in the CMOS RAM. If the values saved in the CMOS cause the system boot to fail, reboot and press the <DEL> key to enter Setup. In Setup, you may load the ROM default values (as described in the section 4.8) or try to change the values that caused the boot to fail.

## 4.11 Quitting Setup

After making all modifications in the Setup program, go to the option "Save Values to CMOS" then press the <Enter> key or simply press the <F10> key. The screen will then display a message asking you whether you would like to save and exit or not.

Use the arrow keys or press  $\langle Y \rangle$  for Yes then the  $\langle Enter \rangle$  key to save your settings before exiting. Press  $\langle N \rangle$  for No then the  $\langle Enter \rangle$  key to exit without saving.

If you made changes to the CMOS values and then press the <ESC> key, the program will prompt you whether you would like to Quit without saving or not.

Press <Y> for Yes then the <Enter> key to quit without saving, or press <N> then the <Enter> key to save your settings first before exiting Setup.



in the

40-012-819111 Version 1.1



## Addendum to **SI54P AlO** User's Manual (for Phoenix BIOS) V1.1->V1.2

There are a number of pages on version 1.1 of the SI54P AIO (for Phoenix BIOS) User's Manual that have to be modified. The relative changes are as follows.

1. Modifications on page 1:

BIOS: Award C BIOS: Phoenix

#### 2. Modifications on page 5:

The data SRAM column of table 2-2 (Second Level Cache Memory Configurations) on the top of the page 5 must be changed as below.



A: Please refer to the Appendix A.

#### 3. Modifications of page 6:

We added the Note 4 below to the bottom of page 6.

Note4: If your SI54P AIO PCB version is v1.3 or after v1.3, the JP8 is removed. As for, the voltage controller is determined by the "Flash Utility" but not JP8.

4. Add the Appendix A:

Appendix A What kind of Data SRAM should you use ?

SI54P AIO mainboard supports either pure 3.3V data SRAM or 3.3V/5V mixed mode data SRAM. Using the wrong type of SRAM could cause severe damage to the mainboard. (Tag and dirty SRAM uses the 5V standard SRAM.)

The following descriptions help you to identify the SRAM type that your SI54P AIO supports.

- 1) PCB rev. 1.0 supports the pure 3.3V SRAM only.
- 2) PCB rev. 1.3 supports pure 3.3V SRAM if there is a label on the center area of PCB shows "PURE 3.3V SRAM ONLY."
- 3) PCB rev. 1.3 supports 3.3V/5V mixed mode SRAM if there is a label on the center area shows "3.3V/5V MIXED MODE SRAM ONLY."

Pure 3.3V SRAM list for reference:

UMC:	61L256-15 (32Kx8), 61L512-15 (64Kx8)
Alliance:	AS7C3256-15 (32Kx8), AS7C3512-15 (64Kx8),
	AS7C31024-15 (128Kx8)
Samsung:	KH68V257P-17 (32Kx8)

3.3V/5V mixed mode SRAM list for reference:

Winbond:	W24M257AK-15 (32Kx8), W24M512AK-15 (64Kx8)	
UMC:	UM61M256-15 (32Kx8), UM61M512-15 (64Kx8)	