Intel® Entry Server Board SE7230NH1-E

Technical Product Specification

Revision 1.4

October 2006

Enterprise Platforms and Services Division

Revision History

Date	Revision Number	Modifications
April 2005	0.5	Preliminary Release; subject to change.
July 2005	0.9	Updated BIOS Setup, connector designators, and jumpers.
October	1.2	Update, BIOS Setup and Network adapter information.
March 2006	1.3	Update, NIC LED, BIOS, Fan Control
October 2006	1.4	Update, SATA Transfer Rate, Riser operation MHz

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1. Introduction

This *Intel® Entry Server Board SE7230NH1-E Technical Product Specification* (TPS) provides a high-level technical description for the Intel® Entry Server Board SE7230NH1-E. It details the architecture and feature set for all functional sub-systems that make up the server board.

1.1 Chapter Outline

This document is divided into the following chapters:

- Chapter 1 – Introduction
- Chapter 2 – Server Board Overview
- Chapter 3 – Functional Architecture
- Chapter 4 – System BIOS
- Chapter 5 – Platform Management Architecture
- Chapter 6 – Error Reporting and Handling
- Chapter 7 – Connectors and Jumper Blocks
- Chapter 8 – Absolute Maximum Ratings
- Chapter 9 – Design and Environmental Specifications
- Chapter 10 – Hardware Monitoring
- Appendix A – Integration and Usage Tips
- Glossary
- Reference Documents

1.2 Server Board Use Disclaimer

Intel Corporation server baseboards contain a number of high-density VLSI* and power delivery components that need adequate airflow to cool. Intel's own chassis are designed and tested to meet the intended thermal requirements of these components when the fully integrated system is used together. It is the responsibility of the system integrator that chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of airflow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of its published operating or non-operating limits.

2. Server Board Overview

The Intel® Entry Server Board SE7230NH1-E is a monolithic printed circuit board with features that is designed to support the entry server market.

2.1 Intel® Entry Server Board SE7230NH1-E Feature Set

The Intel® Entry Server Board SE7230NH1-E supports the following feature set:

- Processor and Front Side Bus (FSB) support
  - Supports Pentium® processor Extreme Edition, Pentium® D, Pentium® 4 and Celeron® D processors in the Intel® LGA775 package
  - Supports Intel® Dual Core Architecture
  - Supports Hyper-Threading Technology
  - Supports Intel® Extended Memory System 64 Technology (Intel® EM64T)
- Intel® E7230 Chipset components
  - Intel® E7230 MCH Memory Controller Hub
  - Intel® ICH7R I/O Controller
  - Intel® 6702 PXH-V-V PCI-X* Hub (LX SKU only)
  - 12-deep In-order Queue
- Memory System
- Four DIMM sockets supporting 400/533/667MHz DDR2 DIMMs
- Data bandwidth per channel of 4.2GB/s or 8.4GB/s in dual channel when using DDR2 667MHz
- Support for up to two DDR2 channels for a total of four DIMMs (2 DIMMs / Channel) providing up to 8GB max memory capacity.
- Support for 256MB, 512MB, 1GB and 2GB DRAM modules
- I/O Subsystem
- LX Board I/O Subsystem (Five independent PCI Buses):
  - Segment A: Two PCI 32-bit/33-MHz 3.3V Universal connectors supporting full length PCI add-in cards *(Adapters which support 5V only are not supported)* and one embedded Intel® 10/100/1000 82541PI Gigabit Ethernet Controller (Supports *PCI Specification, Rev 2.3*)
  - Segment B: One x1 PCI Express* resource implemented as an embedded Intel® 10/100/1000 82573E/V gigabit Ethernet Controller
  - Segment C: One x1 PCI Express* resource implemented as a single x4 PCI Express* connector supporting x1/x2/x4 PCI Express* add-in cards
  - Segment D: One x4 PCI Express* resource supporting PXH-V-V PCI-X Hub. PXH-V-V supports one dedicated PCI-X* 64/100MHz slot and PCI-X portion of Intel Adaptive Slot
  - Segment E: One x8 PCI Express* resource supporting PCI Express* portion of Intel Adaptive Slot. Supports x1/x2/x4/x8 PCI Express* add-in cards via riser card

- LC Board I/O Subsystem (Five independent PCI Buses):
  - Segment A: Two PCI 32-bit/33-MHz 3.3V Universal connectors supporting full length PCI add-in cards *(Adapters which support 5V only are not supported)* and one embedded Intel® 10/100/1000 82541PI Gigabit Ethernet Controller (Supports *PCI Specification, Rev 2.3*)
  - Segment B: One x1 PCI Express* resource implemented as an embedded Intel® 10/100/1000 82573E/V gigabit Ethernet Controller
  - Segment C: One x1 PCI Express* resource implemented as a single x4 PCI Express* connector supporting x1/x2/x4 PCI Express* add-in cards
  - Segment D: One x4 PCI Express* resource implemented as a single x8 PCI Express* connector supporting x1/x2/x4/x8 PCI Express* add-in cards
  - Segment E: One x8 PCI Express* resource implemented as a single x8 PCI Express* connector supporting x1/x2/x4/x8 PCI Express* add-in cards
- Serial ATA host controller
- Four independent SATA ports support data transfer rates up to 3.0 Gb/s (300MB/s) per port
- IDE controller
  - One IDE connector, supporting a maximum of two ATA-100* compatible devices
- Universal Serial Bus 2.0 (USB)
- Two external USB ports with an additional internal header providing two optional USB ports for front panel support.
  - Supports wake-up from sleeping states S1-S4 (S3 not supported)
  - Supports Legacy Keyboard/Mouse connections when using PS2-USB dongle
- LPC (Low Pin Count) bus segment with one embedded device
  - Super I/O controller chips providing all PC-compatible I/O (floppy, serial, keyboard, mouse, two serial com port) and integrated hardware monitoring
  - LC Super I/O = SMsC* LP47M182NR
  - LX Super I/O = National Semiconductor* PC8374LOIBU
- SSI-compliant connectors for SSI interface support
- Standard Intel 34pin SSI front panel and 2x12 and 2x4 power connectors
- Fan Support
- Fans:
  - Two general purpose 3-pin fans
  - Two general purpose 4-pin fans
  - One 4-pin processor fan (active heatsink required)
  - Four 8-pin dual rotor fans for Intel High Density applications (Intel® Server Chassis SC1475 and Intel® Server Platform SR1474NH1-E).
- Diagnostic LEDs to display POST code indicators during boot

The following figure shows the board layout of the Intel® Entry Server Board SE7230NH1-E (LX version). Each connector and major component is identified by letter and is identified in Table 2.

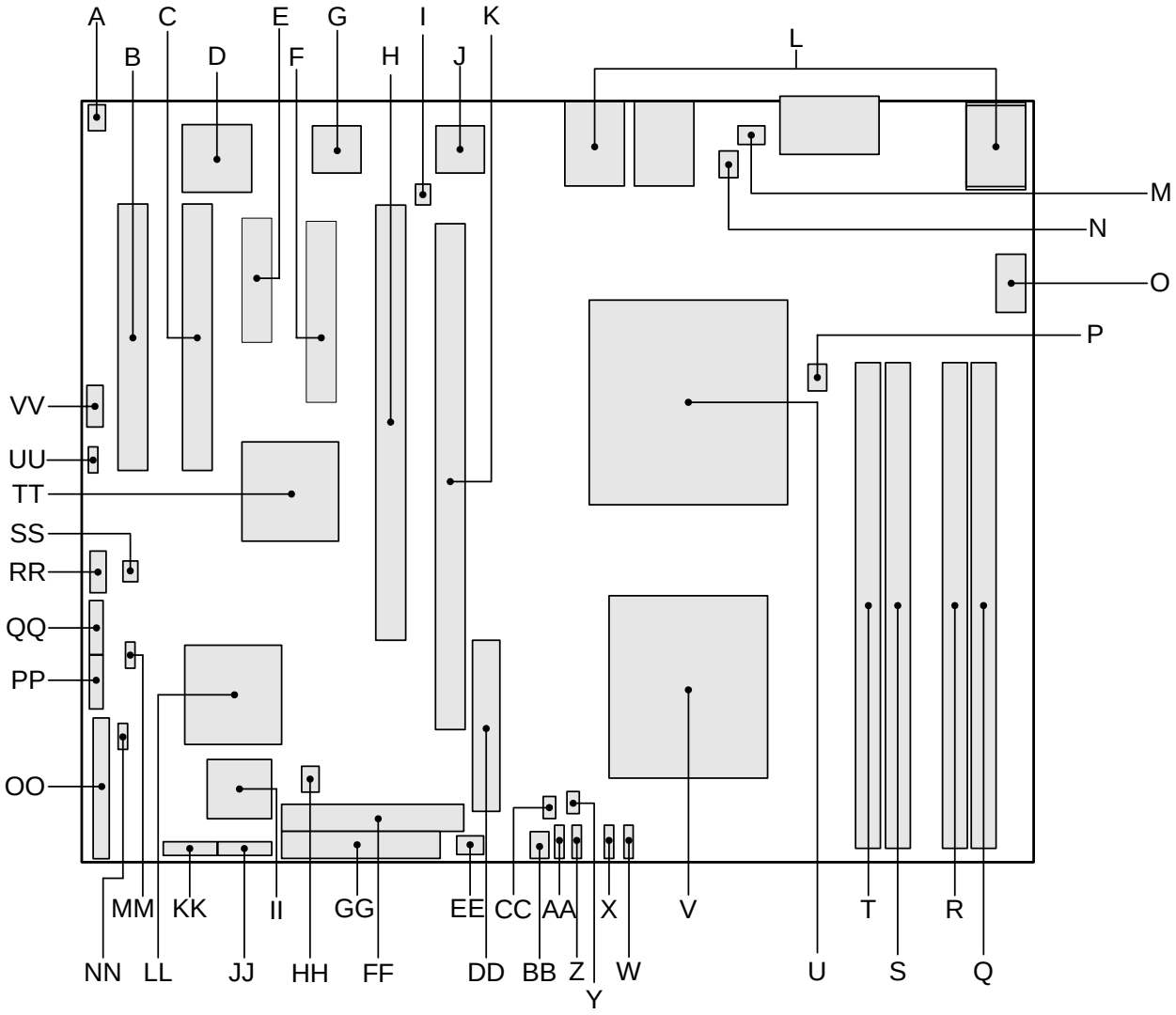


Figure 1. Intel® Entry Server Board SE7230NH1-E (LX Version) Layout

Table 1. Server Board Layout Reference

Ref	Description	Ref	Description	Ref	Description
A	Chassis Intrusion Header	Q	Memory Slot DIMM 2B	GG	Floppy Connector
B	PCI (32bit/33MHz) Slot 1	R	Memory Slot DIMM 1B	HH	SCSI LED Connector (moved)
C	PCI (32bit/33MHz) Slot 2	S	Memory Slot DIMM 2A	II	National* PC8374L0IBU SIO
D	ATI ES1000 Video Controller	T	Memory Slot DIMM 1A	JJ	SATA Port 3
E	PCI Express* x4 (x1 Lane) Slot 3	U	775 Land (LGA) CPU Socket	KK	SATA Port 2
F	PCI Express* x8 (x4 Lane) Slot 4	V	Intel® 7230 MCH	LL	Intel® 82802 ICH7R
G	Intel® 82541PI LAN Controller	W	SysFan8	MM	Clear CMOS Jumper
H	PCI-X* (64bit/133MHz) Slot 5	X	SysFan7	NN	Maintenance Mode Jumper
I	LAN SPI Flash	Y	Hardware Management Controller	OO	Front Panel Connector
J	Intel® 82573E/V LAN Controller	Z	SysFan6	PP	SATA Port 1
K	Intel® Adaptive Slot, Slot 6	AA	SysFan5	QQ	SATA Port 0
L	Back Panel Connectors	BB	SysFan4	RR	External USB Connector
M	SysFan1	CC	Hardware Management Controller	SS	BIOS SPI Flash
N	SysFan2	DD	2 x 12 Power Connector	TT	Intel® 6702 PXH-V-V Controller
O	2 x 4 Power Connector	EE	SysFan3	UU	I^2C Connector
P	CPU Fan	FF	PATA IDE Connector	VV	RMC Connector
				WW	NIC1 FW Enable

The following figure shows the board layout of the Intel® Entry Server Board SE7230NH1-E (LC SKU version). Each connector and major component is identified by letter and is identified in Table 2.

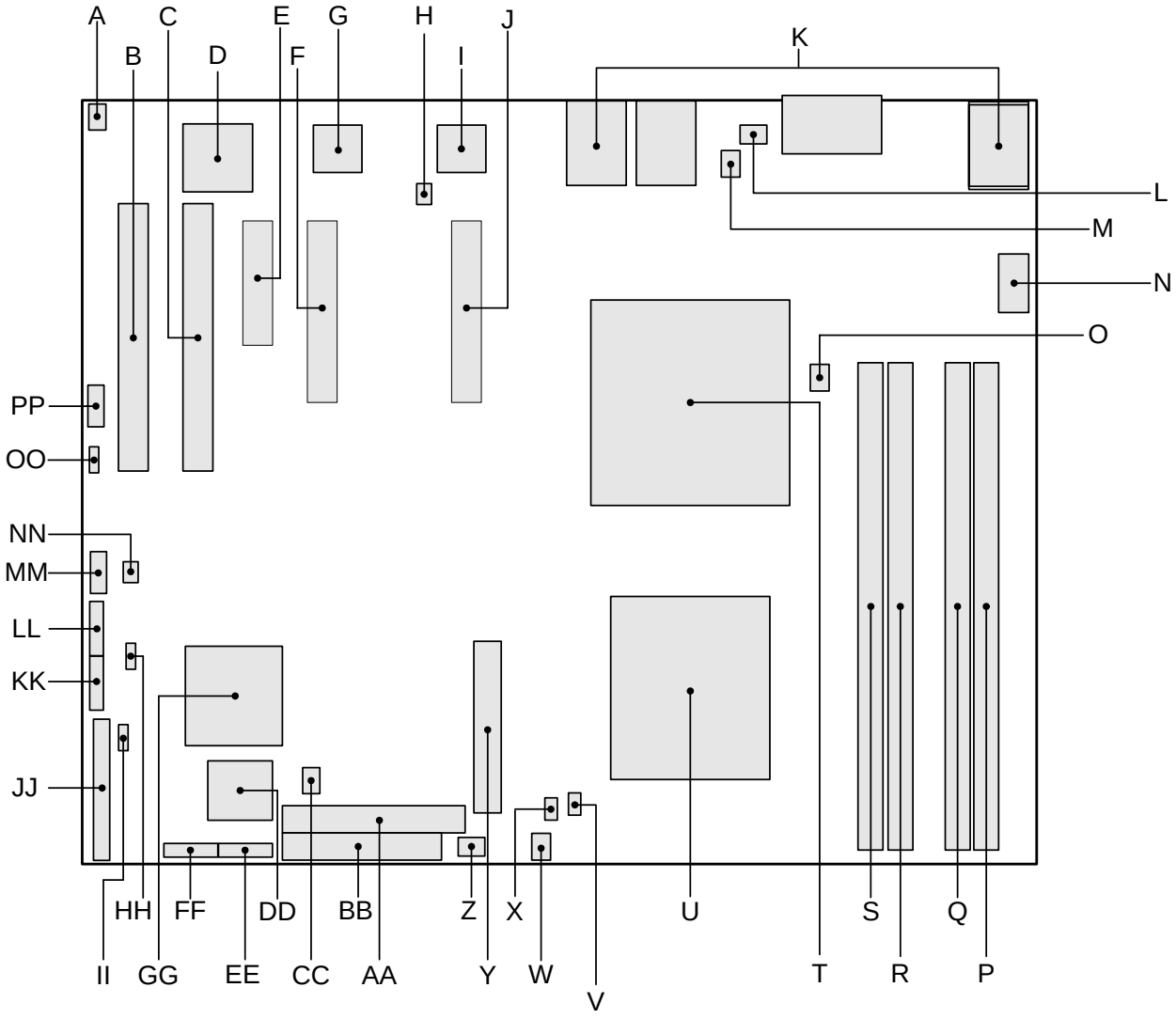


Figure 2. Intel® Entry Server Board SE7230NH1-E (LC SKU) Diagram

Table 2. Server Board Layout Reference

Ref	Description	Ref	Description	Ref	Description
A	Chassis Intrusion Header	O	CPU Fan	CC	SCSI LED Connector (moved)
B	PCI (32bit/33MHz) Slot 1	P	Memory Slot DIMM 2B	DD	SMsC LPC47M182NR SIO
C	PCI (32bit/33MHz) Slot 2	Q	Memory Slot DIMM 1B	EE	SATA Port 3
D	ATI ES1000 Video Controller	R	Memory Slot DIMM 2A	FF	SATA Port 2
E	PCI Express* x4 (x1 Lane) Slot 3	S	Memory Slot DIMM 1A	GG	Intel® 82802 ICH7R
F	PCI Express* x8 (x4 Lane) Slot 4	T	775 Land (LGA) CPU Socket	HH	Clear CMOS Jumper
G	Intel® 82541PI LAN Controller	U	Intel® 7230 MCH	II	Maintenance Mode Jumper
H	LAN SPI Flash	V	Hardware Management Controller	JJ	Front Panel Connector
I	Intel® 82573E/V LAN Controller	W	SysFan4	KK	SATA Port 1
J	PCI Express* x8 (x8 Lane) Slot 6	X	Hardware Management Controller	LL	SATA Port 0
K	Back Panel Connectors	Y	2 x 12 Power Connector	MM	External USB Connector
L	SysFan1	Z	SysFan3	NN	BIOS SPI Flash
M	SysFan2	AA	PATA IDE Connector	OO	I^2C Connector
N	2 x 4 Power Connector	BB	Floppy Connector	PP	RMC Connector

3. Functional Architecture

This chapter provides a high-level description of the functionality associated with the architectural blocks that make up the Intel® Entry Server Board SE7230NH1-E.

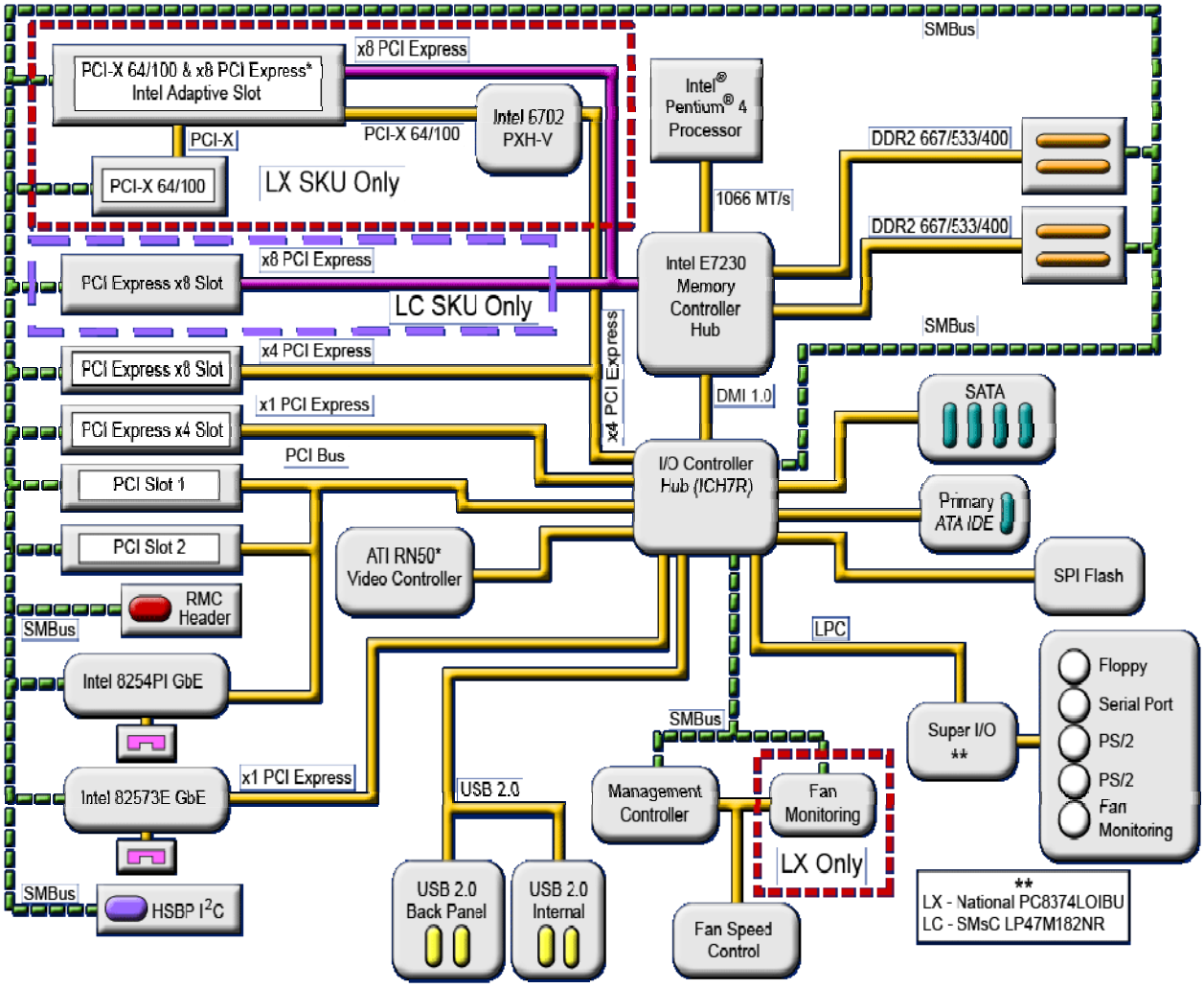


Figure 3. Intel® Entry Server Board SE7230NH1-E Block Diagram

3.1 Processor Sub-System

The Intel® Entry Server Board SE7230NH1-E supports the following:

- Pentium® processor Extreme Edition in the 775-land package
- Pentium® D processors in the 775-land package
- Pentium® 4 processors in the 775-land package
- Celeron® D processors in the 775-land package

The 775-land package is a follow on to Pentium® 4 and Celeron® processors in the 478-pin package with enhancements to the Intel® NetBurst® micro-architecture including but not limited to the following:

- Dual Core Architecture
- Hyper-Threading Technology
- Intel® EM64T
- Pentium® processor Extreme Edition
- Pentium® D
- Pentium® 4
- Celeron® D

The processors built on 90nm and 65nm process technology in the 775-land package utilize Flip-Chip Land Grid Array (FC-LGA4) package technology, and plug into a 775-land LGA socket, referred to as the Intel® LGA775 socket. The processors are as follows:

- Pentium® processor Extreme Edition
- Pentium® D Processor
- Pentium® 4 Processor
- Celeron® D Processor

The above processors in the 775-land package, like their predecessors in the 478-pin package, is based on the same Pentium® 4 micro-architecture. They maintain compatibility with 32-bit software written for the IA-32 instruction set, while supporting 64-bit native mode operation when coupled with supported 64-bit operating systems and applications.

The Celeron® Processor currently does not come in a dual core configuration, support Hyper-Threading Technology or Intel® EM64T.

3.1.1 Processor Voltage Regulator Down (VRD)

The Intel® Entry Server Board SE7230NH1-E has a VRD (Voltage Regulator Down) to support one processor. It is compliant with the *VRM 10.1 DC-DC Converter Design Guide Line* and provides a maximum of 120A, which is capable of supporting the requirements for the following processors:

- Pentium® processor Extreme Edition
- Pentium® D Processor
- Pentium® 4 Processor
- Celeron® D Processor

The board hardware monitors the processor VTTEN (Output enable for VTT) pin before turning on the VRD. If the VTTEN pin of the processors is not identical, the Power ON Logic will not turn on the VRD.

3.1.2 Reset Configuration Logic

The BIOS determines the processor stepping, cache size, et cetera through the CPUID instruction. The requirements are as follows:

- Processors run at a fixed speed, but can be programmed by BIOS to operate at a lower or higher speed.

The processor information is read at every system power-on.

Note: The processor speed is the processor power-on reset default value. No manual processor speed setting options exist either in the form of a BIOS setup option or jumpers.

3.1.3 Processor Support

The Intel® Entry Server Board SE7230NH1-E supports one processor in the Intel® LGA775 package. The support circuitry on the server board consists of the following:

- Intel® LGA775 processor socket supporting:
  - 800MHz Pentium® D Processor
  - Pentium® 4 Processor
  - 1066MHz FSB Pentium® processor Extreme Edition
  - Pentium® processor Extreme Edition
- Processor host bus AGTL+ support circuitry.

Table 3. Processor Support Matrix

Processor Family	Package Type	Frequency	Cache Size	Front Side Bus
Pentium® 4 processor Extreme Edition	Intel® LGA775	3.2GHz	2 x 1MB L2	800MHz
Pentium® 4 processor Extreme Edition	Intel® LGA775	3.73GHz	2MB L2	1066MHz
Pentium® D	Intel® LGA775	3.2 – 4.0GHz	2 x 1MB L2	800MHz
Pentium® 4	Intel® LGA775	3.2 – 4.0GHz	1MB or 2MB L2	800MHz
Celeron® D	Intel® LGA775	2.26 – 3.2 GHz	256K L2	533MHz

Note: For a complete list of all supported processors, please visit the Intel® Entry Server Board SE7230NH1-E support site located at the following URL:
http://support.intel.com/support/motherboards/server/sb/CS-012690.htm

In addition to the circuitry described above, the processor subsystem contains the following:

- Reset configuration logic
- Server management registers and sensors

3.2 Intel® E7230 Chipset

The Intel® Entry Server Board SE7230NH1-E is designed around the Intel® E7230 Chipset. The chipset provides an integrated I/O bridge and memory controller, and a flexible I/O subsystem core (PCI Express*). The chipset consists of three primary components:

3.2.1 Memory Controller Hub (MCH)

3.2.1.1 Intel® E7230 Chipset MCH: Memory Control Hub

The MCH accepts access requests from the host (processor) bus and directs those accesses to memory or to one of the PCI buses. The MCH monitors the host bus, examining addresses for each request. Accesses may be directed to the following:

- A memory request queue for subsequent forwarding to the memory subsystem
- An outbound request queue for subsequent forwarding to one of the PCI buses

The MCH also accepts inbound requests from the Intel® ICH7R. The MCH is responsible for generating the appropriate controls to control data transfer to and from memory.

The MCH is a 1210-ball FC-BGA device and uses the proven components of the following previous generations:

- Pentium® processor Extreme Edition
- Pentium® D Processor
- Pentium® 4 Processor bus interface unit
- Hub interface unit
- DDR2 memory interface unit

In addition, the MCH incorporates an integrated high performance graphics media accelerator and a PCI Express* interface. The PCI Express* interface allows the MCH to directly interface with the PCI Express* devices (like PXH-V/PXH-VD). The MCH also increases the main memory interface bandwidth and maximum memory configuration with a 72-bit wide memory interface.

The MCH integrates the following main functions:

- An integrated high performance main memory subsystem
- A PCI Express* bus which provides an interface to the PCI-Express devices(Fully compliant to the *PCI Express* Base Specification, Rev 1.0a*)
- A DMI which provides an interface to the Intel® ICH7R

Other features provided by the MCH include the following:

- Full support of ECC on the processor bus
- Full support of Intel® x4 Single Device Data Correction on the memory interface with x4 DIMMs
- Twelve deep in-order queue, two deep defer queue
- Full support of un-buffered DDR2 ECC DIMMs
- Support for 256MB, 512MB, 1 GB and 2 GB DDR2 memory modules
- Memory scrubbing

3.2.1.2 MCH Memory Sub-System Overview

The MCH supports a 72-bit wide memory sub-system that can support a maximum of 8 GB of DDR2 memory using two GB DIMMs. This configuration needs external registers for buffering the memory address and control signals. The four chip selects are registered inside the MCH and need no external registers for chip selects.

The memory interface runs at 400/533/667MT/s. The memory interface supports a 72-bit wide memory array. It uses seventeen address lines (BA [2:0] and MA [13:0]) and supports 256 MB, 512 MB, 1 GB, and 2GB DRAM densities. The DDR DIMM interface supports memory scrubbing, single-bit error correction, and multiple bit error detection and Intel® x4 Single Device Data Correction with x4 DIMMs.

3.2.1.2.1 DDR2 Configurations

The DDR2 interface supports up to 8 GB of main memory and supports single- and double-density DIMMs. The DDR2 can be any industry-standard DDR2. The following table shows the DDR2 DIMM technology supported.

Table 4. Supported DDR2 Modules

DDR2-400/533/667 Un-buffered SDRAM Module Matrix					
DIMM Capacity	**DIMM Organization**	**SDRAM Density**	**SDRAM Organization**	**# SDRAM Devices/rows/Banks**	**# Address bits rows/Banks/column**
256MB	32M x 72	256Mbit	32M x 8	9 /1 / 4	13 / 2 / 10
512MB	64M x 72	256Mbit	32M x 8	18 / 2 / 4	13 / 2 / 10
512MB	64M x 72	512Mbit	64M x 8	9 / 1 / 4	14 / 2 / 10
1GB	128M x 72	512Mbit	64M x 8	18 / 2 / 4	14 / 2 / 10
1GB	128M x 72	1Gbit	128M x 8	9 / 1 / 8	14 / 4 / 10
2GB	256M x 72	2GB	128M x 8	18 / 2 / 8	14 / 8 / 10

3.2.1.3 PCI Express*

3.2.1.3.1 x4 PCI Express Subsystem*

The Intel® ICH7R supports one x4-lane PCI Express* interface that can also be configured as a single x1 or x4-lane port. The PCI Express* interface allows direct connection with the PXH-V-V or dedicated PCI-E devices. (Fully compliant to the *PCI Express* Base Specification, Rev 1.0a*).

3.2.1.3.2 x1 PCI Express Subsystem*

The Intel® ICH7R supports 2 x1 PCI Express* buses. One supports a dedicated x4 PCI Express* slot. The other supports the Intel® 82573-gigabit Ethernet controller.

One 32-bit PCI bus segment is directed through the Intel® ICH7R Interface A. This PCI Segment B only has an embedded device, Intel® 82573E/V LAN (NIC2) clocked at 1.5GHz.

3.2.1.3.2.1 Device IDs (IDSEL)

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of AD [31:16], which acts as a chip select on the PCI bus segment in configuration cycles. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached for P32-B devices and corresponding device description:

Table 5. Segment B Configuration IDs

IDSEL Value	Device
19	Intel® 82573E/V LAN (NIC2)

3.2.1.3.2.2 Segment B Arbitration

PCI Segment B supports one PCI masters. All PCI masters must arbitrate for PCI access using resources supplied by the Intel® ICH7R. The host bridge PCI interface arbitration lines REQx* and GNTx* are internal to the Intel® ICH7R. The following table defines the arbitration connections:

Table 6. Segment B Arbitration Connections

Baseboard Signals	Device
PCIX REQ_N0/GNT_N0	Intel® 82541PI LAN (NIC2)

3.2.1.3.2.3 Segment D 64bit/133MHz PCI-X Subsystem

One 64-bit PCI-X* bus segment is directed through the PXH-V. This PCI-X* segment, Segment D interface A, provides the following:

- Two 3.3V 64-bit PCI-X* slots or
- One 3.3V 64-bit PCI-X* riser slot, (Intel® Entry Server Board SE7230NH1LX SKU only)

The PCI-X* slot is capable of speeds up to 133MHz operation and supports full-length PCI and PCI-X adapters. If installed, the riser forces the slot to operate at 100MHz.

3.2.1.3.2.3.1 Device IDs (IDSEL)

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of AD [31:16], which acts as a chip select on the PCI bus segment in configuration cycles. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached for P64-C devices and corresponding device description:

Table 7. Segment D Configuration IDs

IDSEL Value	Device
17	PCI Slot 5 (64bit/66-133MHz) (Intel® Entry Server Board SE7230NH1LX SKU only)
18	PCI Slot 6 (64bit/133MHz) (Riser, Intel® Entry Server Board SE7230NH1LX SKU only)

3.2.1.3.2.3.2 Segment D Arbitration

P64-C supports two PCI masters: two PCI-X slots or one riser slot. All PCI masters must arbitrate for PCI access using resources supplied by the ICH7. The host bridge PCI interface (ICH7) arbitration lines REQx* and GNTx* are a special case in that they are internal to the host bridge. The following table defines the arbitration connections.

Table 8. Segment D Arbitration Connections

Baseboard Signals	Device
PCIX REQ_N0/GNT_N0	PCI Slot 5 (64bit/133MHz) (Intel® Entry Server Board SE7230NH1LX SKU only)
PCIX REQ_N1/GNT_N1	PCI Slot 6 (64bit/133MHz) (Riser, Intel® Entry Server Board SE7230NH1LX SKU only)

3.2.1.3.2.3.3 Segment E PCI-E x8

In this board, Lanes 0~7 are connected to an x8 PCI-E connector directly through the MCH. It can support x1, x4, x 8 PCI-E add-in cards or through the I/O riser through the Intel® Adaptive Slot (LX SKU only)

Table 9. Segment E Connections

Lane	Device
Lane 0~7	Slot 6 or Intel® Adaptive Slot (PCI Express* x8)

3.2.2 PCI-X Hub (PXH)

PXH-V-V: PCI-X Hub (LX SKU Only) The PXH-V hub is a peripheral chip that performs PCI bridging functions between the PCI Express* interface and the PCI bus. The PXH-V contains two PCI bus interfaces that can be independently configured to operate in PCI (33 or 66 MHz), PCI-X Mode1 (66,100,133), for either 32 or 64 bits.

3.2.3 I/O Controller Hub

3.2.3.1 Intel® ICH7R: I/O Controller Hub 7R

The Intel® ICH7R controller has several components. It provides the interface for a 32-bit/33-MHz PCI bus. The Intel® ICH7R can be both a master and a target on that PCI bus. The Intel® ICH7R also includes a USB 2.0 controller and an IDE controller. The Intel® ICH7R is also responsible for much of the power management functions, with ACPI control registers built in. The Intel® ICH7R also provides a number of GPIO pins and has the LPC bus to support low speed Legacy I/O.

The MCH and Intel® ICH7R chips provide the pathway between the processor and the I/O systems. The MCH is responsible for accepting access requests from the host (processor) bus, and directing all I/O accesses to one of the PCI buses or Legacy I/O locations. If the cycle is directed to one of the PCI-E segments, the MCH communicates with the PCI-E Devices (add-in

card, on board devices) through the PCI-E interface. If the cycle is directed to the Intel® ICH7R, the cycle is output on the MCH's DMI bus. All I/O for the board, including PCI and PC-compatible I/O, is directed through the MCH and then through the Intel® ICH7R provided PCI buses.

The Intel® ICH7R is a multi-function device, housed in a 609-pin mBGA device. It provides the following:

- A DMI bus
- A PCI 32-bit/33 MHz interface
- An IDE interface
- An integrated Serial ATA Host controller
- A USB controller
- A PCI-E x4 interface
- A power management controller

Each function within the Intel® ICH7R has its own set of configuration registers. Once configured, each appears to the system as a distinct hardware controller sharing the same PCI bus interface.

The primary role of the ICH7R is providing the gateway to all PC-compatible I/O devices and features. The board uses the following the Intel® ICH7R features:

- PCI 32-bit/33MHz interface for PCI slots 1 and 2 and Intel® 82541PI Gigabit Ethernet Controller
- PCI 32-bit/33MHz interface to dedicated ATI ES1000* video subsystem
- LPC bus interface
- x4 PCI Express* interface for PXH-V-V device (supplies PCI-X on LX SKU only)
- x1 PCI Express* resource for dedicated x4 PCI Express* slot
- x1 PCI Express* interface for Intel® 82573E/V gigabit Ethernet Controller
- DMI (Direct Media Interface)
- IDE interface, with Ultra ATA 100/66/33 capability
- Integrated quad-port Serial ATA Host controller
- Universal Serial Bus (USB) 2.0 interface
- PC-compatible timer/counter and DMA controllers
- APIC and 82C59 interrupt controller
- Power management
- System RTC
- Supports Smbus 2.0 Specification
- General purpose I/O (GPIO)

The following are the descriptions of how each supported feature is used for Intel® ICH7R on the board.

3.2.3.2 IDE Interface (Bus Master Capability and Synchronous DMA Mode)

The Intel® ICH7R acts as a PCI-based Ultra ATA 100/66/33 IDE controller that supports programmed I/O transfers and bus master IDE transfers. The Intel® ICH7R supports one IDE channel, supporting two drives each (drives 0 and 1). The baseboard provides a 40-pin (2x20) IDE connector to access the IDE functionality.

The IDE interface supports Ultra ATA 100/66/33 Synchronous DMA Mode transfers on the 40-pin connector.

3.2.3.3 SATA Controller

The Intel® ICH7R contains four SATA ports. The data transfer rates up to 300Mbyte/s per port.

3.2.3.4 Compatibility Modules (DMA Controller, Timer/Counters, Interrupt Controller)

The Intel® ICH7R provides the functionality of two-cascaded 82C59 with 15 interrupts handling. Support processor system bus interrupt.

3.2.3.5 Advanced Programmable Interrupt Controller (APIC)

Interrupt generation and notification to the processor is done by the APICs in the Intel® ICH7R using messages on the front side bus.

3.2.3.6 Universal Serial Bus (USB) Controller

The Intel® ICH7R contains one EHCI USB 2.0 controller and four USB ports. The USB controller moves data between main memory and up to four USB connectors. All ports function identically and with the same bandwidth. The Intel® Server Board SE7230NH1-E implements four ports on the board.

The baseboard provides two external USB ports on the back of the server board. The dual-stack USB connector is located within the standard ATX I/O panel area. The *Universal Serial Bus Specification, Revision 1.1,* defines the external connectors.

The third/fourth USB port is optional and can be accessed by cabling from an internal 9-pin connector located on the base board to an external USB port located either in front or the rear of a given chassis.

3.2.3.7 Enhanced Power Management

One of the embedded functions of the Intel® ICH7R is a power management controller. This is used to implement ACPI-compliant power management features. The baseboard does support sleep states S1, S4, and S5.

3.3 Memory Sub-System

The baseboard supports up to four DIMM slots for a maximum memory capacity of 8 GB. The DIMM organization is x72, which includes eight ECC check bits. The memory interface runs at 400/533/667MTs. The memory controller supports the following:

- Memory scrubbing
- Single-bit error correction
- Multiple-bit error detection
- Intel® x4 Single Device Data Correction support with x4 DIMMs

Memory can be implemented with either single sided (one row) or double-sided (two row) DIMMs

3.3.1 Memory Configuration

The memory interface between the MCH and the DIMMs is 64-bit (non-ECC) or 72-bit (ECC) wide interface.

There are two banks of DIMMs, labeled 1 and 2. Bank 1 contains DIMM socket locations DIMM_1A and DIMM_2A. Bank 2 contains DIMM socket locations DIMM_1B and DIMM_2B. The sockets associated with each bank or "channel," are located next to each other and the DIMM socket identifiers are marked on the base board silkscreen, near the DIMM socket. Bank 1 is associated with Memory Channel A while Bank 2 is associated with Memory Channel B. When only two DIMM modules are being used, the population order must be DIMM_1A, DIMM_1B to ensure dual channel operating mode.

In order to operate in dual channel dynamic paging mode, the following conditions must be met:

- Two identical DIMMs are installed, one each in DIMM_1A and DIMM_1B
- Four identical DIMMs are installed (one in each socket location)

Note: Installing only three DIMMs is not supported. Do not use DIMMs that are not "matched" (same type and speed). Use of identical memory parts is always the preferred method.

See Figure 4 on the following page for reference.

The system design is free to populate or not to populate any rank on either channel, including either degenerate single channel case.

DIMM and memory configurations must adhere to the following:

- DDR2 400/533/667 , un-buffered, DDR2 DIMM modules
- DIMM organization: x72 ECC or x 64 Non-ECC
- Pin count: 240
- DIMM capacity: 256 MB, 512 MB, 1 GB and 2 GB DIMMs
- Serial PD: JEDEC Rev 2.0
- Voltage options: 1.8 V
- Interface: SSTL2

Table 10. Memory Bank Labels and DIMM Population Order

Location	DIMM Label	Channel	Population Order
J2J1	(DIMM_1A)	A	1
J2J2	(DIMM_2A)	A	3
J1J1	(DIMM_1B)	B	2
J1J2	(DIMM_2B)	B	4

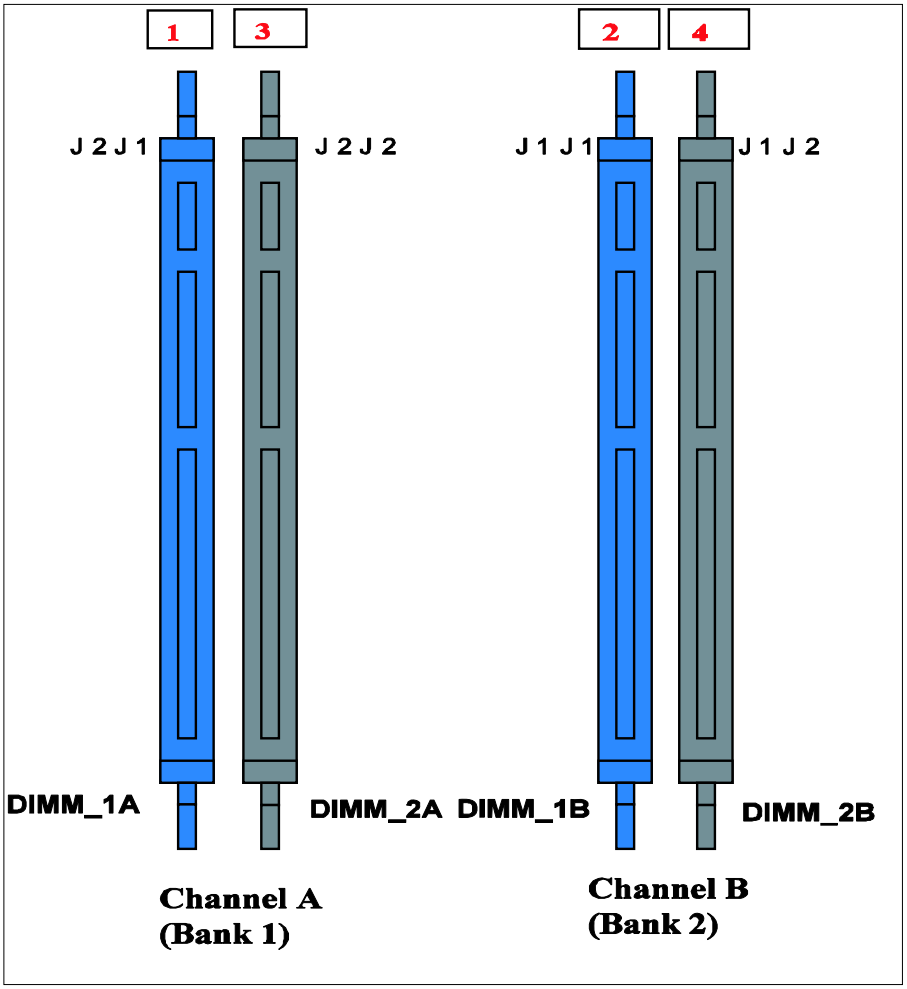
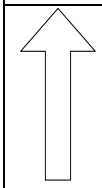


Figure 4. Memory Bank Label Definition

Table 11. Characteristics of Dual/Single Channel Configuration with or without Dynamic Mode

Throughput Level	Configuration	Characteristics
Highest	Dual channel with dynamic paging mode	All DIMMs matched
	Dual channel without dynamic paging mode	DIMMs matched from Channel A to Channel B DIMMs not matched within channels
	Single channel with dynamic paging mode	Single DIMM or DIMMs matched with a channel
Lowest	Single channel without dynamic paging mode	DIMMs not matched

3.3.2 Memory DIMM Support

The board supports un-buffered (not registered) DDR2 400/533/667 ECC or Non-ECC DIMMs operating at 400/533/667MT/s. Only DIMMs tested and qualified by Intel or a designated memory test vendor are supported on this board. A list of qualified DIMMs is available at http://support.intel.com/support/motherboards/server/SE7230NH1E. Note that all DIMMs are supported by design, but only fully qualified DIMMs will be supported on the board.

The minimum supported DIMM size is 256 MB. Therefore, the minimum main memory configuration is 1 x 256 MB or 256 MB. The largest size DIMM supported is 2 GB and as such, the maximum main memory configuration is 8 GB implemented by 4 x 2 GB DIMMs.

- Only un-buffered DDR2 400/533/667 compliant, ECC x8 and Non-ECC x8 or x16 memory DIMMs are supported.
- ECC single-bit errors (SBE) will be corrected while multiple-bit error (MBE) will only be detected.
- Intel® Entry Server Board SE7230NH1-E also supports Intel® x4 Single Device Data Correction with x4 DIMMs.
- The maximum memory capacity is 8 GB via four 2 GB DIMM modules.
- The minimum memory capacity is 256 MB via a single 256 MB DIMM module.

3.4 I/O Sub-System

3.4.1 PCI Subsystem

The primary I/O buses for the Intel® Entry Server Board SE7230NH1-E are five independent PCI bus segments providing PCI, PCI-E and PCI-X* resources (LX SKU only). The PCI buses comply with the *PCI Local Bus Specification, Rev 2.3*.

PCI Segments A, B and C are directed through the Intel® ICH7R. PCI Segment D is independently configured to PXH-V that is through Intel® ICH7R by PCI Express* x4 interface. PCI Segment E is directed through the MCH by PCI-E x8 interface. The table below lists the characteristics of the three PCI bus segments.

Table 12. PCI Bus Segment Characteristics

PCI Bus Segment	Voltage	Width	Speed	Type	PCI I/O Card Slots
A	3.3V	32 bits	33MHz	PCI 32	Slot 1, Slot 2, NIC 1
B	3.3V	1 lane	1.5GHz	x1 PCI-E	NIC 2
C	3.3V	1 lane	1.5GHz	x1 PCI-E	Slot 3
D	3.3V	4 lanes	1.5GHz	x4 PCI-E	Slot 4
D	3.3V	64 bits	66/100/133MHz	PCI-64	Slot 5; (Slot 6 through riser card)
E	3.3V	8 lanes	1.5GHz	x8 PCI-E	Slot 6

3.4.1.1 P32-A: 32-bit, 33-MHz PCI Subsystem

The Intel® ICH7R provides a Legacy 32-bit PCI subsystem and acts as the central resource on this PCI interface. P32-A supports the following embedded devices and connectors:

- One Intel® 82541PI Network Controller
- Two slots capable of supporting full length PCI add-in cards operating at 33 MHz

All 32-bit/33-MHz PCI I/O for the board is directed through the Intel® ICH7R. The 32-bit/33-MHz PCI segment created by the Intel® ICH7R is known as PCI Segment A. Segment A supports the following embedded devices and connectors:

- One 10/100/1000-T Network Interface Controller: Intel® 82541PI Fast Ethernet Controller.

3.4.1.1.1 Device IDs (IDSEL)

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of AD (31:16), which acts as a chip select on the PCI bus segment in configuration cycles. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached for Segment A devices and the corresponding device description.

Table 13. Segment A Configuration IDs

IDSEL Value	Device
19	Intel® 82541PI LAN (NIC2)
18	PCI Slot 1 and 2 (32b/33MHz)

3.4.1.1.2 Segment A Arbitration

PCI Segment A supports two PCI devices: the Intel® ICH7R and one PCI bus masters (NIC). All PCI masters must arbitrate for PCI access, using resources supplied by the Intel® ICH7R. The host bridge PCI interface (ICH7R) arbitration lines REQx* and GNTx* are a special case in that they are internal to the host bridge. The following table defines the arbitration connections.

Table 14. Segment A Arbitration Connections

Baseboard Signals	Device
PCI REQ1_N/GNT_N1	Intel® 82541PI LAN (NIC1)
PCI REQ0_N/GNT_N0	PCI Slot 1 and 2 (32bit/33MHz)

3.4.1.2 PCI Interface for ATI Video subsystem

The server board graphics subsystem is connected to the Intel® ICH7R via a 32/33MHz PCI bus.

3.4.2 Interrupt Routing

The board interrupt architecture accommodates both PC-compatible PIC mode and APIC mode interrupts through use of the integrated I/O APICs in the ICH7.

3.4.2.1 Legacy Interrupt Routing

For PC-compatible mode, the ICH7 provides two 82C59-compatible interrupt controllers. The two controllers are cascaded with interrupt levels 8-15 entering on level 2 of the primary interrupt controller (standard PC configuration). A single interrupt signal is presented to the processors, to which only one processor will respond for servicing. The Intel® ICH7R contains configuration registers that define which interrupt source logically maps to I/O APIC INTx pins.

The ICH7 handles both PCI and IRQ interrupts. The Intel® ICH7R translates these to the APIC bus. The numbers in the table below indicate the Intel® ICH7R PCI interrupt input pin to which the associated device interrupt (INTA, INTB, INTC, INTD, INTE, INTF, INTG, INTH for PCI bus and PXIRQ0, PXIRQ1, PXIRQ2, PXIRQ3 for PCI-X bus) is connected. The Intel® ICH7R I/O APIC exists on the I/O APIC bus with the processors.

Table 15. PCI AND PCI-X Interrupt Routing/Sharing

Interrupt	INT A	INT B	INT C	INT D
Intel® 82573E/V	PIRQC			
PCI Slot 1 and 2 (PCI 32bit/33MHz)	PIRQF	PIRQG	PIRQE	PIRQH
PCI Slot 5 (64bit/133MHz) (LX SKU only)	PXIRQ0	PXIRQ1	PXIRQ2	PXIRQ3
PCI Slot 6 (64bit/133MHz) (Riser LX SKU only)	PXIRQ5	PXIRQ6	PXIRQ7	PXIRQ4

3.4.2.2 APIC Interrupt Routing

For APIC mode, the baseboard interrupt architecture incorporates three Intel® I/O APIC devices to manage and broadcast interrupts to local APICs in each processor. The Intel® I/O APICs monitor each interrupt on each PCI device; including PCI slots in addition to the ISA compatibility interrupts IRQ (0-15).

When an interrupt occurs, a message corresponding to the interrupt is sent across a three-wire serial interface to the local APICs. The APIC bus minimizes interrupt latency time for compatibility interrupt sources. The I/O APICs can also supply greater than 16 interrupt levels to the processor(s). This APIC bus consists of an APIC clock and two bidirectional data lines.

3.4.2.3 Legacy Interrupt Sources

The table below recommends the logical interrupt mapping of interrupt sources on the board. The actual interrupt map is defined using configuration registers in the ICH7.

Table 16. Interrupt Definitions

ISA Interrupt	Description
INTR	Processor interrupt.
NMI	NMI to processor.
IRQ0	System timer
IRQ1	Keyboard interrupt.
IRQ2	Slave PIC
IRQ3	Serial port 1 interrupt from Super I/O* device, user-configurable.
IRQ4	Serial port 1 interrupt from Super I/O* device, user-configurable.
IRQ5	
IRQ6	Floppy disk.
IRQ7	Generic
IRQ8_L	Active low RTC interrupt.
IRQ9	SCI*
IRQ10	Generic
IRQ11	Generic
IRQ12	Mouse interrupt.
IRQ13	Floaty processor.
IRQ14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1.
IRQ15	Secondary IDE Cable
SMI*	System Management Interrupt. General purpose indicator sourced by the Intel® ICH7R to the processors.

3.4.2.4 Serialized IRQ Support

The Intel® Entry Server Board SE7230NH1-E server board supports a serialized interrupt delivery mechanism. Serialized Interrupt Requests (SERIRQ) consists of a start frame, a minimum of 17 IRQ / data channels, and a stop frame. Any slave device in the quiet mode may initiate the start frame. While in the continuous mode, the start frame is initiated by the host controller.

3.5 PCI Error Handling

The PCI bus defines two error pins, PERR# and SERR#, for reporting PCI parity errors and system errors, respectively. In the case of PERR#, the PCI bus master has the option to retry the offending transaction, or to report it using SERR#. All other PCI-related errors are reported by SERR#. SERR# is routed to NMI if enabled by BIOS.

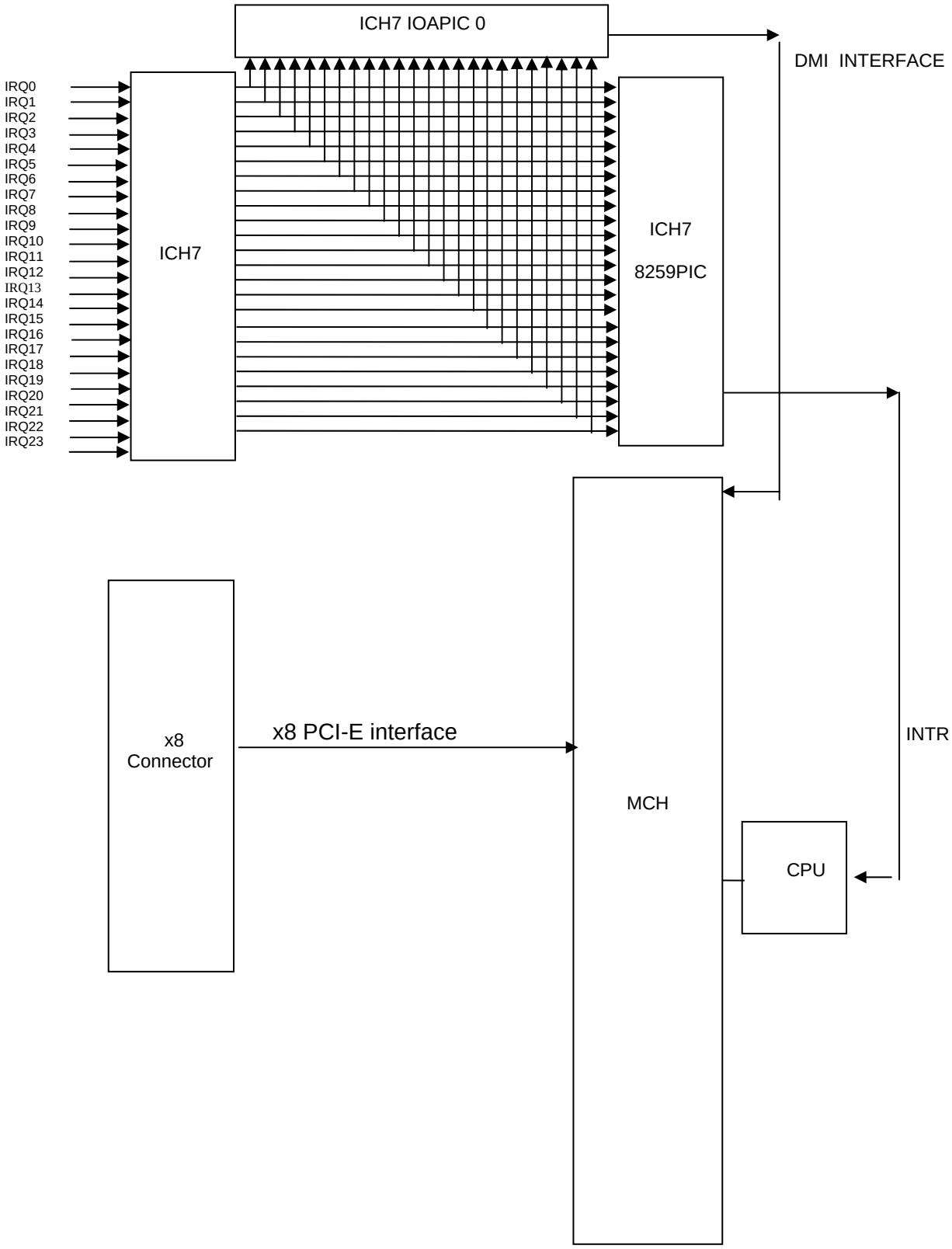

ICH7 IOAPIC 0
DMI INTERFACE
IRQ0
IRQ1
IRQ2
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQ8
IRQ9
IRQ10
IRQ11
IRQ12
IRQ13
IRQ14
IRQ15
IRQ16
IRQ17
IRQ18
IRQ19
IRQ20
IRQ21
IRQ22
IRQ23
ICH7
ICH7
8259PIC
x8
Connector
x8 PCI-E interface
INTR
MCH
CPU

Figure 5. Interrupt Routing Diagram

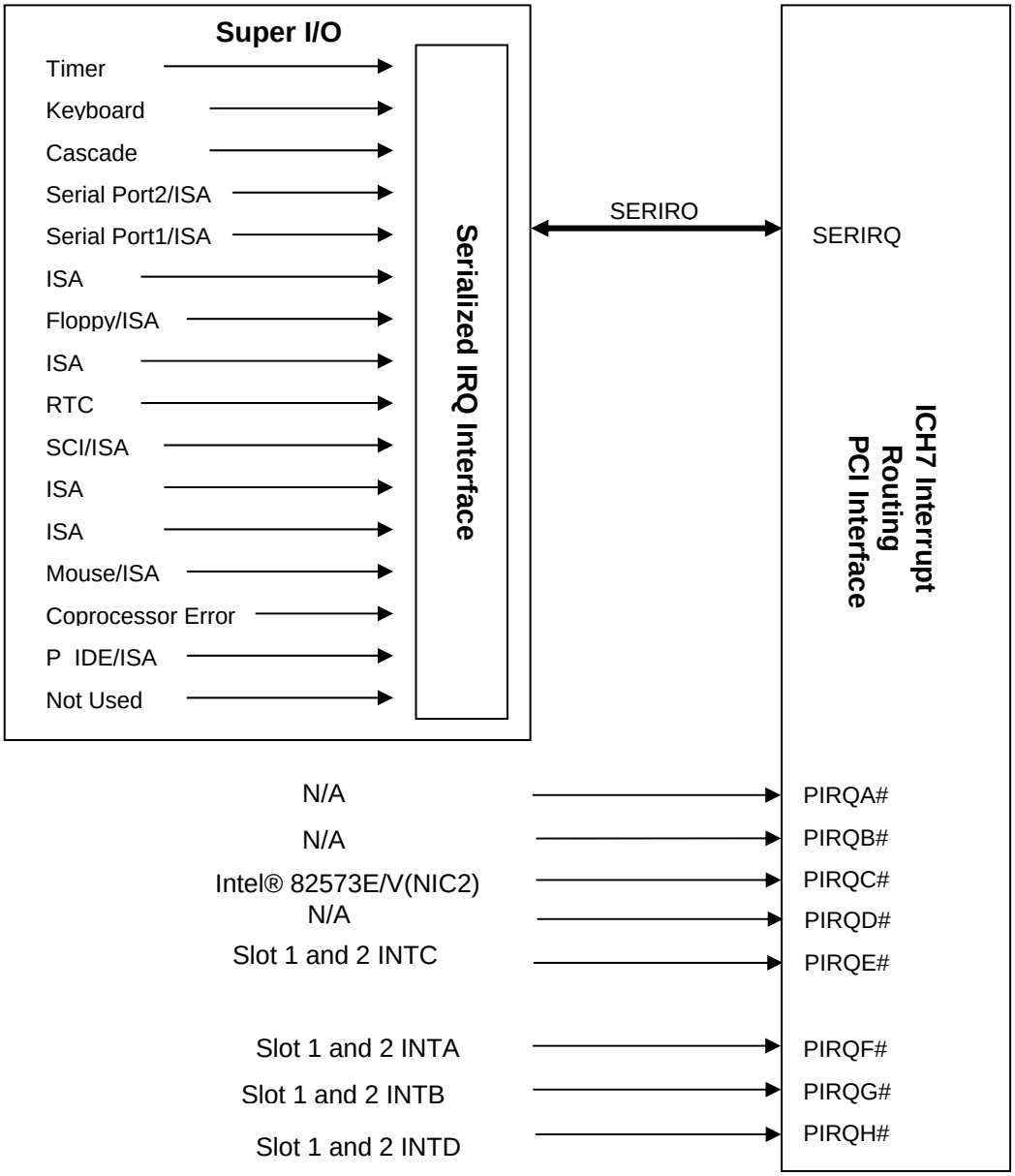


Figure 6. Intel® ICH7R Interrupt Routing Diagram

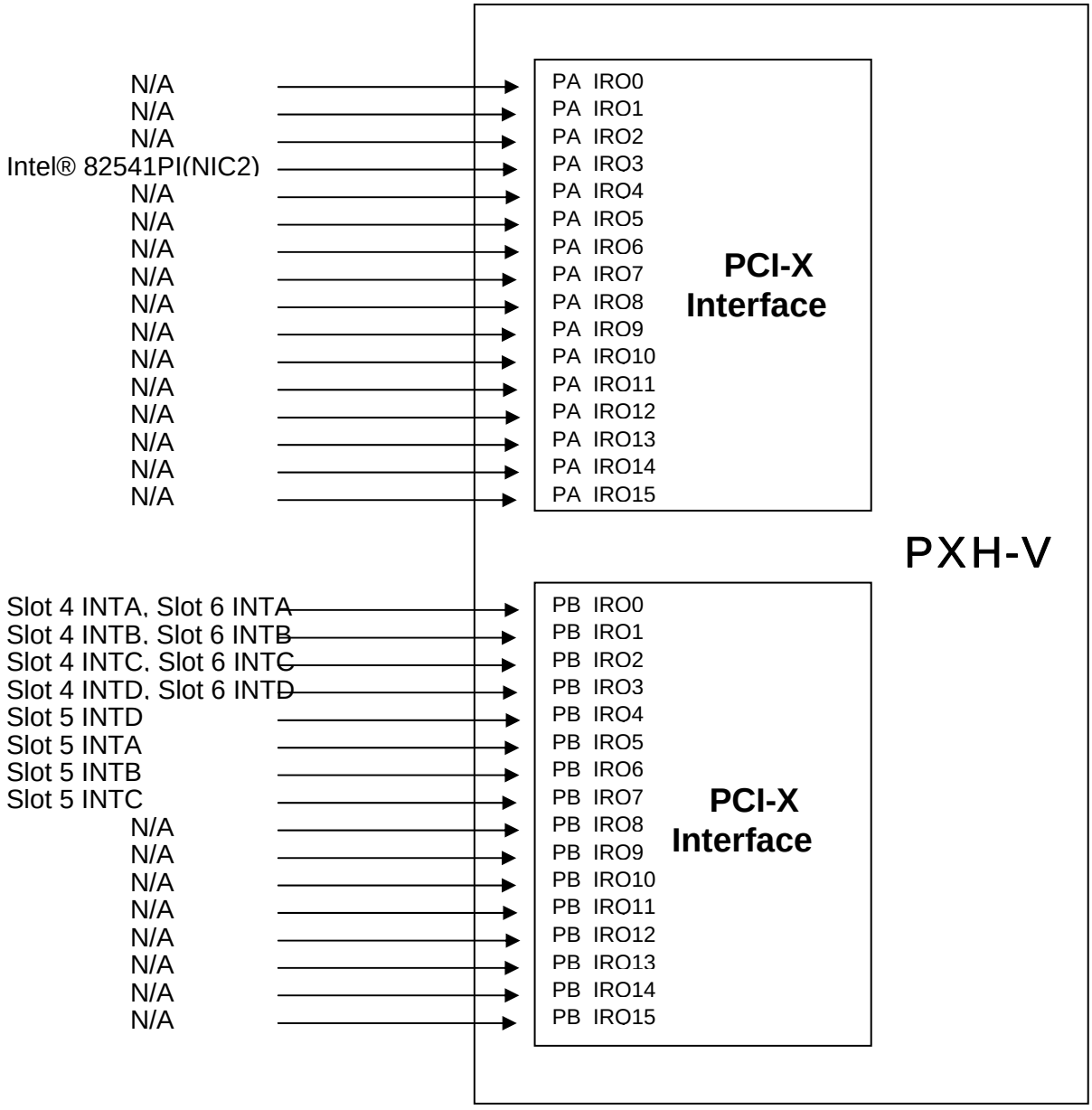


Figure 7. PXH-V Interrupt Routing Diagram

3.5.1 Video Support

The Intel® Entry Server Board SE7230NH1-E includes an integrated stand-alone ATI ES1000* graphics engine that supports standard SVGA drivers with analog display capabilities. The graphics subsystem has 16 MB of dedicated memory to support the onboard video controller. The baseboard provides a standard 15-pin VGA connector at the rear of the system, in the standard ATX I/O opening area. The video controller is disabled by default in BIOS Setup when an off-board video adapter is detected in either the PCI-E or PCI slots.

3.5.1.1 Video Modes

Table 17. Video Modes

2D Mode	Refresh Rate (Hz)	2D Video Mode Support			
		8 bpp	16 bpp	24 bpp	32 bpp
640x480	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
800x600	60, 70, 75, 90, 100	Supported	Supported	Supported	Supported
1024x768	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
1280x1024	43, 60	Supported	Supported	Supported	Supported
1280x1024	70, 72	Supported	–	Supported	Supported
1600x1200	60, 66	Supported	Supported	Supported	Supported
1600x1200	76, 85	Supported	Supported	Supported	–
3D Mode	**Refresh Rate (Hz)**	**3D Video Mode Support with Z Buffer Enabled**			
		8 bpp	**16 bpp**	**24 bpp**	**32 bpp**
640x480	60,72,75,90,100	Supported	Supported	Supported	Supported
800x600	60,70,75,90,100	Supported	Supported	Supported	Supported
1024x768	60,72,75,90,100	Supported	Supported	Supported	Supported
1280x1024	43,60,70,72	Supported	Supported	–	–
1600x1200	60,66,76,85	Supported	–	–	–
3D Mode	**Refresh Rate (Hz)**	**3D Video Mode Support with Z Buffer Disabled**			
		8 bpp	**16 bpp**	**24 bpp**	**32 bpp**
640x480	60,72,75,90,100	Supported	Supported	Supported	Supported
800x600	60,70,75,90,100	Supported	Supported	Supported	Supported
1024x768	60,72,75,90,100	Supported	Supported	Supported	Supported
1280x1024	43,60,70,72	Supported	Supported	Supported	–
1600x1200	60,66,76,85	Supported	Supported	–	–

3.5.1.2 Dual video

-

Dual video mode is not supported using the On-Board graphics controller.

3.5.2 Network Interface Controller (NIC)

The Intel® Entry Server Board SE7230NH1-E supports two 10/100/1000Base-T network interfaces.

- NIC1 is an Intel® 82573E/V gigabit Ethernet controller resourced with an x1 PCI-Express interface from the Intel® ICH7R (PCI Segment B).
- NIC2 is an Intel® 82541PI Gigabit Ethernet Controller is resourced with a 32bit/33MHz PCI Segment from the Intel® ICH7R (PCI Segment A).

Both the Intel® 82573E/V and Intel® 82541PI Gigabit Ethernet Controllers are single, compact components with an integrated gigabit Ethernet Media Access Control (MAC) and physical layer (PHY) function. The Intel® 82573E/V and Intel® 82541PI Gigabit Ethernet Controller allow for a gigabit Ethernet implementation in a very small area that is footprint compatible with current generation 10/100 Mbps Fast Ethernet designs. The Intel® 82541PI Gigabit Ethernet Controller and Intel® 82573E/V integrate and fourth and fifth generation (respectively) gigabit MAC design with fully integrated, physical layer circuitry to provide a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE_TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). The controller is capable of transmitting and receiving data at rates of 1000 Mbps, 100 Mbps, or 10 Mbps. In addition to managing MAC and PHY layer functions, the controller provides a 32-bit wide direct Peripheral Component Interconnect (PCI) 2.3 compliant interface capable of operating at 33 or 66MHz.

Network adapter teaming is not supported with the Intel® 82573E ethernet controller. This adapter supports Intel® iAMT technology and conflicts with teaming implementations.

3.5.2.1 NIC Connector and Status LEDs

The NICs drive two LEDs located on each network interface connector. Intel® Entry Server boards SE7230NH1-E with AA-302 versions -302 and earlier, the NIC LEDs are compliant with tables 19 and 20. Boards with AA -400 and later are compliant with table 21. for both NIC LEDs.

Table 18. Network Connector LED Status

Table 19. Intel® 82573E/V (NIC 1)

LED	Color	LED State	Condition
Left	Green	Off	LAN link is not established.
		On	LAN link is established.
		Blinking	LAN activity is occurring.
Right	N/A	Off	10 Mbit/sec data rate is selected.
	Green	On	100 Mbit/sec data rate is selected.
	Yellow	**On**	1000 Mbit/sec data rate is selected.

Table 20. Intel® 82541PI Gigabit Ethernet Controller (NIC 2)

LED	Color	LED State	Condition
Left	Yellow	Off	LAN link is not established.
		On	LAN link is established.
		Blinking	LAN activity is occurring.
Right	N/A	Off	10 Mbit/sec data rate is selected.
	Yellow	On	100 Mbit/sec data rate is selected.
	Green	**On**	1000 Mbit/sec data rate is selected.

Table 21. Intel® 82573E/V and Intel® 82541 Gigabit Eithernet Controllers, AA D13543-400 or D18675-400 and later

LED	Color	LED State	Condition
Left	Green	Off	LAN link is not established.
		On	LAN link is established.
		Blinking	LAN activity is occurring.
Right	N/A	Off	10 Mbit/sec data rate is selected.
	Green	On	100 Mbit/sec data rate is selected.
	Yellow	**On**	1000 Mbit/sec data rate is selected.

3.5.3 Super I/O Chip

The National Semiconductor PC8374LOIBU* (LX SKU) and SMsC LP47M182NR* (LC SKU) SIO devices contain all of the necessary circuitry to control serial/parallel ports, floppy disk, PS/2-compatible keyboard, mouse and hardware monitor controller. The baseboard implements the following features:

- GPIOs
- One serial port
- Floppy controller
- Keyboard and mouse
- Local hardware monitoring
- Wake up control
- System health support

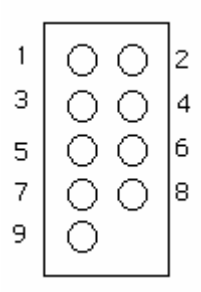
3.5.3.1 Serial Ports

The board provides a single serial port implemented as a stand-alone external 9-pin serial port. The following sections provide details on the use of the serial port.

3.5.3.1.1 Serial Port A

Serial A is a standard DB9 interface located at the rear I/O panel of the server board, below the video connector. Serial A is designated by as “Serial A” on the silkscreen. The reference designator is J8A1.

Table 22. Serial A Header Pin-out

Pin	Signal Name	Serial Port A Header Pin-out
1	DCD	
2	DSR	
3	RX	
4	RTS	
5	TX	
6	CTS	
7	DTR	
8	RI	
9	GND	

3.5.3.2 Fast X-Bus Extension for Boot Flash, Memory and I/O

The fast X-bus Supports I/O and memory read/write operations and 8-bit data bus, 28-bit addressing.

3.5.3.3 Floppy Disk Support

The floppy disk controller (FDC) in the Super I/O is functionally compatible with floppy disk controllers in the DP8473 and N844077. All FDC functions are integrated into the Super I/O* including analog data separator and 16-byte FIFO. The baseboard provides a standard 34-pin interface for the floppy disk controller.

3.5.3.4 Keyboard and Mouse Support

Two external PS/2 ports, located on the back of the baseboard, are provided to access the keyboard or mouse functions.

3.5.3.5 Wake-up Control

The Super I/O contains functionality that allows various events to control the power-on and power-off the system.

3.5.4 BIOS Flash

The board incorporates an Intel® 28F320C3 flash memory component. The Intel® 28F320C3 is a high-performance 32-megabit memory component that provides 2096K x 16 of BIOS and non-volatile storage space. The flash device is connected through the X Bus from Super I/O*.

3.5.5 System Health Support

I_2C interface to Heceta* sensors (Fan Monitor and Control (FMC)

- One PWM-based fan controls
- Software or local temperature feedback control
- Chassis intrusion detection

3.6 Replacing the Back-Up Battery

The lithium battery on the server board powers the RTC for up to ten years in the absence of power. When the battery starts to weaken, it loses voltage, and the server settings stored in CMOS RAM in the RTC (for example, the date and time) may be wrong. Contact your customer service representative or dealer for a list of approved devices.

⚠ WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the equipment manufacturer. Discard used batteries according to manufacturer's instructions.

⚠ ADVARSEL**!**

Lithiumbatteri - Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

⚠ ADVARSEL

Lithiumbatteri - Eksplosjonsfare. Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.

⚠ VARNING

Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.

⚠ VAROITUS

Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

4. System BIOS

4.1 BIOS Setup Utility

The BIOS Setup utility is provided to perform system configuration changes and to display current settings and environment information.

The BIOS Setup utility stores configuration settings in system non-volatile storage. Changes affected by BIOS Setup will not take effect until the system is rebooted. The BIOS Setup Utility can be accessed when prompted during POST by using the F2 key.

4.1.1 Localization

The Setup program and help messages currently support up to six languages. However, depending upon space requirements the following applies with regard to language support.

Flex BIOS handles Languages now based upon OEM requirements. This is a stretch goal.

The default language is US English. This is the only language that is guaranteed to be properly translated and functional.

4.1.2 Configuration Reset

There are different mechanisms for resetting the system configuration to default values. When a reset system configuration request is detected, the BIOS will load the default system configuration values during the next POST.

A reset system configuration request can be generated by moving the Clear CMOS jumper.

4.1.3 Keyboard Commands

The Keyboard Command Bar supports the following keys:

Table 23. BIOS Setup Keyboard Command Bar Options

Key	Option	Description
Enter	Execute Command	The Enter key is used to activate sub-menus when the selected feature is a sub-menu, or to display a pick list if a selected option has a value field, or to select a sub-field for multi-valued features like time and date. If a pick list is displayed, the Enter key will undo the pick list, and allow another selection in the parent menu.
ESC	Exit	The ESC key provides a mechanism for backing out of any field. This key will undo the pressing of the Enter key. When the ESC key is pressed while editing any field or selecting features of a menu, the parent menu is re-entered. When the ESC key is pressed, any sub-menu, the parent menu is re-entered. When the ESC key is pressed, any major menu, the exit confirmation window is displayed and the user is asked whether changes can be discarded. If “No” is selected and the Enter key is pressed, or if the ESC key is pressed, the user is returned to where they were before ESC was pressed without affecting any existing any settings. If “Yes” is selected and the Enter key is pressed, setup is exited and the BIOS continues with POST.

Key	Option	Description
↑	Select Item	The up arrow is used to select the previous value in a pick list, or the previous options in a menu item's option list. The selected item must then be activated by pressing the Enter key.
↓	Select Item	The down arrow is used to select the next value in a menu item's option list, or a value field's pick list. The selected item must then be activated by pressing the Enter key.
↔	Select Menu	The left and right arrow keys are used to move between the major menu pages. The keys have no affect if a sub-menu or pick list is displayed.
Tab	Select Field	The Tab key is used to move between fields. For example, Tab can be used to move from hours to minutes in the time item in the main menu.
-	Change Value	The minus key on the keypad is used to change the value of the current item to the previous value. This key scrolls through the values in the associated pick list without displaying the full list.
+	Change Value	The plus key on the keypad is used to change the value of the current menu item to the next value. This key scrolls through the values in the associated pick list without displaying the full list. On 106-key Japanese keyboards, the plus key has a different scan code than the plus key on the other keyboard, but will have the same effect.
F9	Setup Defaults	Pressing F9 causes the following to appear: **Load Setup Defaults?** **[OK] [Cancel]** If "OK" is selected and the Enter key is pressed, all setup fields are set to their default values. If "Cancel" is selected and the Enter key is pressed, or if the ESC key is pressed, the user is returned to where they were before F9 was pressed without affecting any existing field values.
F7	Discard Changes	Pressing F7 causes the following message to appear: **Discard Changes?** **[OK] [Cancel]** If "OK" is selected and the Enter key is pressed, all changes are not saved and setup is exited. If "Cancel" is selected and the Enter key is pressed, or the ESC key is pressed, the user is returned to where they were before F7 was pressed without affecting any existing values.
F10	Save Changes and Exit	Pressing F10 causes the following message to appear: **Save configuration changes and exit setup?** **[OK] [Cancel]** If "OK" is selected and the Enter key is pressed, all changes are saved and setup is exited. If "Cancel" is selected and the Enter key is pressed, or the ESC key is pressed, the user is returned to where they were before F10 was pressed without affecting any existing values.

4.1.4 Entering BIOS Setup

Access BIOS Setup utility by pressing the <F2> hotkey during POST.

4.1.4.1 Main Menu

The first screen displayed when entering the BIOS Setup Utility is the Main Menu selection. The first screen displayed when entering the BIOS Setup Utility is the Main Menu selection screen. This screen displays the major menu selections available: The following tables describe the available options on the top level and lower level menus. Default values are in **bold** text.

Table 24. BIOS Setup, Main Menu Options

Feature	Options	Help Text	Description
BIOS Version	N/A	N/A	BIOS ID string (excluding the build time and date)
Processor Type	N/A	N/A	
Hyper Threading Technology	**Enable** Disable	N/A	Select Disable if your operating system does not support Hyper Threading
Processor Speed	N/A	N/A	Calculated processor speed
System Bus Speed	N/A	N/A	Dispalyed the system bus speed
System Memory Speed	N/A	N/A	Dispalyed the system memory speed
L2 Chache RAM	N/A	N/A	
Total Memory	N/A	N/A	Amount of physical memory detected
Memory Mode	N/A	N/A	Display the memory mode
Memory Channel A Slot 0	N/A	N/A	Display the memory detected
Memory Channel A Slot 1	N/A	N/A	
Memory Channel B Slot 0	N/A	N/A	
Memory Channel B Slot 1	N/A	N/A	
Additional System Information	N/A	N/A	Selects submenu with additional system information details
System Date	DAY MM/DD/YYYY	Use [TAB] or [SHIFT-TAB] to select a field. Use [+] or [-] to configure System date.	Configures the system date. Default is [Tue 01/01/2002]. Day of the week is automatically calculated
System Time	HH:MM:SS	Use [TAB] or [SHIFT-TAB] to select a field. Use [+] or [-] to configure system time.	Configures the system time on a 24 hour clock. Default is 00:00:00

4.1.4.1.1 Additional System Information Sub-menu

Table 25. BIOS Setup, Additional System Information Sub-menu Selections

Feature	Options	Help Text	Description
System Information			Informational display.

Feature	Options	Help Text	Description
Manufacture	N/A	N/A	
Product Name	N/A	N/A	
Version	N/A	N/A	
Serial Number	N/A	N/A	
Server Board Information			
Manufacture	N/A	N/A	
Product Name	N/A	N/A	
Version	N/A	N/A	
Serial Number	N/A	N/A	
Chassis Information			
Manufacture	N/A	N/A	
Version	N/A	N/A	
Serial Number	N/A	N/A	
Asset Tag	N/A	N/A	

4.1.4.2 Advanced Menu

Table 26. BIOS Setup, Advanced Menu Options

Feature	Options	Help Text	Description
Boot Configuration	N/A	Configure Boot devices	Selects submenu
Peripheral Configuration	N/A	Configure Peripheral devices	Selects submenu
Drive Configuration	N/A	Configure Premary master slave and secondary mater and slave	Selects submenu
Floppy Configuration	N/A	Configure the Floppy drive(s).	Selects submenu
Event Log Configuration	N/A	View th events in the event log or clear current events	Selects submenu
Video Configuration	N/A	Configure the Video	Selects submenu
Hardware Monitoring	N/A	Configure Hardware Monitoring	Selects submenu
Chipset Configuration	N/A	Configure the Chipset	Selects submenu
Management Configuration	N/A	Configure the Management	Selects submenu
USB Configuration	N/A	Configure the USB support.	Selects submenu

4.1.4.2.1 Boot Configuration Sub-menu

Table 27. BIOS Setup, Advanced Menu, Boot Configuration Sub-menu Selections

Feature	Options	Help Text	Description
Num-Lock	Off **On**	Turns keyboard numlock on or off	
CPU Fan Control	Disable **Enable**	Enable or Disable CPU fan control	
System Fan Control	Disable **Enable**	N/A	
Lowest Fan Speed	**Slow** Off	This options defines the lower limit of chassis fan speed operation. Slow: At low system temperatures the fans will continue to run at a slow speed. Off: At low system temperatures the fans will turn off.	
Max CPUID Value Limit	**Disable** Enable	This should be enabled in order to boot Legacy OSes that cannot support CPUs with extended CPUID functions	
Display Setup Prompt	Off **On**	Displays “Press F2 to Enter Setup” message during POST	

4.1.4.2.2 Peripheral Configuration Sub-menu

Table 28. BIOS Setup, Advanced Menu, Peripheral Configuration Sub-menu

Feature	Options	Help Text	Description
Serial Port	Disable **Enable**	N/A	
PCI Express* On-board LAN	Disable **Enable**	Enables or Disables the PCI Express* On-board LAN Device (NIC1 Intel 82573E/V)	
PCI On-board LAN	Disable **Enable**	Enables or Disables the PCI On-board LAN Device (NIC2 Intel 82541P I)	

4.1.4.2.3 Drive Configuration Sub-menu

Table 29. BIOS Setup, Advanced Menu, Drive Configuration Menu Options

Feature	Options	Help Text	Description
Use Automatic Mode	Disable **Enable**		
ATA/IDE Mode	Legacy **Enhanced**	This will configure SATA to be in Enhanced (native) or Legacy mode	Controls state of integrated S-ATA and P-ATAcontroller.

Feature	Options	Help Text	Description
Configure S-ATA as	**IDE** RAID AHCI	This will configure SATA into the corresponding types	In Enhance mode this item will be showed
S.M.A.R.T.	**Enable** Disable	S.M.A.R.T. stands for Self-Monitoring, Analysis, and Reporting Technology.	The Auto setting should work in most cases.
SATA Port 0	N/A	N/A	Display the SATA HDD detected
SATA Port 1	N/A	N/A	Display the SATA HDD detected
SATA Port 2	N/A	N/A	Display the SATA HDD detected
SATA Port 3	N/A	N/A	Display the SATA HDD detected
Primary Master	N/A	N/A	Displays Primary Master PATA device detected
Primary Slave	N/A	N/A	Displays Primary Slave PATA device detected
Hard Disk Pre-Delay (Sec)	0 5 10 15 20 25 30 35	Indicates the amount of time in seconds that the firmware will wait to detect Hard Disk drives	

4.1.4.2.4 Floppy Configuration Sub-menu

Table 30. BIOS Setup, Advanced Menu, Floppy Configuration Sub-menu Selections

Feature	Options	Help Text	Description
Diskette Controller	Disable Enable **Automatic**	Enables or Disables the Floppy Disk Controller	
Diskette Write Protect	**Diable** Enable	Enables or Disables the Floppy Write Protection	
Floppy Type	**1.44 MB** 2.88 MB	Floppy Media Capacity	

4.1.4.2.5 Event Log Configuration Sub-menu

Table 31. BIOS Setup, Advanced Menu, Event Log Configuration Sub-menu Selections

Feature	Options	Help Text	Description
View Eventl Log		Views the events	
Clear Even Log	**Disable** Enable	Clears the events	When Disable is selected, the event log will be cleared during the next system reset

Feature	Options	Help Text	Description
Event Logging	Disable **Enable**		Enables/Disables the event log
ECC Event Loggin	Disable **Enable**		Enables/Disables ECC Events recorded in the event log

4.1.4.2.6 Video Configuration Sub-menu

Table 32. BIOS Setup, Advanced Menu, Video Configuration Sub-menu Selections

Feature	Options	Help Text	Description
Primary Video Adapter	**Auto** Ext PCIE Graphics (PEG) Ext PCI Graphics		

4.1.4.2.7 Chipset Configuration Sub-menu Selections

Table 33. BIOS Setup, Advanced Menu, Chipset Configuration Sub-menu Selections

Feature	Options	Help Text	Description
Memory Configuration	N/A	N/A	Selects submenu with memory configuration details
PCI Express* Configuration	N/A	N/A	Selects submenu with PCI Express* configuration idetails
PCI Latency Timer	32 64 96 128 160 192 224 248		

4.1.4.2.7.1 Memory Configuration Sub-menu

This sub-menu provides information about the DIMMs detected by the BIOS. The DIMM number is printed on the baseboard next to each device.

Table 34. BIOS Setup, Advanced Menu, Chipset Configuation, Memory Configuration Sub-menu Selections

Feature	Options	Help Text	Description
Memory correction	Non-ECC **ECC**	Allow the user to turn error reporting on or off if the system and all the memory installed supports ECC (Error Correction Code)	
Memory frequency	N/A	N/A	Informational display.
SDRAM tCL	N/A	N/A	
SDRAM tRCD	N/A	N/A	
SDRAM tRP	N/A	N/A	
SDRAM tRASmin	N/A	N/A	
DDR2 voltage	N/A	N/A	
Total memory	N/A	N/A	
Memory mode	N/A	N/A	
DIMM 1A	N/A	N/A	
DIMM 2A	N/A	N/A	
DIMM 1B	N/A	N/A	
DIMM 2B	N/A	N/A	

4.1.4.2.7.2 PCI Configuration Sub-menu

This sub-menu provides control over PCI devices and their option ROMs. If the BIOS is reporting POST error 146, use this menu to disable option ROMs that are not required to boot the system.

Table 35. BIOS Setup, Advanced Menu, Chipset Configuation, PCI Express* Configuration Sub-menu Selections

Feature	Options	Help Text	Description
PEG Negotiated Width	N/A	N/A	
Compliance Test Pattern	**Disable** Enable	N/A	

4.1.4.2.8 USB Mass Storage Device Configuration Sub-menu

Table 36. BIOS Setup, Advanced Menu, USB Mass Storage Device Configuration Sub-menu Selections

Feature	Options	Help Text	Description
USB 2.0	**Enable** Disable	N/A	Enable/Disable all USB ports

4.1.4.3 Security Menu

Table 37. BIOS Setup, Security Menu Options

Feature	Options	Help Text	Description
Supervisor password	N/A	Install / Not installed	Informational display.
User password	N/A	Install / Not installed	Informational display
Set supervisor password	N/A	Set supervisor password	Set password to null to clear
Set user password	N/A	Set user password	This node is grayed out until Admin password is installed. Set password to null to clear.
Expansion card text	**Disable** Enable	N/A	
Chassis intrusion	Disable **Enable**	N/A	Chassis intrusion enable will log chassis intrusion to the event log
XD technology	Disable **Enable**	N/A	Enables/Disables the CPU Execute disable Bit.

4.1.4.4 Power Menu

Table 38. BIOS Setup, Power Menu Selections

Feature	Options	Help Text	Description
After Power Failure	**Stay off** Last State Power On	Determines the mode of operation if a power loss occurs. Stays Off: System will remain off once power is restored. Last State: Restores system to the same state is was before power failed. Power On: System will power on once power is restored.	
Wake on LAN from S5	Stay Off Power On	Determines the action taken when the system power is of f and a PCI Power Management wake up event occurs.	

4.1.4.5 Boot Menu

Table 39. BIOS Setup, Boot Menu Selections

Feature	Options	Help Text	Description
Boot menu type	**Normal** Advance	N/A	
Boot device priority	Varies	N/A	Select the boot drive order
Hard drive order	Varies	N/A	Select the boot order of available hard drive devices
CD/DVD-ROM drive order	Varies	N/A	Select the boot order of available CD/DVD devices
Removable drive Oorder	Varies	N/A	Select the boot order of removable devices
Boot to optical devices	Disable **Enable**	Enables or disables boot to optical devices	
Boot to removable devices	Disable **Enable**	Enables or disables boot to removable devices	
Boot to network	Disable **Enable**	Enables or disables boot to network	
USB boot	Disable **Enable**	Enables or disables USB boot	
Zip emulation type	**Floppy** Hard Disk	Sets the emulation type for zip drives	

4.1.4.6 Exit menu

Table 40. BIOS Setup, Exit Menu Selections

Feature	Options	Help Text
Exit saving changes	N/A	Exit system setup after saving the changes. F10 key can be used for this operation.
Exit discarding changes	N/A	Exit system setup without saving any changes. ESC key can be used for this operation.
Load optimal defaults	N/A	Load Ssetup default values for all the setup questions. F9 key can be used for this operation.
Load custom defaults	N/A	Load custom defaults.
Save custom defaults	N/A	Save custom defaults
Discard changes	N/A	Discards changes done so far to any of the setup questions. F7 key can be used for this operation.

4.2 BIOS Updates

4.2.1 Preparing for the Upgrade

Before upgrading the BIOS, prepare for the upgrade by completing the following steps:

1. Record the current BIOS settings.
2. Obtain the upgrade utility.
3. Review the release notes.
4. Make a copy of the current BIOS.

4.2.2 Recording the Current BIOS Settings

1. Boot the computer and press <F2> when you see the message:

   ```
   Press <F2> Key if you want to run SETUP
   ```

2. Write down the current settings in the BIOS Setup program or go to the Exit menu and choose to “Save Custom Defaults”.

Note: Do not skip step 2. These settings will be needed to configure the computer at the end of the procedure.

If the user chooses to “Save Custom Defaults,” after the new BIOS is flashed, the user can restore settings from the “Load Custom Default” option.

4.2.3 Obtaining the Upgrade Utility

The user can upgrade to a new version of the BIOS using the new BIOS files and the BIOS upgrade utility. The user can obtain the BIOS upgrade file and the utility from the Intel Customer Support Web site: http://support.intel.com/support/motherboards/server/SE7230NH1-E.

4.2.4 Creating a Bootable Diskette

1. Use a DOS system to create the diskette.
2. Insert a diskette in diskette drive A.
3. At the C:\ prompt, for an unformatted diskette, type:

   ```
   format a:/s
   ```

   or, for a diskette that has already been formatted, type:

   ```
   sys a:
   ```

4. Press <Enter>.

4.2.5 BIOS update instructions using iFlash utility

1. Download the DOS BIOS update utility from the server board URL site listed above and copy to a DOS bootable diskette or other DOS bootable removable media.

2. Upon boot to DOS, run iflash.exe. Select System BIOS update and continue.

3. The iflash utility will invoke a file selection dialog to select a .BIO file for the upgrade. The only instance should be the BIOS image file downloaded in step 1. Select the .BIO file and hit <Enter> to continue.

4. After the BIOS update successfully completes the utility will prompt to restart the system.

4.2.6 BIOS Update Instructions Using Express BIOS

On the BIOS page for the Intel® Entry Server Board SE7230NH1-E, click on the Express BIOS Update utility.

Either download the file to your hard drive or select “Run from Current Location”. (If you opt to “Run from Current Location”, skip step 3).

Note: Make a note of the path the file is saved to on the hard drive. The user can save this utility onto a floppy disk. This is useful if the user is updating the BIOS for multiple identical systems.

1. Close all other applications.

Note: This is a required step. Your system will be rebooted at the last Express BIOS Update window.

2. Double-click the executable file from the location on the hard drive where it was saved. This runs the update program.

3. Follow the instructions provided in the dialog boxes to complete the BIOS update. On some recent boards, after the system reboots, there will be no video and there will be a series of beeps for approximately 30 seconds.

4.2.7 Resetting CMOS After BIOS Update

As the system reboots, watch the BIOS identifier to make sure the new BIOS version was properly installed.

1. During boot, press the [F2] key to enter the BIOS Setup Utility.

2. Return the CMOS settings to the factory defaults by pressing [F9], then press [ENTER] to load setup defaults.

Note: If the user saved the CMOS setting as custom defaults before the BIOS upgrade, go to the Exit menu and choose the “Load Custom Defaults“ option to return it to the previous custom settings.

3. Press [F10] to save the settings

4. Then press [ENTER] to accept the changes

5. Go through each screen of options

6. Return the CMOS settings to the values previously recorded prior to upgrading the BIOS.

4.2.7.1 BIOS Recovery

In the unlikely event that a FLASH upgrade is interrupted catastrophically, it is possible the BIOS will be left in an unusable state. Recovering from this condition requires the following steps (be sure a power supply and speaker have been attached to the board, and a floppy drive is connected as drive A):

1. Change Flash Recovery jumper to the recovery mode position.

2. Install the bootable upgrade diskette into drive A:

3. Reboot the system.

4. Because of the small amount of code available in the non-erasable boot block area, no video is available to direct the procedure. The procedure can be monitored by listening to the speaker and looking at the floppy drive LED. When the system beeps and the floppy drive LED is lit, the system is copying the recovery code into the FLASH device. As soon as the drive LED goes off, the recovery is complete.

5. Turn the system off.

6. Change the Flash Recovery jumper back to the default position.

7. Remove the upgrade floppy in drive A: and turn the system on.

Note: If the error message “CMOS/GPNV Checksum Bad Press F2 to Run SETUP“ appears during boot, then press [F2] to go into the “BIOS Setup Utility“, press [F9] to load setup defaults, and then press [F10] to save and exit.

4.3 Operating System Boot, Sleep, and Wake

4.3.1 Advanced Configuration and Power Interface (ACPI)

An ACPI-aware operating system generates an SMI to request that the system be switched into ACPI mode. The BIOS responds to enable ACPI mode. The system automatically returns to Legacy mode upon hard reset or power-on reset.

The Intel® Entry Server Board SE7230NH1-E supports S0, S1, S4, and S5 states. When the system is operating in ACPI mode, the OS retains control of the system and OS policy determines the entry methods and wake up sources for each sleep state

Note: Sleep entry and wake up event capabilities are provided by the hardware but are enabled by the operating system.

S0 Sleep State The S0 sleep state is when everything is on. This is the state that no sleep is enabled.

S1 Sleep State The S1 sleep state is a low wake-up latency sleep state. In this state, no system context is lost (Processor or chipset). The system context is maintained by the hardware.

S4 Sleep State The S4 Non-Volatile Sleep state (NVS) is a special global system state that allows system context to be saved and restored (relatively slowly) when power is lost to the baseboard. If the system has been commanded to enter the S4 sleep state, the operating system will write the system context to a non-volatile storage file and leave appropriate context markers.

S5 Sleep State The S5 sleep state is similar to the S4 sleep state except the operating system does not save any context nor enable any devices to wake the system. The system is in the “soft” off state and requires a complete boot when awakened.

4.3.1.1 Power Switch Off to On

The power button input (J1J1 pin 11and 13) provides FP_PWR_BTN_N signal to the mBMC (PC87431M). mBMC will output a MBMC_PWR_BTN_N signal to ICH7. If the PWRBTN# signal of Intel® ICH7R is asserted, the assertion causes a wake event. Then, the SLP_S3 signal of Intel® ICH7R will be not asserted. The SLP_S3 signal will be passed to the PS_ON# signal of ATX power supply through an inverter, and then transition to an ON state.

4.3.1.2 On to Off (Legacy)

The ICH7 is configured to generate an SMI due to a power button event. The BIOS services this SMI and sets the state of the machine in the ICH7 and Super I/O* to the OFF state.

4.3.1.3 System Sleep States

The baseboard is capable of wake up from several sources under a non-ACPI configuration, such as when the operating system does not support ACPI. The wake up sources are defined in the following table.

Table 41. Supported Wake Events

Wake Event	Supported via ACPI (by sleep state)	Supported Via Legacy Wake
Power Button	Always wakes system	Always wakes system
PME from PCI 32/33	S1, S4	S5
PME from primary PCI 64/66	S1, S4	S5
RTC Alarm	S1, S4	No
Mouse	S1	No
Keyboard	S1	No
USB	S1	No

Under ACPI, the operating system programs the Intel® ICH7R and Super I/O to wake up on the desired event, but in Legacy mode, the BIOS enables/disables wake up sources based on an option in BIOS Setup. The operating system or a driver must clear any pending wake up status bits in the associated hardware (such as the Wake on LAN status bit in the LAN application specific integrated circuit (ASIC), or PCI Power Management Event (PME) status bit in a PCI device. The Legacy wake up feature is disabled by default.

5. Platform Management Architecture

5.1 Reset Button

The reset button will generate a hard reset to the system.

5.2 Diagnostic Interrupt Button (Control Panel NMI)

The NMI button will force an NMI to the processors.

6. Error Reporting and Handling

6.1.1 BIOS Generated POST Error Beep Codes

The following table lists POST error beep codes. Prior to system video initialization, the BIOS uses these beep codes to communicate error conditions.

Table 42. BIOS Generated Beep Codes

Beeps	Error Message	POST Progress Code	Description
1	Fatal error		System halted because of an unspecified fatal error that was detected.
2	Processor error		System halted because a fatal error related to a processor was detected.
3	Memory error		System halted because a fatal error related to the memory was detected.
4	Motherboard error		System halted because a fatal error related to the system motherboard hardware was detected.

Table 43. Troubleshooting BIOS Beep Codes

Beeps	Error Message	POST Progress Code	Description
1	Recovery Started	E9h	Start of recovery process
2	Recovery Boot Error	Flashing series of POST codes: EFh, FAh, FBh, F4h, FCh, FDh, FFh	Unable to boot to floppy, ATAPI, or ATAPI CD-ROM. Recovery process will retry.
Series of long low-pitched single beeps	Recovery Failed	FDh	Unable to process valid BIOS recovery images. BIOS already passed control to operating system and flash utility.
2 long high-pitched beeps	Recovery Complete	FFh	BIOS recovery succeeded, ready for power-down, reboot.

6.1.2 BIOS Event Log

The BIOS will output the current boot progress codes on the video screen. Progress codes are 32-bit quantities plus optional data. The 32 bit numbers include Class, subclass, and Operation information. Class and subclass point to the type of the hardware that is being initialized, where as the Operation field represents the specific initialization activity. Based upon the data bit availability to display Progress Code, a progress code can be customized to fit the data width. The higher the data bit, higher the granularity of information, which could send on the progress port. The progress codes may be reported by system BIOS or option ROMs.

The following information can be captured by the BIOS Event Log for later reference:
Processor Thermal Trip,

Multi Bit ECC Error ChA,
Single Bit ECC Error ChA,
Cmos Battery Failure,
Cmos Checksum Error,
Cmos Timer Not Set,
Keyboard Not Found,
Memory Size Decrease,
Intruder Detection,
Spd Tolerant,
Mem Opti Dual,
Mem Opti Single,
Multi Bit ECC Error ChB,
Single Bit ECC Error ChB,
Perr Error,
Serr Error,

The Response section in the following table is divided in three different types:

Warning – The message is displayed on screen and the error is logged in the SEL. The System will continue booting with the degraded state. The User may want to replace the erroneous unit.

Pause – The message is displayed on the screen and the user input is required to continue. The user can take immediate corrective action or can choose to continue booting.

Halt – The system cannot boot unless the error is resolved. The user needs to replace the faulty part and restart the system.

Table 44. POST Error Messages and Handling

Error Code	Error Message	Response
100	Timer Error	Warning
103	CMOS Battery Low	Warning
104	CMOS Settings Wrong	Warning
105	CMOS Checksum Bad	Warning
10B	CMOS memory size different	Warning
112	CMOS time not set	Warning
140	Refresh timer test failed	Halt
141	Display memory test failed	Warning
142	CMOS Display Type Wrong	Pause
147	Unknown BIOS error. Error code = 147 (this is really a PMM_MEM_ALLOC_ERR)	Halt
148	Password check failed	Halt
149	Unknown BIOS error. Error code = 149 (this is really SEGMENT_REG_ERR)	Halt
14A	Unknown BIOS error. Error code = 14A (this is really ADM_MODULE_ERR)	Warning
14B	Unknown BIOS error. Error code = 14B (this is really	Warning

Error Code	Error Message	Response
	LANGUAGE_MODULE_ERR)	
14D	Primary Master Hard Disk Error	Pause
14E	Primary Slave Hard Disk Error	Pause
14F	Secondary Master Hard Disk Error	Pause
150	Secondary Slave Hard Disk Error	Pause
151	Primary Master Drive - ATAPI Incompatible	Pause
152	Primary Slave Drive - ATAPI Incompatible	Pause
153	Secondary Master Drive - ATAPI Incompatible	Pause
154	Secondary Slave Drive - ATAPI Incompatible	Pause
8100	Processor failed BIST	Warning
8110	Processor Internal error (IERR)	Warning
8120	Processor Thermal Trip error	Warning
8160	Processor unable to apply BIOS update	Pause
8170	Processor L2 cache Failed	Pause
8180	BIOS does not support current stepping for Processor	Pause
8190	Watchdog Timer failed on last boot	Warning
8191	12:1 Core to bus ratio: Processor Cache disabled	Pause
8192	L2 Cache size mismatch	Pause
8193	CPUID, Processor Stepping are different	Pause
8194	CPUID, Processor Family are different	Pause
8195	Front Side Bus Speed mismatch. System Halted	Pause
8197	CPU Speed mismatch	Pause
8300	Baseboard Management Controller failed to function	Pause
8301	Front Panel Controller failed to Function	Pause
84F2	Server Management Interface Failed	Pause
84F3	BMC in Update Mode	Pause
84F4	Sensor Data Record Empty	Pause
84FF	System Event Log Full	Warning

6.1.3 POST Code Checkpoints

Table 45. POST Code Checkpoints

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."

Checkpoint	Description
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache - Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor
C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
24	Uncompress and initialize any platform specific BIOS modules.
30	Initialize System Management Interrupt.
2A	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information.
39	Initializes DMAC-1 and DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, … etc.) successfully installed in the system and update the BDA, EBDA…etc.
50	Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7A	Initializes remaining option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.

Checkpoint	Description
87	Execute BIOS setup if needed / requested.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disable NMI as selected
90	Late POST initialization of system management interrupt.
A0	Check boot password if installed.
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A8	Prepare CPU for OS boot including final MTRR values.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector. De-initializes the ADM module.
AB	Prepare BBS for Int 19 boot.
AC	End of POST initialization of chipset registers.
B1	Save system context for ACPI.
00	Passes control to OS Loader (typically INT19h).

6.1.4 Bootblock Initialization Code Checkpoints

The Boot Block initialization code sets up the chipset, memory and other components before the system memory is available. The following table describes the type of checkpoints that may occur during the boot block initialization.

Table 46. Bootblock Initialization Code Checkpoints

Checkpoint	Description
Before D1	Early chipset initialization is done. Early Super I/O* initialization is done including RTC and keyboard controller. NMI is disabled.
D1	Perform keyboard controller BAT test. Check if waking up from power management suspend state. Save power-on CPUID value in scratch CMOS.
D0	Go to flat mode with 4GB limit and GA20 enabled. Verify the bootblock checksum.
D2	Disable CACHE before memory detection. Execute full memory sizing module. Verify that flat mode is enabled.
D3	If memory sizing module not executed, start memory refresh and do memory sizing in Bootblock code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. Main BIOS checksum is tested. If BIOS recovery is necessary, control flows to checkpoint E0. See Bootblock Recovery Code Checkpoints section of document for more information.

Checkpoint	Description
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See POST Code Checkpoints section of document for more information.

6.1.5 Bootblock Recovery Code Checkpoint

The Boot Block initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the boot block initialization.

Table 47. Bootblock Recovery Code Checkpoint

Checkpoint	Description
Before D1	Early chipset initialization is done. Early Super I/O* initialization is done including RTC and keyboard controller. NMI is disabled.
D1	Perform keyboard controller BAT test. Check if waking up from power management suspend state. Save power-on CPUID value in scratch CMOS.
D0	Go to flat mode with 4GB limit and GA20 enabled. Verify the bootblock checksum.
D2	Disable CACHE before memory detection. Execute full memory sizing module. Verify that flat mode is enabled.
D3	If memory sizing module not executed, start memory refresh and do memory sizing in Bootblock code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. Main BIOS checksum is tested. If BIOS recovery is necessary, control flows to checkpoint E0. See Bootblock Recovery Code Checkpoints section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See POST Code Checkpoints section of document for more information.

6.1.6 DIM Code Checkpoints

The Device Initialization Manager (DIM) module takes control at various times during BIOS POST to initialize different Buses. The following table describes the main checkpoints where the DIM module is accessed:

Table 48. DIM Code Checkpoints

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if the system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

6.1.7 ACPI Runtime Checkpoints

ACPI checkpoints are displayed when an ACPI capable operating system either enters or leaves a sleep state. The following table describes the type of checkpoints that may occur during ACPI sleep or wake events

Table 49. ACPI Runtime Checkpoints

Checkpoint	Description
AC	First ASL check point. Indicates the system is running in ACPI mode.
AA	System is running in APIC mode.
01, 02, 03, 04, 05	Entering sleep state S1, S2, S3, S4, or S5.
10, 20, 30, 40, 50	Waking from sleep state S1, S2, S3, S4, or S5.

6.2 Diagnostic LEDs

All port 80 codes are displayed using the Diagnostic LEDs found on the back edge of the baseboard. The diagnostic LED feature consists of a hardware decoder and four dual color LEDs. During POST, the LEDs will display all normal POST codes representing the progress of the BIOS POST. Each code will be represented by a combination of colors from the four LEDs.

The LEDs are capable of displaying three colors: green, red, and amber. The POST codes are divided into two nibbles, an upper nibble, and a lower nibble. Each bit in the upper nibble is represented by a red LED and each bit in the lower nibble is represented by a green LED. If

both bits are set in the upper and lower nibbles then both red and green LEDs are lit, resulting in an amber color. If both bits are clear, then the LED is off.

In the below example, BIOS sends a value of ACh to the Diagnostic LED decoder. The LEDs are decoded as follows:

- Red bits = 1010b = Ah
- Green bits = 1100b = Ch

Since the red bits correspond to the upper nibble and the green bits correspond to the lower nibble, the two are concatenated to be ACh.

Table 50. POST Progress Code LED Example

LEDs	Red	Green	Red	Green	Red	Green	Red	Green
Ach	1	1	0	1	1	0	0	0
Result	Amber		Green		Red		Off	
	MSB						LSB	

6.2.1 Diagnostic LED POST Progress Codes

Table 51. Boot Block POST Progress Codes

	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	Hi			Low	
10h	Off	Off	Off	R	The NMI is disabled. Start Power-on delay. Initialization code checksum verified.
11h	Off	Off	Off	A	Initialize the DMA controller, perform the keyboard controller BAT test, start memory refresh, and enter 4 GB flat mode.
12h	Off	Off	G	R	Get start of initialization code and check BIOS header.
13h	Off	Off	G	A	Memory sizing.
14h	Off	G	Off	R	Test base 512K of memory. Return to real mode. Execute any OEM patches and set up the stack.
15h	Off	G	Off	A	Pass control to the uncompressed code in shadow RAM. The initialization code is copied to Segment 0 and control will be transferred to Segment 0.
16h	Off	G	G	R	Control is in Segment 0. Verify the system BIOS checksum. If the system BIOS checksum is bad, go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.
17h	Off	G	G	A	Pass control to the interface module.
18h	G	Off	Off	R	Decompress of the main system BIOS failed.
19h	G	Off	Off	A	Build the BIOS stack. Disable USB controller. Disable cache.
1Ah	G	Off	G	R	Uncompress the POST code module. Pass control to the POST code module.
1Bh	A	R	Off	R	Decompress the main system BIOS runtime code.
1Ch	A	R	Off	A	Pass control to the main system BIOS in shadow RAM.

	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	Hi			Low	
E0h	R	R	R	Off	Start of recovery BIOS. Initialize interrupt vectors, system timer, DMA controller, and interrupt controller.
E8h	A	R	R	Off	Initialize extra module if present.
E9h	A	R	R	G	Initialize floppy controller.
Eah	A	R	A	Off	Try to boot floppy diskette.
Ebh	A	R	A	G	If floppy boot fails, intialize ATAPI hardware.
Ech	A	A	R	Off	Try booting from ATAPI CD-ROM drive.
Eeh	A	A	A	Off	Jump to boot sector.
Efh	A	A	A	G	Disable ATAPI hardware.

Table 52. POST Progress Codes

	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	Hi			Low	
20h	Off	Off	R	Off	Uncompress various BIOS Modules.
22h	Off	Off	A	Off	Verify password Checksum.
24h	Off	G	R	Off	Verify CMOS Checksum.
26h	Off	G	A	Off	Read Microcode updates from BIOS ROM.
28h	G	Off	R	Off	Initializing the processors. Set up processor registers. Select least featured processor as the BSP.
2Ah	G	Off	A	Off	Go to Big Real Mode.
2Ch	G	G	R	Off	Decompress INT13 module.
2Eh	G	G	A	Off	Keyboard Controller Test: The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller.
30h	Off	Off	R	R	Keyboard/Mouse port swap, if needed.
32h	Off	Off	A	R	Write Command Byte 8042: The initialization after the keyboard controller BAT command test is done. The keyboard command byte will be written next.
34h	Off	G	R	R	Keyboard Init: The keyboard controller command byte is written. Next, issuing the pin 23 and 24 blocking and unblocking commands.
36h	Off	G	A	R	Disable and initialize 8259.
38h	G	Off	R	R	Detect Configuration Mode, such as CMOS clear.
3Ah	G	Off	A	R	Chipset Initialization before CMOS initialization.
3Ch	G	G	R	R	Init System Timer: The 8254 timer test is over. Starting the Legacy memory refresh test next.
3Eh	G	G	A	R	Check Refresh Toggle: The memory refresh line is toggling. Checking the 15 second on/off time next.
40h	Off	R	Off	Off	Calculate CPU speed.
42h	Off	R	G	Off	Init interrupt Vectors: Interrupt vector initialization is done.
44h	Off	A	Off	Off	Enable USB controller in chipset.
46h	Off	A	G	Off	Initialize SMM handler. Initialize USB emulation.
48h	G	R	Off	Off	Validate NVRAM areas. Restore from backup if corrupted.

	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	Hi			Low	
4Ah	G	R	G	Off	Load defaults in CMOS RAM if bad checksum or CMOS clear jumper is detected.
4Ch	G	A	Off	Off	Validate date and time in RTC.
4Eh	G	A	G	Off	Determine number of micro code patches present.
50h	Off	R	Off	R	Load Micro Code To All CPUs.
52h	Off	R	G	R	Scan SMBIOS GPNV areas.
54h	Off	A	Off	R	Early extended memory tests.
56h	Off	A	G	R	Disable DMA.
58h	G	R	Off	R	Disable video controller.
5Ah	G	R	G	R	8254 Timer Test on Channel 2.
5Ch	G	A	Off	R	Enable 8042. Enable timer and keyboard IRQs. Set Video Mode: Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.
5Eh	G	A	G	R	Init PCI devices and motherboard devices. Pass control to video BIOS. Start serial console redirection.
60h	Off	R	R	Off	Initialize memory test parameters.
62h	Off	R	A	Off	Initialize AMI display manager Module. Initialize support code for headless system if no video controller is detected.
64h	Off	A	R	Off	Start USB controllers in chipset.
66h	Off	A	A	Off	Set up video parameters in BIOS data area.
68h	G	R	R	Off	Activate ADM: The display mode is set. Displaying the power-on message next.
6Ah	G	R	A	Off	Initialize language module. Display splash logo.
6Ch	G	A	R	Off	Display Sign on message, BIOS ID and processor information.
6Eh	G	A	A	Off	Detect USB devices.
70h	Off	R	R	R	Reset IDE Controllers.
72h	Off	R	A	R	Displaying bus initialization error messages.
74h	Off	A	R	R	Display Setup Message: The new cursor position has been read and saved. Displaying the Hit Setup message next.
76h	Off	A	A	R	Ensure Timer Keyboard Interrupts are on.
78h	G	R	R	R	Extended background memory test start
7Ah	G	R	A	R	Disable parity and NMI reporting.
7Ch	G	A	R	R	Test 8237 DMA Controller: The DMA page register test passed. Performing the DMA Controller 1 base register test next.
7Eh	G	A	A	R	Init 8237 DMA Controller: The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
80h	R	Off	Off	Off	Enable Mouse and Keyboard: The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
82h	R	Off	G	Off	Keyboard Interface Test: A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
84h	R	G	Off	Off	Check Stuck Key Enable Keyboard: The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
86h	R	G	G	Off	Disable parity NMI: The command byte was written and global data initialization has completed. Checking for a locked key next.
88h	A	Off	Off	Off	Display USB devices.

	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	Hi			Low	
8Ah	A	Off	G	Off	Verify RAM Size: Checking for a memory size mismatch with CMOS RAM data next.
8Ch	A	G	Off	Off	Lock out PS/2 keyboard/mouse if unattended start is enabled.
8Eh	A	G	G	Off	Init Boot Devices: The adapter ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
90h	R	Off	Off	R	Display IDE mass storage devices.
92h	R	Off	G	R	Display USB mass storage devices.
94h	R	G	Off	R	Report the first set of POST Errors To Error Manager.
96h	R	G	G	R	Boot Password Check: The password was checked. Performing any required programming before Setup next.
98h	A	Off	Off	R	Float Processor Initialize: Performing any required initialization before the coprocessor test next.
9Ah	A	Off	G	R	Enable Interrupts 0,1,2: Checking the extended keyboard, keyboard ID, and NUM Lock key next. Issuing the keyboard ID command next.
9Ch	A	G	Off	R	Init FDD Devices. Report second set of POST errors To Error messager.
9Eh	A	G	G	R	Extended background memory test end.
A0h	R	Off	R	Off	Prepare And Run Setup: Error manager displays and logs POST errors. Waits for user input for certain errors. Execute setup.
A2h	R	Off	A	Off	Set Base Expansion Memory Size .
A4h	R	G	R	Off	Program chipset setup options, build ACPI Tables, build INT15h E820h table.
A6h	R	G	A	Off	Set Display Mode.
A8h	A	Off	R	Off	Build SMBIOS table and MP tables.
Aah	A	Off	A	Off	Clear video screen.
Ach	A	G	R	Off	Prepare USB controllers for operating system.
Aeh	A	G	A	Off	One Beep to indicate end of POST. No beep if silent boot is enabled.
000h	Off	Off	Off	Off	POST completed. Passing control to INT 19h boot loader next.

7. Connectors and Jumper Blocks

7.1 Power Connectors

7.1.1 Main Power Connector

The main power supply connection is obtained using the 24-pin connector. The following table defines the pin-outs of the connector.

Table 53. Power Connector Pin-out (J6G1)

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1*	+3.3VDC	Orange	13	+3.3VDC	Orange
	3.3V RS	Orange (24AWG)	14	-12VDC	Blue
2	+3.3VDC	Orange	15	COM	Black
3*	COM	Black	16	PSON#	Green
	COM RS	Black (24AWG)	17	COM	Black
4*	+5VDC	Red	18	COM	Black
	5V RS	Red (24AWG)	19	COM	Black
5	COM	Black	20	Reserved	N.C.
6	+5VDC	Red	21	+5VDC	Red
7	COM	Black	22	+5VDC	Red
8	PWR OK	Gray	23	+5VDC	Red
9	5 VSB	Purple	24	COM	Black
10	+12V3	Yellow			
11	+12V3	Yellow			
12	+3.3VDC	Orange			

Table 54. Auxiliary CPU Power Connector Pin-out (J1B2)

Pin	Signal	18 AWG color	Pin	Signal	18 AWG Color
1	COM	Black	5*	+12V1	White
2	COM	Black		12V1 RS	Yellow (24AWG)
3	COM	Black	6	+12V1	White
4	COM	Black	7	+12V2	Brown
			8*	+12V2	Brown
				12V2 RS	Yellow (24AWG)

7.2 Intel Adaptive Slot

Table 55. Intel Adaptive Slot Pin-Out (J6B2)

Pin-Side B	PCI Spec Signal	Description	Pin-Side A	PCI Spec Signal	Description
1	12V		1	Presnt1#	
2	12V		2	12V	
3	12V		3	12V	
4	GND		4	GND	
5	SMCLK		5	JTAG-TCK	
6	SMDATA		6	JTAG-TDI	
7	GND		7	JTAG-TDO	
8	3.3V		8	JTAG-TMS	
9	JTAG-TRST#		9	3.3V	
10	3.3VAux		10	3.3V	
11	Wake#		11	PERST#	
KEY	KEY		KEY	KEY	
KEY	KEY		KEY	KEY	
12	RSVD		12	GND	
13	GND		13	REFCLK1+	
14	HSOp(0)		14	REFCLK1+	
15	HSOn(0)		15	GND	
16	GND		16	HSIp(0)	
17	Present2#		17	HSIn(0)	
18	GND	1X end	18	GND	
19	HSOp(1)		19	RSVD	
20	HSOn(1)		20	GND	
21	GND		21	HSIp(1)	
22	GND		22	HSIn(1)	
23	HSOp(2)		23	GND	
24	HSOn(2)		24	GND	
25	GND		25	HSIp(2)	
26	GND		26	HSIn(2)	
27	HSOp(3)		27	GND	
28	HSOn(3)		28	GND	
29	GND		29	HSIp(3)	
30	RSVD		30	HSIn(3)	
31	PRSNT2#		31	GND	
32	GND	4X end	32	REFCLK2+	second x4 clock
33	HSOp(4)		33	REFCLK2+	second x4 clock
34	HSOn(4)		34	GND	
35	GND		35	HSIp(4)	
36	GND		36	HSIn(4)	

Pin-Side B	PCI Spec Signal	Description	Pin-Side A	PCI Spec Signal	Description
37	HSOp(5)		37	GND	
38	HSOn(5)		38	GND	
39	GND		39	HSIp(5)	
40	GND		40	HSIn(5)	
41	HSOp(6)		41	GND	
42	HSOn(6)		42	GND	
43	GND		43	HSIp(6)	
44	GND		44	HSIn(6)	
45	HSOp(7)		45	GND	
46	HSOn(7)		46	GND	
47	GND		47	HSIp(7)	
48	PRSNT2#		48	HSIn(7)	
49	GND	8X end	49	GND	
KEY	KEY	Blocks a x16 PCI-Express board	KEY	KEY	and allows a x8 to be used instead
KEY	KEY	Blocks a x16 PCI-Express board	KEY	KEY	
50	-12V		50	12V	
51	+5V		51	INTB#	
52	INTD#		52	+5V	
53	+5V		53	+5V	
54	+5V		54	+5V	
55	INTA#		55	INTC#	
56	GND		56	GND	
57	CLK3		57	REQ3#	
58	GND		58	GND	
59	CLK2		59	GNT3#	
60	GND		60	GND	
61	REQ2#		61	RST#	
62	GND		62	+5V	
63	GND		63	RSVD	
64	CLK1		64	GND	
65	GND		65	GNT2#	
66	REQ1#		66	+3.3V	
67	+3.3V		67	GNT1#	
68	PME2#		68	GND	
69	AD[31]		69	PME1#	
70	AD[29]		70	PME3#	
71	GND		71	AD[30]	
72	AD[27]		72	+3.3V	
73	AD[25]		73	AD[28]	
74	+3.3V		74	AD[26]	

Pin-Side B	PCI Spec Signal	Description	Pin-Side A	PCI Spec Signal	Description
75	C/BE[3]#		75	GND	
76	AD[23]		76	AD[24]	
77	GND		77	AD[22]	
78	AD[21]		78	+3.3V	
79	AD[19]		79	AD[20]	
80	+3.3V		80	AD[18]	
81	AD[17]		81	GND	
82	C/BE[2]#		82	AD[16]	
83	GND		83	PCI-XCAP	
84	IRDY#		84	+3.3V	
85	+3.3V		85	FRAME#	
86	DEVSEL#		86	GND	
87	GND		87	TRDY#	
88	LOCK#		88	GND	
89	PERR#		89	STOP#	
90	+3.3V		90	+3.3V	
91	3.3V		91	SERR#	
92	C/BE[1]#		92	GND	
93	AD[14]		93	PAR	
94	GND		94	AD[15]	
95	AD[12]		95	+3.3V	
96	AD[10]		96	AD[13]	
97	M66EN		97	AD[11]	
98	GND		98	GND	
99	GND		99	AD[09]	
100	AD[08]		100	C/BE[0]#	
101	AD[07]		101	+3.3V	
102	+3.3V		102	AD[06]	
103	AD[05]		103	AD[04]	
104	AD[03]		104	GND	
105	GND		105	AD[02]	
106	AD[01]		106	AD[00]	
107	+3.3V		107	+3.3V	
108	ACK64#		108	REQ64#	
109	+5V		109	+5V	
110	+5V		110	+5V	
111	GND		111	C/BE[7]#	
112	C/BE[6]#		112	C/BE[5]#	
113	C/BE[4]#		113	GND	

Pin-Side B	PCI Spec Signal	Description	Pin-Side A	PCI Spec Signal	Description
114	GND		114	PAR64	
115	AD[63]		115	AD[62]	
116	AD[61]		116	3.3V	
117	3.3V		117	AD[60]	
118	AD[59]		118	AD[58]	
119	AD[57]		119	GND	
120	GND		120	AD[56]	
121	AD[55]		121	AD[54]	
122	AD[53]		122	3.3V	
123	GND		123	AD[52]	
124	AD[51]		124	AD[50]	
125	AD[49]		125	GND	
126	3.3V		126	AD[48]	
127	AD[47]		127	AD[46]	
128	AD[45]		128	GND	
129	GND		129	AD[44]	
130	AD[43]		130	AD[42]	
131	AD[41]		131	3.3V	
132	GND		132	AD[40]	
133	AD[39]		133	AD[38]	
134	AD[37]		134	GND	
135	3.3V		135	AD[36]	
136	AD[35]		136	AD[34]	
137	AD[33]		137	GND	
138	GND		138	AD[32]	
139	Type1	Type(1:0)	139	GND	
		(1U)00 = PCI-Express,			
		(1U)01 = PCI			
		(1U)10 = N/A			
		(1U)11 = N/A			
140	Type0	(2U)00=2xPCI-Express+PCI	140	Size	0=1U, 1=2U
		(2U)01=3x PCI			
		(2U)10=PXH 3 PCI-X			
		(2U)11=No Riser			
	Special Riser Signals				

7.3 I²C Header

Table 56. HSBP Header Pin-out (J9E1)

Pin	Signal Name	Description
1	HR_SMB_5V_DAT	Data Line
2	GND	GROUND
3	HR_SMB_5V_CLK	Clock Line
4	GND	GROUND

7.4 IDE Connector

The board provides one 40-pin ATA-100 IDE connector.

Table 57. ATA 40-pin Connector Pin-out (J7J2)

Pin	Signal Name	Pin	Signal Name
1	RESET#	2	GND
3	IDE_DD7	4	IDE_DD8
5	IDE_DD6	6	IDE_DD9
7	IDE_DD5	8	IDE_DD10
9	IDE_DD4	10	IDE_DD11
11	IDE_DD3	12	IDE_DD12
13	IDE_DD2	14	IDE_DD13
15	IDE_DD1	16	IDE_DD14
17	IDE_DD0	18	IDE_DD15
19	GND	20	KEY
21	IDE_DMAREQ	22	GND
23	IDE_IOW#	24	GND
25	IDE_IOR#	26	GND
27	IDE_IORDY	28	GND
29	IDE_DMAACK#	30	GND
31	IRQ_IDE	32	Test Point
33	IDE_A1	34	DIAG
35	IDE_A0	36	IDE_A2
37	IDE_DCS0#	38	IDE_DCS1#
39	IDE_HD_ACT#	40	GND

7.4.1 OEM RMC Connector

Table 58. RMC Header Pin-out (J9D1)

Pin	Signal Name	Description
1	MBMC_SMC_PHL_DAT	Data Line
2	GND	GROUND
3	MBMC_SMC_PHL_CLK	Clock Line
4	P5V_STBY	POWER
5	POST_STATUS_N	
6	FP_RST_BTN_N	
7	P5V	
8	FP_PWR_BTN_N	

7.5 Front Panel Connector

A standard SSI 34-pin header is provided to support a system front panel. The header contains reset, NMI, power control buttons, and LED indicators. The following table details the pin-out of this header.

Table 59. Front Panel 34-Pin Header Pin-out (J9J3)

Signal Name	Pin	Signal Name	Pin
P5V_STB	1	P5V_STB	2
KEY	3	NC	4
GND	5	NC	6
P5V	7	NC	8
HDD_LED#	9	NC	10
FP_PWR_BTN_N	11	LAN1_ACT_N	12
GND	13	LAN1_LINK_UP_N	14
FP_RST_BTN_N	15	NC	16
RESET switch (GND)	17	NC	18
NC	19	ICH Intruder HDR	20
GND	21	LAN2_ACT_N	22
NMI switch#	23	LAN2_LINK_UP_N	24
Key	25	Key	26
P5V_STB	27	NC	28
FP_ID_LED_N	29	NC	30
FP_ID_BTN_N	31	P5V	32
GND	33	NC	34

Note: NC (No Connect) in this project

7.6 I/O Connectors

7.6.1 VGA Connector

The following table details the pin-out of the VGA connector. This connector is combined with COM1 connector.

Table 60. VGA Connector Pin-out (J2A1)

Signal Name	Pin	Signal Name	Pin
RED	B1	Fused VCC (+5V)	B9
GREEN	B2	GND	B10
BLUE	B3	NC	B11
NC	B4	DDCDAT	B12
GND	B5	HSY	B13
GND	B6	VSY	B14
GND	B7	DDCCLK	B15
GND	B8		

Note: NC (No Connect) in this project

7.6.2 NIC Connectors

The Intel® Server Board SE7230NH1-E supports two NIC RJ45 connectors. The following tables detail the pin-out of the connector.

Table 61. NIC1-Intel® 82541PI (10/100/1000) Connector Pin-out (J5A2)

Signal Name	Pin	Signal Name	Pin
LGND_LAN1	1	LAN1_TRDN3	10
LAN1_TRDP0	2	LAN1_LINK_UP_N	11
LAN1_TRDN0	3	LAN1_ACT_N	12
LAN1_TRDP1	4	9	LAN1_TRDP3
LAN1_TRDN1	5	LAN1_LINK100_N	13
P1V8_STB_LAN1	6	P3V3_STB	14
LAN1_TRDP2	7	LAN1_LINK1000_N	15
LAN1_TRDN2	8	LINK100_L	16

Table 62. NIC2- Intel® 82573E/V (10/100/1000) Connector Pin-out (JA4A1)

Signal Name	Pin	Signal Name	Pin
P1V8_STB_LAN2	1	LAN2_TRDN0	10
LAN2_TRDN2	2	LAN2_TRDP0	11
LAN2_TRDP2	3	P1V8_STB_LAN2	12
LAN2_TRDP1	4	LAN2_LINK100_N	13
LAN2_TRDN1	5	LAN2_LINK1000_N	14
P1V8_STB_LAN2	6	LAN2_LINK_UP_N	15
P1V8_STB_LAN2	7	LAN2_ACT_N	16

Signal Name	Pin	Signal Name	Pin
LAN2_TRDP3	8	GND_CHASSIS	17
LAN2_TRDN3	9	GND_CHASSIS	18

7.6.3 ATA-100 Connector

7.6.4 SATA Connectors

Intel® ICH7R integrated a SATA controller with four SATA ports output. The pin-out for these four connectors is listed below.

Table 63. SATA Connector Pin-out (J9G2, J9H1, J9J2, J8J1)

Pin	Signal Name
1	GND
2	SATA0_TX_P
3	SATA0_TX_N
4	GND
5	SATA0_RX_N
6	SATA0_RX_P
7	GND

7.6.5 Floppy Controller Connector

The board provides a standard 34-pin interface to the floppy drive controller. The following tables detail the pin-out of the 34-pin floppy connector.

Table 64. Legacy 34-pin Floppy Connector Pin-out (J7J3)

Signal Name	Pin	Signal Name	Pin
GND	1	FDDENSEL	2
GND	3	Unused	4
KEY	5	FDDRATE0	6
GND	7	FDINDEX#	8
GND	9	FDMTR0#	10
GND	11	FDR1#	12
GND	13	FDR0#	14
GND	15	FDMTR1#	16
Unused	17	FDDIR	18
GND	19	FDSTEP#	20
GND	21	FDWDATA#	22
GND	23	FDWGATE#	24
GND	25	FDTRK0#	26
Unused	27	FLWP#	28
GND	29	FRDATA#	30
GND	31	FHDSEL#	32
GND	33	FDSKCHG#	34

7.6.6 Serial Port Connectors

One serial port is provided on the Intel® Entry Server Board SE7230NH1-E.

- A standard, external DB9 serial connector is located on the back edge of the baseboard to supply a Serial A interface. This connector is combined with VGA connector (J8A1)

Table 65. External DB9 Serial A Port Pin-out (J2A1)

Signal Name	Pin	Signal Name	Pin
DCD-P	T1	DSR-P	T6
RXD-P	T2	RTS-P	T7
TXD-P	T3	CTS-P	T8
DTR-P	T4	RI-P	T9
GND	T5		

7.6.7 Keyboard and Mouse Connector

Two PS/2 ports are provided for use by a keyboard and a mouse. The following table details the pin-out of the PS/2 connectors.

Table 66. Keyboard and Mouse PS/2 Connectors Pin-out (J1A1)

PS/2 Connectors	Pin	Signal Name
Keyboard	K1	RKBDATA
	K2	NC
	K3	GND
	K4	P5V_KB_MS
	K5	RKBCLK
	K6	NC
Mouse	M1	MSEDATA
	M2	NC
	M3	GND
	M4	P5V_KB_MS
	M5	RMSCLK
	M6	NC

7.6.8 USB Connector

The following table provides the pin-out for the dual external USB connectors. This connector is combined with an RJ45 (connected to COM1 signals).

Table 67. USB Connectors Pin-out (J5A2)

Pin	Signal Name
U1	GND
U2	USB_B5_P
U3	USB_B5_N
U4	VCC_USB5
U5	GND
U6	USB_B4_P
U7	USB_B4_N
U8	VCC_USB4

A header on the server board provides an option to support one additional USB connector. The pin-out of the header is detailed in the following table.

Table 68. Optional USB Connection Header Pin-out (J9F2)

Signal Name	Pin	Signal Name	Pin
Fused VCC (+5V /w over current monitor of both port 1)	1	Fused VCC (+5V /w over current monitor of both port 0)	2
USB_B2_N	3	USB_B1_N	4
USB_B2_P	5	USB_B1_P	6
GND	7	GND	8
Key	9	NC	10

7.7 Fan Headers

There are four general purpose (system) fan headers which support a pedestal chassis configuration, two 3-pin fan headers and two 4-pin fan headers (JP5J1, JP5J2, JP7A1, and JP6A1). These fan headers have the same pin-out and are detailed below.

Table 69. Three-pin Fan Headers Pin-out (Front J6J1, Rear J3B1)

Pin	Signal Name	Type	Description
1	Ground	Power	GROUND is the power supply ground
2	Fan Power	Power	Fan Power with FAN_SPEED_CNTL1 (Fan speed control)
3	Fan Tach	Out	FAN_TACH signal is connected to the Heceta* to monitor the FAN speed.

Table 70. Four-pin Fan Headers Pin-out (Front J5J2, Rear J4B1, CPU J2D1)

Pin	Signal Name	Type	Description
1	Ground	Power	GROUND is the power supply ground
2	Fan Power	Power	Fan Power
3	Fan Tach	Out	FAN_TACH signal is connected to the Heceta* to monitor the FAN speed.
4	PWM	Control	Pulse Width Modulation – Fan Speed Control signal

The Intel® Entry Server Board SE7230NH1-E LX SKU also includes four 8-pin fan headers specifically designed to support an Intel 1U high-density chassis configuration (J6J1, J6J2, J6J3, and J6J4). These fan headers have the same pin-out and are detailed below.

Table 71. Eight-pin Fan Header Pin-out (**Right to Left – J5J1, J4J1, J4J3, J4J2**)

Pin	Signal Name	Type	Description
1	Fan Power	Power	Fan Power with FAN_SPEED_CNTL1 (Fan speed control)
2	Fan Tach	Out	FAN_TACH signal is connected to the Super I/O*/Heceta* to monitor the FAN speed.
3	Ground	Power	GROUND is the power supply ground
4	NC		
5	Ground	Power	GROUND is the power supply ground
6	Ground	Power	GROUND is the power supply ground
7	Fan Tach	Out	FAN_TACH signal is connected to the Super I/O*/Heceta* to monitor the FAN speed.
8	Fan Power	Power	Fan Power with FAN_SPEED_CNTL1 (Fan speed control)

7.8 Miscellaneous Headers and Connectors

7.8.1 Chassis Intrusion Header

A 1x2 pin header J9A1 is used in chassis that support a chassis intrusion switch. This header is monitored by the mBMC. The pinout definition for this header is found in the following table.

Table 72. Intrusion Cable Connector (J9A1)Pin-Out

Pin	Signal Name
1	INTRUDER_N
2	GND

7.8.2 Hard Drive Activity LED Header

There is a 1x2 pin Header for HDD LED Connection. This jumper reserves for PCI add-in card that supports the SCSI or SATA interface with external HDD LED activity cable.

Table 73. HDD LED Header (J1E1) Pin-Out

Pin	Signal Name
1	HDD_LED_ACT_N
2	NC

7.8.3 Back Panel I/O Connectors

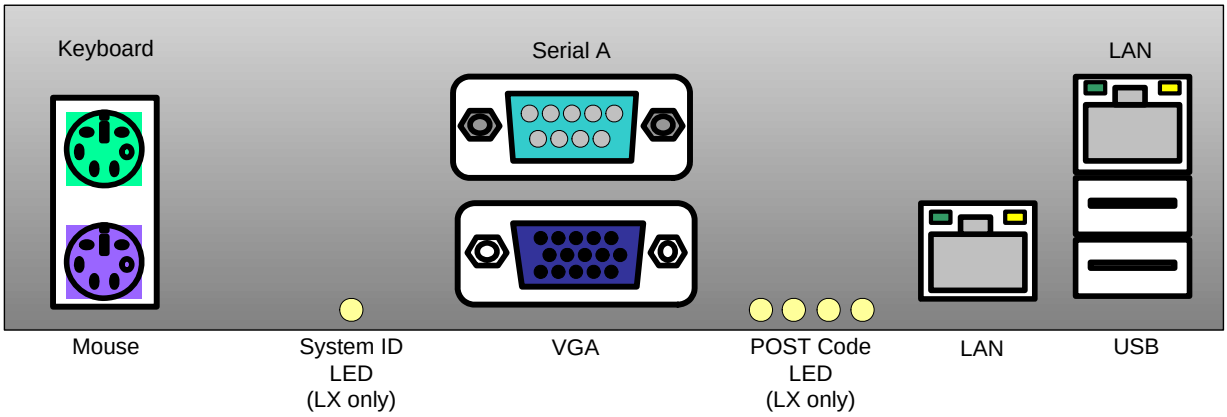


Figure 8. Back Panel I/O Connections (not to scale)

7.8.4 System ID LED – LX SKU Only

A front panel button will toggle the System ID LED on and off.

- The System ID LED will be blue
- The System ID LED will operate on stand-by voltage

7.8.5 POST Code LEDs

Four POST code LEDs will display POST code progression activities using hexadecimal format, read from the least significant bit to the most significant bit. See section 6.2 (Diagnostic LEDs) later in this document for POST code detection schema.

7.9 Jumper Blocks

This section describes configuration jumper options on the Intel® Entry Server Board SE7230NH1-E.

7.9.1 Clear CMOS and System Maintenance Mode Jumpers

Both CMOS Clear and System Maintenance Mode jumpers consist of 2-pin headers (CMOS Clear = J9G3, Config Mode = J9H3) located just beside the Front Panel and SATA 1 connectors. The Intel® Entry Server Board SE7230NH1-E provides a total of two 2-pin jumper blocks that are used to perform Clearing of NVRAM, System BIOS Recovery and System Maintenance Mode options. The factory defaults are set to Normal mode for each function.

The following tables describe each jumper option.

Table 74. System Maintenance Mode (J9H3)

Name	Pin – Pin	Function	Description
Normal	1-2	***Normal Operation***	Allows normal system operation with correct BIOS settings. System will POST normally.
Config (Maintenance)	2-3	***Machine Config Mode***	Maintenance mode overrides incorrect BIOS settings which would otherwise prohibit normal POST with safe settings for specific HW configuration.
Recovery Boot	Off	***BIOS Recovery Mode***	Used to recover from a corrupted BIOS. Bootable media with a valid BIOS ROM and

Table 75. Clear CMOS Jumper Options (J9G3)

Name	Pin – Pin	Function	Description
Normal	1-2	***Normal Operation***	Jumper in normal position allows system to successfully POST and boot to OS environment. BIOS settings are maintained intact.
CMOS Clear	2-3	***Clears CMOS (NVRAM)***	Jumper in CLEAR position initiates clear of NVRAM following POST. System message confirms CMOS clear operation successfull. This setting enforces default BIOS settings which can be changed by entering setup via F2, then exiting setup via F10 and saving changes.

8. Absolute Maximum Ratings

Operating the board at conditions beyond those shown in the following table may cause permanent damage to the system. The table is provided for stress testing purposes only. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 76. Absolute Maximum Ratings

Operating Temperature	5 °C to 50 °C [1]
Storage Temperature	-55 °C to +150 °C
Voltage on any signal with respect to ground	-0.3 V to Vdd + 0.3V [2]
3.3 V Supply Voltage with Respect to ground	-0.3 V to 3.63 V
5 V Supply Voltage with Respect to ground	-0.3 V to 5.5 V

Notes:

1. **Chassis design must provide proper airflow to avoid exceeding the processor maximum case temperature.**
2. **VDD means supply voltage for the device**

8.1 Mean Time Between Failures (MTBF) Test Results

This section provides results of MTBF testing done by a third party testing facility. MTBF is a standard measure for the reliability and performance of the board under extreme working conditions. For the Intel® Entry Server Board SE7230NH1-E, MTBF was measured at **TBD** hours at **35** degrees Centigrade.

9. Design and Environmental Specifications

9.1 Intel® Entry Server Board SE7230NH1-E Power Budget

The following table shows the power consumed on each supply line for the Intel® Entry Server Board SE7230NH1-E that is configured with one processor (128W max). This configuration includes four 1 GB DDR2 DIMMs stacked burst at 70% max. The numbers provided in the table should be used for reference purposes only. Different hardware configurations will produce different numbers. The numbers in the table reflect a common usage model operating at a higher than average stress levels.

Table 77. The Board Power Budget

Watts			Power Supply Rail Voltages						Units
			AMPS						
Functional Unit	**Utilization**	**Power**	**3.3V**	**5.V**	**12.V**	**12V VRM**	**-12v**	**5VSB**	
Base board Input Totals		290.73W	6.26W	8.47W	6.38W	9.28W	0.05W	1.67	
Base board Discrete Totals	50%	32.02W	1.51	1.17	0.00	0.00	0.00	0.00	
Base board Converters	Efficiency	41.90W	3.24	7.29	0.00	9.28	0.00	1.67	
Base board config Totals		246.80W	1.52	0.00	6.38	0.00	0.05	0.00	
System Components		45.12W	0.00	2.40	2.76	0.00	0.00	0.00	
System Totals		335.85W	6.26	10.87	9.14	9.28	0.05	1.67	Amps
3.3v/5v Combined Power									
Power Supply Requirements – 1U		300W	14A	18A	Max 12V+ 12V VRM		0.5A	2A	
		350W peak							
3.3V/5V Combined Power		100W	1Amin	1Amin	2Amin	2Amin	0Amin	1Amin	

9.2 Power Supply Specifications

This section provides power supply design guidelines for the base board, including voltage and current specifications, and power supply on/off sequencing characteristics.

Table 78. The Board Power Supply Voltage Specification

Parameter	Tolerance	Min	Nom	Max	Units
+ 3.3V	- 5% / +5%	+3.14	+3.30	+3.46	Vrms
+ 5V	- 5% / +5%	+4.75	+5.00	+5.25	Vrms
+ 12V	- 5% / +5%	+11.40	+12.00	+12.60	Vrms
- 12V	- 10% / +10%	-11.40	-12.00	-13.08	Vrms
+ 5VSB	- 5% / +5%	+4.75	+5.00	+5.25	Vrms

9.2.1 Power Timing Requirements

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (Tvout_rise) within 5 to 70ms, except for 5VSB - it is allowed to rise from 1.0 to 70ms. The +3.3V, +5V and +12V output voltages should start to rise approximately at the same time**. All outputs must rise monotonically**. The +5V output needs to be greater than the +3.3V output during any point of the voltage rise. The +5V output must never be greater than the +3.3V output by more than 2.25V. Each output voltage shall reach regulation within 50ms (Tvout_on) of each other during turn on of the power supply. Each output voltage shall fall out of regulation within 400msec (Tvout_off) of each other during turn off. Refer to the table below for the timing requirements for the power supply being turned on and off via the AC input, with PSON held low and the PSON signal, with the AC input applied.

Table 79. Output Voltage Timing

Item	Description	MIN	MAX	UNITS
Tvout_rise	Output voltage rise time from each main output.	5.0 *	70 *	msec
Tvout_on	All main outputs must be within regulation of each other within this time.		50	msec
T vout_off	All main outputs must leave regulation within this time.		400	msec

The 5VSB output voltage rise time will be from 1.0ms to 25.0ms

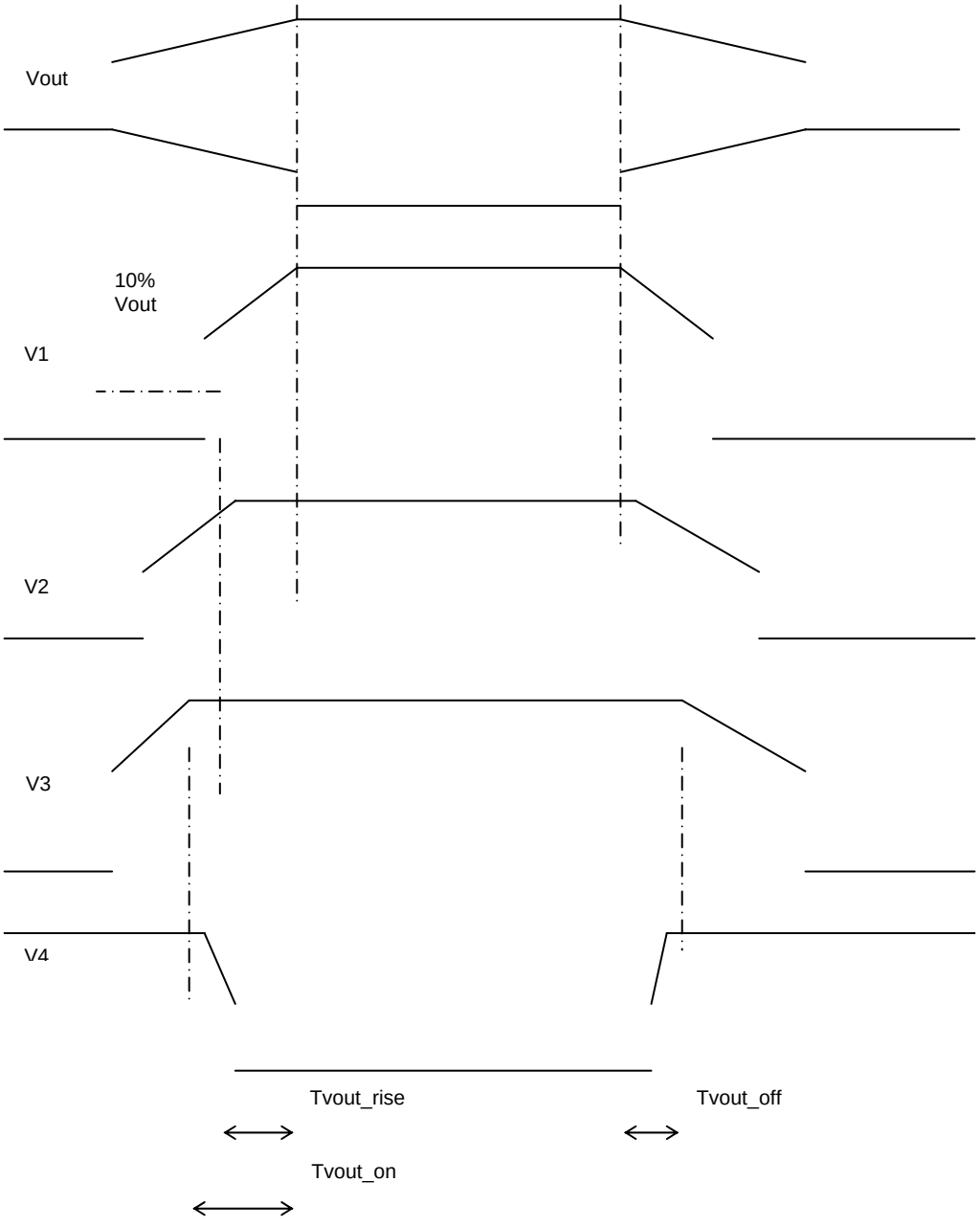


Figure 9. Output Voltage Timing

Table 80. Turn On/Off Timing

Item	Description	Min	Max	Units
Tsb_on_delay	Delay from AC being applied to 5VSB being within regulation.		1500	msec
T ac_on_delay	Delay from AC being applied to all output voltages being within regulation.		2500	msec
Tvout_holdup	Time all output voltages stay within regulation after loss of AC.	21		msec
Tpwok_holdup	Delay from loss of AC to de-assertion of PWOK.	20		msec
Tpson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5	400	msec
T pson_pwok	Delay from PSON# deactive to PWOK being de-asserted.		50	msec
Tpwok_on	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	1000	msec
T pwok_off	Delay from PWOK de-asserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits.	1	200	msec
Tpwok_low	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		msec
Tsb_vout	Delay from 5VSB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	msec
T5VSB_holdup	Time the 5VSB output voltage stays within regulation after loss of AC.	70		msec

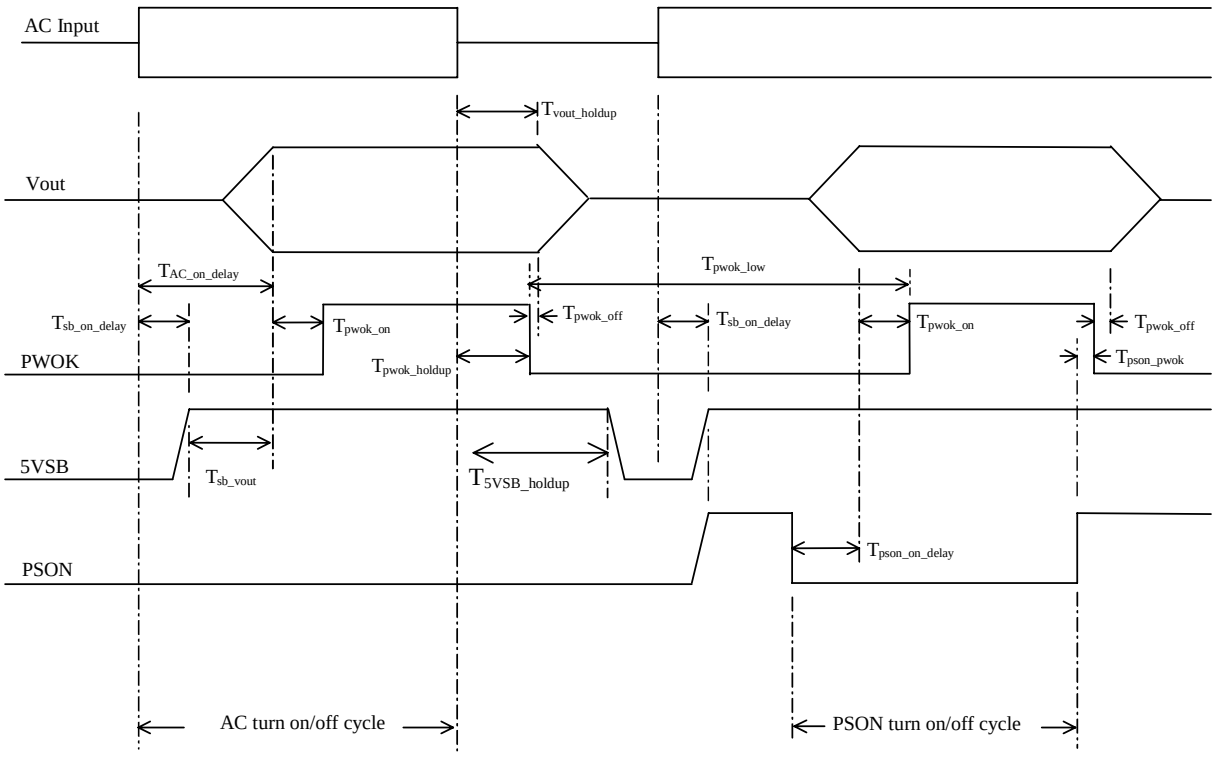


Figure 10. Turn On/Off Timing (Power Supply Signals)

9.2.2 Dynamic Loading

The output voltages shall remain within limits specified for the step loading and capacitive loading specified in the table below. The load transient repetition rate shall be tested between 50Hz and 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the MAX load conditions.

Table 81. Transient Load Requirements

Output	Δ Step Load Size (See note 2)	Load Slew Rate	Test capacitive Load
+3.3V	5.0A	0.25 A/μsec	250 μF
+5V	6.0A	0.25 A/μsec	400 μF
12V	9.0A	0.25 A/μsec	500 μF
+5VSB	0.5A	0.25 A/μsec	20 μF

Notes

1. **Step loads on each 12V output may happen simultaneously.**
2. **For Load Range 2 (light system loading), the tested step load size should be 60% of those listed.**

9.2.3 AC Line Transient Specification

AC line transient conditions will be defined as “sag” and “surge” conditions. “Sag” conditions are also commonly referred to as “brownout”; these conditions will be defined as the AC line voltage dropping below nominal voltage conditions. “Surge” will be defined to refer to conditions when the AC line voltage rises above nominal voltage.

The power supply shall meet the requirements under the following AC line sag and surge conditions.

Table 82. AC Line Sag Transient Performance

AC Line Sag				
Duration	**Sag**	**Operating AC Voltage**	**Line Frequency**	**Performance Criteria**
Continuous	10%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance.
0 to 1 AC cycle	100%	Nominal AC Voltage ranges	50/60Hz	No loss of function or performance.
> 1 AC cycle	>10%	Nominal AC Voltage ranges	50/60Hz	Loss of function acceptable, self recoverable.

Table 83. AC Line Surge Transient Performance

AC Line Surge				
Duration	**Surge**	**Operating AC Voltage**	**Line Frequency**	**Performance Criteria**
Continuous	10%	Nominal AC Voltages	50/60Hz	No loss of function or performance.
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60Hz	No loss of function or performance.

9.2.4 AC Line Fast Transient (EFT) Specification

The power supply shall meet the *EN61000-4-5* directive and any additional requirements in *IEC1000-4-5:1995* and the Level 3 requirements for surge-withstand capability, with the following conditions and exceptions:

- These input transients must not cause any out-of-regulation conditions, such as overshoot and undershoot, nor must it cause any nuisance trips for any of the power supply protection circuits.
- The surge-withstand test must not produce damage to the power supply.
- The supply must meet surge-withstand test conditions under maximum and minimum DC-output load conditions.

9.3 Product Regulatory Compliance

9.3.1 Product Safety Compliance

The Server Board SE7520JR2 complies with the following safety requirements:

- UL60950 – CSA 60950(USA / Canada)
- EN60950 (Europe)
- IEC60950 (International)
- CB Certificate and Report, IEC60950 (report to include all country national deviations)
- GOST R 50377-92 – Listed on one System License (Russia)
- Belarus License – Listed on System License (Belarus)
- CE - Low Voltage Directive 73/23/EEE (Europe)
- IRAM Certification (Argentina)

9.3.2 Product EMC Compliance – Class A Compliance

Note: Legally the product is required to comply with Class A emission requirements as it is intended for a commercial type market place. Intel targets 10db margin to Class A Limits

The Intel® Server Board SE7520JR2 has been has been tested and verified to comply with the following electromagnetic compatibility (EMC) regulations when installed a compatible Intel® host system. For information on compatible host system(s) refer to Intel's Server Builder Web site or contact your local Intel representative.

- FCC /ICES-003 - Emissions (USA/Canada) Verification
- CISPR 22 – Emissions (International)
- EN55022 - Emissions (Europe)
- EN55024 - Immunity (Europe)
- CE – EMC Directive 89/336/EEC (Europe)
- AS/NZS 3548 Emissions (Australia / New Zealand)
- BSMI CNS13438 Emissions (Taiwan)
- GOST R 29216-91 Emissions - Listed on one System License (Russia)
- GOST R 50628-95 Immunity –Listed on one System License (Russia)
- Belarus License – Listed on one System License (Belarus)
- RRL MIC Notice No. 1997-41 (EMC) and 1997-42 (EMI) (Korea)

9.3.3 Certifications / Registrations / Declarations

- UL Certification (US/Canada)
- CE Declaration of Conformity (CENELEC Europe)
- FCC/ICES-003 Class A Attestation (USA/Canada)
- C-Tick Declaration of Conformity (Australia)
- MED Declaration of Conformity (New Zealand)
- BSMI Certification (Taiwan)
- GOST – Listed on one System License (Russia)
- Belarus – Listed on one System License (Belarus)
- RRL Certification (Korea)
- Ecology Declaration (International)

9.3.4 Restrictions of Hazardous Substances (RoHS) Compliance

Intel has a system in place to restrict use of banned substances per in accordance to the European Directive 2002/95/EC. Compliance is based on materials banned in the RoHS Directive are either (1) below all applicable substance threshold limits or (2) an approved/pending RoHS exemption applies. (Note: RoHS implementing details are not fully defined and may change.) Threshold limits and banned substances are noted as follows:

Quantity limit of 0.1% by mass (1000 PPM) for: Lead; Mercury; Hexavalent Chromium; Polybrominated Biphenyls Diphenyl Ethers (PBDE); and Quantity limit of 0.01% by mass (100 PPM) for Cadmium

9.3.5 Product Regulatory Compliance Markings

This product is marked with the following Product Certification Markings:

Table 84. Product Certification Markings

Regulatory Compliance	Country	Marking
UL Mark	USA/Canada	
CE Mark	Europe	
FCC Marking (Class A)	USA	This device complies with Part 15 of the FCC Rules. Operation of this device is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation. Manufactured by Intel Corporation
EMC Marking (Class A)	Canada	CANADA ICES-003 CLASS A CANADA NMB-003 CLASSE A
BSMI Marking (Class A)	Taiwan	 警告使用者： 這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策
RRL MIC Mark	Korea	

9.4 Electromagnetic Compatibility Notices

9.4.1 FCC (USA)

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124-6497
1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates,

uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to an outlet on a circuit other than the one to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment. The customer is responsible for ensuring compliance of the modified product.

Only peripherals (computer input/output devices, terminals, printers, etc.) that comply with FCC Class A or B limits may be attached to this computer product. Operation with noncompliant peripherals is likely to result in interference to radio and TV reception.

All cables used to connect to peripherals must be shielded and grounded. Operation with cables, connected to peripherals that are not shielded and grounded may result in interference to radio and TV reception.

9.4.2 Industry Canada (ICES-003)

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: "Apparelis Numériques", NMB-003 édictee par le Ministre Canadian des Communications.

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled: "Digital Apparatus," ICES-003 of the Canadian Department of Communications.

9.4.3 Europe (CE Declaration of Conformity)

This product has been tested in accordance too, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE Mark to illustrate its compliance.

9.4.4 Taiwan Declaration of Conformity (BSMI)

警告使用者：
這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策

The BSMI Certification Marking and EMC warning is located on the outside rear area of the product.

9.4.5 Korean Compliance (RRL)

1. 기기의 명칭(모델명) :
2. 인증번호 :
3. 인증받은 자의 상호 :
4. 제조년월일:
5. 제조자/제조국가 :

English translation of the notice above:

Type of Equipment (Model Name): On License and Product

Certification No.: On RRL certificate. Obtain certificate from local Intel representative

Name of Certification Recipient: Intel Corporation

Date of Manufacturer: Refer to date code on product

Manufacturer/Nation: Intel Corporation/Refer to country of origin marked on product

9.4.6 Australia / New Zealand

This product has been tested and complies with AS/NZS 3548. The product has been marked with the C-Tick mark to illustrate compliance.

9.5 Calculated Mean Time Between Failures (MTBF)

The MTBF (Mean Time Between Failures) for the Intel® Entry Server Board SE7230NH1-E as configured from the factory is shown in the table below.

Table 85. MTBF Data

Product Code	Calculated MTBF	Operating Temperature
Intel® Entry Server Board SE7230NH1	282569 Hours	35 degrees C
Intel® Entry Server Board SE7230NH1	111326 Hours	55 degrees C
Intel® Entry Server Board SE7230NH1LX	265866 Hours	35 degrees C
Intel® Entry Server Board SE7230NH1LX	104745 Hours	55 degrees C

9.6 Mechanical Specifications

The following figure shows the Intel® Entry Server Board SE7230NH1-E mechanical drawing. This drawing will be updated in a future revision of this document.

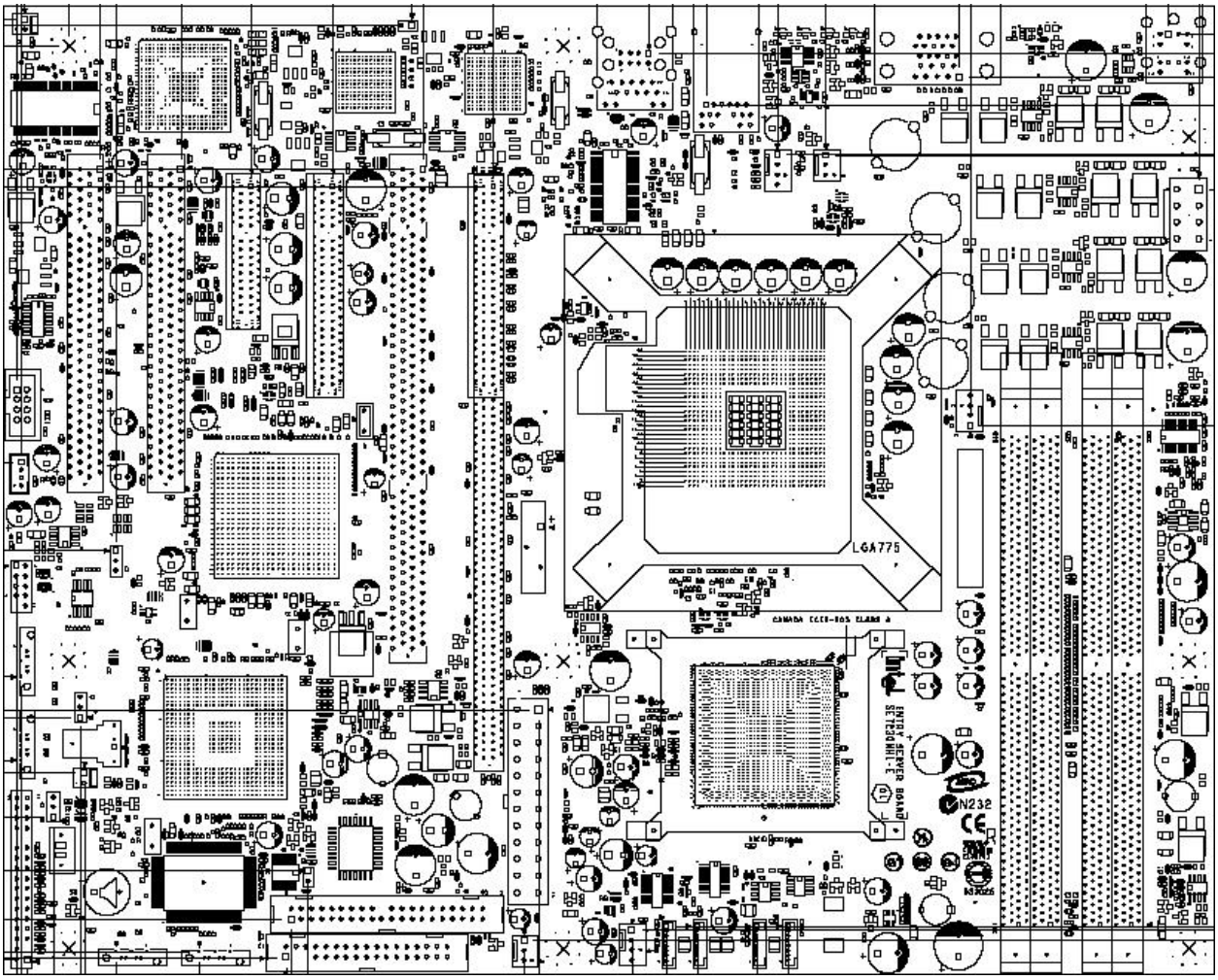


Figure 11. Intel® Entry Server Board SE7230NH1-E Mechanical Drawing

The following figures show the I/O shield mechanical drawings for use in pedestal mount applications such as the Intel® Server Chassis SC5200 for both SKUs (Intel® Entry Server Board SE7230NH1-E and Intel® Entry Server Board SE7230NH1-E (LX).

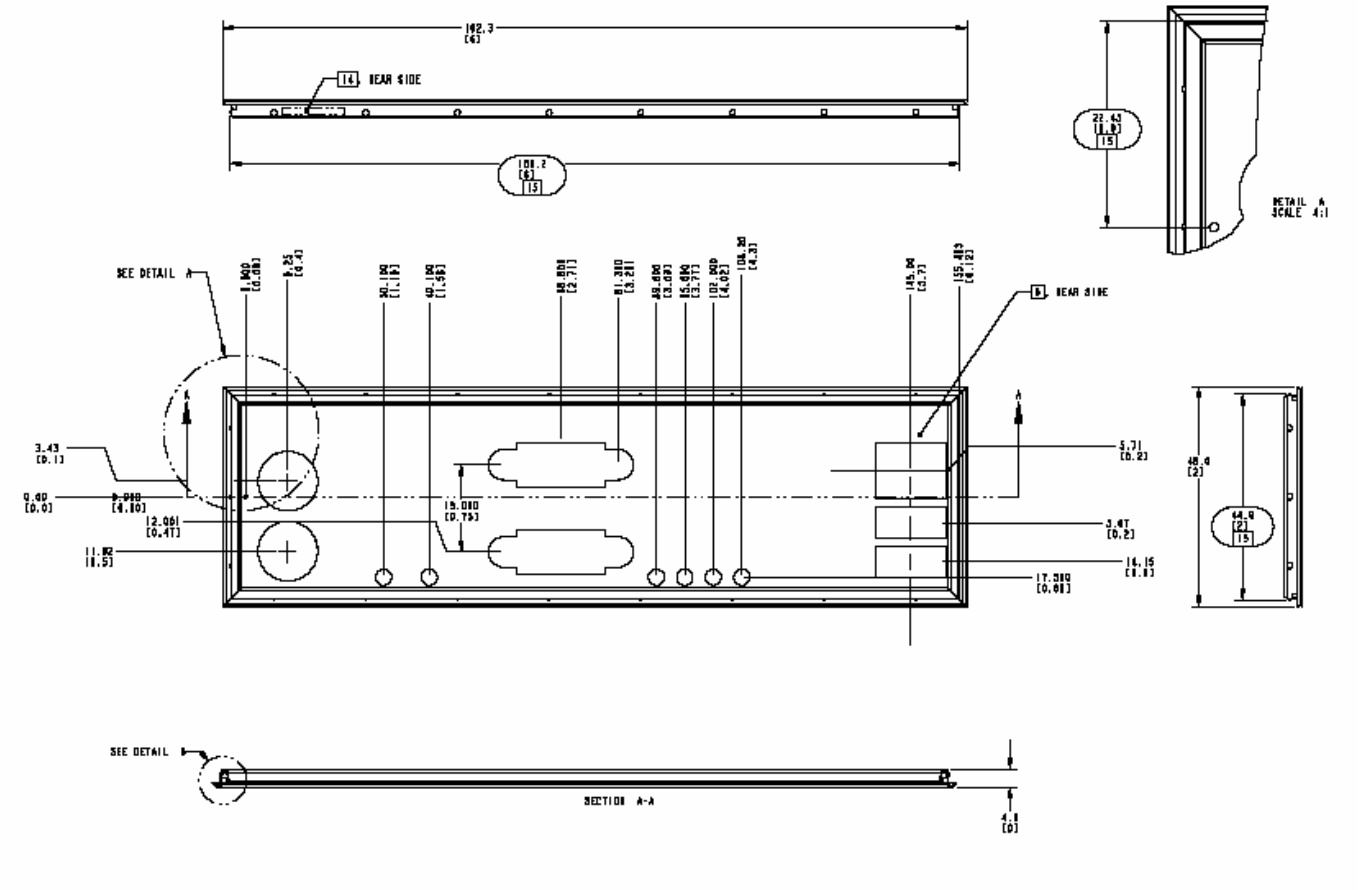


Figure 12. SKU 1 Pedestal Mount I/O Shield Mechanical Drawing

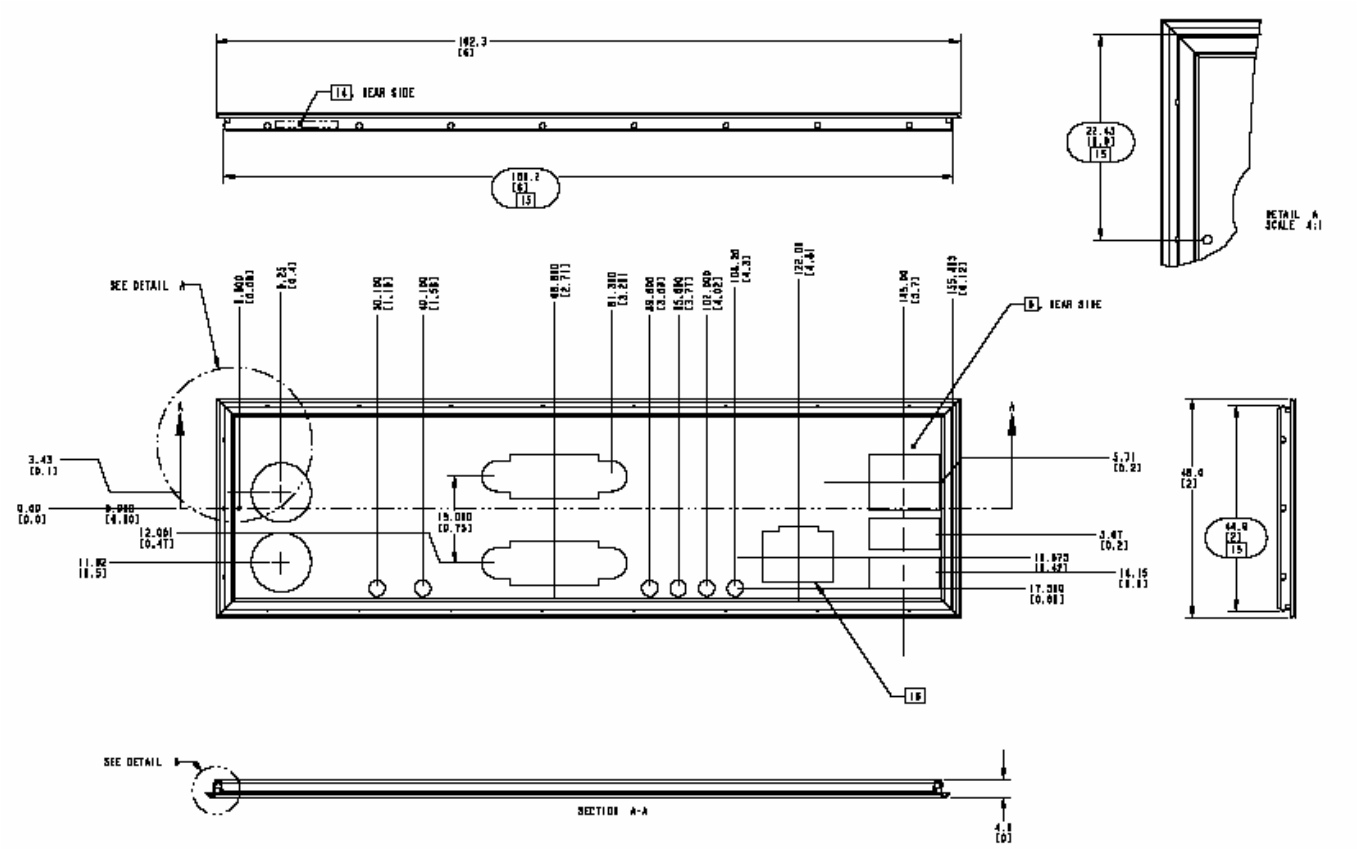


Figure 13. SKU 2 Pedestal Mount I/O Shield Mechanical Drawing

10. Hardware Monitoring

10.1 Monitored Components

The Intel® Entry Server Board SE7230NH1-E has an integrated Heceta* chip that is responsible for hardware monitoring. The Heceta* chip provides basic server hardware monitoring which alerts a system administrator if a hardware problem occurs on the board. The NS Super I/O* PC8374LOIBU and SMsC LP47M182NR have implemented some FAN speed control/monitor pins. Below is a table of monitored headers and sensors on the board.

Table 86. Monitored Components

Item		Description	
Voltage	P_VCC (PIN #24)	Monitors processor voltage	Heceta*
	P12V (PIN #21)	Monitors +12Vin for system +12V supply	Heceta*
	P1V8 (PIN #22)	Monitors 1.8V DDRII power	Heceta*
	P5V (PIN #20)	Monitors +5V	Heceta*
Fan Speed	PWM1 (PIN #24)	Controls system front fans (JP5J1,JP5J2,JP7A1,JP6A1,J6J3,J6J1,J6J4,J6J2)	Heceta*
	PWM2 (PIN #10)	Controls CPU fans (J7A1)	Heceta*
	PWM3 (PIN #13)	N/A	Heceta*
	TACH1 (PIN #11)	Monitors CPU fan (J7A1)	Heceta*
	TACH2 (PIN #12)	Monitors SYS FAN_3 (JP5J1)	Heceta*
	TACH3 (PIN #9)	Monitors SYS FAN_4 (JP5J2)	Heceta*
	FANIN0 (PIN #66)	Monitors SYS FAN_2 (JP7A1) / SYS FAN_5A (J6J1)	Super I/O*
	FANIN1 (PIN #81)	Monitors SYS FAN_1 (JP6A1) / SYS FAN_5B (J6J1)	Super I/O*
	FANIN2 (PIN #77)	Monitors SYS FAN_6A (J6J2)	Super I/O*
	FANIN3 (PIN #76)	Monitors SYS FAN_6B (J6J2)	Super I/O*
	FANIN4 (PIN #75)	Monitors SYS FAN_8A (J6J4)	Super I/O*
	FANIN5 (PIN #83)	Monitors SYS FAN_8B (J6J4)	Super I/O*
	FANIN6 (PIN #36)	Monitors SYS FAN_7A (J6J3)	Super I/O*
	FANIN7 (PIN #9)	Monitors SYS FAN_7B (J6J3)	Super I/O*
Temperature	H_THEMP_DA/C	Monitors processor temperature	Heceta*

10.1.1 Fan Speed Control

The BIOS is configured to manage the fan control. Changes to the fan control is currently not supported with the Intel® ToolKit (iTK) and the Intel® Server **Board SE7230NH1-E.**

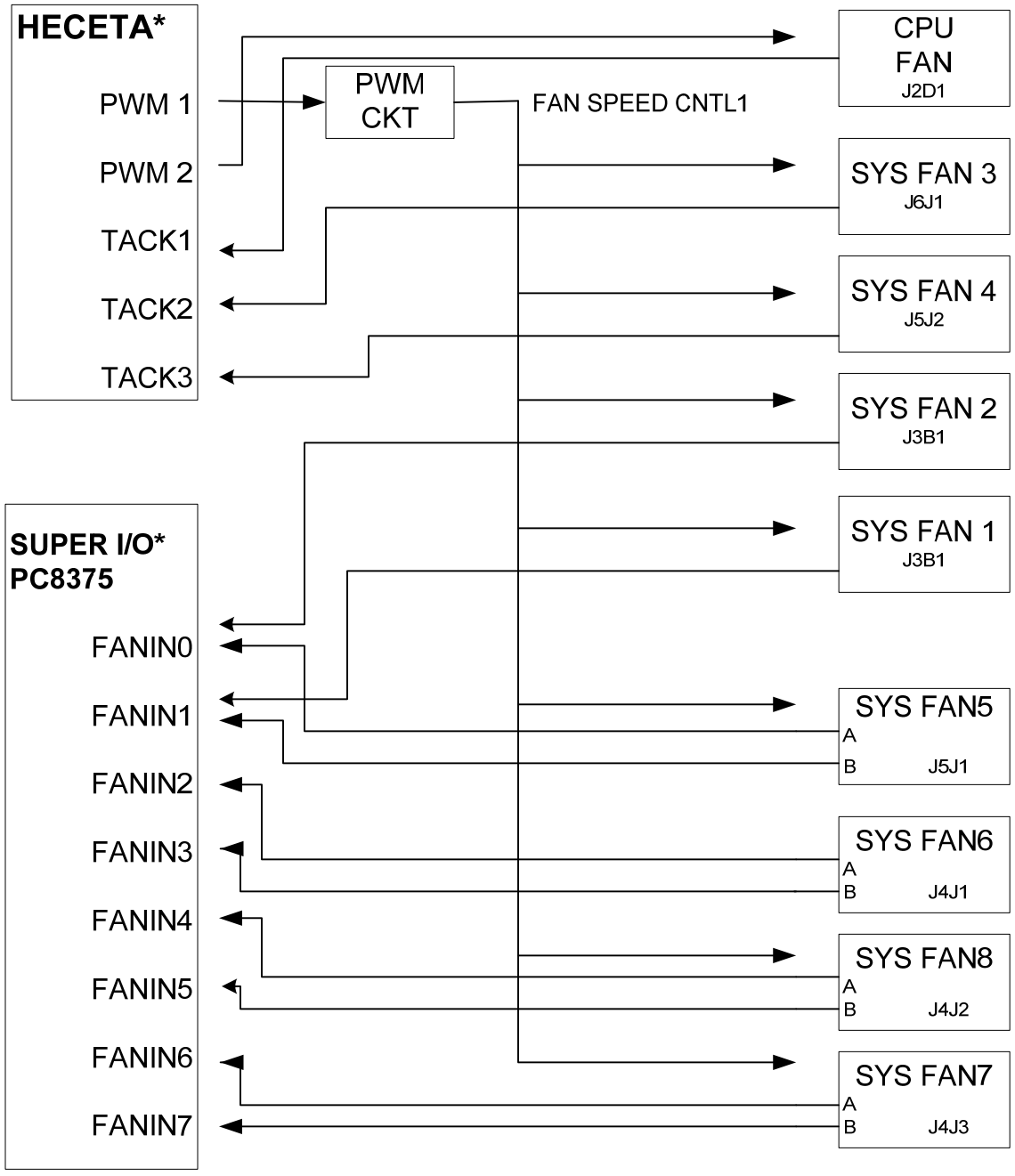


Figure 14. Fan Speed Control Block Diagram

10.1.2 Chassis Intrusion

The Intel® Entry Server Board SE7230NH1-E supports a chassis security feature that detects if the chassis cover is removed. For the chassis intrusion circuit to function, the chassis' power supply must be connected to AC power. The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion connector. When the chassis cover is removed, the mechanical switch is in the open position.

Glossary

This appendix contains important terms used in the preceding chapters. For ease of use, numeric entries are listed first (e.g., “82460GX”) with alpha entries following (e.g., “AGP 4x”). Acronyms are then entered in their respective place, with non-acronyms following.

Term	Definition
ACPI	Advanced Configuration and Power Interface
ANSI	American National Standards Institute
AP	Application Processor
ASIC	Application Specific Integrated Circuit
ASR	Asynchronous Reset
BGA	Ball-grid Array
BIOS	Basic input/output system
Byte	8-bit quantity.
CMOS	In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board.
DCD	Data Carrier Detect
DMA	Direct Memory Access
DMTF	Distributed Management Task Force
ECC	Error Correcting Code
EMC	Electromagnetic Compatibility
EPS	External Product Specification
ESCD	Extended System Configuration Data
FDC	Floppy Disk Controller
FIFO	First-In, First-Out
FRU	Field replaceable unit
GB	1024 MB.
GPIO	General purpose I/O
GUID	Globally Unique ID
Hz	Hertz (1 cycle/second)
HDG	Hardware Design Guide
I2C	Inter-integrated circuit bus
IA	Intel® architecture
ICMB	Intelligent Chassis Management Bus
IERR	Internal error
IMB	Inter Module Bus
IP	Internet Protocol
IRQ	Interrupt Request
ITP	In-target probe
KB	1024 bytes
KCS	Keyboard Controller Style
LAN	Local area network
LBA	Logical Block Address
LCD	Liquid crystal display
LPC	Low pin count

Term	Definition
LSB	Least Significant Bit
MB	1024 KB
MBE	Multi-Bit Error
Ms	milliseconds
MSB	Most Significant Bit
MTBF	Mean Time Between Failures
Mux	multiplexor
NIC	Network Interface Card
NMI	Non-maskable Interrupt
OEM	Original equipment manufacturer
Ohm	Unit of electrical resistance
PBGA	Pin Ball Grid Array
PERR	Parity Error
PIO	Programmable I/O
PMB	Private Management Bus
PMC	Platform Management Controller
PME	Power Management Event
PnP	Plug and Play
POST	Power-on Self Test
PWM	Pulse-Width Modulator
RAIDIOS	RAID I/O Steering
RAM	Random Access Memory
RI	Ring Indicate
RISC	Reduced instruction set computing
RMCP	Remote Management Control Protocol
ROM	Read Only Memory
RTC	Real Time Clock
SBE	Single-Bit Error
SCI	System Configuration Interrupt
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic RAM
SEL	System event log
SERIRQ	Serialized Interrupt Requests
SERR	System Error
SM	Server Management
SMI	Server management interrupt. SMI is the highest priority nonmaskable interrupt
SMM	System Management Mode
SMS	System Management Software
SNMP	Simple Network Management Protocol
SPD	Serial Presence Detect
SSI	Server Standards Infrastructure
TPS	Technical Product Specification
UART	Universal asynchronous receiver and transmitter
USB	Universal Serial Bus

Term	Definition
VGA	Video Graphic Adapter
VID	Voltage Identification
VRM	Voltage Regulator Module
Word	16-bit quantity
ZCR	Zero Channel RAID

Reference Documents

Refer to the following documents for additional information:

- *Board Set Specification*, Intel Corporation, document number xx-xxxx.
- *System Specification*, Intel Corporation, document number xx-xxxx.

[Insert any additional documentation]