

PCI-934

MULTIMEDIA PENTIUM BOARD

TECHNICAL REFERENCE MANUAL

ref.: M934_1-2

NOTE:

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VERSION 1.2 August 1998



FOREWORD

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EXERCISE CAUTION WHILE REPLACING LITHIUM BATTERY



There is a danger of explosion if the battery is incorrectly replaced.

Replace the battery only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.



ATTENTION

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie.

Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabriquant.



ACHTUNG

Explosionsgefahr bei falschem Batteriewechsel.

Verwenden Sie nur die empfohlenen Batterietypen des Herstellers. Entsorgen Sie die verbrauchten Batterien laut Gebrauchsanweisung des Herstellers.



ATENCION

Puede explotar si la pila no este bien reemplazada.

Solo reemplazca la pila con tipas equivalentes segun las instrucciones del manifacturo. Vote las pilas usadas segun las instrucciones del manifacturo.

Read Me First 1

IMPORTANT INFORMATION

Before operating your Single Board Computer, please note the following:

Battery Configuration

Your computer board is equipped with a standard non-rechargeable lithium battery. To preserve the useful life of the battery, the jumper which enables the battery is not installed when you receive the board. If you need a jumper cap, we suggest you use the one on the Watchdog Timer jumper since it is rarely needed; if you wish to purchase jumper caps, you can contact TEKNOR's Sales department to order them.

Connecting Flat Panel Video Display

The PCI-934 board supports many different types of Flat Panel displays. TEKNOR has fully tested a number of these panels and provides all the BIOS software support and the technical information needed.

If you have access to the Internet, many video BIOS files in a binary format and related interconnection charts in a PDF format are available on our web site. You can download these files, if you are a customer of TEKNOR and have a password from TEKNOR. If you do not have your password, contact TEKNOR's Technical Support to obtain it.

To download a video BIOS file or its interconnection chart file, follow this procedure:

- 1. Access the TEKNOR web site. Our address is http://www.teknor.com .
- 2. Go to the Support & Services section.
- 3. Scroll down the list of products until you find the name of your board and click on it. This selection is a link to the board's support area.
- 4. Click on the Video BIOS link.
- 5. The list of tested Flat Panel displays appears. If you find your particular display, you can then ask to download the associated BIOS or interconnection chart files by clicking the appropriate link.
- 6. A pop-up window appears. You must enter your password (case sensitive) and click the SUBMIT button. Entering your e-mail address is optional. Follow the instructions in subsequent pop-ups to download the file.

If you do not have access to our web site, or if you do not see the name of your Flat Panel, then you need to contact TEKNOR's Technical Support department. Since we are always testing new flat panels, it is possible that we have tested your particular type of panel display. Even if we have not tested it, TEKNOR's Technical Support can do it for you and supply the video BIOS and the technical information you need.

Preventing Viruses

TEKNOR INDUSTRIAL COMPUTERS takes every precaution against computer viruses. For your protection, we have *safety sealed* all utility diskettes. If the seal is broken, **do not use the diskette**. Destroy the diskette immediately and contact our Technical Support department for further instructions at (450) 437-5682 (Canada) or at +49 811 / 600 15-0 (Germany).

To safeguard against computer viruses in general, do not freely lend your utility diskettes and regularly perform virus scans on all your computer systems.

Read Me First 3

PART ONE – Product description

5.	UNPACKING	5-1
	 STATIC ELECTRICITY STORAGE ENVIRONMENT POWER SUPPLY 	
4.	SAFETY PRECAUTIONS	4-1
3.	COMPATIBILITY WITH TEKNOR PRO	DUCTS3-1
2.	FEATURES	2-1
1.	PRODUCT OVERVIEW	1-1

PART TWO – Hardware Installation

6.	INSTALLING AND WORKING WITH SYSTEM COMPONENTS						
	6.1	PROCESSOR AND FAN	6-1				
		6.1.1 Processor Characteristics	6-2				
	6.2	INSTALLING MEMORY	6-3				
		6.2.1 System Memory (SDRAM)	6-3				
		6.2.2 Cache Memory	6-6				
	6.3	BACKUP MEMORY	6-6				
	6.4	SUPERVISION FEATURES	6-7				
		6.4.1 WATCHDOG	6-7				
		6.4.2 POWER FAILURE DETECTION	6-9				
		6.4.3 THERMAL MANAGEMENT	6-9				
		6.4.4 I/O REGISTER ADDRESSES	6-9				

7.	INS	TALLING STORAGE DEVICES	7-1
	7.1	FLOPPY DISKS DRIVES	
	1.2		
	7.3	COMPACTELASH DISK	
		7.3.1 INSTALLING COMPACTELASH MODULE	
		7.3.2 WORKING WITH A COMPACTFLASH DISK	7-4
8.	INST	TALLING PERIPHERALS	8-1
	8.1	VIDEO	8-1
	8.2	SERIAL PORTS	
	0	8.2.1 SERIAL PORT 1 (J6) RS-232	
		8.2.2 SERIAL PORT 2 (J7)	8-3
	8.3	PARALLEL PORT	8-6
		8.3.1 STANDARD MODE	8-7
		8.3.2 EPP MODE	8-7
		8.3.3 ECP MODE	8-7
	8.4	PS/2 MOUSE	8-7
	MUL	TI I/O CONNECTOR	8-8
	8.6	USB PORTS	8-9
9.	ЕТН	IERNET	9-1
	50		
10.	PC/1	104-PLUS FEATURES	10-1
11.	SET	TING JUMPERS	11-1

PART THREE – Multimedia Features

12.	EXP	LORING	G THE MULTIMEDIA CAPABILITIES OF THE BOARD	12-1
	12.1	VIDEC	FEATURES	12-3
		12.1.1	FLAT PANEL DISPLAY	12-3
		12.1.2	CRT DISPLAYS	12-6
		12.1.3	PANELLINK [™] INTERFACE	12-7
		12.1.4	NTSC	12-8
		12.1.5	VGA INTERRUPT	12-8
		12.1.6	V-PORT	12-9
	12.2	AUDIC) FEATURES	12-10
		12.2.1	LINE IN	12-10
		12.2.2	LINE OUT	12-10
		12.2.3	MIC IN	12-11
		12.2.4	CD IN	12-11
		12.2.5	AUDIO I/O CONNECTOR	12-12
		12.2.6	SPEAKER TO LINE OUT	12-12

PART FOUR – Software Setups

13.	BIOS	SETUPS	13-1
	13.1	USING THE BIOS SETUP PROGRAM	13-2
	13.2	SAVING CONFIGURATIONS & EXITING AWARD SETUP	13-4
	13.3	STANDARD CMOS SETUP	13-4
	13.4	BIOS FEATURE SETUP	13-5
	13.5	CHIPSET FEATURES SETUP	13-7
	13.6	POWER MANAGEMENT SETUP	13-9
	13.7	PNP/PCI SETUP	13-11
	13.8	INTEGRATED PERIPHERALS SETUP	13-12

PART FOUR – Software Setups (Continued)

14.	UPD	ATING THE BIOS WITH UPGBIOS	14-1
	14.1 14.2	UPDATING THE BIOS CPLD UPGRADE AFTER A BIOS UPDATE	14-1 14-2
15.	VT1	00 MODE	15-1
	1.4	REQUIREMENTS	15-1
	1.5	SETUP & CONFIGURATION	15-1

A.	PRODUCT SPECIFICATIONS A-1					
в.	BOARI	D DIAGRAMSB-1				
C.	CONN	ECTOR PINOUTS C-1				
	C.1	XVGA CONNECTOR - J1 C-1				
	C.2	PANELLINK CONNECTOR - J2C-1				
	C.3	EIDE CHANNEL 1 CONNECTOR - J3 C-2				
	C.4	FLOPPY DISK CONNECTOR - J4C-3				
	C.5	MULTIFUNCTION CONNECTOR - J5 C-3				
	C.6	SERIAL PORT 1 CONNECTOR - J6C-4				
	C.7	SERIAL PORT 2 CONNECTOR (RS-232) - J7C-4				
	C.8	SERIAL PORT 2 CONNECTOR (RS-422/RS-485) - J7 C-4				
	C.9	FAN CONNECTOR - J8C-4				
	C.10	FLAT PANEL CONNECTOR - J9 C-5				
	C.11	EIDE CHANNEL 2 CONNECTOR - J10 C-6				
	C.12	V-PORT CONNECTOR - J11C-6				
	C.13	NTSC OUT CONNECTOR - J12 C-7				
	C.14	PARALLEL PORT CONNECTOR - J13C-7				
	C.15	USB CONNECTOR - J14C-7				
	C.16	PS/2 MOUSE CONNECTOR - J15C-8				
	C.17	I ² S CONNECTOR (NO MPEG) - J16C-8				
	C.18	CD IN CONNECTOR - J17 C-8				
	C.19	AUDIO I/O CONNECTOR - J18 C-8				
	C.20	FLASH DISK CONNECTOR - J19 C-9				
	C.21	CRT VGA CONNECTOR - J20C-9				
	C.22	LINE OUT CONNECTOR - J21C-9				
	C.23	MIC IN CONNECTOR - J22 C-10				
	C.24	LINE IN CONNECTOR - J23 C-10				
	C.25	ETHERNET CONNECTOR - J24 C-10				
	C.26	PC/104-PLUS CONNECTOR - J25 C-11				
	C.27	PC/104 CONNECTORS - P1 AND P2 C-12				

D.	MEMO	DRY AND I/O MAPS	D-1
	D.1	Memory Map Diagram	D-1
	D.2	I/O Mapping	D-2
E.	BIOS	SETUP ERROR CODES	E-1
	E.1	POST MESSAGES	E-1
	E.2	POST BEEP	E-1
	E.3	ERROR MESSAGES	E-2
	E.4	POST CODES	E-5
F.	EMER	GENCY PROCEDURES	F-1
	F.1	SYMPTOMS	F-1
	F.2	MAKING AN EMERGENCY DISKETTE	F-2
	F.3	EMERGENCY PROCEDURE	F-3



PRODUCT DESCRIPTION

- 1. **PRODUCT OVERVIEW**
- 2. FEATURES
- 3. COMPATIBILITY WITH TEKNOR PRODUCTS
- 4. SAFETY PRECAUTIONS
- 5. UNPACKING



1. PRODUCT OVERVIEW

What is multimedia?

Multimedia is turning out to be one of the most appealing capabilities of a computer.

Running a multimedia application means that a huge amount of hardware and software is trying to run at the same time, competing for the attention of all system resources. For example, the hardest thing a PC can do when proceeding tests is to run multimedia applications.

Sub-systems that make multimedia applications possible are the sound system, CD-ROM and hard disk drives, speaker, enhanced local-bus video graphics, big screen color monitor, plenty of memory and finally, the processor.

Working with multimedia requires a computer capable of working fast, smoothly and reliably. The PCI-934 single board computer meets all these conditions.

The PCI-934 is a full-length PC/AT-PICMG form factor single board computer (SBC). It is built around a powerful computing core that characterizes the PCI-9xx board family, associated with high performance multimedia features:

- MPEG-1 hardware decoder implemented to process MPEG coded audio/video stream in real time.
- 2MB EDO DRAM, 64-bit graphics performance LCD/CRT controller with V-Port capabilities.
- SoundBlasterTM Pro compatible controller with MIDI interface that connects to a MIDI wavetable synthesizer for CD-quality sound output, compatible with WSS (Windows Sound System) audio subsystem.
- TV/Composite video output support using an external PAL/NTSC encoder.

Such a configuration allows the board to playback full motion MPEG sequences from standard IDE devices.

The PCI-934 integrates the hottest multimedia features to make it a powerful stand-alone system with direct peripheral connections capabilities:

- Flat panel interface supporting active and passive color display, from VGA to XGA.
- PanelLinkTM interface that drives remote 64-bit accelerated LCD panel over several meters of copper (up to 10 meters / 30 feet).
- UXGA CRT interface (1280x1024 resolution).
- V-Port interface that allows real-time video overlay from an external video source (VIPer Vision TEK-380).
- Standard CD connector input.
- CompactFlash disk interface configured as a standard IDE disk on the secondary IDE channel.
- PC/104-Plus (embedded PCI) stackable module interface.



2. FEATURES

VIDEO CAPABILITIES

Video capabilities are built around the CL-GD7556 high-performance 64-bit video and graphics accelerated LCD/CRT controller, from Cirrus Logic.

The controller provides features such as:

- GUI and true 64-bit accelerations
- 32-bit PCI V2.1 interface
- Acceleration of MPEG-1

V-Port support for the implementation of built-in MPEG video playback, and external TV tuner, video conferencing, and teleconferencing.

The video controller provides a high memory bandwidth, up to 80MHz, which allows the board to support V-Port applications at a resolution of 1024x768.

Video capabilities are as follows:

- Video memory: 2MB EDO 64-bit RAM
- CRT display: 1280 x 1024 x 256, 1024 x 768 x 64K, 800 x 600 x 16M, 640 x 480 x 16M.
- Flat panel: up to 1024 x 768 64K colors Dual-Panel, Dual-Drive, STN and TFT panels
- V-Port Interface: The V-port interfaces video data directly from the MPEG-1 decoder or an external video device through the J11 connector. The video stream is transferred directly into the display memory, bypassing the CPU. The V-Port appears as a multimedia solution that requires no external video processing hardware and additional display memory. The V-port offers high-quality low-cost multimedia options such as live-video preview and capture, TV-in-a-window, hardware assisted MPEG and video conferencing.

The video controller provides all the signals necessary to drive flat-panel (1024x768 max.) and CRT monitor simultaneously. It supports up to 16.8M colors in most VGA and video formats.

The multimedia capabilities include acceleration of video playback, video capture, livevideo presentation and other video applications - all with continuous upscaling to resolution up to 1024x768.

SYSTEM MEMORY

- Four vertical 72-pin SIMM sockets support both FPM and EDO DRAM memory configurations from 8 to 512MB.
- Uses standard 5V, 70ns/60ns single-sided or double-sided 72-pin SIMMs.
- Supports 1, 2, 4, 8, 16, 32M 32/36-bit modules.

STORAGE DEVICES

- Optional Flash Disk: when using the T069 daughter board, a standard CompactFlash TM flash disk can be connected. Contact TEKNOR for available capacity.
- Enhanced IDE interface: Enhanced IDE controller can drive up to four IDE devices with transfer rates up to 22MB/s. The PCI-934 includes two separate IDE data bus and control signals.

ETHERNET

 100Base-TX or 10Base-T interface is implemented with Intel's 82558 Ethernet Controller. The IC resides on the PCI bus, which allows very high transfer rates to and from the DRAM.

BUS SUPPORT

- ISA Bus (IEEE P966 Specification). High-drive buffers let the PCI-934 drive up to 20 slots.
- PCI Local Bus Specification, Revision 2.1.

PICMG INTERFACE

- PICMG 2.0 Bus Specification which defines the ISA bus and the PCI bus.
- The PCI-934 can support memory data streaming up to 112MB/sec. (read) and 121MB/sec. (write)

The PCI-934 provides concurrent PCI master and CPU/DRAM operations. It also implements "delayed transaction" to increase the availability of the PCI bus.

OPERATING SYSTEM

 Runs all operating systems developed for x86 processors: DOS, Windows 3.1, OS/2, Windows 95, Windows NT, UNIX, QNX and NOVELL 4.10, etc.

BIOS AND LICENCE

• Award CPU BIOS, Cirrus Logic Video BIOS.

3. COMPATIBILITY WITH TEKNOR PRODUCTS

The board supports Pentium MMX processors at speed of up to 233MHz. The major difference between the PCI-934 and other products of the PCI-9xx familly, is its high multimedia capabilities, the 100Base-TX Ethernet, and the PanelLinkTM interface for flat panel.

The PCI-934 meets these specifications while using the same form factor as the PCI-933 (i.e., PC/AT and PICMG). The assembly includes an onboard switching regulator to supply the processor, which results in a more efficient use of power.

The board is designed to plug into a standard passive ISA backplane, or into an industry standard PICMG passive backplane.

The PCI-934 may be provided with an optional power connector that makes the board being capable to be integrated as a stand-alone single board computer system.

4. SAFETY PRECAUTIONS

4.1 STATIC ELECTRICITY

Since static electricity can damage a board, the following precautions should be taken:

- 1. Keep the board in its antistatic package, until you are ready to install it.
- 2. Touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
- 3. Handle the board by the edges.

4.2 STORAGE ENVIRONMENT

Electronic boards are sensitive devices. Do not handle or store devices near strong electrostatic, electromagnetic, magnetic or radioactive fields.

4.3 POWER SUPPLY

Before any hardware installation or setup, ensure that the board is unplugged from power sources or subsystems.

5. UNPACKING

Follow these recommendations while unpacking:

- 1. After opening the box, save it and the packing material for possible future shipment.
- 2. Remove the board from its antistatic wrapping and place it on a grounded surface.
- 3. Inspect the board for damage. If there is any damage, or items are missing, notify TEKNOR immediately.

Contents

When unpacking you will find:

- 1. One PCI-934 Single Board Computer
- 2. One Technical Reference Manual.
- 3. A set of cables
- 4. Diskettes, and drivers on a CD-ROM.



HARDWARE INSTALLATION

- 6. INSTALLING AND WORKING WITH SYSTEM COMPONENTS
- 7. INSTALLING STORAGE DEVICES
- 8. INSTALLING PERIPHERALS
- 9. ETHERNET
- 10. PC/104-PLUS FEATURES
- 11. SETTING JUMPERS



CONNECTOR LOCATION



6. INSTALLING AND WORKING WITH SYSTEM COMPONENTS

6.1 PROCESSOR AND FAN

The processor and its cooling system are is installed according to the user configuration. A + 12V DC voltage is available through the J18 connector to supply the fan (the connector's pinout appears in Appendix-C).

Installing Microprocessor



A fan is required when working with the PCI-934 board.

A +12V voltage is available through the J8 connector to supply the fan (The connector's pinout appears in Appendix-C).

Please refer to your processor specifications for more information.

When installing a processor, its type, core voltage, clock speed multiplier, and Core/Bus ratio value must be configured according to your CPU model.

Six jumpers are related to the processor:

W1	Selects the core voltage (Vcore).
W1A-W4-W10	Defines the Core/Bus clock ratio.
W8-W15	Defines the CPU bus clock.
W16	Determines the DRAM refresh rate.
W17-W18	Selects the CPU type within split-plane or single-plane.

6.1.1 Processor Characteristics

Processor characteristics are summarized below:

	Fcore	PCLK	BCLK	Ratio	Туре	VCore
Intel Pentium 100	100	66	33	1.5	Single	3.3V
Intel Pentium 120	120	60	30	2.0	Single	3.3V
Intel Pentium 133	133	66	33	2.0	Single	3.3V
Intel Pentium 150	150	60	30	2.5	Single	3.3V
Intel Pentium 166	166	66	33	2.5	Single	3.3V
Intel Pentium 200	200	66	33	3.0	Single	3.3V
Intel Pentium 166-MMX	166	66	33	2.5	Split	2.8V
Intel Pentium 200-MMX	200	66	33	3.0	Split	2.8V
Intel Pentium 233-MMX	233	66	33	3.5	Split	2.8V
AMD K6-166 ALR	166	66	33	2.5	Split	2.9V
AMD K6-200 ALR *	200	66	33	3.0	Split	2.9V
AMD K6-233 ANR *	233	66	33	3.5	Split	3.2V

To setup jumpers according to your CPU model please refer to Section 11 - Setting Jumpers.

A WARNING

* The new version of the AMD K6 supports a different core voltage (Vcore).

A WARNING

Careful attention should be taken when installing a processor and setting its configuration jumpers. Faulty jumper settings may definitely damage both the board and the processor.

6.2 INSTALLING MEMORY

6.2.1 System Memory (SDRAM)

The PCI-934 board supports FPM and EDO memory types.

Memory specifications are as follows: vertical SIMMs (Single In-line Memory Module), single-sided or double-sided, 5V, 32/36-bit, 70ns/60ns, Error Checking and Correction (ECC) or parity with 36-bit SIMMs.

The memory sockets consist of four 72-pin vertical SIMM sockets divided into two banks labeled: Bank 0 (U29 and U32) and Bank 1 (U34 and U39).



At least 8 MB of system memory (2 SIMMs of 4 MB) must be installed for proper operation. Memory can be configured from 8 MB to 512 MB using the following modules:

1M x 32-bit / 36-bit = 4MB module 2M x 32-bit / 36-bit = 8MB module 4M x 32-bit / 36-bit = 16MB module 8M x 32-bit / 36-bit = 32MB module 16M x 32-bit / 36-bit = 64MB module 32M x 32-bit / 36-bit = 128MB module

NOTE

The memory banks can be populated separately or jointly. Each bank must be installed with the same SIMM capacity, however the SIMM capacity used in one bank may be of a different capacity from the other bank. Recommended DRAM devices are listed below. Many other models are also available and function equally well. Please check with your local distributors for comparable substitutes.

SIMM	VENDOR	PART #	SIMM	VENDOR	PART #
1M*36 (FPM)	Centon	CXCGF6JF1XS283T	4M*32 (EDO)	Abbacom Log	112-01643244-S6T
4MB modules	Centon	CTK1MX36-70SMT	16MB modules	Centon	CTK4MX32-60EST
	Hyundai	HYM536120AW-60		Micron	MT8D432DM-6X
	Micron	MT9D136M-7		Unigen	4X32NEC6KBT2EDO
	Nec	MC-421000A36B-70		Unigen	UG8M43222KBT-6
	Samsung	KMM5361000B-7		Unigen	UG8M43222KBN-6
	Texas Inst.	TM124MBK36R-70	4M*36 (FPM)	Centon	CKEGH6TF2XS121T
	Toshiba	THM361020AS-70	16MB modules	Centon	CTK4MX36-60SMT
	Unigen	UG12M13600DBT-6		Hyundai	HYM536410AM-70
				Mitsubishi	MH4M36ANXJ-7
2M*32 (EDO)	Centon	CTK2MX32-60EST		Nec	MC-424000A36BH-70
8MB modules	Micron	MT4D232DM-6X		Nec	MC-424000A36BJ-70
	Unigen	2X32NEC6KBT2EDO		Samsung	KMM5364100-7
	Unigen	UG16M23220DBT-6		Toshiba	THM364020S-70
				Unigen	UG9M43602KBT-6
2M*36 (FPM)	Centon	CTK2MX36-60SMT	8M*32 (EDO)	Centon	CTK8MX32-60EST
8MB modules	Hitachi	HB56D236BW-7B	32MB modules	Micron	MT16D832DM-6X
	Hitachi	HB56D236B2-7C		Unigen	8X32NEC6KBT2EDO
	Hitachi	HB56D236BS-7BC		Unigen	UG16M83222KBT-6
	Hitachi	HB56D236BW-7C	8M*36 (FPM)	Hitachi	HB56D836BR-70A
	Hyundai	HYM536220W-70	32MB modules	Hitachi	HB56D836BR-60A
	Hyundai	HYM536220AW-60 AA		Toshiba	THM368020SG-60
	Micron	MT18D236M-7		Toshiba	THM368020S-70
	Nec	MC422000A36B-70		Unigen	UG18M83602KBT-6
	Samsung	KMM5362000B-7	16M*32 (EDO)	Unigen	UG216E3254HKT-6
	Toshiba	THM362040AS-60	64MB modules		
	Toshiba	THM362040AS-70	32M*32 (EDO)	Unigen	UG232E3244HKT-6
			128MB modules	Unigen	UG232E3264HKT-6

To install the SIMMs in the sockets, proceed as follows:



- 1. With the board flat on the table, turn it so that the bracket is on the right.
- 2. Hold the module with the notch on the bottom right facing you, and insert the fingers into the socket at a 70° angle from the board. Always start inserting the module in the socket nearest the top edge of the board
- 3. Snap the module to a vertical position. It is fully installed when the retaining pegs snap into the holes at each end of the module.
- 4. Work your way by inserting the other modules, one by one, towards the lower edge of the board.

To remove SIMMs from sockets, pull on the retaining pegs located on each side of the socket. Once the module has snapped out, pull gently on it.

SYSTEM	U34	U39	U29	U32
MEMORY	BAN	IK 1	BANK 0	
8MB	4MB (1Mx36)	4MB (1Mx36)		
8MB			4MB (1Mx36)	4MB (1Mx36)
16MB	4MB (1Mx36)	4MB (1Mx36)	4MB (1Mx36)	4MB (1Mx36)
16MB	8MB (2Mx36)	8MB (2Mx36)		
16MB			8MB (2Mx36)	8MB (2Mx36)
24MB	8MB (2Mx36)	8MB (2Mx36)	4MB (1Mx36)	4MB (1Mx36)
24MB	4MB (1Mx36)	4MB (1Mx36)	8MB (2Mx36)	8MB (2Mx36)
32MB	8MB (2Mx36)	8MB (2Mx36)	8MB (2Mx36)	8MB (2Mx36)
32MB	16MB (4Mx36)	16MB (4Mx36)		
32MB			16MB (4Mx36)	16MB (4Mx36)
40MB	16MB (4Mx36)	16MB (4Mx36)	4MB (1Mx36)	4MB (1Mx36)
40MB	4MB (1Mx36)	4MB (1Mx36)	16MB (4Mx36)	16MB (4Mx36)
48MB	16MB (4Mx36)	16MB (4Mx36)	8MB (2Mx36)	8MB (2Mx36)
48MB	8MB (2Mx36)	8MB (2Mx36)	16MB (4Mx36)	16MB (4Mx36)
64MB	16MB (4Mx36)	16MB (4Mx36)	16MB (4Mx36)	16MB (4Mx36)
64MB	32MB (8Mx36)	32MB (8Mx36)		
64MB			32MB (8Mx36)	32MB (8Mx36)
72MB	32MB (8Mx36)	32MB (8Mx36)	4MB (1Mx36)	4MB (1Mx36)
72MB	4MB (1Mx36)	4MB (1Mx36)	32MB (8Mx36)	32MB (8Mx36)
80MB	32MB (8Mx36)	32MB (8Mx36)	8MB (2Mx36)	8MB (2Mx36)
80MB	8MB (2Mx36)	8MB (2Mx36)	32MB (8Mx36)	32MB (8Mx36)
96MB	32MB (8Mx36)	32MB (8Mx36)	16MB (4Mx36)	16MB (4Mx36)
96MB	16MB (4Mx36)	16MB (4Mx36)	32MB (8Mx36)	32MB (8Mx36)
128MB	32MB (8Mx36)	32MB (8Mx36)	32MB (8Mx36)	32MB (8Mx36)
128MB	64MB (16Mx36)	64MB (16Mx36)		
128MB			64MB (16Mx36)	64MB (16Mx36)
136MB	64MB (16Mx36)	64MB (16Mx36)	4MB (1Mx36)	4MB (1Mx36)
136MB	4MB (1Mx36)	4MB (1Mx36)	64MB (16Mx36)	64MB (16Mx36)
144MB	64MB (16Mx36)	64MB (16Mx36)	8MB (2Mx36)	8MB (2Mx36)
144MB	8MB (2Mx36)	8MB (2Mx36)	64MB (16Mx36)	64MB (16Mx36)
160MB	64MB (16Mx36)	64MB (16Mx36)	16MB (4Mx36)	16MB (4Mx36)
160MB	16MB (4Mx36)	16MB (4Mx36)	64MB (16Mx36)	64MB (16Mx36)
192MB	64MB (16Mx36)	64MB (16Mx36)	32MB (8Mx36)	32MB (8Mx36)
192MB	32MB (8Mx36)	32MB (8Mx36)	64MB (16Mx36)	64MB (16Mx36)
256MB	64MB (16Mx36)	64MB (16Mx36)	64MB (16Mx36)	64MB (16Mx36)
256MB	128MB (16Mx36)	128MB (16Mx36)		
256MB			128MB (16Mx36)	128MB (16Mx36)
512MB	128MB (16Mx36)	128MB (16Mx36)	128MB (16Mx36)	128MB (16Mx36)

The following table describes which SIMM configurations may be implemented on the board, using 72-pin vertical SIMMs:

36-bit modules are shown, however 32-bit modules are supported.

6.2.2 Cache Memory

Internal Cache

The internal cache memory, also known as L1, is CPU integrated. The L1 memory size depends on the CPU model:

- 8K, 8K separated data and instructions L1, for Pentium processors
- 16K, 16K separated data and instructions L1, for Pentium MMX processors
- 32K, 32K separated data and instructions L1, for K6 processors

External Cache

The external cache memory, also known as L2 cache, is implemented with 512KB Synchronous Pipelined SRAM. This feature enhances the operation of the circuit by eliminating wait states on cache accesses.

6.3 BACKUP MEMORY

An onboard 3.6V lithium battery is provided to backup BIOS setup values and the real time clock (RTC).

When replacing, the battery must be connected as follows:



6.4 SUPERVISION FEATURES

6.4.1 WATCHDOG

The PCI-934 provides a two-stage watchdog to monitor the CPU inactivity. The function of the watchdog is to generate a failure signal if the processor is not able to generate a 0-1-0 data toggle for longer than the watchdog timeout period. The feature is useful in embedded systems where human supervision is not required or impossible.

The watchdog configuration may be selected between Dual-Stage, Single-Stage, or disabled, using the W6 jumper (see Section11 – *Setting Jumpers*).

The default timeout period is 1.6 seconds for each stage; however, the timeout period can be changed. Shorting C380/C353 and leaving R249/R230 opened changes the timeout to 100ms. Shorting the resistor and installing a capacitor will change the timeout period of the watchdog according to the following formula:

Timeout (milliseconds) = $\frac{400 \text{ms}}{47 \text{pF}} \text{xC}$ or $C = \frac{\text{Timeout}(\text{ms}) \text{x} 47 \text{pF}}{400 \text{ms}}$

For instance, an external capacity of 100pF will lengthen the watchdog timeout to 851ms and a 1000pF will bring it to 8.5 seconds.

A CAUTION

Modifying the Watchdog timeout period will also modify the value of the Reset period according to the following formula:

(200ms/47pF) x C

Single-Stage Watchdog

In a single-stage configuration, the first watchdog detector monitors the output of the first stage watchdog time-out.

To operate the watchdog, the processor drives the watchdog input (WDI) with an I/O line. It toggles WDI once every 1.6 seconds (typical) to verify the proper software execution. If a hardware or software failure occurs such that WDI is not toggled, the watchdog output (WDO) will go low after 1.6 second, and reset the CPU. If the processor can continue to run a 0-1-0 toggle routine, WDO will be set high by the next transition of WDI.

In dual stage configuration, the WDO signal indicates the second stage watchdog when a failure occurs. **Following a reset, the watchdog is always disabled**.

Dual Stage Watchdog

The dual-stage watchdog consists of a second watchdog in cascade with the first one: in the event the first watchdog failed to toggle, the second stage is set.

Before the second stage watchdog resets the system, the first watchdog output can be tied to the ISA's IOCHK line to generate an NMI to the CPU, while the two watchdog values are stored. These values may be used to determine the cause of the system's reset.

CAUTION

The user program must provide the first access to address 190H (or 290H or 390H depending on the I/O address selected in CMOS setup), and must also include the refresh routine.

Watchdog Flags

The watchdog status can be readout from two bits of the system register located at the address 191h, 291h or 391h (depending on the I/O address selected in CMOS setup). These bits are described as follows:

- x91 Bit 5: **WDO**, indicates that the last system reset was caused by a watchdog timeout.
- x91 Bit 6: **WDO1**#, when goes low, indicates that the first level watchdog timed out.

For more information on system registers, please refer to Page 6-10

6.4.2 POWER FAILURE DETECTION

A power failure may be detected if a low battery condition occurs (battery voltage drops below 3V). The power failure detector status can be readout from one bit of the system register located at the address 191h, 291h or 391h (depending on the I/O address selected in CMOS setup).

This bit is described as follows:

x91 - Bit 0: PFO#, when goes low, indicates that a power failure condition .

For more information on system registers, please refer to Page 6-10

6.4.3 THERMAL MANAGEMENT

The thermal management is built around a digital temperature sensor and a thermal watchdog. The device can be programmed to set its output when the temperature of the processor exceeds a programmable high limit, and reset its output when the temperature is under a programmable low limit. A special routine will throttle the CPU clock until the temperature falls below the programmed low limit.

6.4.4 I/O REGISTER ADDRESSES

Three supervisor I/O registers (Register #1, Register #2, and Register #3) are provided to configure and control special features of the board such as: watchdog control, RS-422/RS-485 mode, and power fail output. These registers are two 8-bit registers which can be located at three different I/O base addresses, 190h 290h or 390h.

When setting Register #1 at one base address (190h, 290h, or 390h), Register #2 and Register #3 are located respectively at the Base Address plus one and Base Address plus two.

Τ¢	o selec	t one	base	address,	use the	BIOS	setup progra	am – C	hipset	Feature	Setup.
----	---------	-------	------	----------	---------	------	--------------	--------	--------	---------	--------

Re	Register #1 (190h, 290h or 390h)					
Bit	Access	Ref.	Function			
0	R/W	ENWD	Enable/Disable External Watchdog Circuit (1: En / 0: Dis)			
1	R/W	CWD	Watchdog Control. To be toggled to activate the external WD circuit when ENWD bit is high.			
2	R/W	ST1	Enable/Disable RTS Output for RS-485 (Serial Port 2)			
3	R/W*	RS232	Enable/Disable RS-232 Operation (Serial Port 2)			
4	R/W*	RS485	Enable/Disable RS-485 Operation (Serial Port 2)			
5	R/W*	Тоит_Аск	Acknowledge Temperature Alarm			
6	R/W*	ENSMI#	Enable External SMI			
7	R/W*	DIS_LAN#	Enable/Disable Ethernet Controller (1: En / 0: Dis)			

* Do not change this bit since it is used by the BIOS

Re	Register #2 (191h, 291h or 391h)				
Bit	Access	Ref.	Function		
0	R	PFO#	Reads the External Power Fail Flag		
1	R	TOUT_ACK	Status of Temperature Controller Alarm (1: temp. alarm / 0: normal)		
2	R	х	Reserved		
3	R	х	Reserved		
4	R	х	Reserved		
5	R	WDO	When high, indicates that the last system reset was caused by a watchdog time out		
6	R	WDO1#	When low, indicates that the first level watchdog timed out		
7	R	PBRES	When high, indicates that the last system reset was caused by a push button reset switch		

Re	egister #3	<mark>3 (192h, 292h</mark>	or 392h)		
Bit	Access Ref.		Function		
0	R/W	CLRHIS#	Clears W	/DO and PBRES status bits (0: clear ; 1: normal)	
1	R/W*	EN_MPEG#	Enable N	I-PEG decoder (1: Disable ; 0: Enable)	
2	R/W*	LOCK	Reserved		
3	R		Reserve	d	
4	R/W	VP_OI_1	General	purpose output for V-Port control	
5	R/W	VP_OI_2	General	purpose input for V-Port control	
6	R/W*	EN_IRQ_MPEG Reserve		d	
7	R/W	EN CAM#	Controls	V-Port buffer (0: external: 1: MPEG)	

 7
 R/W
 EN_CAM#
 Controls V-Port buffer (0: external; 1: MPEG)

 * Do not change this bit since it is used by the BIOS

7. INSTALLING STORAGE DEVICES

7.1 FLOPPY DISKS DRIVES

Floppy disk drives connect to the board using a standard IBM 34-pin flat ribbon cable through the J4 onboard header.



The following list includes approved vendors for the J2 connector's mating parts:

Amp 746285-8 [optional strain relief: 499252-6], Robinson Nugent IDS-C34PK-TG, Thomas & Betts 622-3430 [optional strain relief: 622-3441]. (34-pin flat cable connector).

The J4 floppy connector's pinout is given in Appendix-C – Connector Pinouts.

7.2 EIDE DEVICES

To install Enhanced IDE hard disk drives, use two standard IBM 40-pin flat ribbon cable that connect to J3 and J10: J3 is reserved for Primary EIDE devices while J10 is reserved for Secondary EIDE devices.

Each cable supports directly two IDE devices (Master and Slave). Its recommended maximum length is 18 inches from the IDE device to the board connector). A complete configuration allows a total of four EIDE devices to be connected.



The following is a list of approved vendors for the mating 40-pin flat cable connector:

AMP 746285-9 [optional strain relief: 499252-1], Robinson Nugent IDS-C40PK-TG, Thomas & Betts622-4030 [optional strain relief: 622-4041].

The J3 hard disk connector's pinout is given in Appendix-C - Connector Pinouts.

7.3 COMPACTFLASH DISK

The board supports a IDE compatible flash disk by using the TEK-069 CompactFlash daughterboard. CompactFlash (C-Flash) disks are the world's smallest resident industry-standard ATA/IDE subsystem for application, data, image, and audio storage. They have the same functionality and capabilities as intelligent disk drives, but with the advantages of being very compact, rugged (typical M.T.B.F. is 1,000,000 hours) and low power.

Available capacities are up to 24MB. 40 and 80MB modules will be supported when available.

The C-Flash disk connects on the PCI-934 via the onboard Flash Disk Connector J19 (J19 connector pinout is provided in Appendix-C).

7.3.1 INSTALLING COMPACTFLASH MODULE

Follow this procedure to install a C-Flash module on the TEK-069 and to install the TEK-069 on the board:

1. Slide the C-Flash module into its receptacle and press gently to ensure a good insertion and connection.



2. Clip the spacers into their mounting holes: two are located close to the interface connector, a third one is located at the bottom of the module. The spacer located near the C-Flash module acts as a retention mechanism and prevents it from accidently sliding.
3. To connect the daughterdoard to the SBC, line up the J19 connector and the interface connector, then press firmly the daughterboard into the Single Board Computer's connector to engage the connector and the spacers.



7.3.2 WORKING WITH A COMPACTFLASH DISK

The *CompactFlash* module connects directly on the Secondary EIDE interface. It must be declared the same way as a standard hard disk using the BIOS setup program.

To setup the *CompactFlash* disk for Master or Slave configuration, use the W11 (1-2) jumper to select one configuration. To locate and install W11, please refer to Section 11 - Setting Jumpers.

NOTE

Since data is accessed like it would on an IDE drive, no specific flash disk driver is requires for various operating systems.

8. INSTALLING PERIPHERALS

8.1 VIDEO

Please refer to Section 12 - Exploring the Multimedia Capabilities of the Board.

8.2 SERIAL PORTS

Two serial ports are available on the TEK-934. They are 16C550 compatible and provide 16byte internal FIFO buffers for more efficient data transfers, enabling communication speed up to 115.2KBPS

The Serial Port 1 is buffered for RS-232 operations, while the Serial Port 2 may be set as RS-232 or RS-422/RS-485.

The following list includes approved vendors for the COM1 (J6) and COM2 (J7) connectors' mating parts:

Amp 746285-1 [optional strain relief: 499252-5], Robinson Nugent IDS-C10PK-TG, Thomas & Betts 622-1030 [optional strain relief: 622-1041]. (10-pin flat cable connector).

For information on the programming of serial ports with the use of FIFO buffers, ask for Application Note # AN93007 from TEKNOR's Technical Support department.

8.2.1 SERIAL PORT 1 (J6) RS-232

The Serial Port 1 is configured as RS-232. With the IBM 9-pin DSUB Standard, Serial Port 1 is 100% compatible with the IBM-AT serial port.



TEKNOR offers a 10-pin header to 9-pin DSUB cable for IBM-AT compatibility. This can be purchased from TEKNOR or a cable can be made with a flat cable, a 10-pin flat cable crimp header and a 9-pin DSUB flat cable crimp connector.

NOTE	
	The use of Taïwanese adapter cables is not recommended, since the pinout is often incorrect. The direct crimp design offered by TEKNOR allows the simplest cable assembly. All these cables are available from TEKNOR by contacting the Sales Department.

8.2.2 SERIAL PORT 2 (J7)

By default the Serial Port 2 is set as RS-232. In this configuration, it functions the same way as Serial Port 1, with the same pinout. However, the Serial Port 2 may be set for RS-422/RS-485 operations, using the BIOS Setup program.

RS-232 Mode

As a RS-232 port, and with the IBM 9-pin DSUB Standard, Serial Port 2 is 100% compatible with the IBM-AT serial port. To output RS-232 signals from the 10-pin onboard connector to a 9-pin DSUB connector, please refer to the following diagram:



TEKNOR offers a 10-pin header to 9-pin DSUB cable for IBM-AT compatibility. This can be purchased from TEKNOR or a cable can be made with a flat cable, a 10-pin flat cable crimp header and a 9-pin DSUB flat cable crimp connector. The direct crimp design offered by TEKNOR allows the simplest cable assembly. All these cables are available from TEKNOR by contacting the Sales department.

RS-422/RS-485 Mode

When configured for RS-422/RS-485 operation, the Serial Port 2 can transmit and receive differential signals, in either full-duplex or party line communication.

Communicating with differential signals requires one pair of wires for the transmission and a pair of wires for the reception (RS-422). For a better noise rejection, the use of twisted pair cable is highly recommended. This will enable faster serial transmissions over greater distances than with the common RS-232 protocol.

RS-422 - Full Duplex Operation: The RS-422 protocol uses both RX and TX lines during a communication session. Upon power-up or reset, the Serial Port 2 interface circuits are automatically configured for full duplex operation: pins 3 and 4 of J7 act as the receiver lines and pins 5 and 6 act as the transmitter lines.



In RS-422 mode, software should not use the handshake signals (e.g. DSR or DTR) since they are not connected. However, software handshaking (e.g. XON-XOFF) can be used.

RS-485 - Party Line Operation: The RS-485 offers the ability to transmit and receive over the same pair of wires (RX outputs: pins 3 and 4), and share the same communication line with multiple stations. To ensure this configuration, only one system takes the control of the communication line at the time.



The RS-485 protocol offers some advantages such as increased speed over long distances, improved reliability over similar RS-232 setups, ability to share the transmission line, less cabling requirements than RS-422 protocol.

Upon power-up or reset, the transceiver is by default in "receiver mode" to prevent undesired perturbation on the line.

In RS-485 mode, only both ends of the network must be terminated (120 Ohms resistors). Termination resistors are available: If the board is installed at one end of the network, these resistors may be installed using the W2 and W3 jumpers.

Pinout: When configured for RS-422/485 communication mode, the pin assignation for the onboard Serial Port 2 (J7) appears as follows:

	I/O	Signal	Pin #	Pin #	Signal	I/O
Onboard 10-pin Header	1	DCD	1	2	DSR	Ι
	I/O	R X (-)	3	4	RX(+)	0
	0	TX(-)	5	6	TX(+)	Ι
	0	DTR	7	8	RI	Ι
9	-	GND	9	10	N.C.	-
	Onboard	Serial Port (Connecto	r set as R	S-485	

8.3 PARALLEL PORT

The PCI-934 provides a bi-directional parallel port, compatible with PC/XT, AT, PS/2, EPP and ECP modes.

To operate in EPP or ECP mode, the peripheral must be designed to operate in this mode and the BIOS setup must be configured to support it. The differences between the three modes appear in their pin assignation.



The parallel port connector (J13) is a male 26-pin header located at the top right side of the board.

The following list includes approved vendors for the J13 connector's mating parts:

Amp 746285-6 [optional strain relief: 499252-3],

Robinson Nugent IDS-C26PK-TG,

Thomas & Betts 622-2630 [optional strain relief: 622-2641].

(Polarized IDC female socket connector).

8.3.1 STANDARD MODE

The Standard mode is an unidirectional parallel port. It is used for its compatibility with the IBM PC standard.

8.3.2 EPP MODE

The EPP (Enhanced Parallel Port) mode consists of a hardware independent method of accessing a parallel port configured as EPP. It provides support for single I/O cycle as well as the high performance block I/O transfers. The EPP mode always uses the most optimum method for I/O transfers. For example, if the hardware supports it, EPP mode will perform 32-bit I/O block transfers.

8.3.3 ECP MODE

While the EPP mode may intermix read and write operations without any overhead or protocol handshaking, the ECP mode negotiates data transfers using a request from the host and an acknowledgment from the peripheral.

8.4 PS/2 MOUSE

The board provides a PS/2 mouse header (J15) to output the mouse clock and data signals. An adapter cable is required to make these signals available on a 6-pin PS/2 standard connector: The cable must provide a 4-pin female header at one end, and a 6-pin female PS/2 standard connector at the other end:

Connection



8.5 MULTI I/O CONNECTOR

The onboard multi I/O connector (J5) provides all the necessary signals for connecting keyboard, speaker, reset, and keylock interface devices. It is described as follows:

		Signals Name	Description
	16	FVCC (+5V)	Hard Disk Activity LED
	15	ACT1*	$\stackrel{\begin{tabular}{c}{\label{eq:constant}}}{\longrightarrow}$ No external limiting resistor is required (internal =330 Ω).
	6	VCC (+5V)	Protected Vcc
	4	GND	(No limiting resistor)
	9	ACFAIL*	AC Fail Input
	10	GND	generate an NMI event
	13	PBRES*	Computer Board Reset
	14	GND	board
	7	SPKR	Computer Board Speaker
	8	VCC (+5V)	(Use & onm speaker)
	1	KCLK	Keyboard
	3	KDAT	- See Note 1 -
	2	GND	
	5	VCC (+5V)	
	11		
	12	GND	NOLUSEO
	* 4 at	the second second	

* Active low signal Vcc (+5V) is protected with a 1.1A resettable fuse







The following list includes approved vendors for the J5 connector's mating parts: Amp 746285-3 [optional strain relief: 499252-8], Robinson Nugent IDS-C16PK-TG, Thomas & Betts 622-1630 [optional strain relief: 622-1641]. (16-pin flat cable connector).

8.6 USB PORTS

USB is becoming the new essential peripheral interface. The USB strengths are as follows: the ability to daisy chain as many as 127 devices, a 12Mbps transfer rate, and the standardization of peripheral interfaces into a single format.

USB support Plug and Play and hot swapping operations (OS level) which is the most user friendly feature, since this means that the system will support a new USB device installation without rebooting.

Because of the very low technology barrier, keyboards, mice, speakers, are some of the first peripherals to adopt the USB standard. Sophisticated USB products, like camera, scanners, and printers are becoming available. Monitors are likely to become the main hub for system USB connections.

Connections

The onboard USB capacities are built around the PIIX3 chipset from Intel. Two USB ports are available. Connections are available through J14 - Dual USB header.



External USB connections must be provided as follows:

9. ETHERNET

The board supports both 10Base-T and 100Base-TX on the same RJ-45 edge bracket connector. 10Mbps and 100Mbps network speed is automatically detected and switched.

The onboard Ethernet interface may be set for 10Base-T or 100Base-TX operation modes:

The 10Base-T interface uses UTP (Unshielded Twisted Pair) cables, category 5, 4 or 3 (5 is better), while the 100Base-TX cable must use category 5.



This connection type allows links up to 100m over both shielded twisted pair and data grade (Cat. 5) unshielded twisted pair or equivalent.

The Ethernet controller resides on the PCI bus and is therefore Plug and Play by default. No manual configuration is required. A setup program is provided on the driver CD-ROM to configure the Ethernet controller according to your OS requirements (refer to the OS list on the CD-ROM – File.txt. The CD-ROM provides several operating system network drivers.

To install the drivers, run the "Setup.exe" program.

For other operating system drivers and installation instructions, contact TEKNOR's Technical Support department.

10. PC/104-PLUS FEATURES

The onboard PC/104-Plus interface is a PCI extension of the PC/104 ISA standard. It consists of three connectors referred as P1, P2 and J25, and is provided to receive PC/104 form factor modules to increase the I/O capabilities of the board.

P1 and P2 are assigned to the ISA bus while J25 is assigned to the PCI bus. All signals are provided in the same order as on the edge-card connector, but transformed to the corresponding connector pins.

The maximum number of PC/104-Plus modules depends on the total number of loads installed on the PCI bus. The bus supports four PCI loads, plus the PCI-934 board itself.

A typical module stack may be represented as follows:



The onboard PC/104-Plus interface complies with PC/104-PLUS V1.0 and PCI V2.1 standards. Connector pinouts are provided in Appendix C-26 and C-27.

JUMPER LOCATION



11. SETTING JUMPERS

The jumpers available on the board are summarized below:

Jumper	Description
W1	CPU core voltage setup
W1A	Bus / Core Frequency ratio selection
W2, W3	RS-422 / RS-485 termination type selection (on serial port 2)
W4	Bus / Core Frequency ratio selection
W5	Battery connection
W6	Watchdog setup
W7	IOCHK signal source selection
W8	Main Clock frequency selection
W9	VGA interrupt setup (PCI)
W10	Bus / Core Frequency ratio selection
W11	Flash Disk assignation; Signal settings for PanelLink interface
W12	VGA interrupt setup (Master)
W13	Flat panel supply level
W14	Flat panel Clock-Shift signal polarity
W15	Main Clock frequency selection
W16	DRAM refresh rate selection
W16A	Enables/Disables video on the board
W17, W18	CPU type

Jumper Settings 1/3

CPU Related Jumpers													
₩17 1000 1000 1000 1000	WIA 00 20000 WIA 00 000000000000000000000000000000000												
CPU Model	Clock	c Mul.	Bus/Co	ore Fre	q. Ratio	СР	U Туре		W	1 - V C	ore		Refr.
Selection	W15	W 8	W10	W4	W1A	W17	W18	1-2	3-4	5-6	7-8	9-10	W16
P 100	OFF	ON	OFF	OFF	OFF	ON	1-3 / 2-4	ON	OFF	ON	ON	OFF	ON
P 120	ON	OFF	ON	OFF	OFF	ON	1-3 / 2-4	ON	OFF	ON	ON	OFF	OFF
P 133	OFF	ON	ON	OFF	OFF	ON	1-3 / 2-4	ON	OFF	ON	ON	OFF	ON
P 150	ON	OFF	ON	ON	OFF	ON	1-3 / 2-4	ON	OFF	ON	ON	OFF	OFF
P 166	OFF	ON	ON	ON	OFF	ON	1-3 / 2-4	ON	OFF	ON	ON	OFF	ON
P 200	OFF	ON	OFF	ON	OFF	ON	1-3 / 2-4	ON	OFF	ON	ON	OFF	ON
P 166-MMX	OFF	ON	ON	ON	OFF	OFF	3-5 / 4-6	OFF	OFF	OFF	ON	OFF	ON
P 200-MMX	OFF	ON	OFF	ON	OFF	OFF	3-5 / 4-6	OFF	OFF	OFF	ON	OFF	ON
P 233-MMX	OFF	ON	OFF	OFF	OFF	OFF	3-5 / 4-6	OFF	OFF	OFF	ON	OFF	ON
K6-166 (1)	OFF	ON	ON	ON	OFF	OFF	3-5 / 4-6	ON	OFF	OFF	ON	OFF	ON
K6-200(1)	OFF	ON	OFF	ON	OFF	OFF	3-5 / 4-6	ON	OFF	OFF	ON	OFF	ON
K6-233 (2)	OFF	ON	OFF	OFF	OFF	OFF	3-5 / 4-6	OFF	OFF	ON	ON	OFF	ON
K6-266						Contac	t TEKNOF	R					
K6-300	Contact TEKNOR												
(1) ALR suffix: 2.9V core voltage													



Careful attention should be taken when installing a processor: Faulty jumper settings may damage definitely both your processor and your board.

Jumper Settings 2/3

NAME	FUNCTION	CONFIGURATION	(INITIAL SETTING: *)
W 2 W 3	RS-422/RS-485 Termination Resistors	W2 W3 With Termination	W2 W3 OOOO Without Termination *
W 5	VBAT Internal Battery	Battery ON Danger of Replace only by the manuf manufacture	Battery Disabled * explosion if battery is incorrectly replaced. with the same or equivalent type recommended facturer. Dispose of used batteries according to the r's instructions .
W 6	Watchdog	1 () 3 1 () 3 1 () 3 1 () 3	Dual-Stage Watchdog Single-Stage Watchdog* Watchdog Disabled
W 7	IOCHK Signal Source Selection	1 () 3 1 () 3 1 () 3 1 () 3	From ACFAIL Input From First Stage Watchdog Disabled *
W 9	VGA Interrupt (PCI)	Enabled	OO Disabled *

Jumper Settings 3/3

NAME	FUNCTION	CONFIGURATION (INITIAL SETTING: *)					
W11	FLASH Disk Assignation & Signal Settings for			W11	2 6 0 0 0]	
	PanelLink			Features		Settings]
	Interface		1.0	Flash Disk	ON * Set as Master		1
			1-2	Mast./Slave	OFF	Set as Slave	
			3-4	PanelLink	ON *	Latched on falling	
				Control Edge	OFF	Latched on rising	
			5-6	PanelLink	ON *	Latched on falling	
				Data Edge	OFF	Latched on rising	
W12	Master VGA Interrupt	Disabled * Enabled			○ ○ nabled		
W13	Flat Panel Power Selection	1 🔾 🕡	volt *	l	1 [5 volt	
		areful att aulty pow anel and y	ention ver sele your bo	should be take ction may dam pard.	n when i age defi	installing a flat panel: initely both your flat	
W14	Flat Panel Clock Shift	1 O @ Inve	3 erted		1[ŒOO3 Normal*	
W16A	Video	Enab	led *		D	o o isabled	

11-4



MULTIMEDIA FEATURES

12. EXPLORING THE MULTIMEDIA CAPABILITY OF THE BOARD



12. EXPLORING THE MULTIMEDIA CAPABILITIES OF THE BOARD

The purpose of the multimedia core is the coordination of sound, video stream, and computer graphics with the mouse, touchscreen, and the keyboard input. The board supports specialized sub-systems and connections designed to provide the multimedia delivery of all this information coming from different sources.



Software Applications

These are data (text, picture, sound from games, MPEG software decoding, ...) provided by an application running on the computer.

Software applications are under the supervision of the processor. The more there are applications running, the more the processor is busy and system resources decrease.

Video Stream

Thanks to the onboard MPEG hardware decoder, running a multimedia stream through this path would not take up more than 20% of the CPU bandwidth. During this time, the MPEG decoder receives information from the IDE device, decompresses and splits off the audio and video data that is sent to the SoundBlaster[™] Pro controller and to the video controller.

Sound Controller

It is built around the AD1816-SoundPort[®] controller. The MPEG decoder transfers the sound stream through a serial path (I²S). The sound controller is associated to a solid state digital wavetable that enables the PCI-934 to provide CD-quality audio output.

The wavetable provides a MIDI interpreter, synthesis engine, effect processor, with 1MB sample ROM. It features general MIDI samples set including 128 melodic instruments and 47 percussion sounds. The synthesis engine can generate up to 32 simultaneous notes. Digital reverberation and chorusing effects are included.

V-Port Support

The implementation of the V-Port interface allows the board to provide live-video preview/capture, TV-in-a-window, video conferencing, or external hardware-assisted MPEG. This interface allows off-loads video bandwidth from the PCI bus by transferring the video stream directly into the display memory, bypassing the CPU. The video data source may be selected from the onboard MPEG decoder or an external video source through the Register #3 - bit 1 and bit 7 (See Section 13.3 I/O Addresses).

12.1 VIDEO FEATURES

12.1.1 FLAT PANEL DISPLAY

The onboard flat panel interface provides two connectors which output digital data to drive panels up to 1024x768 pixels (XGA). The two connectors are described below:

- J9 Provides direct connection for 18 and 24 bits TFT and DSTN flat panels (640x480 and 800x600 display modes).
- J1 When used simultaneously with J9, this connector provides direct connection for 36 bits TFT and DSTN flat panels (1024x768 display mode).

Characteristics

Supported display modes are:

640x480 - VGA:	TFT and DSTN flat panel types at up to 16M colors
800x600 - SVGA:	TFT and DSTN flat panel types at up to 16M colors
1024x768 - XGA:	TFT and DSTN flat panel types at up to 64K colors

Connection

640x480 and 800x600 flat panel connects directly to J9, using an 18 inches maximum length flat cable with a 50-pin female header at one end, and an adequate connector, adapted to the flat panel model at the other end.

1024x768 flat panel requires an additional cable connected to J1. This extra cable must be 18 inches maximum length, and provide a 26-pin dual-row female header at one end, and an adequate connector, adapted to connector of the flat panel model at the other end.



The PCI-934 board supports many different types of Flat Panel displays. TEKNOR has fully tested a number of these panels and provides all the BIOS software support and the technical information needed to properly interface your PCI-934 board with your selected Flat Panel display.

Downloading Files From the TEKNOR Web Site

If you have access to the Internet, many video BIOS files in a binary format and related interconnection charts in a PDF format are available on our web site. You can download these files, if you are a customer of TEKNOR and have a password from TEKNOR. If you do not have your password, contact TEKNOR's Technical Support to obtain it.

To download a video BIOS file or its interconnection chart file, follow this procedure:

- 1. Access the TEKNOR web site. Our address is <u>http://www.teknor.com</u>.
- 2. Go to the Support & Services section.
- 3. Scroll down the list of products until you find the name of your board and click on it. This selection is a link to the board's support area.
- 4. Click on the Video BIOS link.
- The list of tested Flat Panel displays appears. If you find your particular display, you can then ask to download the associated BIOS or interconnection chart files by clicking the appropriate link.
- 6. A pop-up window appears. You must enter your password (case sensitive) and click the SUBMIT button. Entering your e-mail address is optional. Follow the instructions in subsequent pop-ups to download the file.

More Available From TEKNOR

If you do not have access to our web site, or if you do not see the name of your Flat Panel display on our site for your specific TEKNOR board, then you need to contact TEKNOR's Technical Support department. Since we are always testing new flat panels, it is possible that we have tested your particular type of panel display. Even if we have not tested it, TEKNOR's Technical Support can do it for you and supply the video BIOS and the technical information you need.

BIOS File

The BIOS files are self-extracting files (VXX_XXX.EXE), each including two files: the flat panel BIOS file (VXX_XXX.BFP) and a DOS text file (VXX_XXX.DOC) for the BIOS update utility program.

The letters which form the BIOS name are made up of the following parts:

V	XX _	XX	Х
Video	Video	Version	Revision
BIOS	Controller		

Once you have the correct video BIOS file, you need to copy the video BIOS file to your board's Flash BIOS device. This is done with the BIOS update utility program; see Section 14 to learn how to perform a video BIOS file update with this TEKNOR utility.

Technical Information File

The related technical information file, which includes the interconnection chart, is a PDF (Portable Document Format) file. The name of this file identifies the Flat Panel and the TEKNOR board with its video controller.

Note:

The column labeled EXTERNAL in the Display Interconnection table of the PDF file refers to the external circuitry or supplies which are needed in certain cases. This is usually an external power supply or an inverter frequently used in the clock circuit "SHFCLK" (in the case of V_{LCD} and V_{ADJ} , consult the manufacturer's flat panel data sheet for the actual voltage). An inverter is shown as — \bigcirc —. When no special circuits are shown in this column, connections are direct.

12.1.2 CRT DISPLAYS

The PCI-934 board supports VGA (16M colors), SVGA (16M colors), and XGA (64K colors) standards, and 1280x1024 (256 colors) resolution mode display.

The CRT display connects directly to the standard D-SUB 15-pin male connector located at the edge bracket of the board.

CRT only Display Mode

To setup your system for CRT display only configuration, set the CRT & LCD option to "CRT Only" in the Standard CMOS Setup screen.

Flat Panel Only Display Mode

To setup your system for flat panel display only configuration, set the CRT & LCD option to "LCD Only" in the Standard CMOS Setup screen.

Simultaneous Display Mode

CRT and flat panel displays may be used simultaneously when enabling this mode using the BIOS setup program.

The only restriction when using this mode: both the CRT and the flat panel must be at the same resolution (1024x768 max.).

To setup your system to use both flat panel and CRT displays, set the CRT & LCD option to "Both" in the Standard CMOS Setup screen.

12.1.3 PANELLINK[™] INTERFACE

The board provides a low voltage differential signal (LVDS) implemented through the PanelLinkTM technology. The major advantage of this high-speed interface is to enable a flat panel display to be connected at up to 30 feet from the board using a 3 data pairs and a clock pair cable.

The onboard Panel Link interface may be represented as follows:



Characteristics

The Panel Link is capable of supporting true colors XGA Active Matrix Liquid Crystal Display panels. DSTN with VGA and SVGA resolutions is also possible.

The transmitter takes parallel video/graphics data from the video controller and transmits it serially to a PanelLink receiver at 195MB/sec.

Full color (up to 16.7M colors/pixel for 640x480 and 800x600 resolutions), high-resolution (64K colors for 1024x768 resolution) Active matrix liquid crystal displays at 65MHz pixel clock are supported.

Connection

Connecting a flat panel through the Panel Link connector (J2) requires a Panel Link receiver interface. This interface decodes the serial data and transmit it in parallel to the flat panel, through an 8-pair cable and a 20-pin dual-row female header at one end, and an adequate connectors at the other end for the flat panel display connection.

The cable length is 6 feet with twisted flat cable, and can be increase to 30 feet using high performance individually shielded-pair cable.

Settings

The amplitude of the differential signal is adjusted using the BIOS setup program (BIOS Feature Setup – PanelLink Adjustment option). Higher amplitude provides a better noise immunity but generates more EMI.

The parameter (0-15) should be adjusted to the smallest acceptable value.

12.1.4 NTSC

Video signals are provided to support a future TV-OUT extension for a connection to a CRT monitor via a composite encoder module.

Characteristics

Due to the differences in the standard between PC displays and CRT monitors, the NTSC output depends on of the PAL/NTSC encoder. It may not work in all graphic modes.

Please refer to your encoder documentation

Connection

Please contact the Technical Support Department for more information.

12.1.5 VGA INTERRUPT

The video controller can generate an interrupt request (INTR) signal to indicate that the controller has reached the end of an active field (VSYNC pulse to the CRT monitor).

The interrupt can be connected to and available on the PCI bus INTB line for any PCI devices connected on the bus, or the interrupt can generate an ISA interrupt request.

Settings

To enable the VGA interrupt, install the jumper W12. To connect the interrupt request to the PCI INTB line, install the jumper W9.

12.1.6 V-PORT

The V-Port provides a dedicated video path to the display memory. It is intended to support either a source of live video incoming from an external video source or a MPEG play back from the onboard MPEG decoder.

Characteristics

The interface supports AccuPack or compressed YUV color space format when bandwidth of display memory is limited. The compression/decompression is transparent to the application software. The video data rate through the V-Port path is independent from the surrounding video graphics. Normally, any video loaded through the V-Port is on the top of the surrounding graphics but color key support allows the graphics to occlude the video window with insignificant or loss of video performance.

The V-Port accepts video data at the rate of the original video data and stores it in display memory either in compressed format or directly. As the data transfer rate can be different (and typically lower) that the rate at which the display device is operating, the data can be simultaneously read out from the frame buffer and displayed at the display device rate with real time decompression and transparently to the application software.

Connection

The V-Port interface is available through the J11 connector. This connector is located so it can be combined with the PC/104 connectors (P1/P2) to receive a stackable 8-bit interface for PC/104 form factor products.

A Video Camera Interface PC-104 module is provided by TEKNOR for live video inputs (NTSC, PAL, or S-video formats). It is referred to as TEK-380.

12.2 AUDIO FEATURES

Audio features are provided by the SoundPort[®] chip (AD1816A from Analog Devices), plug and play multimedia audio subsystem, implemented to process multiple digital streams of 16-bit stereo audio requirements.

The chip maintains full legacy compatibility with applications written for SoundBlaster and AdLib, while servicing Microsoft PC 97 application requirements.

Provided features are:

12.2.1 LINE IN

Characteristics

Stereo analog input (left/right): each channel can be independently gained or attenuated from +12dB to -34.5dB in 1.5dB steps. The left and right Line In signals can be mixed in the analog domain with left and right Line Out signals.

Connection

Line In signals connect directly through the J23 Jack connector located on the edge bracket.

12.2.2 LINE OUT

Characteristics

The analog stereo output can be post mixed with any of the analog input signals (Line In, CD, Mic In). The summed analog signal enters the volume stage where each channel of the Line Out can be muted or attenuated from 0dB to -46.5dB in 1.5dB steps.

Connection

Line Out signals are available through the J21 Jack connector located on the edge bracket. The same signals are also available on the Audio I/O connector (J18, pins 13 and 14).

12.2.3 MIC IN

Characteristics

Mono microphone input: Electret type are supported by default, for dynamic microphone utilization, please refer to the factory. The analog signal can be either line level (Line In) or -20dB attenuated from line level, the difference is made up through a software controlled -20dB gain stage.

The microphone input may be processed for conversion or gained/attenuated from +12dB to 34.5dB in 1.5dB steps then mixed with left and right Line Out signals before the volume stage.

Connection

The microphone connects directly to the board through the J22 Jack connector located on the edge bracket. The microphone signal can also be input via the Audio I/O connector (J18, pin 9).

12.2.4 CD IN

Characteristics

Stereo CD-ROM input: each analog channel can be independently gained or attenuated from +12dB to -34.5dB in 1.5dB steps. The left and right CD In signals can be mixed in the analog domain with left and right Line Out signals.

Connection

The CD-ROM connects directly to the board through the J17 onboard connector.

The board provides a standard 4-pin male connector. To connect a CD-ROM use the CD-ROM manufacturer cable.

12.2.5 AUDIO I/O CONNECTOR

Characteristics

The Audio I/O connector provides extra multimedia inputs and outputs connections:

- **AUX1** Stereo audio connector for a video input: left and right signals can be gained and attenuated from +12dB to -34.54dB in 1.5dB steps and mixed with the Line Out signals.
- AUX2 Stereo audio input: left and right signals can be gained and attenuated from +12dB to -34.54dB in 1.5dB steps and mixed with the Line Out signals.
- **OUT** Stereo audio output: same signals as the Line Out signals provided on the J21 Jack connector.
- **MIC** Mono microphone input: same signal as the Mic In signal provided on the J22 Jack connector.

Connection

This connector is provided for customized implementation. The cable must be adapted to the system configuration: It must provide a 14-pin dual-row female header at one end and the adequate connectors, adapted to each device connector.

12.2.6 SPEAKER TO LINE OUT

By default, system PC speaker sounds are provided on both the Multi-I/O connector (J5) and the audio Line Out jack (J21).

To output system PC speaker sounds through the Multi-I/O connector only, use the BIOS setup program to disable this option.

The stereo sound path still remains available for multimedia applications.



SOFTWARE DESCRIPTION

- 13. BIOS SETUPS
- 14. UPDATING THE BIOS WITH UPGBIOS
- 15. VT100 MODE



13. BIOS SETUPS

The PCI-934 uses the AWARD Setup program, a setup utility in EEPROM that is accessed by pressing the DELETE key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.



To run the BIOS setup program incorporated in the ROM BIOS:

Turn on or reboot the system.

Hit the DELETE key before or when the message - "PRESS **DEL** TO ENTER SETUP" appears near the bottom of the screen.

The main menu appears on the screen:

CMOR SETUP UTILITY AWARD SOFTWARE, INC.					
STANDARD CMOS SETUP	INTEGRATED PERIPHERALS				
BIOS FEATURES SETUP	SUPERVISOR PASSWORD				
CHIPSET FEATURES SETUP	USER PASSWORD				
POWER MANAGEMENT SETUP	IDE HDD AUTO DETECTION				
PNP/PCI CONFIGURATION	HDD LOW LEVEL FORMAT				
LOAD BIOS DEFAULTS	SAVE & EXIT SETUP				
LOAD SETUP DEFAULTS	EXIT WITHOUT SAVING				
Esc : Quit	$\uparrow \downarrow \rightarrow \leftarrow$: EXIT WITHOUT SAVING				
F10 : Save & Exit Setup	(Shift)F2 : Change Color				
Time, Date, Hard Disk Type					

13.1 USING THE BIOS SETUP PROGRAM

The arrow keys $(\uparrow \downarrow \rightarrow \leftarrow)$ are used to highlight items on the menu and the PageUp and PageDown keys are used to change the entry values for the highlighted item. To select an entry, press the Enter key. Also, you can press the F1 key to obtain help information or the Esc key to leave an option, close a menu or to quit the program.

The following table provides more details on how to navigate in the Setup program:

Up arrow (↑)	Move to previous item.
Down arrow (\downarrow)	Move to next item.
Left arrow (\leftarrow)	Move to the item in the left hand.
Right arrow (\rightarrow)	Move to the item in the right hand.
Esc key	In Main Menu: Quit settings (Type 'Y' to save changes into CMOS).
	In sub-menus: Exit and return to Main Menu.
PgUp key	Increase the numeric value or make changes.
PgDn key	Decrease the numeric value or make changes.
+ key	Increase the numeric value or make changes.
- key	Decrease the numeric value or make changes.
F1 key	General help.
F2 and Shift F2 keys	Change color from total 16 colors: F2 to select color forward, Shift F2 to select color backward.
F4 key	Reserved.
F5 key	In sub-menu: Restore the previous setup values from BIOS Default Table.
F6 key	In sub-menu: Load the default setup values from BIOS Default Table.
F7 key	In sub-menu: Load the setup values from the Setup Default Table .
F8 key	Reserved.
F9 key	Reserved.
F10 key	When in Main Menu: Save all the CMOS changes.

The Main Menu includes the following categories:

Standard CMOS Setup	This Setup page includes all the items in a standard, AT-compatible BIOS.
BIOS Features Setup	This Setup page includes all the items of AWARD's special enhanced features.
Chipset Features Setup	This Setup page includes all the items of the chipset's special features.
Power Management Setup	This Setup page sets power conservation options.
PnP/PCI Configuration	This Setup page sets Plug and Play and PCI Local Bus configuration options.
Integrated Peripherals	I/O sub-systems that depend on the integrated peripherals controller in your system.
Supervisor/User Password Setting	Change, set, or disable password. It allows you to limit access to the system and the Setup, or just to the Setup.
IDE HDD Auto Detection	Automatically detect and configure hard disk parameters. This ability is included in the event you are uncertain of your hard disk's parameters.
HDD Low Level Format	This option does not appear in many BIOS versions. Most manufacturers of IDE hard drives strongly recommend that you do not run a low-level format on their drives, because of the danger that the bad-track table may be over-written. Award supplies this utility for service personnel only.
	If you feel you need to run a low-level format on your hard drive, contact your drive manufacturer for instructions!
Load BIOS Defaults	The BIOS defaults represent settings that provide the minimum requirements for your system to operate.
Load Setup Defaults	The chipset defaults are settings that provide for maximum system performance.

13.2 SAVING CONFIGURATIONS & EXITING AWARD SETUP

Use one of the following options available from the Main Menu:

Save & ExitUse this option to save the configuration in CMOS RAM. Value
changes are not saved in the Flash EPROM. To update the Flash
memory, use the 'BIOS Setup Feature/Save CMOS in Flash' option.Exit Without
SavingUse this option to exit AWARD Setup without saving the
configuration to CMOS RAM.

13.3 STANDARD CMOS SETUP

This part of the setup allows you to set the time, date, hard disk type, types of floppy drives and video type.

Date/Time	Setup date and time values through the keyboard.			
Hard Disks	Two IDE controllers are defined: Primary and Secondary. Each can support two disks: Master Disk (bootable) or Slave Disk.			
Drive A / Drive B	Identifies floppy disk types (drive A or B) connected to the board.			
Video	Specifies the type of the display adapter card installed in the system.			
CRT & LCD	Use this option to select within CRT display mode only, Flat panel mode only, or both CRT and flat panel display.			
Halt on	This option specifies the type of errors that will stop the system during the BIOS booting procedure. Settings are All errors, No errors, All but keyboard (default setting), All but diskette and All but disk/key.			
Memory	This option summarizes the amount of Base, Extended and other types of memory installed in the system.			

13.4 BIOS FEATURE SETUP

Option	BIOS Default	Setup Default	Possible Settings	Description
Virus Warning	Dis.	Dis.	Dis. ; En.	When Enabled, occurs a warning message if a program (specifically, a virus) attempts to write to the boot sector or the partition table of the hard disk drive. This feature protects only the boot sector, not the entire hard drive.
				Note: Many disk diagnostic programs that access the boot sector table can trigger the virus warning message. If you plan to run such a program, we recommend that you first disable the virus warning.
CPU Internal Cache	En.	En.	Dis. ; En.	Enables or Disables the CPU Internal Cache.
External Cache	Dis.	En.	Dis. ; En.	Enables or Disables the CPU external Cache.
Quick Power On Self Test	Dis.	Dis.	Dis. ; En.	Select Enabled. to reduce the amount of time required to run the power-on self test (POST). A quick POST skips certain steps. We recommend that you normally disable quick POST. It is better to find a problem during POST than lose data during your work.
Boot Sequence	A, C	A, C	C, A, SCSI ; C, CDROM, A ; CDROM, C, A ; D, A SCSI ; E, A, SCSI ; F, A, SCSI ; SCSI, A, C ; SCSI ; SCSI, C only ; A, C, SCSI	The original IBM PCs load the DOS operating system from drive A (floppy disks), so IBM PC-compatible systems are designed to search for an operating system first on drive A, then on drive C (hard disk). However, modern computers usually load the operating system from the hard drive, and may even load it from a CD-ROM drive.
Swap Floppy Drive	Dis.	Dis.	Dis. ; En.	This field is effective only in systems with two floppy drives. Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B.
Boot Up Floppy Seek	Dis.	Dis.	Dis. ; En.	When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360KB floppy drives have 40 tracks; drives with 720KB, 1.2MB, and 1.44MB capacity all have 80 tracks. Because very few modem PCs have 40 track floppy drives, we recommend that you set this field to "Disabled" to save time.
Boot Up NumLock Status	Off	Off	On ; Off	Toggle between On or Off to control the state of the NumLock key when the system boots. When toggled On, the numeric keypad generates numbers instead of controlling cursor operations.
Boot Up System Speed	High	High	Low ; High	Select High to boot at the default CPU speed; select Low to boot at the speed of the AT bus. Some add-in peripherals or old software (such as old games) may require a slow CPU speed. The default setting is High.
Typematic Rate Setting	Dis.	Dis.	Dis. ; En.	When Disabled, the following two items (Typematic Rate and Typematic Delay) are irrelevant. Keystrokes repeat at a rate determined by the keyboard controller in your system. When Enabled, you can select a typematic rate and a typematic delay.
Typematic Rate (Chars/Sec)	6	6	6 to 30 char. per second	When the typematic rate setting is Enabled, you can select a typematic rate (the rate at which characters repeat when you hold down a key in a second).
Typematic Delay (Msec)	250	250	250 ; 500 ; 750 ; 1000 ms	When the typematic rate setting is Enabled, you can select a typematic delay (the delay before key strokes begin to repeat).
Security Option	Setup	Setup	Setup ; System	If you have set a password, select whether the password is required every time the system boots, or only when you enter Setup.
OS Select For DRAM>64MB	Non- OS/2	Non- OS2	Non-OS/2 ; OS/2	Select OS2 only if you are running an OS/2 operating system with greater than 64MB of RAM.

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Option BIOS Setup Description Possible Defau Default Settings When enabled, saves the CMOS parameters in the Flash memory which makes them available in the case of a battery failure. Save CMOS also in Fn Fn Dis. : En. Flash PanelLink Adjustment 7 7 0 to 15 Use this option to control the voltage drive of the PanelLink interface. Increase the value to obtain a higher drive voltage. Video BIOS Shadow En. En. Dis. ; En. Software that resides in a read-only memory (ROM) chip on a device called *firmware*. The Award BIOS allows shadowing of firmware such as the system BIOS, video BIOS, and similar operating instructions that come with some expansion peripherals (for CC000-CFFFF Dis. Dis. Dis.; En. Shadow example, a D0000-D3FFF Shadow Dis. Dis. SCSI adaptor). Shadowing copies of firmware from ROM into system RAM, where the CPU can read it through the 16-bit or 32-bit DRAM Dis.; En. bus. D4000-D7FFF Shadow Dis. Dis. Dis. ; En. Firmware not shadowed must be read by the system through the 8bit X-bus. Shadowing improves the performance of the system D8000-DBFFF Shadow Dis. Dis. Dis.; En. BIOS and similar firmware for expansion peripherals, but it also reduces the amount of high memory (640KB to 1MB) available for loading device drivers, etc. Enable shadowing into each section of memory separately. Many system designers hardwire shadowing of the system BIOS and eliminate a System BIOS Shadow option. Video BIOS shadows into memory area C0000-CBFFF. The remaining areas shown on the BIOS Features Setup screen may be DC000-DFFFF Dis. Dis. Dis. : En. Shadow occupied by other expansion card firmware. If an expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies to shadow it into the correct area of RAM.

BIOS FEATURES SETUP (Continued)

Option Description BIOS Setup Possible Defaul Defaul Settings Auto Configuration selects predetermined optimal values of chipset Auto Configuration En. En. En. ; Dis. parameters. When Disabled, chipset parameters revert to setup information stored in CMOS. Many fields in this screen are not available when Auto Configuration is Enabled. The value in this field depends on performance parameters of the installed memory chips (DRAM). Do not change the value from the DRAM Timing 70 ns 70ns 70 ns, 60ns factory setting unless you install new memory that has a different performance rating than the original DRAMs. Select the number of CPU clocks allocated for the Row Address DRAM RAS# 4 4 4 · 3 Strobe (RAS#) signal to accumulate its charge before the DRAM is Precharge Time refreshed. If insufficient time is allowed, refresh may be incomplete and data lost DRAM R/W Leadoff 7/6 7/6 7/6 ; 6/5 Select the combination of CPU clocks the DRAM on your board Timing requires before each read from or write to the memory. Changing the value from the setting determined by the board designer for the installed DRAM may cause memory errors. Fast RAS# to CAS# 3 3 3;2 When DRAM is refreshed, both rows and columns are addressed Delay separately. Use this item to determine the transition timing from RAS to Column Address Strobe (CAS). DRAM Read Burst x444/x444 Sets the timing for reads from EDO (Extended Data Output) or FPM x444/x x444/x (EDO/FPM) 444 444 x333/x444 (Fast Page Mode) memory. The lower the timing numbers, the faster the system addresses memory. Selecting timing numbers lower than x222/x333 the installed DRAM is able to support can result in memory errors. DRAM Write Burst x444 x444 x444 ; x333 ; Sets the timing for writes to memory. The lower the timing numbers, Timina x222 the faster the system addresses memory. Selecting timing numbers lower than the installed DRAM is able to support can result in memory errors. Turbo Read Leadoff Dis. Dis. En. : Dis. Select Enabled to shorten the leadoff cycles and optimize performance in cacheless, 50-60 MHz, or one-bank EDO DRAM systems. A read request from the CPU to the DRAM controller includes the DRAM Speculative Dis Dis En Dis memory address of the desired data. When Enabled, Speculative Leadoff Leadoff lets the DRAM controller pass the read command to memory sightly before it has fully decoded the address, thus speeding up the read process. When Enabled, the chipset inserts one extra clock to the tum-around of back-to-back DRAM cycles. Turn-Around Insertion Dis. Dis. En.; Dis. ISA Clock PCI PCI PCICLK/4; You can set the speed of the AT bus at one-third or one-fourth of the CLK/4 CLK/4 PCICLK/3 CPU clock speed. System BIOS Dis. En. En., Dis. Selecting Enabled allows caching of the system BIOS ROM at E0000h-FFFFFh, resulting in better system performance. However, Cacheable if any program writes to this memory area, a system error may occur. Video BIOS Cacheable Dis. En. En., Dis. Selecting Enabled allows caching of the video BIOS ROM at C0000h to C8FFFh, resulting in better video performance. However, in any program writes to this memory area, a system error may occur. 8 Bit I/O Recovery 3 1;2;3;4;5; The I/O recovery mechanism adds bus clock cycles between PCI-1 Time 6:7:8:NA originated I/O cycles to the ISA bus. This delay takes place because the PCI bus is so much faster than the ISA bus. These two fields let you add recovery time (in bus clock cycles) for 16-bit and 8-bit I/O. 16 Bit I/O Recovery 1;2;3;4; 2 1 Time NA

13.5 CHIPSET FEATURES SETUP

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Option	BIOS	Setup	Possible	Description	
	Default	Default	Settings		
Peer Concurrency	En.	En.	En. ; Dis.	Peer concurrency means that more than one PCI device can be active at a time.	
Chipset Special Features	Dis.	En.	En. ; Dis.	When Disabled, the chipset behaves as if it were the earlier Intel 82430FX chipset.	
DRAM ECC/PARITY Select	Parity	Parity	ECC ; Parity	Set this option according to the type of DRAM installed in your system: error-correcting code (ECC) or parity (default).	
Memory Parity/ECC Check	Auto	Auto	En. ; Dis. ; Auto	In Auto mode, the BIOS enables memory checking automatically when it detects the presence of ECC or parity DRAM.	
Single Bit Error Report	En.	En.	En. ; Dis.	If ECC is enabled, selecting Enabled here tells the system to report an error (NMI) when a correctable single-bit error occurs.	
				When disabled, a single-bit error will be corrected but not reported. Use this option if your operating system does not support ECC error scrubing.	
L2 Cache Cacheable Size	64MB	64MB	64MB ; 512MB	Select 512MB only if your system RAM is greater than 64MB.	
Chipset NA# Asserted	En.	En.	En. ; Dis.	Selecting Enabled allows pipelining, in which the chipset signals the CPU for a new memory address before all data transfers for the current cycle are complete, resulting in faster performance.	
Pipeline Cache Timing	Faster	Faster	Faster ; Fastest	For a secondary cache of 256KB (one bank), select Faster. For a secondary cache of 512KB (two banks), select Fast (3-1-1-1, 2-1-1) or Fastest (3-1-1, 1-1-1). Cache timing 3-1-1 is at the CPU access speed. It requires special SRAMs because the 3-1-1-1 timing is at the CPU clock rate.	
Passive Release	En.	En.	En. ; Dis.	Select Enabled, to allow CPU to PCI bus accesses during passive release otherwise the arbiter only accepts another PCI master access to local DRAM.	
Delayed Transaction	Dis.	Dis.	En. ; Dis.	The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI version 2.1.	
Memory Hole Location	None	None	512K-640K ; 15M-16M ; None	You can reserve this area of system memory for ISA adapter ROM. When this area is reserved, it cannot be cached. The user information of peripherals that need to use this area of system memory usually discusses their memory requirements.	
Supervisor I/O Base Addr.	190h	190h	190h ; 290h ; 390h	This parameter must reflect the jumper settings for TEKNOR I/O Base Port.	

CHIPSET FEATURES SETUP (Continued)

13.6 POWER MANAGEMENT SETUP

Option	BIOS Default	Setup Default	Possible Settings	Description	
Power Management	Dis.	Dis.	Min Saving ; Max Saving ; User Define, Dis.	This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. Max Saving: Maximum power savings. Inactivity period is 1 minute in each mode. Min Saving: Minimum power savings. Inactivity period is the maximum setting in each mode (1 hour for Doze, Standby and Suspend). User Define: Set each mode individually. Select time-out periods in the PM Timers section (see below).	
PM Control by APM	Yes	Yes	Yes ; No	If Advanced Power Management (APM) is installed on your system, selecting Yes gives better power savings. This enables power management control by an external program (generally the operating system).	
Video Off Method	V/H SYNC + Blank	V/H SYNC + Blank	V/H SYNC + Blank ; DPMS ; Blank Screen	Determines the manner in which the monitor is blanked. V/H SYNC + Blank: System turns off vertical and horizontal synchronization ports and writes blanks to the video buffer. DPMS Support: Select this option if your monitor supports the Display Power Management Signaling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsytem to select video management values.	
Modem Use IRQ	NA	NA	NA;3;4;5;	Assignes the IRQ line to the modem (if any) on your system. Activity	
PM Timers			7,9,10,11	The following modes are Green PC power saving functions. They are user-configurable only during User Defined Power Management mode.	
Doze Mode	Dis.	Dis.	1 - 40 min 1 hour ; Dis.	After the selected period of system inactivity (1 minute to 1 hour), the CPU clock runs at lower speed while all other devices still operate at full speed.	
Standby Mode	Dis.	Dis.	1 - 40 min 1 hour ; Dis.	After entering Doze mode, when the selected period of system inactivity prior to Standby mode (1 minute to 1 hour) has elapsed, the fixed disk drive and the video shut off while all other devices still operate at full speed.	
Suspend Mode	Dis.	Dis.	1 - 40 min 1 hour ; Dis.	After entering Standby mode, when the selected period of system inactivity prior to Suspend mode (1 minute to 1 hour) has elapsed, all devices except the CPU shut off.	
HDD Power Down	Dis.	Dis.	1 - 15 min	After the selected period of drive inactivity (1 to 15 min), the hard disk drive powers down while all other devices remain active.	
Thermal Management	Dis.	Dis.	En. ; Dis.	When enabled, CPU temperature is monitored. Whenever the CPU overheats, it slows down to lower the temperature	
CPU Low Temp.	58	58	30 to 60	The CPU will run at full speed when it is at the selected temperature or lower.	
CPU Overheat	64	64	40 to 70	The CPU will be slowed down when it reaches the selected temperature or higher. Full speed will be resumed when the temperature comes down to the selected 'CPU Low Temp.'.	
CPU Temperature	varies	varies	varies	Display the current CPU temperature, when Thermal Management option is enabled and after the system has been rebooted.	

•••

POWER MANAGEMENT SETUP (Continued)

Option	BIOS Default	Setup Default	Possible Settings	Description
Wake Up Events			On, Off	In Doze or Standby mode, you may disable activity monitoring of
IRQ3	Off	On		svstem.
IRQ4	Off	On		The default wake-up event is keyboard activity. In these wake-up event fields, you can turn On or Off four commonly used interrupts.
IRQ8	Off	On		For example, if you have a modem on IRQ3, you can turn on IRQ3 as a wake-up event, so an interrupt from the modem can wake up the
IRQ12	Off	On		system. Or you may wish to turn Off IRQ12 (the PS/2) mouse as a wake-up event, so accidentally brushing the mouse does not awaken the system.
Power Down and Resume Events			On, Off	You may disable monitoring of common interrupt requests so they do not reset activity timers.
IRQ3 (COM 2)	Off	On		
IRQ 4 (COM 1)	Off	On		
IRQ 5 (LPT2)	Off	On		
IRQ 6 (Floppy Disk)	Off	Off		
IRQ 7 (LPT 1)	Off	On		
IRQ 8 (RTC Alarm)	Off	Off		
IRQ 9 (IRQ 2 Redir)	Off	On		
IRQ 10 (Reserved)	Off	On		
IRQ 11 (Reserved)	Off	On		
IRQ12 (PS/2 Mouse)	Off	On		
IRQ 13 (Coproc.)	Off	On		
IRQ 14 (Hard Disk)	Off	On		
IRQ 15 (Reserved)	Off	On		

13.7 PNP/PCI SETUP

Option	BIOS Default	Setup Default	Possible Settings	Description	
PNP OS Installed	No	No	Yes ; No	If the operating system (OS) is Plug-and-Play, select 'Yes' if you want the OS to allocate resources according to PnP standards, or 'No' if you want the same resource allocation at every system boot- up. Select 'No' when the OS is not PnP (for example DOS).	
Resources Controlled By	Auto	Man.	Auto ; Manual	The Award Plug and Play BIOS can automatically configure all the boot and Plug and Play-compatible devices. If you select Auto, all the interrupt requests (IRQs) and DMA assignment fields disappear, as the BIOS automatically assigns them.	
Reset Configuration Data	Dis.	Dis.	En. ; Dis.	Normally, you leave this field Disabled. Select En. to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.	
IRQ <i>n</i> Assigned To (n=0, 1, 3, 5, 6, 7)			PCI/ISA PnP ; Legacy ISA	When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt:	
				Legacy ISA Devices compliant with the original PC AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1).	
				PCI/ISA PnP Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.	
DMA <i>n</i> Assigned To (n=3, 4, 5, 7, 9, 11, 12, 13, 14, 15)			PCI/ISA PnP ; Legacy ISA	When resources are controlled manually, assign each system DMA channel as one of the following types, depending on the type of device using the interrupt:	
				Legacy ISA Devices compliant with the original PC AT bus specification, requiring a specific DMA channel. PC/ISA PnP Devices compliant with the Plug and Play standard, whether deviced the DC and A bus exhibited the device of the second sec	
PCI IRQ Activated By	Level	Level	Level ; Edge	Leave the IRQ trigger set at <i>Level</i> unless the PCI device assigned to the interrupt specifies Edge-triggered interrupts.	
PCI IDE IRQ Map To	PCI- Auto	PCI- Auto	PCI-Auto; ISA; PCI-SLOT1; PCI-SLOT2; PCI-SLOT3; PCI-SLOT4	This field lets you select PCI IDE IRQ mapping or PC AT (ISA) interrupts. If your system does not have one or two PCI IDE connectors on the system board, select values according to the type of IDE interface(s) installed in your system (PCI or ISA). Standard ISA interrupts for IDE channels are IRQ14 for primary and IRQ15 for secondary.	
Primary IDE INT# Secondary IDE INT#	A	A	A ; B ; C ; D	Each PCI peripheral connection is capable of activating up to four interrupts: $INT# A$, $INT# B$, $INT# C$ and $INT# D$. By default, a PCI connection is assigned INT# A. Assigning INT# B has no meaning unless the peripheral device requires two interrupt services rather than just one. Because the PCI IDE interface in the chipset has two channels, it requires two interrupt services. The primary and secondary IDE INT# fields default to values appropriate for two PCI IDE channels, with the primary PCI IDE channel having a lower interrupt than the secondary.	
Used Mem Base Address	N/A	N/A	NA; C800; CC00 ; D000; D400; D800; DC00	Select a base address for the memory area used by any peripheral that requires high memory.	
Used Mem Length	-	-	4K, 16K, 32K, 64K	Select a length for the memory area specified in the previous field. This field does not appear if no base address is specified.	

13.8 INTEGRATED PERIPHERALS SETUP

Option	BIOS Default	Setup Default	Possible Settings	Description
IDE HDD Block Mode	Dis.	En.	En. ; Dis.	Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.
PCI Slot IDE 2nd Channel	En.	En.	En. ; Dis.	You may separately disable the second channel on an IDE interface installed in a PCI expansion slot.
On-Chip Primary/Secondary PCI IDE	En.	En.	En. ; Dis.	The integrated peripheral controller contains an IDE interface with support for two IDE channels. Select Enabled to activate each channel separately.
IDE Primary/Secondary, Master/Slave PIO	Auto	Auto	Mode 0, 1, 2, 3, 4, Auto	The four IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device.
USB Controller	En.	En.	En. ; Dis.	Select Enabled if your system contains a Universal Serial Bus (USB) controller and you have USB peripherals.
Onboard FDC Controller	En.	En.	En. ; Dis.	Select Enabled if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install an add-in FDC or the system has no floppy drive, select Disabled in this field.
Onboard Serial Ports 1 and 2	Auto	Auto	Dis. ; 3F8/IRQ4 ; 2F8/IRQ3 ; 3E8/IRQ4 ; 2E8/IRQ3 ; Auto	Select a logical COM port name and matching address for the first and second serial ports.
Serial Port 2 mode	RS-232	RS-232	RS-232 ; RS-422 ; RS-485	Communication mode selection for Serial Port 2.
VT100 Mode on Serial Port			1;2	Select a serial port to communicate in VT100 mode with a remote computer. See VT100 Mode section.
Onboard Parallel Port	378/IRQ 7	378/IRQ 7	378h/IRQ7 ; 278h/IRQ5 ; 3BCh/IRQ7 ; Dis.	Select a logical LPT port name and matching address for the physical parallel (printer) port.
Parallel Port Mode	ECP+ EPP 1.9	ECP+ EPP1.9	ECP+EPP1.9; Normal, EPP1.7+SPP; ECP+EPP1.7; SPP; EPP1.9+SPP; ECP	Select an operating mode for the onboard parallel port. Select ECP or EPP unless you are certain both your hardware and software does not support EPP or ECP mode.
ECP Mode Use DMA	3	3	1, 3	Select a DMA channel for the port.

14. UPDATING THE BIOS WITH UPGBIOS

14.1 UPDATING THE BIOS

UPGBIOS is an utility that allows you to take BIOS files from a disk and update the Boot Block Flash BIOS with them.

The command line format is as follows:

UPGBIOS [/ALL filename] • [/VGA VGA_filename] • [/?] [/h]

where:

filename	is the name of the 256KB BIOS file containing all BIOS files. The .BIN extension is used for all BIOS files in a single file.
VGA_filename	is the name of the 64KB file (or less) containing the video BIOS. It will accept various extensions: .VGA, .BFP (flat panel),
? or h	displays instructions on using the UPGBIOS program.

Please note that the UPGBIOS utility program is presently in development. A complete version of UPGBIOS is upcoming.

14.2 CPLD UPGRADE AFTER A BIOS UPDATE

During the first system bootup after you update the Boot Block Flash BIOS with the UPGBIOS utility, the BIOS may need to upgrade the CPLD devices.

WARNING

Whenever the BIOS performs a CPLD hardware upgrade, do not interrupt the system in any way (power down, reset, mouse or keyboard functions). The devices will be damaged and your board rendered inoperative if you disturb the update process!

The following message appears on the screen when the BIOS writes to the devices:

```
A hardware upgrade will be performed on some CPLDs. Follow the instructions below with special care. Do not disturb the process.

DO NOT RESET OR POWER DOWN THE BOARD!!!

Device 1 DO 0% DOMNON DOWN DOWN THE BOARD!!!

Device 2 DO 0% DOMNON DOWNON D
```

The color of the boxes displayed in the message indicates these functions:

Device OK	Green
Device busy	Blue
Device will be updated	Red

• If your device upgrade was successful, the following message is displayed under the "Status:" line prior to rebooting:

Update complete successfully, wait for the automatic reboot. Rebooting in 5 second(s).

If the update is not successful, the following message appears under the "Status:" line:

ERROR: general failure programming CPLDs! Please contact Teknor Industrial Computers technical support.

You must contact TEKNOR's technical support for further instructions.

15. VT100 MODE

The VT100 operating mode allows remote setups of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

1.4 REQUIREMENTS

The terminal should emulate a VT100 or ANSI terminal. Terminal emulation programs such as Telix or Procomm can also be used.

NOTE

Some strange characters may appear on the screen. This occurs because the VT100 recognizes some control characters, and causes them to perform a specific function, for example, screen erase, cursor position, and so on.

1.5 SETUP & CONFIGURATION

Follow these steps to set up the VT100 mode:

- 1. Connect a monitor and a keyboard to your board and turn on the power
- 2. Enter into the CMOS Setup program.
 - 3. Select the VT100 mode and the appropriate COM port and save your setup.
- 4. Connect the communications cable as shown in the next page.

Note: If you do not require a full cable for your terminal, you can set up a partial cable by using only the TXD and RXD lines. To ignore control lines simply loop them back as shown in VT100 Partial Setup cable diagram.

- 5. Configure your terminal to communicate using 8 bits, no parity. The following speeds are available: 2400, 9600, 19200, 38400, 57600, 115200BPS.
- 6. Use the remote keyboard and display to setup the BIOS
- 7. Save the setup, exit, and disconnect the remote computer from the board to operate in stand-alone configuration.

VT100 Full Setup



VT100 Partial Setup

1.6 RUNNING WITHOUT A TERMINAL

The board can boot up without a screen or terminal attached. However, if VT100 Mode is desired, but the terminal is to be disconnected, you must ensure the control lines are in an active state. Failing this, the system may "hang" while waiting for the control lines to become active. Wiring the system according to the Partial Setup allows the lines to remain active. This does not apply if the VT100 mode is disabled.

Furthermore, you can run without any console at all by simply not enabling VT100 Mode and by disabling the onboard video function.



APPENDIX

- A. BOARD SPECIFICATIONS
- B. MEMORY AND I/O MAPS
- C. BOARD DIAGRAMS
- D. CONNECTOR PINOUTS
- E. BIOS SETUP ERROR CODES



A. PRODUCT SPECIFICATIONS

PCI-934			DESCRIPTION	
Overview	Multimedia P	entium MMX Sys	tem Board.	
Supported Microprocessors	Intel Pentium Intel Pentium AMD K6	°® n MMX™	166MHz, 200MHz. 166MHz, 200MHz, 233MHz. Contact TEKNOR.	
Bus Interface	PICMG 2.0, PCI Rev. 2.1 ; 121MB/s PCI burst write, 112MB/s PCI burst read.			
	IBM PC/AT I	mechanical forma	t.	
	ISA: high but	s drive capability.		
	PC/104 ; PC	/104-Plus compation	tible.	
Data Path	64-bit on CPU and video memory bus, 32-bit on PCI bus, 16-bit on ISA bus.			
System Memory	Up to 512MB EDO or FPM DRAM, through four 72-pin SIMMS sockets.			
Cache Memory	Level 1: 32KB (CPU). Level 2: 512KB, write-back with extended cacheability, 15ns pipelined burst.			
Flash Disk	Up to 80MB using CompactFlash device.			
Serial Number	Unique silicon serial number in EEPROM.			
VOs	Serial USB	2 serial ports. 2 Universal Seri	Serial Port 1 configured as RS-232. Serial Port 2 configurable as RS-232, RS-422 or RS-485. al Bus (USB) ports.	
	Parallel	1 multimode parallel port with support of PC/XT, AT, F EPP and ECP operations.		
	Hard Disk	Two Enhanced IDE interfaces for up to 4 devices in Master/Slave configuration. The secondary channel interfaces to CompactFlash disk.		
	Floppy	Two floppy disk	s (1.2MB or 1.44MB).	
	Keyboard	Standard AT ke	yboard	
	Mouse	Standard PS/2	nouse	
	Ethernet	10/100Base-TX	interface	

PCI-934		DESCRIPTION		
Features	BIOS	Award BIOS in Boot Block Flash (256KB) for instant configuration recovery Auto configuration, extended setup, PnP tables Programmable CPU and memory wait states BIOS shadowing in RAM Extension for diskless, keyboardless and videoless operations Ability to boot MS-DOS and user applications from the CompactFlash disk		
	Power Management	Doze, Standby, Suspend, HDD P SMI/SMM Power Management su APM 1.2 compatible	'ower Down upport	
	Thermal	CPU temperature management w	ith low temperature and	
	Clock	Real time clock with battery back	n	
	Supervisory	Two-stage watchdog timer	μ	
	Litilities	Power failure / I ow battery detect	or	
Connectors	CRT	DB-15	I/O bracket	
Connectore	Ethernet	RJ-45 : link/activity LEDs	I/O bracket	
	Line In	3.5mm audio jack	I/O bracket	
	Line Out	3.5mm audio jack	I/O bracket	
	Mic In	3.5mm audio jack	I/O bracket	
	Floppy	34-pin shrouded	onboard	
	EIDE	40-pin shrouded (2)	onboard	
	Flat Panel (FP)	50-pin shrouded	onboard	
	FP Expansion	26-pin shrouded	onboard	
	PanelLink	20-pin shrouded	onboard	
	Kbd, spk, rst	16-pin combo shrouded	onboard	
	Serial	10-pin shrouded (2)	onboard	
	Parallel	26-pin shrouded	onboard	
	USB	10-pin shrouded	onboard	
	V-Port	26-pin	onboard	
	CD In	4-pin locking	onboard	
	Mic In, AUX1 In, AUX2 In, Line C	, 10-pin Dut	onboard	
	I2S Digital Audio	o 4-pin	onboard	
	PS/2 Mouse	4-pin locking	onboard	
	CPU Fan	2-pin locking	onboard	
	PC/104 Plus	Expansion header	onboard	

PCI-934	DESCRIPTION			
Electrical/Mechanical Characteristics	Conforms to IEEE P996 PC/AT bus, PCI Rev.2.1, PICMG 2.0, and PC/104-Plus Rev.1.0 specifications.			
Dimensions	13.3 x 4.80 x 0.062 inches 338 x 122 x 1.57 mm			
Operating System Compatibility	PC and MS-DOS [®] Windows [®] 3.X Windows [®] 95 Windows [®] NT NOVELL TM OS/2 [®] WARP QNX TM UnixWare TM SCO UNIX TM			
Audio, MPEG-1 and VIPerVision API support	PC and MS-DOS [®] , Windows [®] 95, Windows [®] NT, (MPEG-1 pending for Windows NT)			
Power Requirements	Supply Voltage Pentium MMX ICC typ. * +5V ICC suspend * +5V +12V * Measured with 16MB DRAM, fl	Vcc=+5V ±5% / =+12V ±5% Dual DC/DC for split voltage Pentium. 166 200 233 3.79A 4.04A 2.26A 2.19A 2.22A 2.26A 250mA 250mA 250mA		
Reliability	MTBF Agency Approvals USB ank keyboard current pr	Over 90,000 hours (MIL-HDBK-217F) FCC 47 CFR Part 15 ; Level A, CE Mark to CISPR 22 Class B otected by self-resetting fuses		
Environnemental Conditions	Operating Temperature Storage Temperature Humidity	0 to 60°C (w/airflow) - 5 to 95% RH -20 to 70°C - 0 to 95% RH 5% to 95% RH		

B. BOARD DIAGRAMS

B-1 PCI-934 – ASSEMBLY DIAGRAM (TOP)



B-2 PCI-934 – ASSEMBLY DIAGRAM (BOTTOM)



B-3 PCI-934 – CONFIGURATION DIAGRAM



B-4 PCI-934 – MECHANICAL DIAGRAM



C. CONNECTOR PINOUTS

C.1 XVGA CONNECTOR - J1

Pin Number		Top View
Signal		
BFP20	1	
BFP21	3	
BFP22	5	
BFP23	7	
BFP26	9	
BFP27	11	
BFP28	13	
BFP29	15	
BFP32	17	
BFP33	19	
BFP34	21	
BFP35	23	
POT_HI	25	

	Pin Number
	Signal
2	GND
4	GND
6	GND
8	GND
10	GND
12	GND
14	GND
16	GND
18	GND
20	FPVCC_SW
22	FPVCC_SW
24	VCON
26	POT_LO

C.2 PANELLINK CONNECTOR - J2

Pin Number		Top View		Pin Number
Signal				Signal
GP0	1		2	+12V
GP1	3		4	GND
GP2	5		6	GND
VCC	7		8	VCC
TXC-	9		10	TXC+
VCC3	11		12	VCC3
TX0-	13		14	TX0+
TX1-	15		16	TX1+
TX2-	17		18	TX2+
FPVCC_SW	19		20	PD

C.3 EIDE CHANNEL 1 CONNECTOR - J3

Pin Number	Top View		Pin Number	
Signal				Signal
RESET#	1		2	GND
D7	3		4	D8
D6	5		6	D9
D5	7		8	D10
D4	9		10	D11
D3	11		12	D12
D2	13		14	D13
D1	15		16	D14
D0	17		18	D15
GND	19		20	Not Connected
DRQ0	21		22	GND
IOW#	23		24	GND
IOR#	25		26	GND
IORDY	27		28	PU
DAK0	29		30	GND
IRQ	31		32	IOCS16#
A1	33		34	GND
A0	35		36	DA2
CS1#	37	39 40	38	CS3#
ACT#	39		40	GND

Active Low Signal

C.4 FLOPPY DISK CONNECTOR - J4

Pin Number		Top View	Pin Number	
Signal				Signal
GND	1		2	DRVEND#
GND	3		4	Not Connected
GND	5		6	Not Connected
GND	7		8	INDEX#
GND	9		10	MTR0#
GND	11		12	FPDS1#
GND	13		14	FPDS0#
GND	15		16	MTR1#
Not Connected	17		18	FPDIR#
GND	19		20	STEP#
GND	21		22	WDATA#
GND	23		24	WGATE#
GND	25		26	TRK0#
Not Connected	27		28	WRTPRT#
Not Connected	29		30	RDATA#
GND	31	35 36	32	HDSEL#
Not Connected	33		34	DSKCHG#

Active Low Signal

C.5 MULTIFUNCTION CONNECTOR - J5

Pin Number	Top View	
Signal		
KCLK	1	1
KDAT	3	
VCC	5	
SPKR	7	
ACFAIL#	9	
Not Used	11	
PBRES#	13	
HDACT#	15	15 16

Pin Number					
	Signal				
2	GND				
4	GND				
6	VCC				
8	VCC				
10	GND				
12	GND				
14	GND				
16	VCC				

Active Low Signal

C.6 SERIAL PORT 1 CONNECTOR - J6

Pin Number Signal	Top View	Pin Number Signal	
DCD# RXD 3 TXD 5 DTR# GND 5	$ \begin{bmatrix} 1 & & & & \\ 3 & & & & \\ 5 & & & & \\ 7 & & & & \\ 9 & & & & \\ \end{bmatrix} $	2 DSR 4 RTS# 6 CTS# 8 RI# 10 Not Connected	

Active Low Signal

C.7 SERIAL PORT 2 CONNECTOR (RS-232) - J7

Pin Number		Top View	Pin Number	
Signal				Signal
DCD# RXD TXD DTR# GND	1 3 5 7 9		2 4 6 8 10	DSR RTS# CTS# RI# Not Connected

Active Low Signal

C.8 SERIAL PORT 2 CONNECTOR (RS-422/RS-485) - J7

Pin Number	Pin Number		Pin Number	
Signal				Signal
DCD# RX(-) TX(-) DTR# GND	1 3 5 7 9		2 4 6 8 10	DSR RX(+) TX(+) RI# Not Connected

Active Low Signal

C.9 FAN CONNECTOR - J8



C.10 FLAT PANEL CONNECTOR - J9

Pin Number		Top View		Pin Number
Signal				Signal
BFP2	1		2	BFP3
BFP4	3		4	BFP5
BFP8	5		6	BFP9
BFP10	7		8	BFP11
BFP13	9		10	BFP12
BFP7	11		12	BFP6
BFP17	13		14	BFP16
BFP15	15		16	BFP14
GND	17		18	BFPVDCLK
GND	19		20	BFP25
GND	21		22	BLF5
BFP1	23		24	BFP18
GND	25		26	BFPDE
GND	27		28	GND
BFP24	29		30	GP0
GP1	31		32	GND
BFPVEE	33		34	GND
BLLCLK	35		36	GND
BFPVEE	37		38	BFPVCC
BFP0	39		40	GP2
STANDBY#	41		42	BFP30
BFP19	43		44	BFP31
ACTI	45		46	FPDECTL
FPVCC_SW	47	49 50	48	FPVCC_SW
+12V	49		50	+12V

Active Low Signal

C.11 EIDE CHANNEL 2 CONNECTOR - J10

Pin Number		Top View		Pin Number
Signal				Signal
RESET#	1		2	GND
D7	3		4	D8
D6	5		6	D9
D5	7		8	D10
D4	9		10	D11
D3	11		12	D12
D2	13		14	D13
D1	15		16	D14
D0	17		18	D15
GND	19		20	Not Connected
DRQ1	21		22	GND
IOW#	23		24	GND
IOR#	25		26	GND
IORDY	27		28	PU
DAK1	29		30	GND
IRQ0	31		32	IOCS16#
A1	33		34	GND
A0	35		36	A2
CS1#	37	39 40	38	CS3#
ACT#	39		40	GND

C.12 V-PORT CONNECTOR - J11

Pin Number	Top View	
Signal		
GND	Z1	Z1 🔲 🖸 Y1
GND	Z2	
GND	Z3	
I2C_DATA	Z4	
VP_VSYNC	Z5	
EN_CAM#	Z6	
VCC	Z7	
GND	Z8	
GND	Z9	
GND	Z10	
GND	Z11	
ZVPCLK	Z12	
VACTI	Z13	Z13 🔲 🔲 Y13

	Pin Number
	Signal
Y1	VPC0
Y2	VPC1
Y3	VPC2
Y4	VPC3
Y5	VPC4
Y6	VPC5
Y7	VPC6
Y8	VPC7
Y9	I2C_CLK
Y10	VP_HSYNC#
Y11	VP_IO_1
Y12	VP_IO_2
Y13	GND

Active Low Signal

C.13 NTSC OUT CONNECTOR - J12

Pin Number		Top View	Pin Number	
Signal				Signal
RED	1	1 2	2	GND
GREEN	3		4	GND
BLUE	5		6	GND
CSYNC	7		8	GND
TVON	9		10	GND
NTSC_PAL	11		12	GND
HSYNC	13	13 14	14	VSYNC

C.14 PARALLEL PORT CONNECTOR - J13

Pin Number		Top View
Signal		
STB#	1	
PD0	3	
PD1	5	
PD2	7	
PD3	9	
PD4	11	
PD5	13	
PD6	15	
PD7	17	
ACK#	19	
BUSY	21	
PE	23	
SLCT	25	250 0 26

	Pin Number
	Signal
2	ALF#
4	ERR#
6	INIT#
8	SLCTIN#
10	GND
12	GND
14	GND
16	GND
18	GND
20	GND
22	GND
24	GND
26	GND

Active Low Signal

C.15 USB CONNECTOR - J14

Pin Number	Top View	
Signal		
SVB0 SBP0- SBP0+ GND GND	1 3 5 7 9	

	Pin Number
	Signal
2	SVB1
4	SBP1-
6	SBP1+
8	GND
10	GND

C.16 PS/2 MOUSE CONNECTOR - J15

Pin Number	Front View	
Signal		
MCLOCK	1	
GND	2	
MDAT	3	
VCC	4	5

C.17 I²S CONNECTOR (NO MPEG) - J16

Pin Number	Top View	
Signal		
BCLK	1	
LRCLK	2	
DATA	3	1 4
GND	4	

C.18 CD IN CONNECTOR - J17

Pin Number	Pin Number	
Signal	Signal	
L_CD AUDIOGND R_CD AUDIOGND	1 2 3 4	1 4

C.19 AUDIO I/O CONNECTOR - J18

Pin Number		Top View	Pin Number	
Signal				Signal
R_AUX1	1	1 2	2	AUDIOGND
L_AUX1	3		4	AUDIOGND
R_AUX2	5		6	AUDIOGND
L_AUX2	7		8	AUDIOGND
MIC_IN	9		10	AUDIOGND
AUDIOGND	11		12	AUDIOGND
LL_OUT	13	13 14	14	RL_OUT

Pin Number Top View **Pin Number** Signal Signal D11 1 GND 2 2 D12 3 4 D3 D13 5 6 D4 7 D5 D14 8 D15 9 10 D6 CS3# 11 12 D7 Not Connected 14 CS1# 13 Not Connected 15 16 IOR# Not Connected 17 18 IOW# MIRQ0 19 20 VCC VCC 21 22 VCC GND 23 24 GND RESET# 25 26 GND FD_MASTER# 27 28 A2 ACT# 29 A1 30 Not Connected 31 32 A0 D8 D0 33 34 36 D9 DD1 35 DD2 37 38 D10 39 40 IOCS16# 39 40 GND

C.20 FLASH DISK CONNECTOR - J19

C.21 CRT VGA CONNECTOR - J20

Signal		Signal		Signal		Top View
RED	1	Analog GND	6	Not Connected	11	6
GREEN	2	Analog GND	7	Not Connected	12	
BLUE	3	Analog GND	8	HSYNC	13	
Not Connected	4	Not Connected	9	VSYNC	14	0 <mark>00</mark>
GND	5	GND	10	Not Connected	15	5-0-15

C.22 LINE OUT CONNECTOR - J21





C.23 MIC IN CONNECTOR - J22

Signal				Top View
GND	1	4 V		1
MIC_IN	2	3		
GND	3		5	3
Not Connected	4	1	4	2
GND	5			

C.24 LINE IN CONNECTOR - J23



C.25 ETHERNET CONNECTOR - J24

Signal	
TX+	1
TX-	2
RX+	3
Not Connected	4
Not Connected	5
RX-	6
Not Connected	7
Not Connected	8

Top View



	Α	В		С	D	
1	5V_KEY	RESERVED		+5V	AD00	1
2	VI/O (5V)	AD02		AD01	+5V	2
3	AD05	GND		AD04	AD03	3
4	C/BE0#	AD07		GND	AD06	4
5	GND	AD09	ABCD	AD08	GND	5
6	AD11	VI/O (5V)	1	AD10	MM66EN	6
7	AD14	AD13		GND	AD12	7
8	+3.3V	C/BE1#		AD15	+3.3V	8
9	SERR#	GND		SB0#	PAR	9
10	GND	PERR#		+3.3V	SDONE	10
11	STOP#	+3.3V		LOCK#	GND	11
12	+3.3V	TRDY#		GND	DEVSEL#	12
13	FRAME	GND		IRDY#	+3.36V	13
14	GND	AD16		+3.3V	C/BE2#	14
15	AD18	+3.3V		AD17	GND	15
16	AD21	AD20		GND	AD19	16
17	+3.3V	AD23		AD22	+3.3V	17
18	IDSEL0 (AD24)	GND		IDSEL1 (AD25)	IDSEL2 (AD16)	18
19	AD24	C/BE3#		VI/O (5V)	IDSEL3 (AD27)	19
20	GND	AD26		AD25	GND	20
21	AD29	+5V		AD28	AD27	21
22	+5V	AD30	30	GND	AD31	22
23	REQ0	GND		REQ1#	VI/O (5V)	23
24	GND	REQ2#		+5V	GNT0#	24
25	GNT1	VI/O (5V)		GNT2#	GND	25
26	+5V	CLK		GND	CLK	26
27	CLK	+5V		CLK	GND	27
28	GND	INTD#		+5V	RST#	28
29	+12V	INTA#		INTB#	INTC#	29
30	-12V	RESERVED		RESERVED	3.3V_KEY	30

C.26 PC/104-PLUS CONNECTOR - J25

Active Low Signal

C.27 PC/104 CONNECTORS - P1 AND P2

	P1			P2		
	D	С		A	В	
			A B	IOCHK# SD7 SD6	GND Reset Drv	1 2 3
0				SD5 SD4 SD3 SD2 SD1	VCC (+5V) IRQ9 -5V DRQ2 -12V	4 5 6 7 8
0 1 2 3 4 5	MEMCS16# IOCS16# IRQ10 IRQ11	GND SBHE# LA23 LA22 LA21		IOCHRDY AEN SA19 SA18 SA17	0WS# +12V GND SMEMW# SMEMR#	9 10 11 12 13
5 6 7 8 9	IRQ12 IRQ15 IRQ14 DACK0# DRQ0	LA20 LA19 LA18 LA17 MEMR#	P2	SA17 SA16 SA15 SA14 SA13	IOW# IOR# DACK3# DRQ3	14 15 16 17 18
10 11 12 13	DACK5# DRQ5 DACK6# DRQ6	MEMW# SD8 SD9 SD10		SA12 SA11 SA10 SA9	DACK1# DRQ1 REFRESH# SYSCLK	19 20 21 22
14 15 16 17 18	DACL7# DRQ7 VCC (+5V) MASTER# GND	SD11 SD12 SD13 SD14 SD15		SA8 SA7 SA6 SA5 SA4	IRQ6 IRQ5 IRQ4 IRQ3	23 24 25 26 27
19	GND	GND		SA3 SA2 SA1 SA0	DACK2# T/C BALE VCC (+5)()	28 29 30 31
				GND	OSC14M GND GND	32

C-12

D. MEMORY AND I/O MAPS

D.1 MEMORY MAP DIAGRAM



ADDRESS	FUNCTION	
00000-9FFFF	0-640 KB DRAM	
A0000-BFFFF	Video DRAM	
C0000-CBFFF	Video BIOS	
CC000-DFFFF	Free DRAM	
E0000-FFFFF	System BIOS	
100000-Top of DRAM	1 MB - Top of DRAM	

D.2 I/O MAPPING

ADDRESS	OPTIONAL ADDRESS			FUNCTION
000-00F				DMA Controller 1
020-03F				Interrupt Controller 1
040-043				Timer
060-064				Keyboard (8742)
070-071				Real-time clock, NMI mask
080-09F				DMA Page Register
0A0-0BF				Interrupt Controller 2
0C0-0DF				DMA Controller 2
0EC-0EF				Configuration Registers
190-197	290-297	390-397		TEKNOR Control Port
0F0-0FF				Math Coproc/ Config. Reg.
1F0-1F7, 3F6				Primary IDE
170-177, 376				Secondary IDE
3F0-3F7	370-377			Floppy Disk
378-37A	3BC-3BE	278-27A		Parallel Port (LPT1 by default)
3F8-3FF	2F8-2FF (COM2)	3E8-3EF	2E8-2EF	UART1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	3E8-3EF (COM3)	2E8-2EF (COM4)	UART2 (COM2 by default)
3C0-3CF, 3D0-3DF, 3B0-3BB				Graphics Controller

NOTE

The I/O addresses for the onboard Plug and Play Ethernet device are automatically allocated by the System BIOS.

E. BIOS SETUP ERROR CODES

E.1 POST MESSAGES

During the Power On Self Test (POST), if the BIOS detects an error requiring your attention, it will either sound a beep code, display a message, or both.

If a message is displayed, it will be accompanied by: "PRESS F1 TO CONTINUE, DEL TO ENTER SETUP".

E.2 POST BEEP

Currently there is only one beep code in BIOS. This code indicates that a video error has occurred and BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps.
E.3 ERROR MESSAGES

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

CMOS BATTERY HAS FAILED

CMOS battery is no longer functional and should be replaced, or battery jumper is removed and should be installed.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This can indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace it if necessary. It can also happen if the battery jumper is removed: in such a case, it should be installed.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP

Type of diskette drive installed in the system is different from CMOS definition. Run Setup to reconfigure the drive type correctly.

DISPLAY TYPE HAS CHANGED SINCE LAST BOOT

Since last powering off the system, the display adapter has been changed. You must configure the system for the new display type.

ERROR ENCOUNTERED INITIALIZING HARD DRIVE

Hard drive cannot be initialized. Be sure the adapter is installed correctly and all cables are correctly and firmly attached. Also be sure the correct hard drive type is selected in Setup.

ERROR INITIALIZING HARD DRIVE DISK CONTROLLER

Cannot initialize controller. Make sure the cord is correctly and firmly installed on the CPU board. Be sure the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set on the hard drive.

FLOPPY DISK CNTRLR ERROR OR NO CNTRLR PRESENT

Cannot find or initialize the floppy drive controller. Make sure the controller is installed correctly and firmly. If there are no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause BIOS to ignore the missing keyboard and continue the boot.

MEMORY ADDRESS ERROR AT ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory.

MEMORY PARITY ERROR AT ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory.

MEMORY VERIFY ERROR AT ...

Indicates an error verifying a value already written to memory. You can use this location along with the memory map for your system to find and replace the bad memory.

OFFENDING SEGMENT

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

PRESS A KEY TO REBOOT

This will be displayed at the bottom of the screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a non-maskable interrupt condition during boot, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

RAM PARITY ERROR - CHECKING FOR SEGMENT ...

Indicates a parity error in Random Access Memory.

E.4 POST CODES

NOTE

ISA POST codes are output to port address 80h.

POST (hex)	Name	Description	
01	BOOT BLOCK	Boot Block in EMERGENCY : Clear Base Memory Area.	
03	Initialize Chips	1. Clear CMOS shutdown byte.	
		 Initialize EISA extended registers. (Not for us since we don't have EISA bus.) 	
04	Test Memory Refresh Toggle	RAM must be periodically refreshed in order to keep the memory from decaying.	
05	Blank Video, Initialize Keyboard	1. Clear CMOS reset status byte. Boot Block in <u>EMERGENCY</u> : Initialize Keyboard Controller.	
		2. Early Keyboard initialization.	
06	EPROM Checksum	 Test F000h segment shadow readable and writeable for POST access correct. If not, show POST FE and beep continuously 	
		2. Autodetect Flash EPROM.	
07	Test CMOS Interface and	1. Install the TEKNOR segment.	
	Battery Status	2. Verifies CMOS is working correctly (walking bit test).	
		3. Restore CMOS from Flash if option is enabled.	
		4. Check for OVERRIDE KEY (INSERT key).	
08	Program Chipset default	Program Chipset default (show POST BEh).	
09	Early Cache Initialization	1. Check for Intel's and/or Cyrix CPU.	
		 Early Cache Initialization when cache is separate from chipset. 	
		3. Turn off Gate A20.	
0A	Setup Interrupt Vector Table	 Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize int. 00h-1Fh according to INT_TBL. 	
		2. Early Power Management Initialization.	

PCI-934 Technical Reference Manual

POST (hex)	Name	Description		
0B	Test CMOS RAM Checksum	1.	Verify time and date for valid	d values.
		2.	If Override enabled, check for If Override key pressed, Kill	or Override key. I CMOS checksum.
		3.	Check CMOS Battery (usele enabled since it's already do	ess if save CMOS in FLASH one).
		4.	Verify Checksum, if bad, loa	ad defaults.
		5.	Copy CMOS in the stack.	
		6.	Clear CMOS Alarm date.	
		7.	Clear HD if Hidden.	
		8.	Clear Floppy "B" if only one	drive.
		9.	Detect for a Math Co-proces	ssor.
		10.	Set Fast Gate A20 Flag in C	CMOS.
		11.	If "B" drive only is set the 2 [Drive are set
		12.	Program Chipset for early P	ower Management.
		13.	P6 Bios Update (if applicabl	e).
		14.	Kill Onboard PnP IO.	
		15.	PnP Early Initialization.	
		16.	PnP System Resource: 1. Get ESCD. 2. Create default SYSTEM_ 3. Decode/Record ISA ESCI 4. Record I/O port for PnP o	MAP. D resources. peration.
		17.	Chipset Early Shadow.	
0C	Initialize Keyboard	1.	Open Xilinx I/O Port location to x90h (X=1,2 or 3) inside the chipset (if necessary).	Boot Block 1 st : Verify BIOS checksum.
		2.	Disable (if necessary). Thermal Management.	Boot Block in EMERGENCY 2 nd : Init. vector 00h through 77h
		3.	Disable (if necessary) Ethernet Chip.Set IDE Detect counter to 0.	
		4.	Set CD-ROM found variable to 0.	
		5.	Initialize zone 40:0h for the keyboard buffer.	

E-6

POST (hex)	Name	Description	
OD	Initialize Video Interface & Chipset	 On M1 set the cache for the memory installed. On PCI, do a PCI ROM init. On P6, Init. Apic. Init. Chipset. Turn ON CPU Cache. Set Maximum Speed. Measure CPU Clock Speed. Restore Speed. Turn Off CPU Cache. Early Video Shadow. Read CMOS location 14h to find out type of video to use. Detect and initialize Video Adapter. Init. T380 if necessary. 	
OE	Test Video Memory	 If CGA or MONO, test video memory. Beep the speaker. Show the LOGO. Install VT100 driver if necessary. Write sign-on message to screen. Write Copyright message to screen. Write Evaluation message to screen. Show CPU type and speed. 	
0E	Tost DMA Controllor 0	6. Show CFO type and speed.	
10	Test DMA Controller 1	Test DMA Controller 0.	
11	Test DMA Page Registers	Test DMA Page Registers	
12	Reserved	Reserved for 8254 Counter 0 - Not implemented	
13	Reserved	Reserved for 8254 Counter 1 - Not implemented	
14	Test Timer Counter 2	Test 8254 Timer () Counter 2	
15	PIC Test 8259-1 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off	
		and on the interrupt lines.	
16	PIC Test 8259-2 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	
17	Test Struck 8259's Interrupt Bits	Nothing	
18	Test 8259 Interrupt functionality	Force an interrupt and verify that the interrupt occurred (IRQ 0 - clock int. 8h).	
19	Test Struck NMI Bits (Parity/ IO check)	Nothing.	
1A : : 1E	Reserved : : Reserved	Reserved : : Reserved	
1F	Set EISA Mode	If EISA non-volatile memory checksum is good, execute EISA initialization. If no, execute ISA test and clear EISA mode flag. Test EISA Configuration Memory integrity (checksum & communication interface).	

POST (hex)	Name	Description	
20			
:	Enable Slot 0 to 15	Initialize slot 0 (System Board) to slot 15.	
2F			
30	Size Base & Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB.	
31	Test Base & Extended Memory	1. Test base memory from 256K to 640K and extended memory above 1MB using various patterns.	
		2. The last test if filling memory with 0's.	
		 On a quick memory test or if user press the ESC key while testing memory, only the last test is performed. 	
		NOTE: This will be skipped in EISA mode and can be "skipped" with ESC key in EISA mode.	
32	Test EISA Extended Memory	If EISA Mode flag is set, then test EISA memory found in slots Initialization.	
		NOTE 1: This will be skipped in ISA mode and can be "skipped" with ESA key in EISA mode.	
		NOTE 2: This POST also Detect & Report I/O PORTS and also Init. Super IO.	
33	Reserved	Reserved	
:	:	:	
:	:	:	
3B	Reserved	Reserved	
3C	Setup Enable		
3D	Initialize & Install PS/2 Mouse	Detect if mouse is present. Initialize mouse. Install interrupt vector.	
3E	Setup Cache Controller	Initialize cache controller.	
3F	Reserved	Reserved	
40	Reserved	Reserved	
41	Initialize Floppy Drive & Controller	 Verify if we should enter setup. If so, enter setup. Initialize floppy disk drive controller and any drive. Boot Block in <u>EMERGENCY</u>: Scan for Floppy for emergency disk 	
42	Initialize Hard Drive & Controller	Initialize hard drive controller and any drive. (Call HD_INSTALL).	
43	Detect & Initialize Serial/Parallel/Joystick ports	Initialize any serial, parallel and game ports.	
44	Reserved	Reserved	
45	Detect & Initialize Math Coprocessor	Initialize Math Coprocessor.	
46	Reserved	Reserved	

POST (hex)	Name	Description
47	Set Speed for Boot	Set Speed for Boot.
48 : :	Reserved : :	Reserved
40		Reserved
4D	Init. PC-Speaker to LINE OUT	(T934).
4E	Manufacturing POST Loop or display Messages	 Reboot if Manufacturing POST Loop pin is set. Otherwise display any messages (i.e., any non-fatal errors that were detected during POST). Enter SETUP if needed.
4F	Security Check	Ask password security if needed.
50	Write CMOS	Write all CMOS values back to CMOS-RAM and clear screen.
51	Pre-Boot Enable	 Enable Parity checker. Enable NMI. Enable cache before boot.
52	Initialize Option (ROM scan)	 Call POST 81 Initialize any ROM's present from C8000h to DBFFFh. Disable POST code from segment E0000h. Initialize any ROM's present from DC000h to E0800h. NOTE: When FSCAN option is enabled, will initialize from C8000h to F7FFFh.
53	Initialize Time Value	Initialize Time value in 40h: BIOS area.
54 : : 5F	Reserved : : Reserved	Reserved : : Reserved
60		Store boot partition of head & cylinder.
61	Final Init	For last µs detail before boot.
62	Num Lock ON	Put Num Lock ON and Daylight Saving.
63	Boot Attempt	 Call POST 82. Set Low stack. Boot via int 19h.
64	Reserved	Reserved
: : 7F	: : Reserved	: : Reserved

POST (hex)	Name	Desci	ription
80	Teknor Segment Move 1	Install the Teknor segment from Flash to DC00:0h.	
81	Teknor Segment Move 2	Install the Teknor segment from DC00:0h to 7000:0h.	
82	Teknor Segment Move 3	Install the Teknor segment from 7	'000:0h to EC00:0h.
83	Check & Program CPLD	Check & Program CPLD for valid	UserCode & IDCode.
84	Reserved	Reserved	
:	:	:	
:	:	:	
AF	Reserved	Reserved	
B0	Spurious	If interrupt occurs in protected mo	ode.
B1	Unclaimed NMI	If unmasked NMI occurs, display:	
		Press F1 to disable NMI, F2 rebo	ot.
B2	Reserved	Reserved	
:	:	:	
:		:	
BD	Reserved	Reserved	
BE	Early Prog Chipset Def.	Going to early program chipset to POST_8s).	default values (called from
BF	Program Chip Set	Called early at POST 0Dh to prog	ram chipset from CT-TABLE.
C0	Turn ON/OFF Cache	OEM Specific - Cache control.	Boot Block: First POST.
C1	Memory presence	OEM Specific - Test to size on- board memory test.	Boot Block: Search for Boot Block Signature "*BBSS*".
C2	Early Memory Initialization	OEM Specific - Board Initialization	۱.
C3	Extended Memory Initialization	OEM Specific - Turn ON extended memory DRAM select.	Boot Block: Expand compressed BIOS
C4	Special Display Switch Handling	OEM Specific - Display/Video swi errors never occur.	tch handling so that display switch
C5	Early Shadow	OEM Specific - Early Shadow enable for fast boot.	Boot Block: Early Shadow System BIOS.
C6	Cache Programming	OEM Specific - Routine for programming which region are cacheable.	Boot Block: Cache Sizing
C7	Reserved	Reserved	
C8	Special Speed Switching	OEM Specific - Routine to handle speed switching.	
C9	Special Shadow Handling	OEM Specific - Normal Shadow routine.	
CA	Very Early Initialization	OEM Specific – Initialize hardware before any other hardware initialization.	
СВ	Reserved	Reserved	
:	:	:	
:	:		
CF	Reserved	Reserved	

POST (hex)	Name	Description
D0	Power Management Full speed	Trying to go back or into full speed mode.
D1	Power Management Doze mode	Trying to go or in Doze mode.
D2	Power ManagementSleep mode	Trying to go or in Sleep mode.
D3	Power Management – Suspend mode	Trying to go or in Suspend mode.
:	:	:
:	:	:
DF	Debug	Available POST codes for use by source code customers during development.
E0	Reserved	Reserved
:	:	:
:	:	:
EE	Setup Page	Page 14
EF	Shadow Error	In POST 6 to signal a Shadow Error.
F0	Reserved	Reserved
:	:	:
:	:	:
FE	Reserved	Reserved
FF	Boot	The system is now booted or waiting for an OS.

F. EMERGENCY PROCEDURES

Follow this procedure only in case of emergency such as a critical error during the boot block flash BIOS update (when using UPGBIOS utility program or saving AWARD parameters in flash) or if you meet one of the following symptoms at anytime.

F.1 SYMPTOMS

- 1. No POST code on a power up (when using a POST code card).
- 2. System stops at POST 41h (when using a POST code card; see tables in previous section), associated beep code is generated and the system tries to read from the floppy drive.
- 3. Board does not boot.

F.2 MAKING AN EMERGENCY DISKETTE

Use a system that has a 1.44MB floppy drive A.

- 1. Insert the TEKNOR EMERGENCY diskette in drive A:
- 2. Copy the two files WDISK.COM and EMERDISK.TEK from drive A: to your hard drive (those files are available in your TEKNOR diskette package).
- 3. Remove the TEKNOR EMERGENCY diskette
- 4. Format a diskette in drive A:.
- 5. At the DOS prompt of your hard drive (the same directory as the two files WDISK.COM and EMERDISK.TEK), type WDISK and then press Enter.

The program may display one of the following messages:

"Emergency Code transferred"

The emergency diskette has been successfully created.

Take the appropriate actions and restart from step 4 when you see the following messages:

"Write to disk failure!"

Verify if your floppy diskette is write-protected.

"The file to program in flash was not found"

Be sure that EMERDISK.TEK file is in your current directory.

"Unable to read the binary file" or "Unable to close the opened file"

Possible floppy diskette corruption or bad data transfer between floppy disk and host system.

"Unable to allocate a memory block of 256 Kbytes"

Not enough memory to run the WDISK program.

F.3 EMERGENCY PROCEDURE

To run an emergency procedure, proceed as follows:

- 1. Remove battery jumper W5 to disconnect the battery from the board circuitry.
- 2. Install the EMERGENCY diskette in the floppy drive A (1.44MB) connected to the PCI-934 board.
- 3. Power on the board. (Nothing appears on the screen.)
- 4. The Boot Block Flash update will be completed when you see POST code 55 (when using a POST code card; see table below) or hear the associated beep code (see table below) or when the floppy drive stops. If you see POST code 22, 33 or 44, an error has occured. You should repeat the emergency procedure. If repeated attempts at updating the boot block flash fail, that is, you are unable to generate POST code 55, contact the TEKNOR Technical Support department.
- 5. After the procedure is successfully completed, power down the board, set your battery jumper as it was previously and power up the board. Your PCI-934 boot block flash BIOS should be correctly programmed and the system should run properly.

NOTE

If the emergency disk has been lost, see section G.2: Making an *Emergency Diskette*.

Emergency Procedure POST Codes

POST	Description
Code	
XX	Post code counter displaying emergency file block number loaded from floppy.
11	Begin the flash reprogramming process.
22	Error when getting the boot block flash ID code.
33	Error when erasing the boot block flash.
44	Error when programming the boot block flash.
55	Success of the boot block recovery code.

Emergency Procedure Beep Codes

POST Code	Beep Code	Description
41	**_*	Enterring the boot block recovery code (i.e. Main BIOS checksum error).
22	*_*_*	Error when getting the boot block flash ID code.
33	*_*_*	Error when erasing the boot block flash.
44	*_*_*_*	Error when programming the boot block flash.
55	*_*	Success of the boot block recovery code. The board is ready to be manually reset.

⁴ 1 Beep code

Silence

GETTING HELP

At TEKNOR we take great pride in our customer's successes. We strongly believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, you may contact our Technical Support department at:

CANADIAN HEADQUARTERS	EUROPEAN REGIONAL OFFICE
Tel.: (450) 437-5682	Tel.: +49 811 / 600 15-0
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If you have any questions about TEKNOR, our products or services, you may reach us at the above numbers or by writing to:

TEKNOR INDUSTRIAL	TEKNOR INDUSTRIAL
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J7G 2A7 CANADA	GERMANY

LIMITED WARRANTY

TEKNOR INDUSTRIAL COMPUTERS INC. ("the seller") warrants its boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

Getting Help 1

Returning Defective Merchandise

If your TEKNOR product malfunctions, please do the following before returning any merchandise:

- Call our Technical Support department in Canada at (450) 437-5682 or in Germany at +49 811 / 600 15-0. Make certain you have the following at hand: <u>the TEKNOR</u> <u>Invoice #, your Purchase Order #, and the Serial Number of the defective board.</u>
- 2) Give the serial number found on the back of the board and explain the nature of your problem to a service technician.
- 3) If the problem cannot be solved over the telephone, the technician will further instruct you on the return procedure.
- 4) Prior to returning any merchandise, make certain you receive an RMA # from TEKNOR's Technical Support and clearly mark this number on the outside of the package you are returning. To request a number, follow these steps: make a copy of the request form on the following page, fill it out and fax it to us.
- 5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.
- 6) When returning a TEKNOR board:
 - i) Make certain that the board is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.
 - ii) Ship prepaid to (but not insured, since incoming units are insured by TEKNOR):

TEKNOR INDUSTRIAL
COMPUTERS INC.TEKNOR INDUSTRIAL
COMPUTERS INC.616 Cure BoivinZeppellin Str. 4Boisbriand, QuebecD-85399 HallbergmoosJ7G 2A7 CANADAGERMANY

Getting Help 2



RETURN TO MANUFACTURER AUTORIZATION REQUEST

Contact Name:		
Company Name:		
Street Address:		
City:	Province / State:	
Country:	Postal / Zip Code:	
Phone Number:	Fax Number:	
Extension:		

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)
		RMA-02

Fax this form to TEKNOR's Technical Support department in Canada at (450) 437-8053 or in Germany at +49 811 / 600 15-33