DIGITAL 5/233i CompactPCI™ Single-Board Computer

User Manual

Order Number: EK–SB233–UM. A01

This manual describes the DIGITAL 5/233i single-board computer (SBC); explains how to configure, maintain, and troubleshoot the SBC; and provides information on technical details such as address mapping and system interrupts.

Revision/Update Information: This is a new manual.

Digital Equipment Corporation
Maynard, Massachusetts

First Printing, May 1998

FCC Notice:

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Warning!

This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

Achtung!

Dieses ist ein Gerät der Funkstörgrenzwertklasse A. In Wohnbereichen können bei Betrieb dieses Gerätes Rundfunkstörungenauftreten, in welchen Fällen der Benutzer für entsprechende Gegenmaßnahmen verantwortlich ist.

Attention!

Ceci est un produit de Classe A. Dans un environment domestique, ce produit risque de créer des interférences radioélectriques, il appartiendra alors à l'utilisateur de prendre les mesures spécifiques appropriées.

Canadian EMC Notice:

“This Class [A] digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.”

“Cet appareil numérique de la class [A] respecte toutes les exigences du règlement sur le matériel broilleur du Canada.”

Note: Shielded data cables must be used to interconnect this equipment to comply with the FCC limits for a Class A device.

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Preface

Purpose of this Manual

This manual describes the DIGITAL 5/233i single-board computer (SBC); explains how to configure, maintain, and troubleshoot the SBC; and provides information on technical details such as address mapping and system interrupts.

Intended Audience

This manual is for OEM system integrators who are designing and building a DIGITAL 5/233i single-board computer (SBC) into specific application systems. These systems may range in scope from a single DIGITAL 5/233i SBC to highly complex multiprocessor systems that include a variety of hardware. Hardware and mechanical engineers refer to the physical and environmental specifications. Field and manufacturing technicians and support specialists use information in this manual to configure systems and diagnose problems.

This manual assumes readers have prerequisite knowledge and experience with the following:

- System design
- CompactPCI design and specifications

Structure of this Manual

This manual consists of nine chapters, two appendixes, and an index organized as follows:

- Chapter 1, Specifications and Requirements, provides product specifications; physical, power, and environmental requirements; and FCC regulations.
- Chapter 2, Module Components, introduces the physical components of the SBC.
- Chapter 3, Functional Components, describes the SBC's functional components.
- Chapter 4, System Startup, discusses powering the system on and off.
- Chapter 5, Configuring the System, explains how to use the American Megatrends' WINBIOS Setup utility.

- Chapter 6, Upgrading and Replacing SBC Components, explains how to remove the SBC from a system, upgrade or replace main memory, and adjust jumper settings.
- Chapter 7, Connectors and Headers, describes the DIGITAL 5/233i SBC and rear transition module connectors and headers.
- Chapter 8, System Address Mapping and Interrupts, discusses system address mapping and system interrupts.
- Chapter 9, System Management, describes and explains how to use watchdog timer and system monitoring features.
- Chapter 10, Troubleshooting System Problems, provides some guidance with troubleshooting SBC problems.
- Appendix A, BIOS Option Summary, summarizes the BIOS menu options.
- Appendix B, Error Messages and Checkpoint Codes, lists error messages, blink codes, and checkpoint codes generated by the DIGITAL 5/233i SBC.

Conventions

This section defines terminology, abbreviations, and other conventions used in this manual.

Bit Notation

Multiple-bit fields can include contiguous and noncontiguous bits contained in angle brackets (< >). Multiple contiguous bits are indicated by a pair of numbers separated by a colon (:). For example, <9:7,5,2:0> specifies bits 9, 8, 7, 5, 2, 1, and 0. Similarly, single bits are frequently indicated with angle brackets. For example, <27> specifies bit 27.

Keyboard Keys

The following keyboard key conventions are used throughout this manual.

Convention	Example
Control and Alt key sequences are represented as Ctrl/*X*. Press Ctrl or Alt while you simultaneously press the *X* key.	Ctrl/C
In plain text, key names match the name on the actual key.	Return key
In tables, key names match the name of the actual key and appear in square brackets ([ ]).	[Return]

Examples

Prompts, input, and output in examples are shown in a monospaced font. Interactive input is differentiated from prompts and system output with bold type. For example:

```
>>> echo This is a test.[Return]
This is a test.
```

Ellipsis points indicate that a portion of an example is omitted.

Names and Symbols

The following table lists typographical conventions used for names of various items throughout this manual.

Items	Example
Bits	**sysBus<32:2>**
BIOS option	**External Cache** option
BIOS option values	***Enabled***
Files and pathnames	`/usr/foo/bar`
Pins	LIRQ pin
Signals	**iogrant** signal
Variables	*n*, *x*, *mydev*

Numbering

Numbers are decimal unless otherwise indicated. The prefix h indicates a hexadecimal number. For example, 19 is decimal, but h19 and h19A are hexadecimal. Otherwise, the base is indicated by a superscript; for example, 100^2 is a binary number.

Ranges and Extents

Ranges are specified by a pair of numbers separated by two periods (..) and are inclusive. For example, a range of integers 0..4 includes the integers 0, 1, 2, 3, and 4.

Extents are specified by a pair of numbers in angle brackets (< >) separated by a colon (:) and are inclusive.

Bit fields are often specified as extents. For example, bits <7:3> specifies bits 7, 6, 5, 4, and 3.

Register and Memory Figures

Register figures have bit and field position numbering starting at the right (low-order) and increasing to the left (high-order).

Memory figures have addresses starting at the top and increasing toward the bottom.

Syntax

The following syntax elements are used throughout this manual. Do not type the syntax elements when entering information.

Element	Example	Description
[ ]	[**-file** *filename*]	The enclosed items are optional.
|	- | + | =	Choose one of two or more items. Select one of the items unless the items are optional.
{ }	{- | + | =}	You must specify one (and only one) of the enclosed items.
( )	(a,b,c)	You must specify the enclosed items together.
...	arg...	You can repeat the preceding item one or more times.

UNPREDICTABLE and UNDEFINED

This manual uses the terms UNPREDICTABLE and UNDEFINED. Their meanings are different and must be carefully distinguished.

UNPREDICTABLE results or occurrences do not disrupt the basic operation of the processor. The processor continues to execute instructions in its normal manner. In contrast, UNDEFINED operations can halt the processor or cause it to lose information.

Special Notices

This section lists special notices that are used in this manual.

Warning

A warning indicates the presence of a hazard that can cause personal injury if the hazard is not avoided.

Caution

A caution indicates the presence of a hazard that might cause damage to hardware or might corrupt software.

Note

A note emphasizes important information.

Abbreviations

The following abbreviations are used in this manual:

Abbreviation	Meaning
BIOS	Basic input/output system
CD-ROM	Compact-disc read only memory
CPU	Central processing unit
DMA	Direct memory access
DRAM	Dynamic random access memory
EDO	Extended data out
EIDE	Enhanced integrated drive electronics
ESD	Electrostatic discharge
FPM	Fast page mode
HDD	Hard disk drive
HP	Horizontal pitch
IDE	Integrated drive electronics
I/O	Input/output
IRQ	Interrupt request
ISA	Industry standard architecture
MMX	Multimedia Extension
MS–DOS	Microsoft Disk Operating System
OEM	Original equipment manufacturer
PCI	Peripheral components interface
PICMG	PCI Industrial Computers Manufacturers Group
POST	Power-on self test
PSU	Power supply unit
ROM	Read only memory
RTC	Real-time clock
RTM	Rear transition module
SBC	Single-board computer
SCSI	Small computer system interconnect
SIMM	Single in-line memory modules
SVGA	Super video graphics array
TOY	Time of year
TSR	Terminate stay resident

Abbreviation	Meaning
USB	Universal serial bus
Windows NT	Microsoft Windows NT environment
ZIF	Zero insertion force

For More Information

For more information, refer to the following:

- Your supplier
- The DIGITAL OEM web site at `http://www.digital.com/oem`
- The following documentation:
  - *DIGITAL 5/233i-8 CompactPCI System Warranty and Parts Information*, EK–SY233–WI
  - DIGITAL 5/233i-8 CompactPCI System online help, **http://www.digital.com/oem**
  - *PCI Local Bus Specification*, Revision 2.1
  - *CompactPCI Specification*, Revision 2.0
  - *PCI to PCI Bridge Architecture Specification*, Revision 1.0

Latest Product Information and Updates

You can access product information and download the latest BIOS, device drivers, and software updates over the Internet from:

http://www.digital.com/oem

1
Specifications and Requirements

This chapter discusses specifications and requirements for the DIGITAL 5/233i CompactPCI single-board computer (SBC). Specifically, Sections 1.1 through 1.4 discuss:

- Product Specifications
- Physical Requirements
- Power Requirements
- Environmental Specifications

Section 1.5 discusses the product's regulatory compliance.

1.1 Product Specifications

Table 1–1 lists the DIGITAL 5/233i CompactPCI SBC specifications.

Table 1–1 DIGITAL 5/233i CompactPCI SBC Specifications

CPU	Pentium with MMX technology at 233 MHz
Bus interface	PCI bus (220-pin) fast/fully buffered (33 MHz) 2 mm pin-and-socket connector (IEC 1076-4-101)
Cache	32 KB CPU cache 512 KB Level 2 write-back cache 8 ns synchronous pipelined burst with extended capability
Memory	Two banks of two 72-pin SIMM sockets Up to 256 MB of 60 ns EDO memory Parity or ECC via Intel 82430HX chipset
Addressing	Real (36-bit) and protected (32-bit on bus access)
Data paths	64-bit on CPU bus 32-bit on PCI bus
Interrupts	11 edge-sensitive and configurable Four PCI level sensitive configurable to any interrupt vector plug and play compatibility ISA on-card interrupts are plug and play compliant
DMA channels	Four 8-bit Three 16-bit Support scatter-gather, F type DMA

Table 1–1 DIGITAL 5/233i CompactPCI SBC Specifications (Continued)

I/O	Two Universal Serial Bus (USB) ports Two RS 232 (16550) serial ports with 16-byte FIFO Bidirectional parallel port that supports all IEEE 1284 protocols Industry-standard diskette interface Bus master PCI EIDE with LBA and mode 4 support PCI Ultra Fast/Wide SCSI-3 (Adaptec 7880) Shielded twisted-pair (STP) PCI 10/100 Mb Ethernet, 10BASE-T, 100 BASE-TX (82557ETherExpress(TM) Pro/100B compatible) PCI SVGA with 1 MB of EDO memory (Cirrus Logic GD5446)
Clock/calendar	Real-time clock with replaceable battery backup Includes CMOS
SBC connectors	Two USB ports PS/2 keyboard/mouse combination (6-pin mini-DIN) Two serial ports (dual stacked 9-pin micro-D) Parallel port (25-pin micro-D) SCSI-3 (68-pin receptacle) SVGA (15-pin D-sub) Ethernet (RJ-45)
BIOS features	AMI WIN BIOS in flash EPROM Field upgradable Auto configuration/extended setup Serial and parallel ports can be remapped Extensions for systems that run without a disk, keyboard, or video monitor BIOS POST and Setup console can be redirected to a serial port Programmable memory wait states System and video BIOS shadowing
Supervisory	Software programmable, 2-level watchdog timer (17.8 ms to 291 sec.) that drives interrupt 11 (configurable), NMI, or system reset Monitor microcontroller for backplane voltage, SBC temperature (user definable alarm on IRQ 11) Guarded reset switch on front panel Front panel LEDs: power OK (green), speaker output (amber), alarm (red), link (green), activity (amber), disk activity (green)
Mechanical	6U x 8HP wide (233 mm x 160 mm x 41 mm) Conforms to PICMG CompactPCI 2.0 and PCI SIG 2.1 specifications
Power input	~40 W (without cache or DRAM)

Table 1–1 DIGITAL 5/233i CompactPCI SBC Specifications (Continued)

Power requirements	+5 V 5.5 A (dual DC/DC for split voltage Pentium) +12 V 0.1 A +3.3 V 1.6 A
Reliability	MTBF: 1,000,000 hours @ 25 degrees C (MIL-HDBK_217F)
Regulatory conformance	FCC Class A CE Mark

1.2 Physical Requirements

The DIGITAL 5/233i CompactPCI SBC has the industry-standard 6U form factor and requires a single backplane slot and dual-width (8 HP) front panel space in a CompactPCI chassis.

1.3 Power Requirements

The DIGITAL 5/233i CompactPCI SBC requires power voltages of +3.3V, +5 V, and +12 V. The CompactPCI backplane provides the power to the logic of the SBC through the P1 and P2 CompactPCI connectors.

Table 1–2 provides the power ratings for the various voltage supplies supported by the DIGITAL 5/233i CompactPCI SBC.

Table 1–2 Input Power Requirements

Voltage Supply	Maximum Memory	Minimum Memory
+3.3 V	1.5 A	1.6 A
+5 V	5.5 A	5.0 A
+12 V	0.100 A	0.100 A

1.4 Environmental Specifications

Table 1–3 shows the environmental specifications for the DIGITAL 5/233i CompactPCI SBC.

Table 1–3 Environmental Specifications

Condition	Range or Value
Operating	
Temperature range	0° C to 50° C (32° F to 122° F)
Relative humidity	10% to 95% noncondensing
Altitude	10,000 feet with derating
Maximum wet bulb	28° C (82° F)
Minimum dew point	2° C (36° F)
Vibration	5-16 Hz 0.020 in. (0.5mm) DA 16-200 Hz 0.25G peak (2.5 m/sec.) 200-500 Hz 0.1G peak (1.0 m/sec.)

Table 1–3 Environmental Specifications (Continued)

Condition	Range or Value
Shock	10 G 30 ms
Meantime between failures	> 100,000 hours @ 55 ° C (MIL-HDBK_217F)
Nonoperating	
Temperature range	–40 ° C to 66 ° C (–40 ° F to 151 ° F)
Storage (shipping)	40,000 feet
Relative humidity	0 to 95% noncondensing
Maximum wet bulb	32 ° C (90 ° F)
Vibration	1.5 G

Notes

Real failures for MBTF figures are defined as random component failures that are not caused by customer errors, workmanship related failures, third-party component issues, or design related problems where corrective action has been implemented.

The operating temperature range is 0 ° C to 50 ° C. This is dependent on sufficient enclosure air flow to keep the CPU case temperature at or below 70 ° C.

1.5 Regulatory Compliance

The DIGITAL 5/233i CompactPCI SBC has been tested and shown to operate within a suitable enclosure with the following regulatory compliances for a Class A device:

- EMC
- CE
- VCCI limits

These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used as instructed in the *DIGITAL 5/233i- CompactPCI SBC Installation Guide*, may cause harmful interference to radio communications. Operation of a DIGITAL 5/233i CompactPCI SBC in a residential area is likely to cause harmful interference, in which case the interference is required to be corrected at the user's own risk.

When used in an appropriate enclosure, a DIGITAL 5/233i CompactPCI SBC can operate at the level of a Class A device. If used as a Class A device, your application may require shielded cables for all I/O interfaces.

Note

It is incumbent upon Original Equipment Manufacturers (OEMs) to obtain regulatory FCC approval for a consolidated system.

2

SBC Module Components

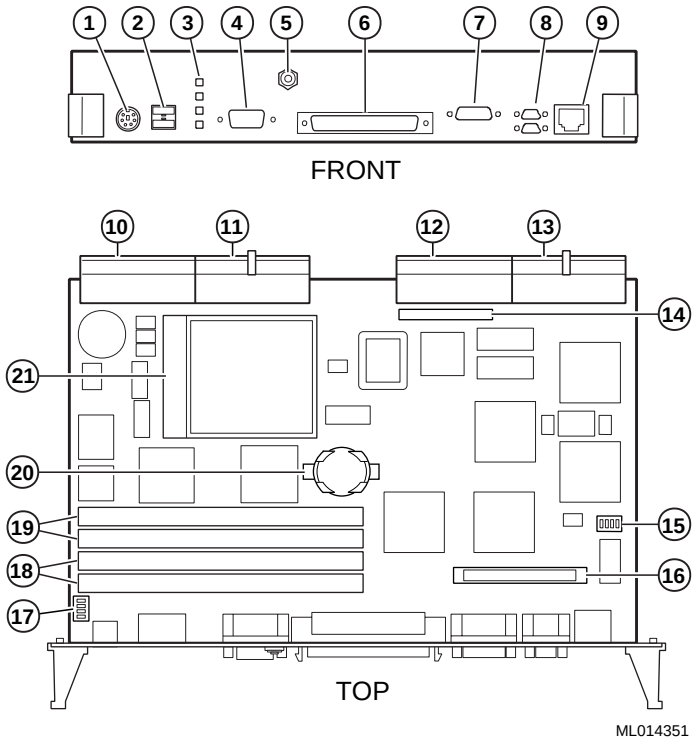
The DIGITAL 5/233i single-board computer (SBC) consists of a single CPU module and support modules that provide memory. This chapter describes the SBC module components. The chapter describes the following:

- CPU Module
- Memory Modules

2.1 CPU Module

Figure 2–1 shows the layout and identifies connectors, headers, and jumpers on the SBC.

Figure 2–1 SBC Layout



The numeric callouts in the figure identify the following key components:

1 PS/2 keyboard and mouse connector — 6-pin PS/2 female

2 USB connectors — dual 4-pin USB

3 Status LEDs (top-to-bottom – power, hard disk drive, speaker, alarm)

4 SVGA connector — 15-pin D-SUB

5 CPU reset button

6 SCSI connector — 68-pin high density

7 Bidirectional, EPP/ECP parallel port — 25-pin micro-D

8 Serial ports 1 and 2 (16550) — 9-pin micro-D

9 Ethernet connector — RJ45

10 J5 Compact PCI connector

11 J4 CompactPCI connector

12 J2 CompactPCI I/O connector

13 J1 CompactPCI I/O connector

14 Reserved

15 Ethernet jumper for front or rear I/O selection

16 Reserved

17 USB jumper for front or rear I/O selection

18 SIMM connectors for memory bank 0

19 SIMM connectors for memory bank 1

20 Lithium battery

21 Pentium P55C MMX CPU

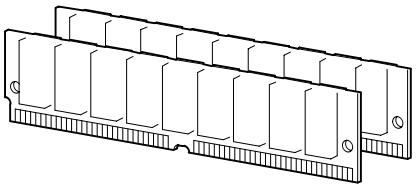
2.2 Memory Modules

The DIGITAL 5/233i SBC is shipped with at least 32 MB of dynamic random access memory (DRAM) and supports memory configurations that range from 32 to 256 MB of DRAM. This memory is accessible from the CPU and PCI bus.

You can plug either two or four 36-bit 16, 32, or 64 MB SIMMs into the memory connectors on the SBC. SIMMs must be 36 bits wide.

Figure 2–2 shows a typical pair of memory modules.

Figure 2–2 Pair of Memory Modules



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When installing memory, you must adhere to the following requirements:

- SIMMs must be installed in pairs. That is, you must populate the memory banks with one of the following combinations:
  - Two slots: slot 0 (J6) of bank 0 and slot 1 (J7) of bank 0
  - Two slots: slot 0 (J8) of bank 1 and slot 1 (J9) of bank 1
  - Four slots: slots 0 and 1 of banks 0 and 1

- SIMMs installed in a given memory bank must be of the same size. For example, if you install a 64 MB SIMM in slot 0 of bank 0 you must install a 64 MB SIMM in slot 1 of bank 0.
- All SIMMs must be 60 ns extended data out (EDO) SIMMs.

Table 2–1 shows valid SIMM combinations.

Table 2–1 Valid SIMM Combinations

Total Memory	Bank 0 Slot 0 (J6)	Bank 0 Slot 1 (J7)	Bank 1 Slot 0 (J8)	Bank 1 Slot 1 (J9)
32 MB	16 MB	16 MB		
64 MB	16 MB	16 MB	16 MB	16 MB
64 MB	32 MB	32 MB		
96 MB	16 MB	16 MB	32 MB	32 MB
96 MB	32 MB	32 MB	16 MB	16 MB
128 MB	32 MB	32 MB	32 MB	32 MB
128 MB	64 MB	64 MB		
160 MB	16 MB	16 MB	64 MB	64 MB
160 MB	64 MB	64 MB	16 MB	16 MB
192 MB	32 MB	32 MB	64 MB	64 MB
192 MB	64 MB	64 MB	32 MB	32 MB
256 MB	64 MB	64 MB	64 MB	64 MB

3

SBC Functional Components

This chapter describes the functional components associated with the DIGITAL 5/233i CompactPCI single-board computer (SBC). Topics include:

- Functional Component Overview
- Intel Pentium Processor with MMX Technology
- Memory
- Level 2 Cache
- Flash ROM
- Local PCI Bus and Bridges
- Clocks and Timers
- Ethernet Controller
- Ultra SCSI Controller
- Video Controller
- Ultra I/O Controller
- LM78 System Monitor

3.1 Functional Component Overview

Figure 3–1 identifies the functional components of the DIGITAL 5/233i Compact-PCI single-board computer (SBC). The SBC is based on the 32-bit Pentium P55C MMX processor and runs at 233 MHz. Either two or four main memory SIMMs provide from 32 to 256 MB of EDO memory. In addition, the SBC provides 512 KB of Level 2 (L2) pipelined burst cache.

The SBC uses a high-performance 32-bit PCI bus as its local system bus. The processor and memory subsystem connects to the PCI bus through a PCI bus host bridge. This bridge provides a low latency path through which the processor directly accesses PCI devices mapped anywhere in memory or I/O address spaces. The bridge also provides a high-bandwidth path that allows PCI bus masters direct access to main memory.

The processor and memory subsystem interfaces with integrated peripheral controllers and add-on option modules through the PCI host bridge and over the local PCI bus. As Figure 3–1 shows, onboard integrated peripheral controllers include:

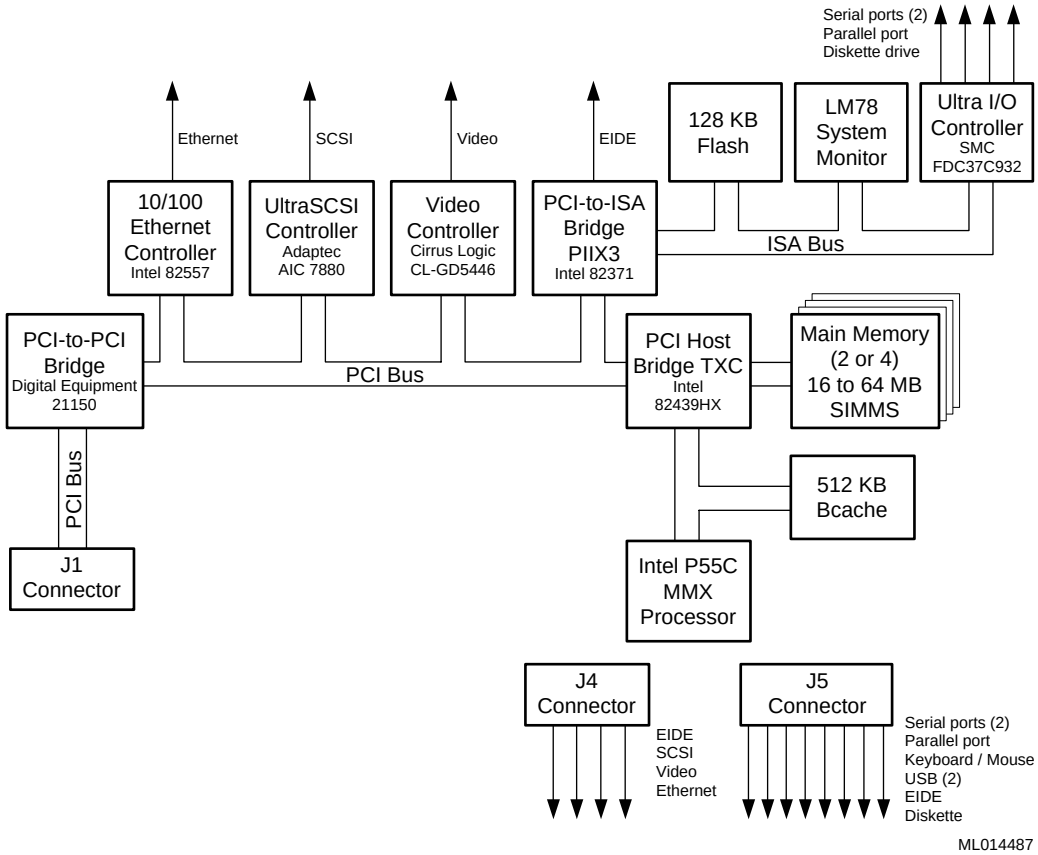
- 10/100 Fast Ethernet controller
- Ultra Wide SCSI controller
- SVGA Video controller

A PCI-to-ISA bus bridge provides access to:

- IDE device control
- Universal serial bus (USB) control
- 128 KB of flash ROM
- LM78 system monitor
- Ultra I/O controller, which supports serial ports, a parallel port, and the diskette drive

A third bridge, the PCI-to-PCI bridge, provides PCI access to the J1 connector on the CompactPCI backplane.

Figure 3–1 Functional Components of the SBC



3.2 Intel Pentium Processor with MMX Technology

The SBC is based on the 32-bit Intel Pentium processor with MMX technology at 233 MHz. This is a superscalar pipelined processor manufactured using enhanced Intel CMOS silicon technology.

In addition to supporting standard features of the Pentium processor family, such as a 64-bit data bus, the Pentium processor with MMX technology features:

- MMX technology for supporting highly parallel, repetitive sequences found in multimedia and communication applications

- 32 KB of onchip cache — 16 KB of code cache and 16 KB of write-back data cache — that uses the MESI cache protocol
- Improved branch prediction
- Enhanced pipelines and pipelined integer, MMX, and floating-point units
- Deeper write buffers
- Virtual mode extensions

For more information, see the processor data sheet and documentation available on the Intel web site at `http://www.intel.com`/design/MMX/ and `http://www.intel.com`/design/pcisets/.

3.3 Memory

The SBC supports two or four dynamic random access memory (DRAM) SIMMs for memory configurations that range from 32 to 256 MB. The memory resides in two banks. The SIMMs in a given bank must be the same size (16, 32, or 64 MB) and all must be 60 ns extended data out (EDO) SIMMs. Table 2–1 lists valid SIMM combinations. The amount of main memory installed is detected by the BIOS automatically when the SBC is powered on.

The width of the memory data path is 64 bits. Operating at this width, the memory bus can achieve a maximum burst bandwidth of 264 MB/sec (8 bytes at 33 MHz).

Parity generation and checking is provided for each byte of memory. Additionally, the chip set provides single-bit error checking and correction (ECC) and double bit detection with parity error generation for 36-bit SIMMs. ECC, if supported by the operating system, greatly enhances reliability and data integrity.

3.4 Level 2 Cache

The SBC provides 512 KB of onboard secondary Level 2 write-back cache. This cache consists of two 32-bit x64 KB 7 ns onboard pipelined burst SRAMs. Features of the Level 2 cache include tag and control logic that is contained in the 82434NX PCMC core.

3.5 Flash ROM

The onboard BIOS is stored in a 256 KB (2 Mb) flash ROM. The flash ROM has a boot block and can be reprogrammed at power up from a diskette. The SBC has a catastrophic flash recovery process.

3.6 Local PCI Bus and Bridges

The local PCI bus serves as the base of the I/O subsystem, connecting all of the system's PCI devices. The PCI bus is an industry standard, high-performance 32-bit bus with multiplexed address and data lines. The bus can operate at up to 33 MHz and has a peak bandwidth of 132 MB.

The local PCI bus interconnects the processor/memory subsystem with components of the I/O subsystem, which includes integrated peripheral controllers and peripheral expansion modules. The I/O subsystem consists of the following PCI devices:

Device	Manufacturer/Part Number	Description
PCI host bridge, TXC	Intel, 82439HX	Connects the processor and memory subsystems to the PCI bus and each other.
PCI-to-ISA bridge, PIIX3	Intel, 82371	Provides integrated USB and IDE control while connecting the ISA bus components — Flash memory, LM78 system monitor, and Ultra I/O — to the PCI bus.
Video controller	Cirrus Logic, CLGD5446	Video controller.
Ultra SCSI controller	Adaptec, AIC 7880	SCSI controller.
Ethernet controller	Intel, 82558	Ethernet controller.
PCI-to-PCI bridge	DIGITAL, 21150	Connects the CompactPCI J1 connector to the PCI bus.

Extensive buffering and buffer management within bridges ensures maximum efficiency in all three bus environments: the host CPU bus, PCI bus, and ISA bus.

The PCI host bridge provides a low latency path through which the processor directly accesses PCI devices mapped in memory or I/O address spaces. This bridge also provides a high-bandwidth path that gives PCI bus masters direct access to main memory.

Auto-configuration support for PCI expansion boards and components simplifies system upgrades and expansion.

Table 3–1 shows the PCI interrupt routing.

Table 3–1 PCI Interrupt Routing

Component	Bus #	IDSel	Device #	Req/Grant	INTA	INTB	INTC	INTD
Host bridge	0	—	00h	N/A	—			
PCI-to-ISA bridge	0	AD18	07h	PHOLD	—			
Ethernet controller	0	AD31	14h	0	PIRQB			
Video controller	0	AD30	13h	—	PIRQC			
PCI-to-PCI bridge	0	AD29	12h	1	—			
SCSI controller	0	AD28	11h	2	PIRQD			
Slot 1	1	AD31	0Fh	1–0	PIRQD	PRIQA	PIRQB	PIRQC
Slot 2	1	AD30	0Eh	1–1	PIRQC	PIRQD	PIRQA	PIRQB

Table 3–1 PCI Interrupt Routing (Continued)

Component	Bus #	IDSel	Device #	Req/Grant	INTA	INTB	INTC	INTD
Slot 3	1	AD29	0Dh	1–2	PIRQB	PIRQC	PIRQD	PIRQA
Slot 4	1	AD28	0Ch	1–3	PIRQA	PIRQB	PIRQC	PIRQD
Slot 5	1	AD27	0Bh	1–4	PIRQD	PIRQA	PIRQB	PIRQC
Slot 6	1	AD26	0Ah	1–5	PIRQC	PIRQD	PIRQA	PIRQB
Slot 7	1	AD25	09h	1–6	PIRQB	PIRQC	PIRQD	PIRQA

3.7 Clocks and Timers

The DIGITAL 5/233i CompactPCI SBC includes:

Table 3–2 Clocks and Timers

Clock or Timer	Description
Time-of-year (TOY) clock	Standard TOY clock with battery backup. The TOY clock is integrated into the SMC Ultra I/O controller.
Watchdog timer	Programmable timer that supports four modes and count-down timeout values that range from 18 milliseconds to 291 seconds. The timer is protected from being enabled accidently. You program the timer by using registers in the ISA I/O memory map. For more information, see Chapter 9.

3.8 Ethernet Controller

The 10/100 Fast Ethernet controller (Intel, 82558) provides system networking capabilities. The controller behaves:

- As a bus slave when communicating with the PCI bus to gain access to configuration and control/status registers
- As a bus master when communicating with memory

The Ethernet controller handles the following types of cycle termination:

- Target-initiated retry
- Abort
- Device select abort

Target-aborted terminations cause an interrupt.

The physical connection to the network is through an RJ45 Ethernet 10/100 BASE-T shielded twisted-pair connector, which supports a maximum distance between nodes of 100 feet. The Ethernet controller supports front access I/O through the SBC or rear access I/O through a rear transition module. By default, the SBC is set up for rear access I/O. If you want to use the connector on the SBC, you must set the Ethernet jumper accordingly, as explained in Section 6.4.

Caution

Be sure to connect an Ethernet cable to only one of the available system Ethernet connectors. Powering the system on with cables connected to both connectors can damage your system.

Vorsicht!

Vergewissern Sie sich, daß Sie nur ein Ethernet-Kabel nur an eine der verfügbaren Ethernet-Anschlüsse anschließen. Wenn an beiden Anschlüssen Kabel angeschlossen sind und Sie das System einschalten, kann das System beschädigt werden.

3.9 Ultra SCSI Controller

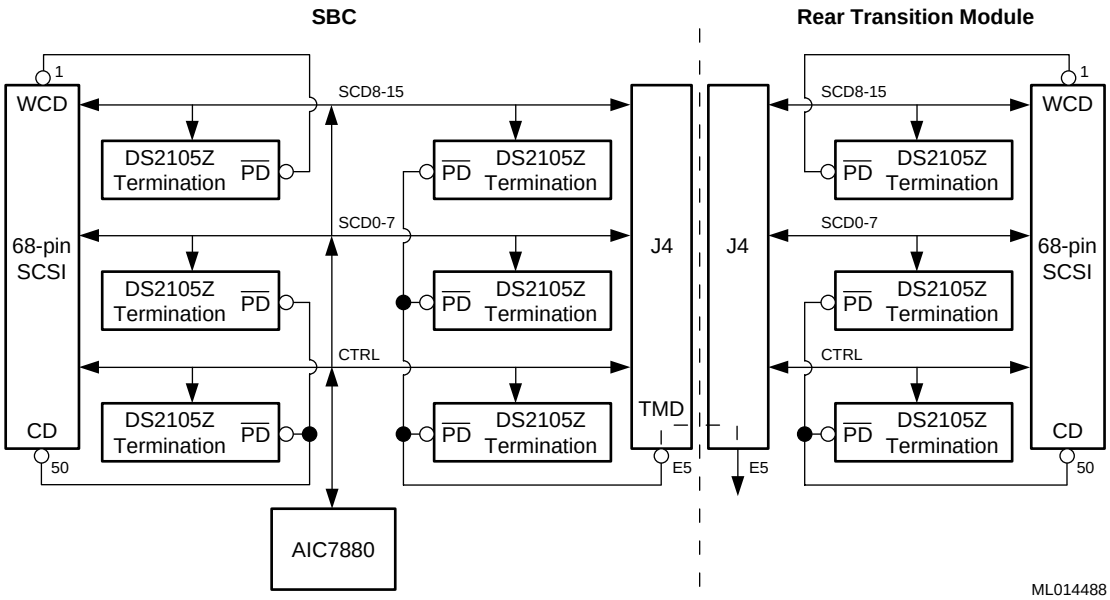
The Ultra SCSI controller (Adaptec, AIC 7880) allows you to attach up to seven narrow SCSI devices or a mix of 14 wide and narrow SCSI devices to your system. You can attach SCSI devices to the front, rear, or both the front and rear of the system.

The controller's circuitry provides for automatic termination when a device is connected to the front or rear of the system. Ground pins on the SCSI connector are reassigned to act as cable or device detects. Two ground pins distinguish between 16- and 8-bit devices.

The active SCSI terminator is the Dallas Semiconductor DS2105Z. The terminator's power-down pin (PD-) disconnects the termination from the bus when it is driven low. This pin has an internal pull-up resistor.

Figure 3–2 shows the SCSI termination scheme. As the figure shows, pin E5 is grounded. This disables the SBC's terminators next to J4. This is due to the end of the SCSI bus being at the 68-pin connector on the rear transition module. If you connect a non-wide device into the rear transition module's 68-pin connector, pin 50 becomes grounded. This turns off the terminators for the CTRL and SCD0-7 signals. The last device on the cable provides termination for these signals.

Figure 3–2 SCSI Termination



If you connect a wide device into the rear transition module's 68-pin connector, pin 1 is grounded and all three terminators are turned off. In this case, you must connect a wide device at the end of the cable.

Note

If you use a 68-to-50 pin SCSI adapter, the adapter must have straight through connections with no pins hooked together. With this controller's termination scheme, some of these adapters short all ground pins together causing the terminator for the SCD8-15 signals to be turned off when it should not be.

3.10 Video Controller

The Cirrus Logic PCI video controller (GD5446) provides video support for systems that do not include a CompactPCI video adapter option module. The controller supports DDC2 display data channel serial monitor communications. If you install a CompactPCI video module in your system, the onboard video is disabled by default. This default setting allows you to upgrade video simply by installing the option module. You also have the option of disabling the video support completely, if appropriate for your application.

The SBC provides 1 MB of onboard video memory for the Cirrus Logic 64-bit VisualMedia Accelerator (GD5446) that provides the standard VGA and extended video modes listed in Tables 3–3 and 3–4.

Table 3–3 Standard Video Modes

Mode[1]	VESA Mode[2]	Colors	Char. xR	Char. Cells	Pixels	Display Mode	Pixel Freq.	Horizontal Freq.	Vertical Freq.
00/01	-	16/256	40x25	9x16	360x400	Text	14	31.5	70
02/03	-	16/256	80x25	9x16	720x400	Text	28	31.5	70
04/05	-	4/256	40x25	8x8	320x200	Graphics	12.5	31.5	70
06	-	2/256	80x25	8x8	640x200	Graphics	25	31.5	70
07	-	mono	80x25	9x16	720x400	Text	28	31.5	70
0D	-	16/256	40x25	8x8	320x200	Graphics	12.5	31.5	70
0E	-	16/256	80x25	8x8	640x200	Graphics	25	31.5	70
0F	-	mono	80.25	8x14	640x350	Graphics	25	31.5	70
10	-	16/256	80x25	8x14	640x350	Graphics	25	31.5	70
11	-	2/256	80x30	8x16	640x480	Graphics	25	31.5	60
11+	-	2/256	80x30	8x16	640x480	Graphics	31.5	37.9	72
11+	-	2/256	80x30	8x16	640x480	Graphics	31.5	37.9	75
12	-	16/256	80x30	8x16	640x480	Graphics	25	31.5	60
12+	-	16/256	80x30	8x16	640x480	Graphics	31.5	37.9	72
12+	-	16/256	80x30	8x16	640x480	Graphics	31.5	37.5	75
13	-	256/256	40x25	8x8	320x200	Graphics	12.5	31.5	70

[1] Some modes are not supported by all CL-GD543X controllers.
[2] Some modes are not supported by all monitors. The best quality refresh rate for the monitor type is used automatically.

Table 3–4 Extended Video Modes

Mode[1]	VESA Mode[2]	Colors	Char. xR	Char. Cells	Pixels	Display Mode	Pixel Freq.	Horizontal Freq.	Vertical Freq.
14	-	16x256K	132x25	8x16	1056x400	Text	41.5	31.5	70
54	10A	16.256K	132x43	8x8	1056x350	Text	41.5	31.5	70
55[7]	109	16/256K	132x43	8x8	1056x350	Text	41.5	31.5	70
58, 6A	102	16/256K	100x37	8x16	800x600	Graphics	36	35.2	56
58, 6A	102	16/256K	100x37	8x16	800x600	Graphics	40	37.8	60
58, 6A	102	16/256K	100x37	8x16	800x600	Graphics	50	48.1	72
58, 6A	102	16/256K	100x37	8x16	800x600	Graphics	49.5	46.9	75
5C	103	256/256K	100x37	8x16	800x600	Graphics	36	35.2	56
5C	103	256/256K	100x37	8x16	800x600	Graphics	40	37.9	60

Table 3–4 Extended Video Modes (Continued)

Mode[1]	VESA Mode[2]	Colors	Char. xR	Char. Cells	Pixels	Display Mode	Pixel Freq.	Horizontal Freq.	Vertical Freq.
5C	103	256/256K	100x37	8x16	800x600	Graphics	50	48.1	72
5C	103	256/256K	100x37	8x16	800x600	Graphics	49.5	46.9	75
5Di	104	16/256K	128x48	8x16	1024x768	Graphics	44.9	35.5	43[4]
5D	104	16/256K	128x48	8x16	1024x768	Graphics	65	48.3	60
5D	104	16/256K	128x48	8x16	1024x768	Graphics	75	56	70
5D	104	16/256K	128x48	8x16	1024x768	Graphics	77	58	72
5D	104	16/256K	128x48	8x16	1024x768	Graphics	78.7	60	75
5E	100	256/256K	80x25	8x16	640x400	Graphics	25	31.5	70
5F	101	256/256K	80x30	8x16	640x480	Graphics	25	31.5	60
5F	101	256/256K	80x30	8x16	640x480	Graphics	31.5	37.9	72
5F	101	256/256K	80x30	8x16	640x480	Graphics	31.5	37.5	75
60i	105	256/256K	128x48	8x16	1024x768	Graphics	44.9	35.5	43[4]
60	105	256/256K	128x48	8x16	1024x768	Graphics	65	48.3	60
60	105	256/256K	128x48	8x16	1024x768	Graphics	75	56	70
60	105	256/256K	128x48	8x16	1024x768	Graphics	77	58	72
60	105	256/256K	128x48	8x16	1024x768	Graphics	78.7	60	75
64	111	64K	-	-	640x480	Graphics	25	31.5	60
64	111	64K	-	-	640x480	Graphics	31.5	37.9	72
64	111	64K	-	-	640x480	Graphics	31.5	37.5	75
65[3]	114	64K	-	-	800x600	Graphics	36	35.2	56
65[3]	114	64K	-	-	800x600	Graphics	40	37.8	60
65[3]	114	64K	-	-	800x600	Graphics	50	48.1	72
65[3]	114	64K	-	-	800x600	Graphics	49.5	46.9	75
66	110	32K[3]	-	-	640x480	Graphics	25	31.5	60
66	110	32K[3]	-	-	640x480	Graphics	31.5	37.9	72
66	110	32K[3]	-	-	640x480	Graphics	31.5	37.5	75
67	113	32K[3]	-	-	800x600	Graphics	36	35.2	56
67	113	32K[3]	-	-	800x600	Graphics	40	37.8	60
67	113	32K[3]	-	-	800x600	Graphics	50	48.1	72
67	113	32K[3]	-	-	800x600	Graphics	49.5	46.9	75
71	112	16M	-	-	640x480	Graphics	25	31.5	60

[1] Some modes are not supported by all CL-GD543X controllers.
[2] Some modes are not supported by all monitors. The best quality refresh rate for the monitor type is used automatically.
[3] 32K direct color/256 color mixed mode.

[4] A character “i” stands for interlaced mode. 43.5 Hz or 87 Hz interlaced.
[5] 16M colors, but with 32 bit-per-pixel format. 16M+A indicates the same.
[6] Implementations using the CL-GD5434 controller restrict 1024x768 at 72 Hz refresh. In those implementations, 70 Hz refresh is substituted. For a higher refresh rate select 75 Hz.
[7] Mode 55 uses a 16 dot high font with the bottom two lines truncated in the absence of the 8x14 font TSR (TSRFONT). The characters “g,” “j,” “p,” “q,” “y,” and “y” are truncated using a middle and bottom line algorithm to avoid truncation of descenders. For compatibility with MS-DOS applications that use the 8x14 font, use the TSRFONT utility.
[8] VESA has recently proposed a new specification for 43 Hz interlaced and 60 Hz timing for 1280x1024 resolution modes. Currently Cirrus Logic uses timings for these modes other than the timings proposed.

3.11 Ultra I/O Controller

The Ultra I/O controller (SMC, FDC37C932) resides on the ISA bus and provides an interface to the diskette interface, parallel port, serial ports, USB, and PS/2 mouse and keyboard ports. This controller also provides the real-time clock and battery backed CMOS RAM.

3.11.1 Diskette Interface

The diskette interface supports a 3.5” 1.44 MB diskette drive by way of a diskette drive header on a rear transition module.

For information on enabling and disabling the diskette interface, see Section 5.8.

3.11.2 Parallel Port

The parallel port (front or rear) operates in a normal, extended capabilities port (ECP), or enhanced parallel port (EPP) mode. The ECP and EPP modes are bidirectional data transfer modes that adhere to IEEE P1284 specifications. ECP mode uses the DMA protocol to achieve transfer rates of approximately 2.5 MB and provides symmetric bidirectional communications. EPP mode uses existing parallel port signals to provide asymmetric bidirectional data transfers that are driven by a host device.

For information on configuring support for a parallel port, see Section 5.12. For information on the parallel port connector, see Section 7.4.

3.11.3 Serial Ports

The SBC supports two serial ports (front or rear) that are 16550 compatible and can operate at up to 120 K baud with ESD protection to 15 KV.

For information on enabling or disabling serial ports, see Section 5.11. For information on the serial port connectors, see Section 7.6.

3.11.4 USB Ports

The SBC supports two USB ports (front or rear) that are capable of transfer rates of 1.2 Mb/sec to 12 Mb/sec. You can route USB signals to the front panel of the SBC or a rear transition module. The signals are routed for rear access I/O by default. If your application requires the use of the USB ports on the front panel of the SBC, you must remove the jumper block as shown in Section 6.4.

For information on configuring USB support, see Section 5.13. For information on the USB port connectors, see Section 7.7.

3.11.5 Keyboard/Mouse Interface

The keyboard/mouse interface supports keyboard and mouse ports (front or rear). On the SBC, the keyboard and mouse connect to a single front panel PS/2 keyboard/mouse connector through a standard PS/2 Y-cable. It is also possible to use connectors on a rear transition module.

For information on configuring keyboard and mouse support, see Section 5.6. For information on the keyboard/mouse connector, see Section 7.5.

3.12 LM78 System Monitor

The LM78 system monitor resides on the ISA bus and allows you to:

- Measure and set maximum and minimum thresholds for +3.3 V, +5.5 V, +12 V, –12 V, and CPU core voltages
- Monitor intrusions
- Monitor fan tachometer (TACH) signals
- Monitor the SBC temperature and set a maximum temperature threshold and a minimum (hysteresis) limit

Note

To use the monitor intrusion feature, an external sensor with a rear access I/O connector must be installed in the system.

You can program the LM78 to assert either nonmaskable interrupt (NMI) or system management interrupt (SMI) interrupt signals when a monitored event (for example, when the system crosses a specified threshold) occurs. These signals are preconfigured to output a logic low based on input to the LM78 device.

You should enable the SMI interrupt signals for monitoring the SBC temperature. To protect the CPU from damage and to ensure reliable operation, set the maximum temperature threshold to 55° C.

You configure the server management features with the WINBIOS Setup utility. For information on system management, see Chapter 9. For information on configuring the LM78 system management features, see Section 5.18.

4

System Startup

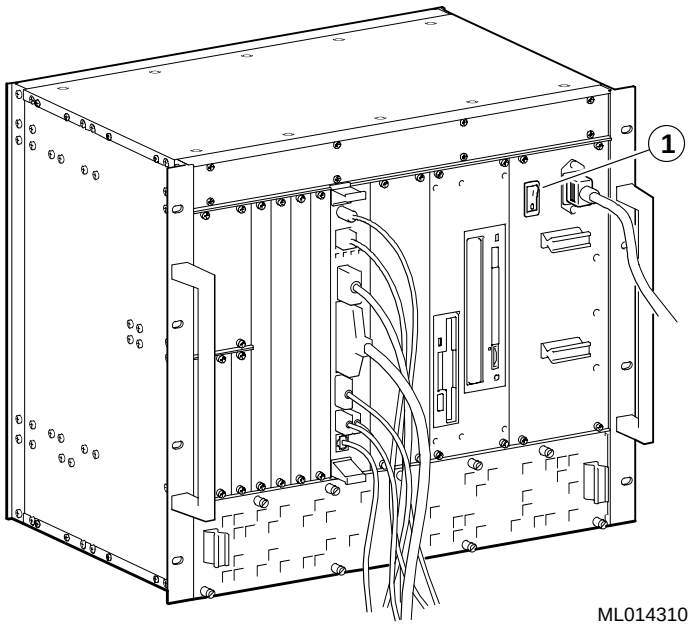
This chapter introduces you to and explains how to set up your system. Topics include:

- Powering the System On
- Considering System Configuration Changes
- Powering the System Off
- Restarting the System

4.1 Powering the System On

To power the system on, press the On/Off button on the front panel of the power supply bay as shown in Figure 4–1. The button stays depressed in the On (1) position.

Figure 4–1 Powering the System On



4.1.1 System Startup

Figure 4–2 shows the system startup screen display. The callouts in the figure identify the following:

1 The CPU type and speed.

2 Power-on self test (POST) diagnostic messages.

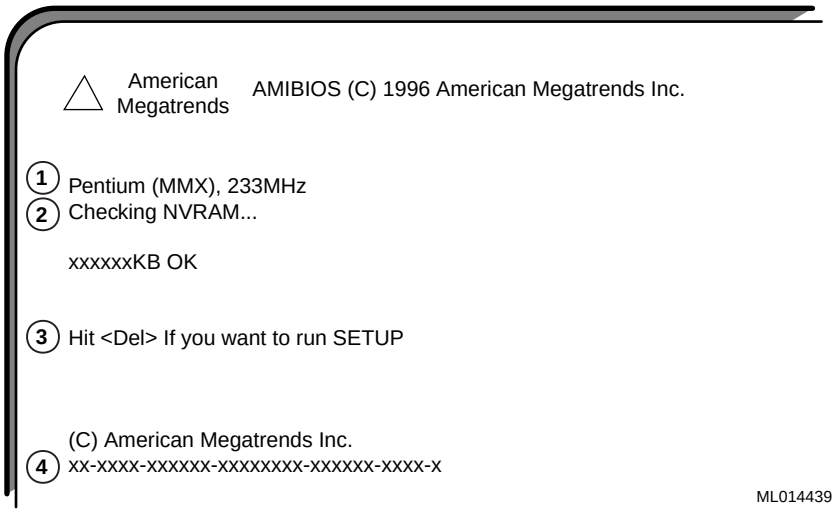
When you power on or reset the system, AMIBIOS runs the POST diagnostics. The POST diagnostic that is identified on the screen is the memory test.

3 Instruction on how to invoke the WINBIOS Setup utility.

If you need to adjust the system configuration, press the Delete key.

4 AMIBIOS identification string.

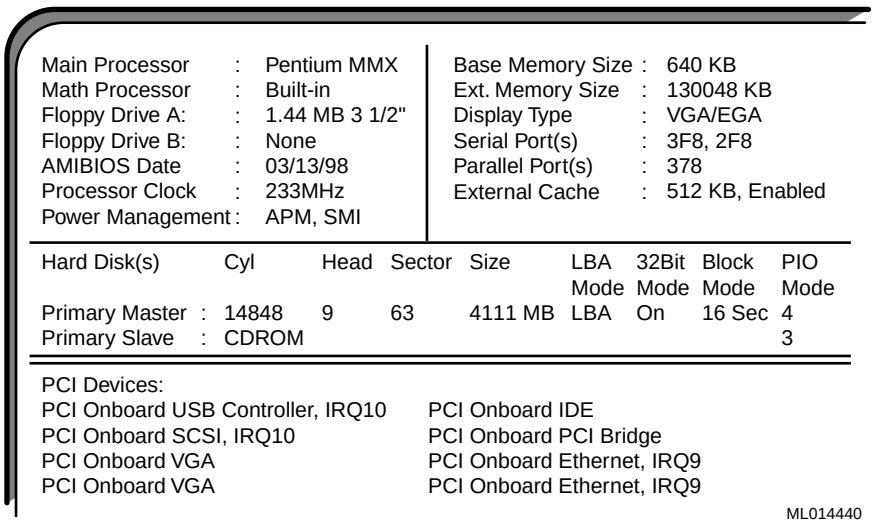
Figure 4–2 System Startup Screen Display



When the memory tests complete, AMIBIOS configures the IDE devices and then prompts you to press Ctrl/A if you want to run the SCSISelect Utility.

When the POST diagnostics complete, AMIBIOS displays the system's configuration as shown in Figure 4–3.

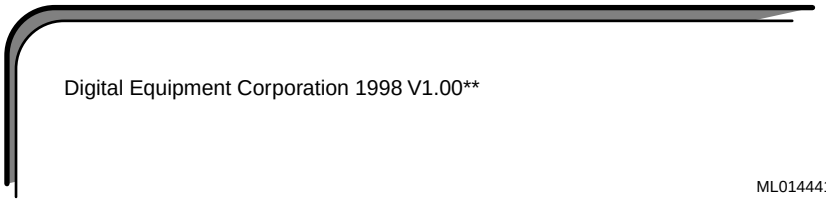
Figure 4–3 System Configuration Screen Display



4.1.2 BIOS Version

After displaying the configuration, AMIBIOS identifies the version of the BIOS that is running. Figure 4–4 shows the BIOS version message.

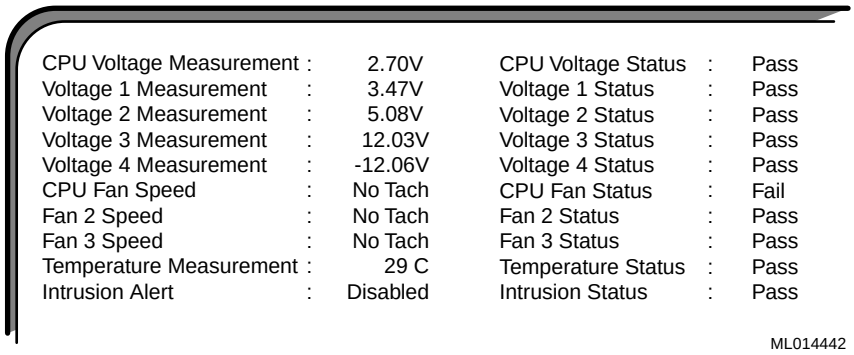
Figure 4–4 BIOS Version Screen Display



4.1.3 System Management Measurement and Status Screen Display

AMIBIOS then reports the measurement and status of the system's voltages, fans, temperature, and intrusion. Figure 4–5 shows how this information is reported.

Figure 4–5 System Management Measurement and Status Screen Display



The BIOS then tries to find the boot device.

Note

A normal power-up emits a single blink on the status LED on the front panel of the CPU module. A sequence of blinks during startup indicates errors. If the system fails the startup tests or you see multiple blinks and the system halts, power the system off, wait approximately 15 seconds, and then power it on again. If the system continues to fail the tests or emits multiple blinks, consult Chapter 10 for information on trouble-shooting possible problems.

4.2 Considering System Configuration Changes

Depending on the option modules installed, the I/O devices being used, and other application-specific system requirements, you may need to adjust the system configuration. Chapter 5 explains how to use the BIOS setup utility to verify and change system configuration settings.

4.3 Powering the System Off

You may need to power the system off to resolve system hangs or similar problems.

Caution

Before you power your computer off, make sure you save and close all open files if at all possible. If the system shuts down before you save and close open files, you may lose data.

To power the system off:

1. Close application data files that are open.
2. Close applications that are running.
3. Click the Start icon at the lower left corner of your screen.
4. Click the Shutdown icon and then on `Yes` to shut down your system.
5. After the message `You can now safely turn off your computer` appears on the screen, press the power On/Off button on the front panel of the power-supply module.

If you need to power your system off for an extended period, power the system off and unplug the power cord from the system's power inlet.

4.4 Restarting the System

You can restart your system by using a hard boot or a soft boot.

Method	How to Invoke	Action Performed
Hard boot	Power the system off for five seconds, then back on, by pressing the power On/Off button on the front panel of the power supply module.	Runs memory tests and clears all terminate stay resident (TSR) programs and memory registers.
Soft boot	Press [Ctrl]/[Alt]/[Delete]	Does not run memory tests but clears all TSR programs and memory registers.

5
Configuring the System

This chapter explains how to configure a DIGITAL 5/233i-8 CompactPCI system, using the American Megatrends' WINBIOS Setup utility. Topics include:

- About WINBIOS Setup
- WINBIOS Basics
- Setting the Date and Time
- Configuring System Security
- Configuring a Display Monitor and Adapter
- Configuring Keyboard and Mouse Support
- Configuring Hard Disk and CD–ROM Devices
- Configuring the Diskette Drive
- Configuring the Onboard SCSI Controller
- Configuring the Onboard Ethernet Controller
- Configuring Onboard Serial Ports
- Configuring the Onboard Parallel Ports
- Configuring USB Support
- Configuring Memory
- Configuring Boot Options
- Configuring Display Modes
- Configuring PCI Plug and Play Capabilities
- Configuring LM78 System Management Features
- Updating the BIOS Flash

5.1 About WINBIOS Setup

WINBIOS Setup enables you to select and store information about the system's hardware and software in the battery-backed memory of CMOS RAM. The stored information takes effect each time the system boots and you can change it at any time by using WINBIOS Setup.

Caution

Be sure to read and understand the information in this chapter before attempting to change the factory BIOS settings. If you are not careful, you can adjust settings such that the system will not operate properly.

Vorsicht!

Wichtig! Bevor Sie die ab Fabrik eingestellten BIOS-Einstellungen ändern, sollten Sie die Informationen in diesem Kapitel gelesen und verstanden haben. Wenn Sie bei der Änderung der BIOS-Einstellungen nicht sorgfältig vorgehen, können Sie die Einstellungen so verändern, daß das System nicht mehr einwandfrei funktioniert.

WINBIOS Setup is an easy-to-use configuration tool that features a window and icon-based graphical user interface (GUI). The main window groups the setup options into four subwindows:

Window...	Allows You to Set...
Setup	System configuration options
Security	Password and anti-virus checking options
Utility	IDE detection and a language for prompts and messages
Default	Options as original (for a given session), optimal, or fail-safe defaults

Within each of these windows, icons identify categories or types of configuration information. For example, a chipset icon identifies chipset configuration options.

The main window also includes a message bar, which appears across the bottom of the window. Messages that appear in this bar describe the items on which you click within the window.

You can use a keyboard or mouse to point and click configuration categories and navigate through pop-up option menus.

5.2 WINBIOS Basics

Sections 5.2.1 through 5.2.7 introduce you to WINBIOS Setup by discussing the following:

- Configuration categories, Section 5.2.1
- How to get help, Section 5.2.2

- How to use the mouse, Section 5.2.3
- How to use the keyboard, Section 5.2.4
- Automatic option selection, Section 5.2.5
- How to start WINBIOS Setup, Section 5.2.6
- How to exit WINBIOS Setup, Section 5.2.7
- How to use default WINBIOS settings, Section 5.2.8

5.2.1 Configuration Categories

Table 5–1 lists the categories of configuration information that you can set. The categories are represented as icons in the four windows that appear within the WINBIOS main menu. Figure 5–1 shows how you can maneuver through the setup windows.

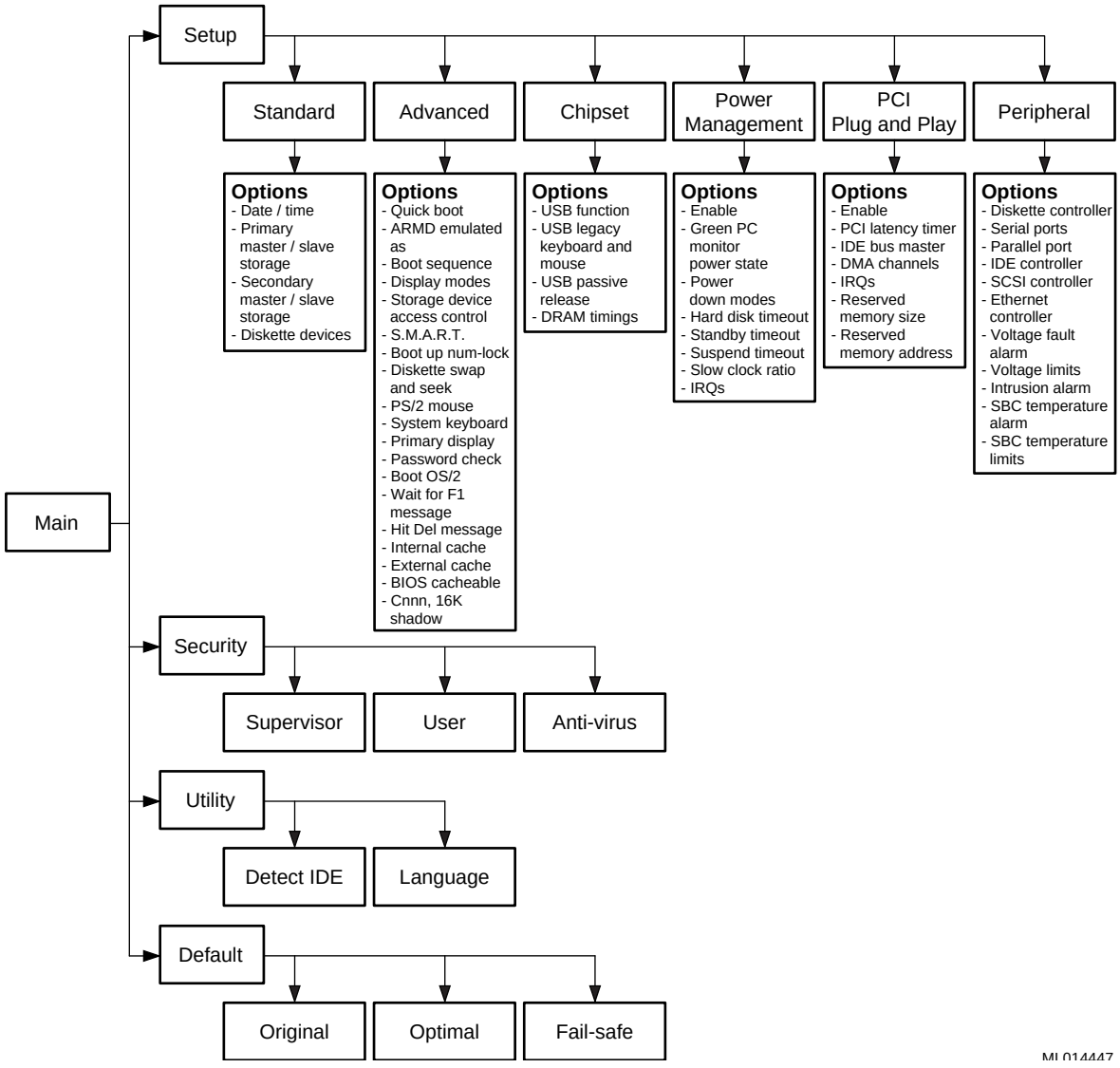
Table 5–1 WINBIOS Setup Configuration Categories

Category...	Allows You to Set...
Setup Window	
Standard	Primary and secondary master and slave IDE device options, date and time, and diskette device options.
Advanced	System performance options: quick boot, ATAPI removable media device (ARMD) as a diskette or hard disk drive, boot sequence, initial and ROM initialization display mode, diskette and hard disk access control, hard disk S.M.A.R.T., boot Num-Lock, diskette drive swap and seek, PS/2 mouse and keyboard support, primary display, password check, boot OS/2, boot messages, and cache and shadowing options.
Chipset	Chipset options: universal serial bus (USB) enable, USB keyboard and mouse legacy support, USB passive release enable, and DRAM timing options.
Power management	Power conservation options. These options *are not* supported.
PCI plug and play	PCI plug and play options: plug and play aware operating system enable, PCI latency timer, PCI IDE bus master, DMA channel, IRQ, reserved memory size, and reserved memory addresss options.
Peripheral	I/O support options: onboard diskette drive controller, serial ports, IDE controller, SCSI controller, and Ethernet controller options, and system management options.
Security Window	
Supervisor	Supervisor password
User	User password
Anti-virus	Anti-virus software enabled or disabled.
Utility Window	

Table 5–1 WINBIOS Setup Configuration Categories (Continued)

Category...	Allows You to Set...
Detect IDE	The programmed I/O mode, block mode, and large (LBA) mode. Also shows the settings of auto-detected IDE devices, including the device type, number of cylinders, number of heads, write pre-compensation, number of sectors, and capacity.
Language	English only.
Default Window	
Original	All option settings back to the values present at the start of the setup session.
Optimal	Optimal option values for optimizing system performance. Factory default.
Fail-safe	Fail-safe option values for system stability.

Figure 5–1 WINBIOS Setup



5.2.2 Getting Help

In addition to the messages that appear in the message bar on the main window, WINBIOS Setup provides Help screens for options on the Advanced, Chipset, Power Management, and Peripheral setup windows and use of the mouse and keyboard.

To get help on a specific setup option, click the option and then press Alt+H. For help on mouse or keyboard usage, press Alt/H while the input focus is outside the context of the windows that offer setup option help.

5.2.3 Using the Mouse

WINBIOS Setup supports the following mouse devices:

- PS/2 type
- Mice that use IRQs 3, 4, or 5 (IRQ2 is not supported)
- Microsoft compatible M, V, and W Series that use the and M and M+ protocols
- Logitech C-Series compatible that use the MM protocol

Use the mouse as follows:

To...	Do...
Select a category of configuration options	Double-click MB1 on the category icon
Move to an option field	Single-click MB1 on the option field or click the up or down arrow on the scroll bar until you reach the field of choice
Select or change the values of global and selected options	Single-click MB1 on the option field
Increment a value	Single-click MB1 on the + button
Decrement a value	Single-click MB1 on the – button
Close the current pop-up window and return to the previous level	Single-click MB1 on the small square button in the upper left corner of the window
Return to the beginning of the text	Single-click MB1 at the beginning of the text
Advance to the end of the text	Single-click MB1 at the end of the text
Enter alphabetic input in the virtual keyboard (not case-sensitive)	Single-click MB1 on each input value
Enter numeric input in the virtual keyboard and numeric keypad	Single-click MB1 on each input value

5.2.4 Using the Keyboard

You have the option of using a keyboard to navigate through and set option values in the WINBIOS configuration windows. Use the keyboard as follows:

To...	Press...
Move to the next window or option field	[Tab]
Move to the next option field to the right, left, above, or below	Right, left, up, or down keyboard arrow keys (keypad arrow keys are not supported)
Select the value in the current option field	[Enter]
Increment a value	[Shift]+[+]
Decrement a value	[–]
Close the current window and return to the previous level	[Esc]
Return to the previous window	[Page Up]
Advance to the next window	[Page Down]
Return to the beginning of the text	[Home]
Advance to the end of the text	[End]
Access a help window	[Alt]+[H]
Exit WINBIOS Setup	[Alt]+[Spacebar]
Enter alphabetic input in the virtual keyboard (not case-sensitive)	Alphabetic keys
Enter numeric input in the virtual keyboard and numeric keypad	Numeric keys

5.2.5 Automatic Option Selection

AMIBIOS is configured to reflect dependencies between AMIBIOS features and WINBIOS Setup options. For example, the **External Cache** option in the Advanced Setup window is configured to be displayed for the DIGITAL 5/233i-8 CompactPCI system because the system has secondary cache memory installed. However, if secondary cache memory were not present, AMIBIOS would be configured such that the **External Cache** option is omitted.

If the selection of a WINBIOS option setting determines the settings for one or more other options, AMIBIOS automatically assigns values to dependent settings and does not allow you to change those settings unless you change the setting for the parent option. Invalid options appear in gray type.

For example, you can set the **Onboard Serial Port** options to ***Auto***, ***Disabled***, ***3F8h***, ***2F8h***, ***3E8h***, or ***2E8h***. If you set **Onboard Serial Port 1** to ***2F8h***, AMIBIOS disables the ***2F8h*** value for **Onboard Serial Port 2**.

5.2.6 Starting WINBIOS Setup

If the system powers on successfully, the BIOS displays identification information and the following instructions on how to invoke WINBIOS Setup:

```
Hit <DEL> if you want to run SETUP
```

Press the Delete key to start WINBIOS Setup.

5.2.7 Exiting WINBIOS Setup

To exit WINBIOS Setup, press the Alt and Spacebar keys simultaneously. An exit setup window appears. If you have made changes that you want to preserve, save the changes and exit. Otherwise, just exit.

5.2.8 Using Default WINBIOS Settings

WINBIOS Setup offers two groups of default settings and a mechanism for recalling settings that were enabled at the start of a configuration session. You can use these features to:

- Expedite the configuration process
- Optimize the configuration for performance
- Optimize the configuration for stable operation
- Recover when the system is having configuration-related problems

To use a default setting:

1. Select one of the following icons in the Default window:

To...	Select...
Recall the system configuration settings that were in effect at the start of the current WINBIOS Setup session	**Original**
Load system configuration settings that optimize system performance	**Optimal**
Load system configuration settings that provide far from optimal performance, but are the most stable	**Fail-Safe**

Note

The factory configuration uses the Optimal settings, and AMIBIOS automatically loads the Optimal settings if CMOS RAM is corrupted.

2. Respond to the No/Yes prompt.
3. Exit the Option window.

Note

Throughout the remainder of this chapter, default settings apply to both the Optimal and Fail-Safe group settings unless specified otherwise.

5.3 Setting the Date and Time

To set the date and time:

1. Select the **Standard** icon in the Setup window.
2. Select the **Date/Time** icon in the Standard Setup window.
3. Select a date or time value to change. The selected value is highlighted.
4. Select the + button to increase the value or the – button to decrease the value.
5. Repeat steps 3 and 4 for other values that need to change.
6. Exit the Date and Time window.
7. Exit the Standard Setup window.

5.4 Configuring System Security

You have the option of setting the following system security features:

- Supervisor password
- User passwords
- Password checking to run WINBIOS Setup
- Password checking when the system is powered on and to run WINBIOS Setup
- Enable anti-virus checking

Sections 5.4.1 through 5.4.3 explain how to:

- Set up password security
- Change a password
- Enable anti-virus protection

5.4.1 Setting Up Password Security

To set up password security:

1. Select the Supervisor icon in the Security window.

   You must set up a supervisor password prior to setting up any user passwords.

2. Enter a 1- to 6-character password in the input field of the Supervisor Setup window by using one of the following methods:
   - Type the password on the keyboard.
   - Point and click characters on the virtual keyboard.
   - Confirm the password.

Note

Make note of the password that you enter and keep it in a secure place. If you forget or lose the password, you must drain CMOS RAM and reconfigure the system.

3. Exit the Supervisor Setup window.
4. Select the User icon in the Security window if you need to set up user passwords. If you do not need to set up a user password, skip to step 7.
5. Enter a 1- to 6-character password in the input field of the User Setup window by using one of the methods listed in step 2.

Note

Make note of the password that you enter and keep it in a secure place. If you forget or lose the password, you must drain CMOS RAM and reconfigure the system.

6. Exit the User Setup window.
7. Decide whether it is sufficient that the system prompt for and check a password only when someone attempts to run WINBIOS Setup. This is the default level of security if a password has been set. If this level of security is sufficient, skip to step 12. If it is necessary for the system to also prompt for and check a password each time the system is powered on, continue to step 8.
8. Select the **Advanced** icon in the Setup window.
9. Select the **Password Check** option.
10. Select the option value ***Always***. When set, this value causes the system to prompt for and check a password each time the system is powered on and when someone attempts to run WINBIOS Setup. The value ***Setup*** instructs the system to prompt and check for a password only when WINBIOS Setup is run.
11. Exit the Option window.
12. Exit the Advanced Setup window.

5.4.2 Changing a Password

To change a password:

1. Select the Supervisor or User icon in the Security window, as appropriate.
2. Enter a 1- to 6-character password in the input field of the Supervisor Setup window by using one of the following methods:
   - Type the password on the keyboard.
   - Point and click characters on the virtual keyboard.

Note

Make note of the password that you enter and keep it in a secure place. If you forget or lose the password, you must drain CMOS RAM and reconfigure the system.

3. Reenter the new password as prompted.

   If the password confirmation is incorrect, an error message appears. Try reentering the password.

   If the password confirmation is correct, the new password is stored in CMOS RAM when WINBIOS Setup exits and takes effect the next time the system boots.

4. Exit the Supervisor Setup or User Setup window, as appropriate.

5.4.3 Enabling Anti-Virus Protection

You have the option of enabling anti-virus protection. This feature is disabled by default. When enabled, AMIBIOS issues a warning when a program (or virus) issues a disk format command or attempts to write to the boot sector of the hard disk drive.

The following messages appear after an attempt to format a cylinder, head, or sector of a hard disk drive with the BIOS INT 13 Hard Disk Drive Service:

```
Format!!!
Possible VIRUS: Continue (Y/N)? _
```

AMIBIOS displays the following messages when a program attempts to write to the boot sector of the hard disk drive:

```
Boot Sector Write!!!
Possible VIRUS: Continue (Y/N)? _
```

If either of these messages appears, you may need to enter `N` several times to prevent the format or write operation.

5.5 Configuring a Display Monitor and Adapter

You may need to configure the system's display monitor support. By default, the system is set up to support a VGA/EGA display monitor. If you connect a different type of display monitor or if the system is set up without a display monitor, you must adjust the configuration.

1. Select the **Advanced** icon in the Setup window.
2. Select the **Primary Display** option.
3. Set the option value to ***Absent***, ***VGA/EGA***, ***CGA 40x25***, ***CGA 80x25***, or ***Mono***, as appropriate.
4. Exit the Option window.
5. Exit the Advanced Setup window.

5.6 Configuring Keyboard and Mouse Support

WINBIOS Setup options are available for:

- Configuring systems that do not have a keyboard
- Enabling and disabling support for a PS/2 mouse

5.6.1 Configuring Systems that Do Not Use a Keyboard

If you are configuring a system that does not have a keyboard attached, specify that a keyboard is not present to suppress error messages that the BIOS would display otherwise. By default, the BIOS assumes a keyboard is connected and needs to be configured. If a keyboard is not present and the system is not configured accordingly, the BIOS displays error messages.

To supress error messages resulting from a keyboard not being attached to the system:

1. Select the **Advanced** icon in the Setup window.
2. Select the **System Keyboard** option.
3. Set the option value to ***Absent*** (the default is ***Present***).
4. Exit the Option window.
5. Exit the Advanced Setup window.

5.6.2 Disabling and Enabling Support for a PS/2 Mouse

By default, the system supports PS/2 mice. If you are using a mouse type other than PS/2, you should disable PS/2 mouse support. To disable or enable PS/2 mouse support:

1. Select the **Advanced** icon in the Setup window.
2. Select the **PS/2 Mouse Support** option.
3. Set the option value to ***Disabled*** or ***Enabled***, as appropriate.
4. Exit the Option window.
5. Exit the Advanced Setup window.

5.7 Configuring Hard Disk and CD–ROM Devices

Section 5.7.1 provides configuration information for hard disk drives and Section 5.7.2 explains how to enable and disable onboard IDE controller channels. Sections 5.7.3 through 5.7.6 explain how to configure the following types of storage devices:

- Modified frequency modulation (MFM) hard disk drive
- User-defined hard disk drive (SCSI, MFM, RLL, ARLL, or ESDI)
- IDE hard disk drive
- CD–ROM drive

Section 5.7.7 explains how to specify hard disk drive access control.

5.7.1 Disk Configuration Information

While configuring a hard disk drive, you may need to enter values for the following hard disk drive parameters manually:

Table 5–2 Hard Disk Drive Parameters

Parameter	Description
Cylinders (Cyl)	The number of cylinders in the disk drive.
Heads (Hd)	The number of heads.
Write precompensation (WP)	The track number where write precompensation begins. The size of a sector gets progressively smaller as the track diameter diminishes. Yet each sector must still hold 512 bytes. Write precompensation circuitry on the hard disk compensates for the physical difference in sector size by boosting the write current for sectors on inner tracks.
Sectors (Sec)	The number of sectors per track. MFM drives have 17 sectors per track. RLL drives have 26 sectors per track. ESDI drives have 34 sectors per track. SCSI and IDE drives have more sectors per track.
Capacity (Size (MB))	The formatted capacity of the drive is the product of: *number-of-heads* X *number-of-cylinders* X *number-of-sectors-per-track* X *512-bytes-per-sector.*

Table 5–3 lists drive parameter values for typical disk drives.

Table 5–3 Typical Hard Disk Drive Information

Type	Cylinders	Heads	Write	Sector	Capacity	PIO Mode	Block Mode	LBA Mode
User	3128	16	512	63	1.6 GB	4	On	On
User	4092	16	512	63	2.1 GB	4	On	On
User	6256	16	65535	63	3.2 GB	4	On	On
User	14848	9	256	63	4.3 GB	4	On	On
User	13328	15	65535	63	6.4 GB	4	On	On

5.7.2 Enabling and Disabling the Onboard IDE Controller Channels

You can configure the IDE controller to use the IDE primary channel, secondary channel, or both channels. The onboard IDE controller is set to use both the primary and secondary channels by default. If you need to disable or adjust this setting at any time, you can do so as follows:

1. Select the **Peripheral** icon in the Setup window.
2. Select the **Onboard IDE** icon in the Peripheral Setup window.

3. Select one of the following option values:

To...	Select...
Disable the controller	***Disabled***
Set the controller to use the primary channel (the default)	***Primary***
Set the controller to use the secondary channel	***Secondary***
Set the controller to use the primary and secondary channels (the default)	***Both***

4. Exit the Option window.
5. Exit the Peripheral Setup window.

5.7.3 Configuring MFM Hard Disk Drives

To configure an MFM hard disk drive:

1. Make note of the following information concerning the disk drive:
   - Number of heads
   - Number of cylinders
   - Number of sectors
   - Starting write precompensation cylinder
   - Capacity
2. Select the **Standard** icon in the Setup window.
3. Select the **Pri Master**, **Pri Slave**, **Sec Master**, or **Sec Slave** icon in the Standard Setup window, as appropriate.
4. Select the **Type** option in the device window.
5. Select the **43**, **44**, **45**, or **46** option on the drive parameter window. If the drive parameters listed for the type you selected do not match the drive parameters of the MFM drive, go back to the device window and configure the device as a user-defined hard disk drive (see Section 8). If the parameters match, continue to step 6.

   If the drive type is other than 43 to 46, select ***User*** and enter appropriate values for the parameters.
6. Exit the drive parameter window.
7. Exit the device window.
8. Exit the Standard Setup window.

5.7.4 Configuring User-Defined Hard Disk Drives

To configure a user-defined hard disk drive, such as a SCSI drive or an MFM, RLL, ARLL, or ESDI drive with parameters that do not match the parameters for types **43** to **46**:

1. Make note of the following information concerning the disk drive:
   - Number of heads

- Number of cylinders
- Number of sectors
- Starting write precompensation cylinder
- Capacity

2. Select the **Standard** icon in the Setup window.
3. Select the **Pri Master**, **Pri Slave**, **Sec Master**, or **Sec Slave** icon in the Standard Setup window, as appropriate.
4. Select the **Type** option in the device window.
5. Select the **User** option in the drive parameter window.

   Enter values for the disk drive parameters. Table 5–2 lists typical hard disk drive parameter values.
6. Exit the drive parameter window.
7. Exit the device window
8. Exit the Standard Setup window.

5.7.5 Configuring IDE Hard Disk Drives

To configure an IDE hard disk drive:

1. Make note of the following information concerning the disk drive:
   - Number of heads
   - Number of cylinders
   - Number of sectors
   - Starting write precompensation cylinder
   - Capacity
2. Select the **Standard** icon in the Setup window.
3. Select the **Pri Master**, **Pri Slave**, **Sec Master**, or **Sec Slave** icon in the Standard Setup window, as appropriate.
4. Select the **Type** option in the device window.
5. Select the **Auto** option in the drive parameter window.
6. Select the **Detect IDE** icon in the Utility window. This utility automatically detects and displays all IDE parameters, including those for ATAPI CD–ROM drives.
7. Click the OK button to accept the parameters. If you are absolutely certain that you know the correct IDE parameters and you prefer to enter the parameters manually, you can do so.
8. Return to the device menu.

9. Enter values for the following IDE disk drive options:.

Option	Description
LBA/Large Mode	When set to ***On***, enables support for IDE drives with capacities greater than 528 MB. The default is ***Off***. If you do not enable this option, the system will allow use of up to 528 MB only, even though the operating system supports greater than 528 MB.
Block Mode	When set to ***On***, enables support for IDE drives that use block mode. Block mode increases the performance of data transfers by increasing the amount of data transferred for each operation. Only 512 bytes of data can be transferred per interrupt, when block mode is disabled. The default is ***Off***.
32-Bit Mode	When set to ***On***, enables support for IDE drives that use a 32-bit data path. The default is ***Off***, allowing use of a 16-bit data path.
PIO Mode	Specifies the programmed I/O (PIO) mode for an IDE drive. This mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode value increases, the cycle time decreases. Valid values are ***Auto***, ***0***, ***1***, ***2***, ***3***, ***4***, or ***5***. Modes ***3*** to ***7*** are advanced PIO modes. Support for the I/O ready (IORDY) signal is required for these modes. If you select mode ***Auto***, AMIBIOS automatically finds the PIO mode for the drive being configured.

Note

If you choose to set the PIO mode manually by selecting ***0***, ***1***, ***2***, ***3***, ***4***, or ***5*** you must make absolutely certain that you are selecting a PIO mode supported by the IDE drive.

10. Exit the device window.
11. Exit the Standard Setup window.

5.7.6 Configuring CD–ROM Drives

To configure a CD–ROM drive:

1. Select the **Standard** icon in the Setup window.
2. Select the **Pri Master**, **Pri Slave**, **Sec Master**, or **Sec Slave** icon in the Standard Setup window, as appropriate.
3. Select the **Type** option in the device window.
4. Select the first **ARMD** option in the drive parameter window.

5. Select the **Detect IDE** icon in the Utility window. This utility automatically detects and displays all IDE parameters, including those for ATAPI CD–ROM drives.
6. Click the OK button to accept the parameters. If you are absolutely certain that you know the correct IDE parameters and you prefer to enter the parameters manually, you can do so.
7. Return to the device menu.
8. Enter values for the following IDE disk drive options:

Option	Description
LBA/Large Mode	When set to ***On***, enables support for IDE drives with capacities greater than 528 MB. The default is ***Off***. If you do not enable this option, the system will allow use of up to 528 MB only, even though the operating system supports greater than 528 MB.
Block Mode	When set to ***On***, enables support for IDE drives that use block mode. Block mode increases the performance of data transfers by increasing the amount of data transferred for each operation. Only 512 bytes of data can be transferred per interrupt, when block mode is disabled. The default is ***Off***.
32-Bit Mode	When set to ***On***, enables support for IDE drives that use a 32-bit data path. The default is ***Off***, allowing use of a 16-bit data path.
PIO Mode	Specifies the programmed I/O (PIO) mode for an IDE drive. This mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode value increases, the cycle time decreases. Valid values are ***Auto***, ***0***, ***1***, ***2***, ***3***, ***4***, or ***5***. Modes ***3*** to ***7*** are advanced PIO modes. Support for the I/O ready (IORDY) signal is required for these modes. If you select mode ***Auto***, AMIBIOS automatically finds the PIO mode for the drive being configured.

Note

If you choose to set the PIO mode manually by selecting ***0***, ***1***, ***2***, ***3***, ***4***, or ***5*** you must make absolutely certain that you are selecting a PIO mode supported by the IDE drive.

9. Exit the device window.
10. Exit the Standard Setup window.

5.7.7 Specifying Hard Disk Drive Access Control

By default, hard disk drives are configured to allow read-write access control. If necessary, you can change this setting to read-only access.

To change the hard disk drive access control:

1. Select the **Advanced** icon in the Setup window.
2. Select the **Hard Disk Access Control** option.
3. Set the option value to ***Read-Only*** or ***Read-Write***, as appropriate.
4. Exit the Option window.
5. Exit the Advanced Setup window.

5.7.8 Enabling and Disabling Hard Disk Drive S.M.A.R.T. Options

You can enable or disable the System Management and Reporting Technologies (S.M.A.R.T.) protocol for system hard disk drives. This protocol reports server system information over the network. These options are disabled by default.

To enable or disable the S.M.A.R.T. options:

1. Select the **Advanced** icon in the Setup window.
2. Select the **S.M.A.R.T. for Hard Disk** option.
3. Set the option value to ***Enabled*** or ***Disabled***, as appropriate.
4. Exit the Option window.
5. Exit the Advanced Setup window.

5.8 Configuring the Diskette Drive

Section 5.8.1 explains how to disable and enable the onboard diskette controller. Section 5.8.2 explains how to configure the drive's capacity and size. Section 5.8.3 explains how to specify the drive's access control.

5.8.1 Disabling and Enabling the Onboard Diskette Controller

The system's onboard diskette controller is enabled by default. If you need to disable or reenable the controller at any time, you can do so as follows:

1. Select the **Peripheral** icon in the Setup window.
2. Select the **Onboard FDC** icon in the Peripheral Setup window.
3. Select one of the following option values:

To...	Select...
Instruct AMIBIOS to automatically enable and configure the controller	***Auto***
Disable the controller (Fail-Safe default)	***Disabled***
Enable and configure the controller manually (Optimal default)	***Enabled***

4. Exit the Option window.
5. Exit the Peripheral Setup window.

5.8.2 Configuring the Diskette Drive Capacity and Size

To configure a diskette drive's capacity and size:

1. Make note of the capacity and size of the drive being configured.
2. Select the **Standard** icon in the Setup window.
3. Select the **Floppy A** or **Floppy B** icon in the Standard Setup window, as appropriate.
4. Select one of the following option values:
   - ***Not installed***
   - ***360 KB 5 1/4”***
   - ***1.2 MB 5 1/4”***
   - ***720 KB 3 1/2”***
   - ***1.44 MB 3 1/2”***
   - ***2.88 MB 3 1/2”***
5. Exit the drive parameter window.
6. Exit the Standard Setup window.

5.8.3 Specifying Diskette Drive Access Control

By default, the diskette drive is configured to allow read-write access control. If necessary, you can change this setting to read-only access.

To change the diskette drive access control to read-only:

1. Select the **Advanced** icon in the Setup window.
2. Select the **Floppy Access Control** option.
3. Set the option value to ***Read-Only*** or ***Read-Write***, as appropriate.
4. Exit the Option window.
5. Exit the Advanced Setup window.

5.8.4 Swapping Diskette Drives A: and B:

To swap diskette drives A: and B: you must enable the **Floppy Drive Swap** option. To enable this option:

1. Select the **Advanced** icon in the Setup window.
2. Select the **Floppy Drive Swap** option.
3. Set the option value to ***Enabled***.
4. Exit the Option window.
5. Exit the Advanced Setup window.

5.8.5 Configuring Diskette Drive A: to Seek During a System Boot

If you want diskette drive A: to perform a seek operation when the system boots, enable the **Floppy Drive Seek** option. To enable this option:

1. Select the **Advanced** icon in the Setup window.
2. Select the **Floppy Drive Seek** option.
3. Set the option value to ***Enabled***.

4. Exit the Option window.
5. Exit the Advanced Setup window.

5.8.6 Emulating an ARMD as a Diskette or Hard Disk Drive

ATAPI removable media device (ARMD) options allow a primary master, primary slave, secondary master, or secondary slave ARMD to emulate a diskette or hard disk drive. For example, you might use this option to emulate an ATAPI CD–ROM device as a bootable hard disk drive for system booting purposes.

To set up ARMD emulation:

1. Select the **Advanced** icon in the Setup window.
2. Select one of the following ARMD options:
   - ***Pri Master ARMD Emulated as***
   - ***Pri Slave ARMD Emulated as***
   - ***Sec Master ARMD Emulated as***
   - ***Sec Slave ARMD Emulated as***
3. Select one of the following option values:

To...	Select...
Default to the appropriate storage device type for the device being used (for example, diskette drive emulation for an LS120 device and hard disk drive emulation for MO and Imega zip devices)	***Auto***
Disable ARMD emulation	***Disabled***

4. Exit the Option window.
5. Exit the Advanced Setup window.

5.9 Configuring the Onboard SCSI Controller

The onboard SCSI controller allows the use of the system's front and rear SCSI ports simultaneously. To use either port, the SCSI controller must be enabled. The controller is enabled by default. If the application does not use the SCSI ports, you have the option of disabling the controller.

To disable or enable the controller:

1. Select the **Peripheral** icon in the Setup window.
2. Select the **Onboard PCI SCSI** option.
3. Set the option value to ***Disabled*** or ***Enabled***, as appropriate.
4. Exit the Option window.
5. Exit the Peripheral Setup window.

For information about the SCSI controller and SCSI termination, see Section 3.9.

5.10 Configuring the Onboard Ethernet Controller

Initially, the system is configured to use a rear I/O access Ethernet port. If you need to use front access I/O or you need to disable the onboard Ethernet controller, you need to adjust the configuration. To use the Ethernet port on the SBC, you must set the Ethernet front/rear access I/O jumper, accordingly, as explained in Section 6.4.

To disable or enable the onboard Ethernet controller:

1. Select the **Peripheral** icon in the Setup window.
2. Select the **Onboard Ethernet Controller** option.
3. Set the option value to ***Disabled*** or ***Enabled***, as appropriate.
4. Exit the Option window.
5. Exit the Peripheral Setup window.

5.11 Configuring Onboard Serial Ports

The serial port configuration applies to both the front and rear access serial ports. However, you can connect to only the front or rear ports at any given time.

Serial ports 1 and 2 each have an assigned address and associated interrupt. The optimal default enables serial port 1 at address 3F8h and serial port 2 at address 2F8h. If you are using both serial ports, you need to specify a different address for the second port. If you are using fail-safe defaults, the serial ports are disabled.

If you need to adjust the configuration of the serial ports:

1. Select the **Peripheral** icon in the Setup window.
2. Select the **Onboard Serial Port 1** or **Onboard Serial Port 2** option, as appropriate.
3. Select one of the following option values:

To...	Select...
Instruct AMIBIOS to automatically enable and configure the port	***Auto***
Disable the port (Fail-Safe default)	***Disabled***
Enable and set the base I/O address for the port manually (Optimal default is ***3F8h)***	***3F8h***, ***2F8h***, ***3E8h***, or ***2E8h***, as appropriate

4. Specify whether the front or rear access port is being used.
5. Exit the Option window.
6. Repeat steps 2 through 5 to configure the second serial port, if appropriate.
7. Exit the Peripheral Setup window.

5.12 Configuring the Onboard Parallel Ports

The parallel port configuration applies to both the front and rear access parallel ports. However, you can connect to only one of the two ports at any given time.

To configure the parallel ports:

1. Select the **Peripheral** icon in the Setup window.
2. Select the **Onboard Parallel Port** option.
3. Select one of the following option values:

To...	Select...
Instruct AMIBIOS to automatically enable and configure the port (the default)	***Auto***
Disable the port	***Disabled***
Enable and set the base I/O address for the port manually	***378h***, ***278h***, or ***3BC***h, as appropriate

4. Exit the Option window.
5. If you selected ***Auto*** or ***Disabled*** in step 3, skip to step 19.
6. Select the **Parallel Port Mode** option.
7. Select one of the following option values:

To Enable...	Select...
Normal mode.	***Normal***
Enhanced Parallel Port (EPP) mode. EPP mode supports devices that adhere to the IEEE P1284 EPP specification. This mode uses the existing parallel port signals to provide asymmetric bidirectional data transfer that is driven by the host device.	***EPP***
Extended Capabilities Port (ECP) mode (the default). ECP mode supports devices that adhere to the IEE P1284 ECP specification. This mode uses the DMA protocol to achieve transfer rates of approximately 2.5 Mbs and provides symmetric bidirectional communications.	***ECP***

8. Exit the Option window.
9. If you selected ***Normal*** or ***ECP*** in step 7, skip to step 13.
10. Select the **EPP Version** option.
11. Set the value to ***1.7*** or ***1.9***, as appropriate.
12. Exit the Option window.
13. Select the **Parallel Port IRQ** option.
14. Select one of the following option values:

To...	Select...
Instruct AMIBIOS to select an IRQ line automatically	***Auto***
Set the IRQ line to IRQ 5 or IRQ 7 manually	***5*** or ***7***

15. Exit the Option window.
16. Select the **Parallel Port DMA Channel** option.

17. Select one of the following option values:

To...	Select...
Instruct AMIBIOS to select an DMA channel automatically	***Auto***
Set the DMA channel manually	***0***, ***1***, or ***3***

18. Exit the Option window.
19. Exit the Peripheral Setup window.

5.13 Configuring USB Support

Sections 5.13.1 through 5.13.3 explain how to:

- Enable and disable USB support
- Enable and disable USB support for legacy keyboards and mice
- Enable and disable the passive release feature of the USB

5.13.1 Enabling and Disabling USB Support

USB support is enabled by default. To disable or reenable the support:

1. Select the **Chipset** icon in the Setup window.
2. Select the **USB Function** option.
3. Set the option value to ***Disabled*** or ***Enabled***, as appropriate.
4. Exit the Option window.
5. Exit the Chipset Setup window.

5.13.2 Enabling and Disabling USB Support for Legacy Keyboards and Mice

USB support for legacy keyboards and mice is enabled by default. To disable or reenable the support:

1. Select the **Chipset** icon in the Setup window.
2. Select the **USB Keyboard/Mouse Legacy Support** option.
3. Set the option value to ***Disabled*** or ***Enabled***, as appropriate.
4. Exit the Option window.
5. Exit the Chipset Setup window.

5.13.3 Enabling and Disabling Passive Release for the USB

By default, the USB passive release option is disabled. If your application requires the use of this option, you must enable it. To enable or disable the option:

1. Select the **Chipset** icon in the Setup window.
2. Select the **USB Passive Release Enable** option.
3. Set the option value to ***Enabled*** or ***Disabled***, as appropriate.
4. Exit the Option window.

5. Exit the Chipset Setup window.

5.14 Configuring Memory

WINBIOS Setup provides options for configuring memory. Sections 5.14.1 through 5.14.5 explain how to:

- Specify DRAM speed
- Specify caching options
- Shadow the system BIOS to system memory
- Control the location of the contents of ROM

5.14.1 DRAM Speed Setting

The DIGITAL 5/233i CompactPCI SBC requires that all SIMMs have a RAS access speed of 60 ns. Thus, the setting of the **DRAM Speed** option on the Chipset Setup window must be ***60 ns***.

5.14.2 Specifying Caching Options

You can disable or enable use of a write-back caching algorithm for Level 1 (L1) internal cache memory and you can disable or enable Level 2 (L2) secondary cache. This write-back algorithm for internal cache significantly improves the performance of data access operations.

When optimal default settings are in effect, the write-back algorithm is enabled for internal cache and external cache is enabled. Caching is disabled when fail-safe default settings are in effect.

To modify the caching options for internal or external cache:

1. Select the **Advanced** icon in the Setup window.
2. Select the **Internal Cache** or **External Cache** option, as appropriate.
3. Select one of the following option values:

To...	**Select...**
Disable L1 internal cache and L2 secondary cache (fail-safe default)	***Disabled***
Enable L2 secondary cache (optimal default)	***Enabled***
Use the write-back caching algorithm for L1 internal cache (optimal default)	***WriteBack***

4. Exit the Option window.
5. Exit the Advanced Setup window.

5.14.3 Setting the DRAM Data Integrity Mode

The **DRAM Data Integrity Mode** option allows you to enable error correction code (ECC) Level 1 or Level 2 mode for single-bit error correction. When in ECC Level 1 mode, multibit errors are detected and reported as parity errors and single-bit errors are corrected by the chipset. Corrected bits of data from memory are not written back to DRAM system memory.

When in ECC Level 2 mode, multibit errors are detected and reported as parity errors, single-bit errors are corrected by the chipset, and the errors are written back to DRAM system memory. If a soft (correctable) error occurs, writing the fixed data back to DRAM system memory resolves the problem. Most DRAM errors are soft errors. If a hard (uncorrectable) error occurs, writing fixed data back to DRAM system memory does not solve the problem. In this case, the second time the error occurs in the same location, a Parity Error is reported, indicating an uncorrectable error. If ECCI is selected, the BIOS automatically enables the System Management Interface (SMI).

To disable or change the DRAM data integrity mode:

1. Select the **Chipset** icon in the Setup window.
2. Select the **DRAM Data Integrity Mode** option.
3. Set the option to one of the following values:

To...	Select...
Disable all DRAM data integrity modes (fail-safe default)	***Disable***
Enable ECC level 1 mode	***ECC Level 1***
Enable ECC level 2 mode (optimal default)	***ECC Level 2***

4. Exit the Option window.
5. Exit the Chipset Setup window.

5.14.4 Shadowing the BIOS to System Memory

You can optimize the execution of the BIOS by shadowing the contents of the BIOS ROM to system memory. When shadowing is enabled, the contents of the BIOS ROM, starting at address F0000h of the system memory segment, are always copied to system memory, providing faster execution.

When optimal default settings are in effect, the shadowing option is enabled. The option is disabled when fail-safe default settings are in effect.

To change the setting of the shadowing option:

1. Select the **Advanced** icon in the Setup window.
2. Select the **System BIOS Cacheable** option.
3. Set the option value to ***Enabled*** or ***Disabled***, as appropriate.
4. Exit the Option window.
5. Exit the Advanced Setup window.

5.14.5 Controlling the Location of the Contents of ROM

You can control the location of the contents of the 16 KB ROM, beginning at named memory locations. If no adaptor ROM is using a named ROM area, the area is made available to the local bus.

To configure the location for a named memory location:

1. Select the **Advanced** icon in the Setup window.
2. Select one of the following named memory locations:
   - **C000, 16K Shadow**
   - **C400, 16K Shadow**
   - **C800, 16K Shadow**
   - **CC00, 16K Shadow**
   - **D000, 16K Shadow**
   - **D400, 16K Shadow**
   - **D800, 16K Shadow**
   - **DC00, 16K Shadow**
3. Select one of the following option values:

To...	Select...
Write the contents of addresses C000h to C7FFFh to the same addresses in system RAM for faster execution	***Enabled***
Write the contents of the named ROM area to the same address in system RAM for faster execution and allow the associated address space to be read from and written to cache memory (optimal default)	***Cache***
Not copy ROM to RAM — the contents of the ROM cannot be copied to system RAM (fail-safe default)	***Disabled***

4. Exit the Option window.
5. Repeat steps 2 and 3 for each option, as appropriate.
6. Exit the Advanced Setup window.

Note

For the Intel Hx chipset, the E000h page is used as ROM during the POST, but shadowing is disabled and the ROM CS# signal is disabled to make the E000h page available on the local bus.

5.15 Configuring Boot Options

WINBIOS Setup options are available for controlling system boots. Sections 5.15.1 through 5.15.4 explain how to:

- Enable quick boots

- Specify the boot device sequence
- Enable the use of numeric keypad arrow keys
- Enable OS/2 compatibility mode
- Disable boot prompts and messages

5.15.1 Enabling and Disabling Quick Boots

You have the option of instructing AMIBIOS to boot quickly when the system is powered on. When the **Quick Boot** option is disabled (the default) and the system is powered on, AMBIOS tests all system memory and introduces the following delays:

- Waits up to 40 seconds for a READY signal from IDE hard disk drives.
- Waits for 0.5 second after sending a RESET signal to the IDE drive to allow the drive time to get ready again.
- Prompts you to press the Delete key to invoke WINBIOS Setup and waits.

Note

If you enable the **Quick Boot** option, AMIBIOS does not test system memory above 1 MB and does not introduce the preceding delays. This ensures a quick boot. However, you must be aware of the following consequences:

- If AMIBIOS does not receive a READY signal from an IDE drive immediately, the drive is not configured.
- You will not have an opportunity to invoke WINBIOS Setup.

To enable or disable the **Quick Boot** option:

1. Select the **Advanced** icon in the Setup window.
2. Select the **Quick Boot** option.
3. Change the option value to ***Enabled*** or ***Disabled***, as appropriate.
4. Exit the Option window.
5. Exit the Advanced Setup window.

5.15.2 Specifying the Boot Device Sequence

You can specify the order of devices from which AMIBIOS is to attempt to boot the system. By default, AMIBIOS uses the following boot sequence:

1. 1st — ***Floppy***
2. 2nd — ***1st IDE-HDD***
3. 3rd — ***ATAPI CD–ROM***
4. Other — ***Yes***

To specify a boot device sequence:

1. Select the **Advanced** icon in the Setup window.
2. Select the **1st Boot Device** option.
3. Set the option value to ***Disabled, 1st IDE***, ***2nd IDE, 3rd IDE, 4th IDE, Floppy***, ***ARMD-FDD***, ***ARMD HDD***, ***ATAPI CD-ROM***, ***SCSI***, or ***Network***.
4. Select the **2nd Boot Device** option.
5. Set the option value to ***Disabled, 1st IDE***, ***2nd IDE, 3rd IDE, 4th IDE, Floppy***, ***ARMD-FDD***, ***ARMD HDD***, ***ATAPI CD-ROM***, or ***SCSI***.
6. Select the **3rd Boot Device** option.
7. Set the option value to ***Disabled, 1st IDE***, ***2nd IDE, 3rd IDE, 4th IDE, Floppy***, ***ARMD-FDD***, ***ARMD HDD***, or ***ATAPI CD-ROM***.
8. Select the **Try Other Boot Devices** option.
9. Set the option value to ***Yes*** or ***No***.
10. Exit the Option window.
11. Exit the Advanced Setup window.

5.15.3 Disabling and Enabling the Use of Numeric Keypad Arrow Keys

By default, at system boot time, the keyboard arrow keys and the arrow keys on the numeric keypad are available. If you want to disable the arrow keys on the numeric keypad, you can do so by setting the **BootUp Num-Lock** option.

To disable or enable the use of the numeric keypad arrow keys:

1. Select the **Advanced** icon in the Setup window.
2. Select the **BootUp Num-Lock** option.
3. Set the option value to ***Off*** or ***On***, as appropriate.
4. Exit the Option window.
5. Exit the Advanced Setup window.

5.15.4 Enabling or Disabling OS/2 Compatible Mode

You have the option of configuring AMIBIOS such that it can run with the IBM OS/2 operating system. By default this feature is disabled.

To enable or disable OS/2 compatibility:

1. Select the **Advanced** icon in the Setup window.
2. Select the **Boot to OS/2** option.
3. Set the option value to ***Yes*** or ***No***, as appropriate.
4. Exit the Option window.
5. Exit the Advanced Setup window.

5.15.5 Disabling and Enabling “Hit <DEL>” and “Wait for <F1>” Boot Messages

During a system boot, AMIBIOS displays messages and prompts. One such message is the “Hit <DEL> if you want to run Setup” message. A second message is the “Press <F1> to continue” message that may appear while the POST diagnostics run. In the case of this second message, AMIBIOS waits for a response before continuing. Both of these messages are enabled by default. To disable them:

1. Select the **Advanced** icon in the Setup window.
2. Select the **Hit <DEL> Message Display** or **Wait for <F1> If Error** option, as appropriate.
3. Set the option value to ***Disabled***.
4. Exit the Option window.
5. Exit the Advanced Setup window.

5.16 Configuring Display Modes

You can set the system’s initial display mode and the display mode at the time the BIOS POST initializes an optional adapter ROM.

To specify a display mode:

1. Select the **Advanced** icon in the Setup window.
2. Select the **Initial Display Mode** or **Display Mode at Add-On ROM Init** option, as appropriate.
3. Set the option value as follows:

For the Option...	Set the Value to...
Initial Display Mode	***BIOS*** or ***Silent***. If you set the option to ***BIOS***, the standard BIOS boot messages displayed before booting the system appear on the system monitor. If you set the option to ***Silent***, the standard BIOS boot messages do not appear on the system monitor and the system boots to the operating system immediately. Only BIOS error messages appear.
Display Mode at Add-On ROM Init	***Force BIOS*** or ***Keep Current***. If you set the option to ***Force BIOS***, the display mode currently being used by AMIBIOS is used. If you set the option to ***Keep Current***, the current display mode is used.

4. Exit the Option window.
5. Exit the Advanced Setup window.

5.17 Configuring PCI Plug and Play Capabilities

WINBIOS Setup plug and play options allow you to:

- Enable the plug and play features
- Set the PCI latency timer
- Declare the PCI IDE bus master

- Allocate IRQ lines for PCI devices
- Specify IRQ lines for legacy ISA adapter cards

5.17.1 Enabling and Disabling PCI Plug and Play Features

AMIBIOS detects and enables PCI plug and play ISA adapter cards that are required for system booting. In addition, the Windows NT operating system detects and enables all other plug and play adapter cards. The optimal and fail-safe default settings for this option are ***No***. However, before adding PCI plug and play adapter cards to the system, you must set this option to ***Yes*** to ensure that the cards are configured properly.

To enable or disable PCI plug and play features:

1. Select the **PCI/PnP** icon in the Setup window.
2. Select the **Plug and Play Aware O/S** option.
3. Set the option value to ***Yes*** or ***No***, as appropriate.
4. Exit the Option window.
5. Set other plug and play options, as appropriate.
6. Exit the PCI/PnP Setup window.

5.17.2 Setting the PCI Latency Timer

The default PCI latency timer setting is 64 (PCI clocks). To adjust this setting:

1. Select the **PCI/PnP** icon in the Setup window.
2. Select the **PCI Latency Timer (PCI Clocks)** option.
3. Set the option value to ***32***, ***64***, ***96***, ***128***, ***160***, ***192***, ***224***, or ***248***. The default is ***64***.
4. Exit the Option window.
5. Exit the PCI/PnP Setup window.

5.17.3 Declaring the PCI IDE Bus Master

You can declare the IDE controller on the PCI local bus as bus master. As bus master, the controller has specific capabilities for controlling access to the bus. To declare the controller as bus master:

1. Select the **PCI/PnP** icon in the Setup window.
2. Select the **PCI IDE Bus Master** option.
3. Set the option value to ***Enabled***.
4. Exit the Option window.
5. Exit the PCI/PnP Setup window.

5.17.4 Allocating IRQ Lines for PCI Devices

When AMIBIOS configures onboard PCI plug and play devices, it acquires an IRQ line for each device from a pool of available IRQ lines. If you have a need to explicitly remove an IRQ line from the pool of available lines for explicit use by a PCI device, remove the line as follows:

Up to four IRQs can be allocated to the PCI bus. The IRQs are allocated according to PCI slot position and the capabilities of the PCI option card.

Assuming all IRQs are available to the PCI bus, the order of allocation is as follows: 11, 10, 9, 15, 5, 3, 7, 4, 12, and 14.

To allocate an IRQ line to a PCI device:

1. Select the **PCI/PnP** icon in the Setup window.
2. Select the **IRQ*n*** option that corresponds to an IRQ line to be allocated.
3. Set the value to ***PCP/PnP***.

   AMIBIOS removes the corresponding IRQ line from the pool of available IRQ lines that can be assigned automatically to configured onboard PCI plug and play devices.
4. Exit the Option window.
5. Exit the PCI/PnP Setup window.

5.17.5 Configuring Legacy ISA/EISA Adapter Cards

The system supports the use of both ISA/EISA plug and play adapter cards and legacy ISA/EISA adapter cards. By default, the system assumes that any adapter cards that you install are plug and play cards. If you install a legacy ISA/EISA adapter card, you need to identify the IRQ lines and DMA channels to be used by the device and specify the starting address and amount of ROM needed to support the device.

To configure a legacy ISA/EISA adapter card:

1. Select the **PCI/PnP** icon in the Setup window.
2. Select the **Reserved Memory Size** option.
3. Set the option value to ***16K***, **32K**, or **64K**, as appropriate.

   If multiple ISA/EISA adapter cards are installed, this value must accomodate all cards.
4. Exit the Option window.
5. Select the **Reserved Memory Address** option.
6. Set the starting address of the reserved area of memory to hexadecimal value ***C0000***, ***C4000***, ***C8000***, ***CC000***, ***D0000***, ***D4000***, ***D8000***, or ***DC000***.
7. Exit the Option window.
8. Select the **IRQ*n*** option that corresponds to an IRQ line to be used by ISA/EISA devices.
9. Set the option value to ***ISA/EISA***.

When set to ***ISA/EISA,*** AMIBIOS removes the corresponding IRQ line from the pool of available IRQ lines that can be assigned automatically to configured onboard PCI plug and play devices. The default setting for the **IRQ*n*** options is ***PCP/PnP***.

Up to four IRQs can be allocated to the PCI bus. The IRQs are allocated according to PCI slot position and the capabilities of the PCI option card.

10. Exit the Option window.
11. Select the **DMA Channel *n*** option that corresponds to the DMA channel to be reserved for use by ISA/EISA devices.
12. Set the option value to ***ISA/EISA***.

    When set to ***ISA/EISA,*** AMIBIOS removes the corresponding DMA channel from the pool of available channels that can be assigned automatically to configured onboard PCI plug and play devices. The default setting for the **DMA Channel *n*** options is ***PnP***.
13. Exit the Option window.
14. Exit the PCI/PnP Setup window.

5.18 Configuring LM78 System Management Features

Use WINBIOS Setup to configure the following LM78 system management features:

- Voltage fault alarm and minimum and maximum limits for the CPU core voltage and +3.3, +5, +12, and –12 voltages. A value outside the specified range triggers the voltage fault alarm.
- Intrusion alarm.
- SBC temperature alarm, a maximum temperature threshold, and a minimum (hysteresis) limit. A temperature that exceeds the maximum threshold triggers the temperature alarm. If this occurs and then the temperature falls below the hysteresis value, the temperature alarm is triggered again.

Sections 5.18.1 through 5.18.3 explain how to configure these features.

Note

Because the DIGITAL 5/233i-8 CompactPCI system uses variable-speed fans for cooling, the LM78 fan monitoring feature is disabled.

5.18.1 Configuring Voltage Monitoring Support

To configure voltage monitoring support:

1. Select the **Peripheral** icon in the Setup window.
2. Select the **Volt Fault Alarm** option.

3. Select one of the following option values:

To...	Select...
Disable voltage monitoring (fail-safe default)	***Disabled***
Enable voltage monitoring through the SMI (optimal default)	***SMI***
Enable voltage monitoring through the NMI	***NMI***

4. Exit the Option window.
5. If you selected ***Disabled*** in step 3, skip to step 7.
6. Specify a minimum and maximum threshold (as a percentage) for each of the following voltage options. The default settings for each option is –10% and +10%.
   - ***+3.3 V Alarm***
   - ***CPU Alarm***
   - ***+5 V Alarm***
   - ***+12 V Alarm***
   - ***–12 V Alarm***
7. Exit the Option window.
8. Exit the Peripheral Setup window.

5.18.2 Configuring Intrusion Alert Support

To use the intrusion alert support, an external sensor with a rear access I/O connector must be installed. To configure the support:

1. Select the **Peripheral** icon in the Setup window.
2. Select the **Intrusion Alarm** option.
3. Select one of the following option values:

To...	Select...
Disable the intrusion alarm (the default)	***Disabled***
Enable the intrusion alarm through the SMI	***SMI***
Enable the intrusion alarm through the NMI	***NMI***

4. Exit the Option window.
5. Exit the Peripheral Setup window.

5.18.3 Configuring Temperature Monitoring Support

To configure temperature monitoring support:

1. Select the **Peripheral** icon in the Setup window.
2. Select the **SBC Temp Alarm** option.

3. Select one of the following option values:

To...	Select...
Disable temperature monitoring (fail-safe default)	***Disabled***
Enable temperature monitoring through the SMI (optimal default)	***SMI***
Enable temperature monitoring through the NMI	***NMI***

4. Exit the Option window.
5. If you selected ***Disabled*** in step 3, skip to step 7.
6. Specify a minimum (hysteresis) temperature value and a maximum temperature threshold in degrees C by selecting and adjusting the values of options **Min (C)** and **Max (C)**.
7. Exit the Option window.
8. Exit the Peripheral Setup window.

5.19 Updating the BIOS Flash

At some point, you might have a need to upgrade the system's BIOS flash. This section explains the update procedure.

To get the latest version of the BIOS flash upgrade files, send an electronic mail request to:

compactPCI@digital.com

Note

Follow the steps for updating the flash ROM carefully. If you do not complete the procedure correctly, you can render the system unusable until the boot ROM or SBC is replaced.

To update the system's Flash BIOS:

1. Copy the binary BIOS image to a diskette and rename the file AMIBOOT.ROM.
2. Insert the diskette into the diskette drive.
3. Power on the system.
4. Hold the Ctrl and Home keys down simultaneously immediately after powering on the system (do not wait for video).

   Hold the keys down until the diskette drive access light comes on. The light indicates the update has started. The BIOS is automatically updated within approximately three minutes. The diskette drive access light stays lit and the video screen stays blank during the update.
5. Remove the diskette.
6. Reboot the system.

7. Reconfigure the system.

a. Start WINBIOS Setup.

a. Load the optimal default configuration.

b. Check the configuration settings. You may need to autodetect the hard disk drives and set up any customized options.

c. Exit WINBIOS Setup.

6

Upgrading and Replacing SBC Components

This chapter explains how to upgrade and replace SBC components. Topics include:

- What You Need
- Taking Precautions During System Maintenance
- Removing and Installing the SBC
- Adjusting Jumpers for Front Access I/O
- Upgrading and Replacing Memory
- Replacing the Lithium Battery

6.1 What You Need

To complete the procedures explained in this chapter, you need:

- The parts being added or used for replacement
- Phillips screwdriver
- Antistatic wriststrap or isolation gloves

6.2 Taking Precautions During System Maintenance

To avoid possible injury and damage to the system, take appropriate power supply and antistatic precautions before and while performing system maintenance procedures. Section 6.2.1 discusses power supply precautions and Section 6.2.2 discusses antistatic precautions.

6.2.1 Taking Power Supply Precautions

Before removing any enclosure panels, CompactPCI modules, filler panels, or removable bays or trays, take the following power supply precautions:

1. Power off external devices connected to the system.
2. Power off the system.
3. Unplug the power cord from the system's AC power inlet.

After you complete the maintenance procedure, reverse these steps to restore power.

6.2.2 Taking Antistatic Precautions

When handling circuit boards and associated internal computer components, use an antistatic wriststrap or wear isolation gloves.

Caution

Circuit boards and associated system components are sensitive to and can be damaged by electrostatic discharge (ESD). To avoid damaging boards or components, take appropriate precautions when handling them.

Vorsicht!

Gedruckte Schaltungen und dazu gehörende Systemkomponenten reagieren empfindlich auf elektrostatische Entladung und können durch elektrostatische Entladung sogar beschädigt werden. Treffen Sie die erforderlichen Vorsichtsmaßnahmen, damit Schaltplatten oder Systemkomponenten beim Ein- und Ausbau nicht beschädigt werden.

In addition to using an antistatic wriststrap or wearing isolation gloves, consider the following precautions:

- Do not allow a circuit board or other component to make contact with non-conductors, including your clothing.
- Keep loose circuit boards inside or on top of conductive plastic bags.
- Before touching a loose circuit board or component, discharge static electricity.

6.3 Removing and Installing the SBC

Before you remove or install the SBC, make sure you:

1. Power off external devices connected to the system.
2. Power off the system.
3. Unplug the power cord from the system's AC power inlet.

Caution

Take care when handling the SBC. Circuit boards are sensitive to and can be damaged by electostatic discharge (ESD). To avoid damaging the SBC, take appropriate precautions when handling it.

Vorsicht!

Seien Sie vorsichtig beim Umgang mit der SBC-Platine. Gedruckte Schaltungen und dazu gehörende Systemkomponenten reagieren empfindlich auf elektrostatische Entladung und können durch elektrostatische Entladung sogar beschädigt werden. Treffen Sie die erforderlichen Vorsichtsmaßnahmen, damit die SBC-Platine nicht beschädigt wird.

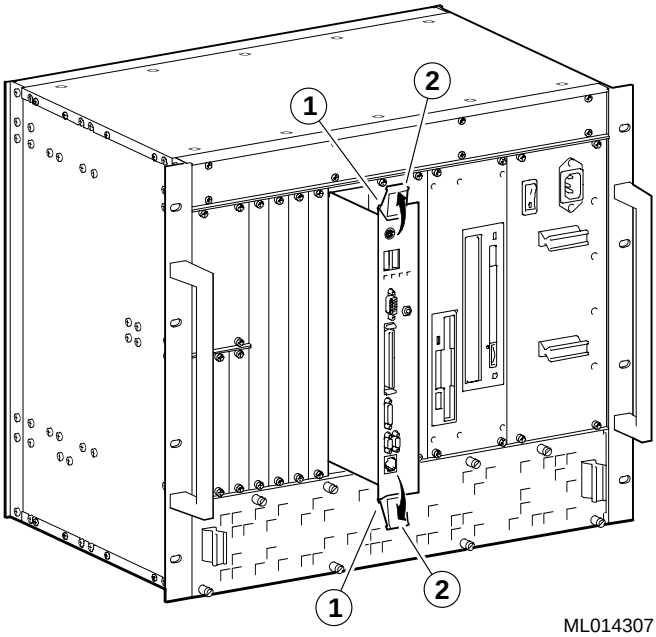
Sections 6.3.1 and 6.3.2 explain how to remove and install the SBC.

6.3.1 Removing the SBC

To remove the SBC, complete the following steps. Refer to Figure 6–1 as necessary.

1. Loosen the two captive screws (1), behind the handles, which secure the module to the chassis.
2. Simultaneously move the injector/ejector levers (2) of the two handles to the outward position.
3. Slide the module out of the chassis.

Figure 6–1 Removing the SBC

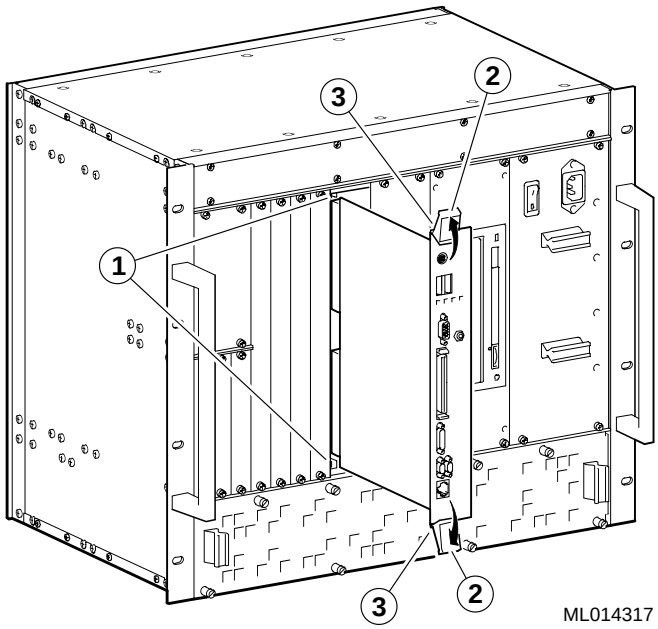


6.3.2 Installing the SBC

To install the SBC complete the following steps. Refer to Figure 6–2 as necessary.

1. Place the top and bottom edges of the module in the guides (1) of the chassis for slot 1 (the system slot).
2. Check that the injector/ejector levers (2) of the two handles are in the outward position.
3. Slide the module into the chassis until you feel resistance (approximately 1/4 inch short of full insertion).
4. Simultaneously move the injector/ejector levers of the two handles to the inward position.
5. Verify that the module is seated properly.
6. Tighten the two captive screws (3), behind the handles, which secure the module to the chassis.

Figure 6–2 Installing the SBC



6.4 Adjusting Jumpers for Front Access I/O

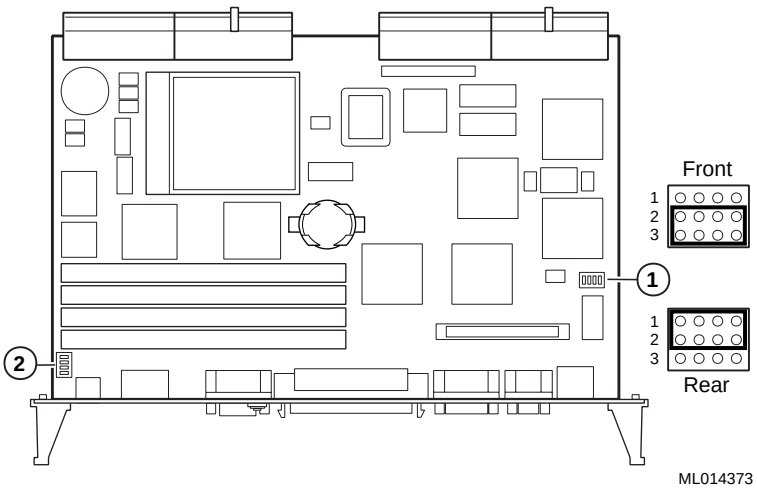
By default, the DIGITAL 5/233i-8 CompactPCI system assumes rear access I/O. If front access I/O is required or more appropriate for your application, you must adjust the settings of Ethernet and universal serial bus (USB) front/rear I/O access jumpers.

To adjust the jumpers for rear access I/O:

1. Remove the SBC from the chassis as explained in Section 6.3.1.
2. Adjust the jumpers.

Figure 6–3 identifies the Ethernet (1) and USB (2) front/rear I/O access jumper blocks on the SBC. To adjust Ethernet access, you must set the jumper for rear or front access as shown in Figure 6–3. To adjust USB access, you must install or remove the jumper block. When the jumper block is installed, the system is set up for rear I/O access. For front USB access, remove the jumper block.

Figure 6–3 Setting Front/Rear I/O Access Jumpers



3. Reinstall the SBC as explained in Section 6.3.2.

6.5 Upgrading and Replacing Memory

Before upgrading or replacing memory, make sure you are familiar with the system's memory configuration requirements and options. Section 2.2 discusses valid memory configurations.

To upgrade memory or replace bad SIMMs, you need to install and remove SIMMs as explained in Sections 6.5.2 and 6.5.3.

Caution

Take care when handling SIMMs. Circuit boards are sensitive to and can be damaged by electostatic discharge (ESD). To avoid damaging the memory modules, take appropriate precautions when handling them.

Vorsicht!

Seien Sie vorsichtig beim Umgang mit SIMM-Modulen. Gedruckte Schaltungen reagieren empfindlich auf elektrostatische Entladung und können durch elektrostatische Entladung sogar beschädigt werden. Treffen Sie die erforderlichen Vorsichtsmaßnahmen, damit die SIMM-Module nicht beschädigt werden.

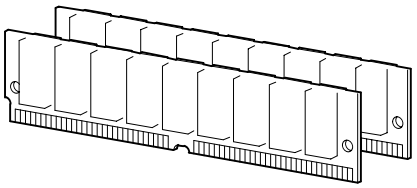
6.5.1 Memory Configurations

The DIGITAL 5/233i CompactPCI SBC is shipped with at least 32 MB of dynamic random access memory (DRAM) and supports memory configurations that range from 32 to 256 MB of DRAM. This memory is accessible from the CPU and PCI bus.

You can plug either two or four 36-bit 16, 32, or 64 MB SIMMs into the memory connectors on the SBC. SIMMs must be 36 bits wide.

Figure 6–4 shows a typical pair of memory modules.

Figure 6–4 Pair of Memory Modules



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When installing memory, you must adhere to the following requirements:

- SIMMs must be installed in pairs. That is, you must populate the memory banks with one of the following combinations:
  - Two slots: slot 0 (J6) of bank 0 and slot 1 (J7) of bank 0
  - Two slots: slot 0 (J8) of bank 1 and slot 1 (J9) of bank 1
  - Four slots: slots 0 and 1 of banks 0 and 1
- SIMMs installed in a given memory bank must be of the same size. For example, if you install a 64 MB SIMM in slot 0 of bank 0 you must install a 64 MB SIMM in slot 1 of bank 0.
- All SIMMs must be 60 ns extended data out (EDO) SIMMs.

Table 6–1 shows valid SIMM combinations.

Table 6–1 Valid SIMM Combinations

Total Memory	Bank 0 Slot 0 (J6)	Bank 0 Slot 1 (J7)	Bank 1 Slot 0 (J8)	Bank 1 Slot 1 (J9)
32 MB	16 MB	16 MB		
64 MB	16 MB	16 MB	16 MB	16 MB
64 MB	32 MB	32 MB		
96 MB	16 MB	16 MB	32 MB	32 MB
96 MB	32 MB	32 MB	16 MB	16 MB
128 MB	32 MB	32 MB	32 MB	32 MB
128 MB	64 MB	64 MB		
160 MB	16 MB	16 MB	64 MB	64 MB
160 MB	64 MB	64 MB	16 MB	16 MB
192 MB	32 MB	32 MB	64 MB	64 MB
192 MB	64 MB	64 MB	32 MB	32 MB
256 MB	64 MB	64 MB	64 MB	64 MB

6.5.2 Installing SIMMs

To install SIMMs on the SBC, complete the following steps. Refer to Figure 6–5, as necessary.

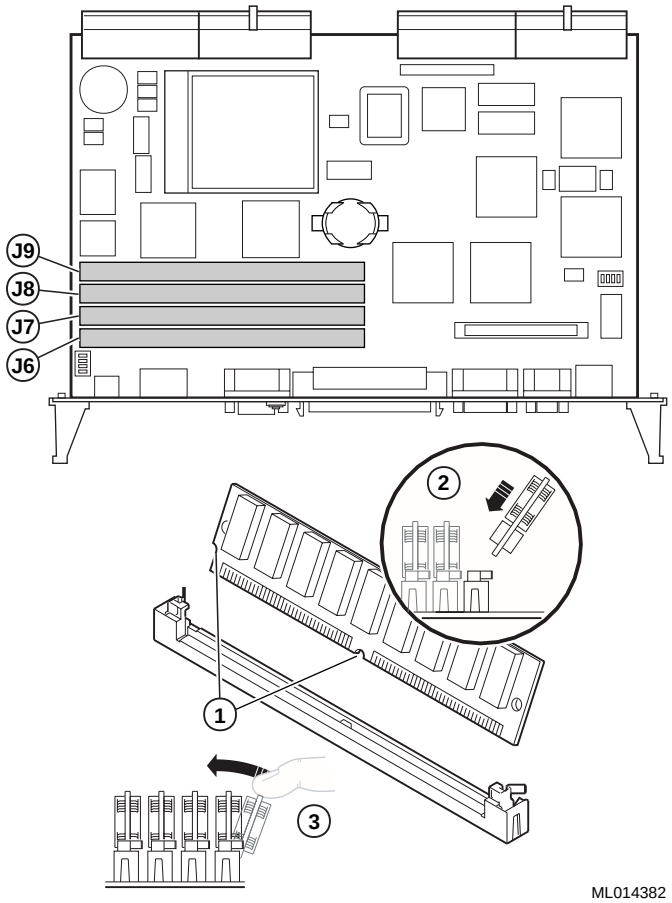
1. Remove the SBC from the chassis as explained in Section 6.3.1.
2. Locate the memory connectors into which the SIMMs are to be installed.

Note

Because you install SIMMs at a 45-degree angle, it may be necessary to remove existing SIMMs to install a new SIMM.

3. Align pin 1 of the SIMM with pin 1 on the connector. The position of the orientation notches (1) on the SIMM assure proper connectivity.
4. Install the SIMM into the connector at a 45-degree angle (2). Rock the SIMM gently until it seats evenly into the bottom of the connector.
5. Tip the SIMM upright until the retaining clips at the ends of the connector engage (3).
6. Repeat steps 3 through 5 for other SIMMs being installed.
7. Reinstall the SBC as explained in Section 6.3.2.
8. Plug the power cord into the system's AC power inlet and power on the system and any external devices.
9. Reboot the system. After the system reboots, it recognizes the new memory.

Figure 6–5 Installing a SIMM



6.5.3 Removing SIMMS

To remove SIMMs from the SBC, complete the following steps. Refer to Figure 6–6, as necessary.

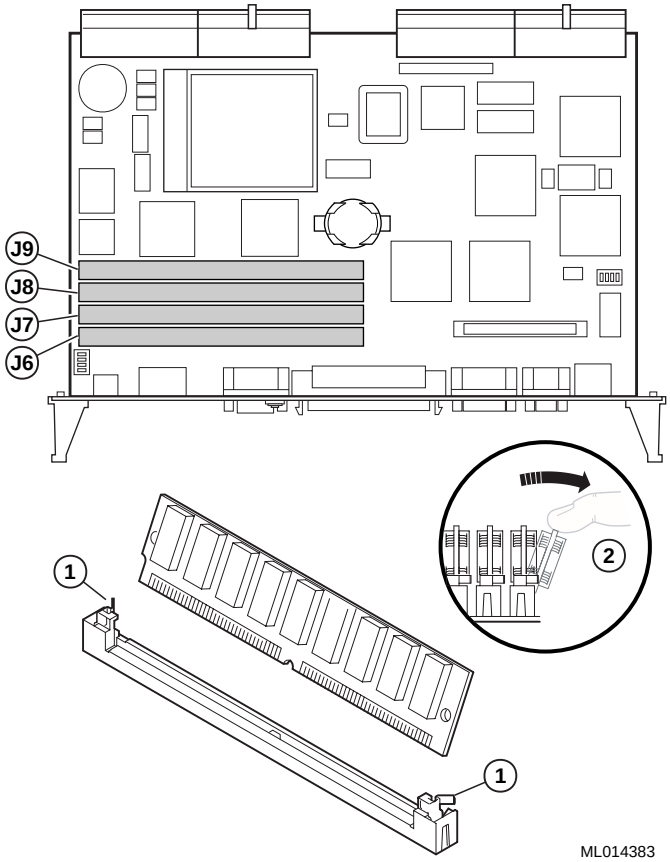
1. Remove the SBC from the chassis as explained in Section 6.3.1.
2. Locate the SIMMs that you need to remove.

Note

Because you remove SIMMs at a 45-degree angle, it may be necessary to remove multiple SIMMs to remove a specific SIMM of interest.

3. Apply pressure to the retaining clips (1) at the ends of the SIMM connector until the clips disengage.
4. Tip the SIMM until it is at a 45-degree angle (2).
5. Rock the SIMM gently as you remove it from the connector.
6. Repeat steps 3 through 5 for other SIMMs being removed.

Figure 6–6 Removing a SIMM



After you remove the SIMMs, install new SIMMs, if appropriate, as explained in Section 6.5. If you are not installing new SIMMs, install the SBC as explained in Section 6.3.2.

6.6 Replacing the Lithium Battery

The system lithium battery runs the system clock and retains configuration information when the system is powered off.

To replace the battery, complete the following steps. Refer to Figure 6–7, as necessary.

1. If the battery is not dead, use WINBIOS Setup to check and record the system's configuration settings.
2. Power off external devices connected to the system.
3. Power off the system.
4. Unplug the power cord from the system's AC power inlet.
5. Remove the SBC from the chassis as explained in Section 6.3.1.
6. Locate the battery on the SBC.
7. Carefully remove the old battery (1) from the battery connector (2).
8. Install the new battery such that the + side faces up.

Caution

The lithium battery can explode if you install it incorrectly. To prevent damage to the system, be sure the + side faces up when you install the new battery. Also, be sure you replace the battery with a CR2032 or equivalent 3 V dc lithium battery.

Depending on the locality, the system's battery might be considered hazardous waste. Make sure you follow any state or local statute to properly dispose of the old battery.

Vorsicht!

Die Lithiumbatterie kann bei falschem Einbau explodieren. Um eine Beschädigung des Systems zu vermeiden, sollte Sie sich vergewissern, daß Sie die neue Batterie mit der + Seite nach oben eingelegt haben. Vergewissern Sie sich außerdem, daß Sie die Batterie mit einer CR2032 oder einer entsprechenden 3 V DC Lithiumbatterie ausgetauscht haben.

Je nach Standort kann die Batterie des Systems als gefährlicher Abfall angesehen werden. Entsorgen Sie die alte Batterie gemäß der geltenden Umweltschutzvorschriften.

Avertissement

Mal installée, une batterie au lithium présente des risques d'explosion. Pour éviter d'endommager votre système, vérifiez que le côté positif (+) soit face vers le haut lorsque vous installez une nouvelle batterie. En outre, n'installez que des batteries au lithium 3V DC type CR2032 ou équivalent.

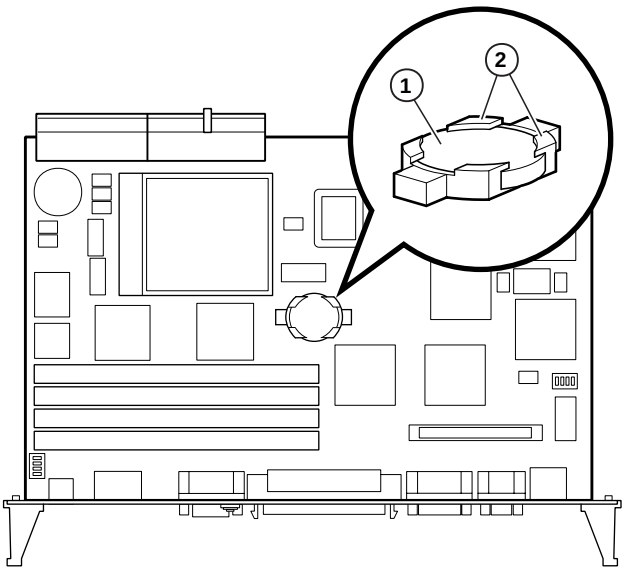
Il est possible que la législation en vigueur interdise de jeter les batteries. Renseignez-vous sur cette législation et appliquez-là à vos vieilles batteries.

---

9. Reinstall the SBC as explained in Section 6.3.2.

10. Plug the power cord into the system's AC power inlet.
11. Power on external devices connected to the system.
12. Power on the system.
13. If you were able to record the system's configuration settings in step 1 or if you kept a record of the settings, run WINBIOS Setup to reconfigure the system with the previous settings. If you do not have a record of the previous settings, load the default optimal BIOS settings as explained in Section 5.2.8

Figure 6–7 Installing the System Battery Clock



7

Connectors and Headers

This chapter describes the DIGITAL 5/233i CompactPCI single-board computer (SBC) connectors and headers. Topics include:

- J4 CompactPCI I/O Connector
- J5 CompactPCI I/O Connector
- Parallel Port Connector and Header
- PS/2 Keyboard/Mouse Connector
- Serial Port Connectors
- Universal Serial Bus Port Connectors
- Ethernet Connectors
- SCSI Connectors
- Video Connectors
- SIMM Connectors

7.1 Connectors and Headers

The SBC and rear transition module provide several connectors and headers for attaching devices. Connectors are located on the module front panels. Headers are mounted on the module circuit boards.

Warning

To reduce the risk of personal injury, always power off the system and unplug the power cord before connecting peripherals to the SBC or rear transition module.

ACHTUNG!

Schalten Sie immer das System aus und ziehen Sie das Netzkabel aus der Steckdose, bevor Sie Peripheriegeräte an den Zentralprozessor(SBC) oder das hintere Übergangsmodul anschließen.

7.2 J4 CompactPCI I/O Connector

The J4 CompactPCI I/O connector handles signals for the primary EIDE, diskette, SCSI, video, and Ethernet devices. Figure 7–1 shows the pin layout for the J4 connector as seen from the rear of the SBC. Table 7–1 lists the connector pin assignments. Table 7–2 defines the signals associated with the pins.

Note

An asterisk (*) in a signal name indicates that the signal is active low.

Figure 7–1 J4 Connector Pin Layout

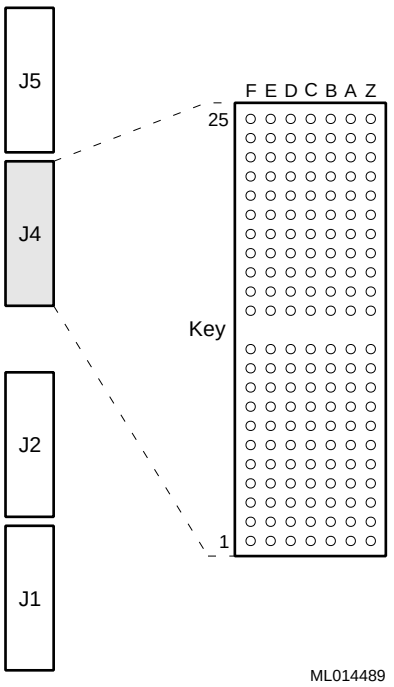


Table 7–1 J4 Connector Pin Assignments

Row	F	E	D	C	B	A	Z
25	GND	VCC	NC	NC	NC	NC	GND
24	GND	BTI*	GND	DASP*	CS3FX*	CS1FX*	GND
23	GND	DA2	DA0	GND	DA1	IOCS16*	GND
22	GND	INTRQ	DMAK*	NC	IORDY	GND	GND
21	GND	DIOR*	GND	DIOW*	GND	DMARQ	GND
20	GND	PDIAG*	GND	bDD15	bDD0	bDD14	GND
19	GND	bDD1	bDD13	bDD2	bDD12	bDD3	GND
18	GND	bDD11	bDD4	bDD10	bDD5	bDD9	GND

Table 7–1 J4 Connector Pin Assignments (Continued)

Row	F	E	D	C	B	A	Z
17	GND	bDD6	bDD8	bDD7	GND	DRESET*	GND
16	GND	GND	RD*	RD	TD*	TD	GND
15	GND	LED1_2	LED3	VCC	VCC	GND	GND
Key							
11	GND	GND	GND	NC	DACVSS	BLUE	GND
10	GND	GREEN	RED	FVSYNC	FHSYNC	MID3	GND
9	GND	MID2	MID1	MID0	GND	GND	GND
8	GND	SCD12	SCD13	SCD14	SCD15	SCDPH-2	GND
7	GND	SCD0	SCD1	SCD2	SCD3	SCD4	GND
6	GND	SCD	SCD6	SCD7	SCDPL-2	GND	GND
5	GND	GND	VCC	VCC	GND	GND	GND
4	GND	ATN-2	GND	BSY-2	SACK-2	SRST-2	GND
3	GND	MSG-2	SEL-2	CD-2	SREQ-2	IO-2	GND
2	GND	SCD8	SCD9	SCD10	SCD11	PBYPASS	GND
1	GND	FAN3	FAN2	INTRUDER*	SSDA	SSL	GND

Table 7–2 J4 Connector Signal Definitions

Signal	Definition
General	
GND	To SBC ground plane
NC	No connection
VCC	SBC +5 V power
EIDE (ATA–2), TTL Levels	
BTI*	Board temperature interrupt — input connected to the LM78 system monitor chip that can be driven by an LM75 temperature sensor chip
CS1FX*	Chip select drive 0 and command register block select
CS3FX*	Chip select drive 1 and command register block select
DA<2:0>	Drive register and data port address lines
DASP*	Drive active/slave present
DD<15:0>	Drive data lines, bits 15 to 0
DIOR*	Drive I/O read
DIOW*	Drive I/O write
DMAK*	Drive DMA acknowledge

Table 7–2 J4 Connector Signal Definitions (Continued)

Signal	Definition
DMARQ	Drive DMA request
DRESET*	Reset signal to drive
INTRQ	Drive interrupt request
IOCS16*	Indicates a 16-bit register has been decoded
IORDY	Indicates drive is ready for I/O cycles
PDIAG	Output generated from drive 1 and monitored by drive 0
Ethernet	
LED1_2	Transmit
LED3	Link
RD*	Receive lines
TD*	Transmit lines
SCSI	
SCD<15:0>	Data lines
ATN-2	Driven as an indicator when a special condition occurs
BSY-2	Driven by the initiator as a hand-shake during arbitration
CD-2	Indicates the command or message phase when asserted and the data phase when deasserted
IO-2	Indicates the “in” direction when asserted and the “out” direction when deasserted
MSG-2	Indicates the message phase when asserted and the command or data phase when deasserted
SACK-2	An initiator will assert ACK to indicate a byte is ready for or was received from the target
SCDPH-2	Provides odd parity for data lines 2SCD<15:8>
SCDPL-2	Provides odd parity for data lines 2SCD<7:0>
SEL-2	Drive after a successful arbitration to select as an initiator or reselect as a target
SREQ-2	A target will assert REQ to indicate a byte is ready or is needed by the target
SRST-2	Interpreted as a hard reset
Video	
BLUE	Blue signal
DACVSS	Shielded ground wire
FHSYNC	Horizontal synchronization pulse
FVSYNC	Vertical synchronization pulse
GREEN	Green signal

Table 7–2 J4 Connector Signal Definitions (Continued)

Signal	Definition
MID<3:0>	Bidirectional output that reflects the address into the palette DAC or input that can be used to drive pixel values into the palette DAC
RED	Red signal
Miscellaneous	
PBYPASS*	LM78 output from the SBC that can be used, under software control, for power supply bypass control, fan control, or general purpose output
FAN3	Tachometer for fan 2 rotational speed input to the SBC
FAN2	Tachometer for fan 3 rotational speed input to the SBC
INTRUDER*	Battery backed signal that can be asserted by an external monitoring device when enclosure security is breached
SSDA	LM78 system monitor I2C serial bus data
SSCL	LM78 system monitor I2C serial bus clock

7.3 J5 CompactPCI I/O Connector

The J5 CompactPCI I/O connector handles signals for the serial ports, parallel port, keyboard and mouse, universal serial bus (USB) ports, and secondary EIDE devices. Figure 7–2 shows the pin layout for the J5 connector as seen from the rear of the SBC. Table 7–3 lists the connector pin assignments. Table 7–4 defines the signals associated with the pins.

Note

An asterisk (*) in a signal name indicates that the signal is active low.

Figure 7–2 J5 Connector Pin Layout

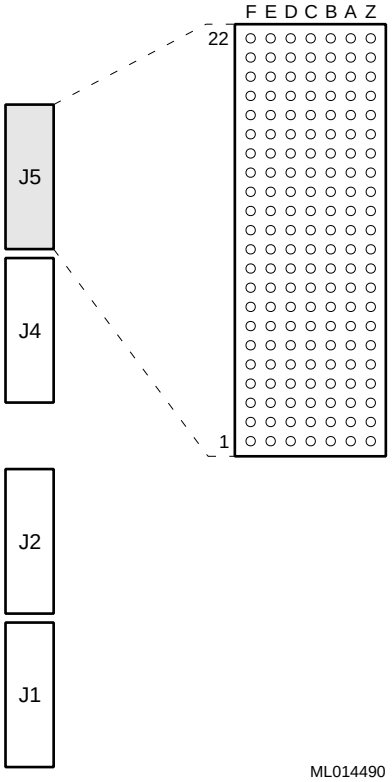


Table 7–3 J5 Connector Pin Assignments

Row	F	E	D	C	B	A	Z
22	GND	SPKR*OC	VCC	DIAG*OC	GND	PBRESET*	GND
21	GND	AUXCLK	AUXDAT	VCC[1]	KBDCLK	KBDDAT	GND
20	GND		GND[1]			VCC[1]	GND
19	GND	UDATA0-	UDATA0+	VCC[1]	GND[1]	STB*	GND
18	GND	VCC[1]	GND[1]	UDATA1-	UDATA1+	AFD*	GND
17	GND	PD0	ERR*	PD1	INIT*	PD2	GND
16	GND	SLIN*	PD3	PD4	PD5	PD6	GND
15	GND	PD7	ACK*	BUSY	PE	SLCT	GND
14	GND	DTRa	GND	RIa	CTSa	RTSa	GND
13	GND	TXDa	DSRa	RXDa	VCC	DCDa	GND
12	GND	DTRb	VCC	RIb	CTSb	RTSb	GND
11	GND	TSCb	DSRb	RXDb	GND	DCDb	GND
10	GND	DSKCHG*	HDSEL*	RDATA*	WPROT*	TR0*	GND
9	GND	WGATE*	WDATA*	STEP*	DIR*	MTR1*	GND
8	GND	DS0*	DS1*	MTR0*	INDEX*	DRVDENS1	GND

Table 7–3 J5 Connector Pin Assignments (Continued)

Row	F	E	D	C	B	A	Z
7	GND	DRVDENS0	DASP*	DA1	CS3FX*	CS1FX*	GND
6	GND	DA2	DA0	PDIAG*	GND	IOCS16*	GND
5	GND	DIOR*	DMACK*	DIOW*	IORDY	DMARQ	GND
4	GND	INTRQ	DD15	GND	DD0	DD14	GND
3	GND	DD1	DD13	DD2	DD12	DD3	GND
2	GND	DD11	DD4	DD10	DD5	DD9	GND
1	GND	DD6	DD8	DD7	DRESET*	RESET*	GND

[1] You can limit the current or do EMI filtering on these lines for direct cabling purposes.

Table 7–4 J5 Connector Signal Definitions

Signal	Definition
General	
GND	To ground plane
VCC	+5 V power supply
Diskette Drive, TTL Levels	
DSKCHG*	Indicates the drive door is open
DIR*	Controls the direction of the head during step operations
DRVDENS<1:0>	Disk density select communication
DS<1:0>*	Drive selects
HDSEL*	Selects the top or bottom side head
INDEX*	Indicates the beginning of a track
MTR<1:0>*	Motor enable
RDATA*	Read data from the drive
STEP*	Step - pulses move the head in or out
TR0*	Indicates that the head is positioned above track 00
WDATA*	Write data to the drive
WGATE*	Enables the head write circuitry of the drive
WPROT*	Indicates a diskette is write protected
EIDE (ATA-2), TTL Levels	
CS1FX*	Chip select drive 0 and command register block select
CS3FX*	Chip select drive 1 and command register block select
DA<2:0>	Drive register and data port address lines

Table 7–4 J5 Connector Signal Definitions (Continued)

Signal	Definition
DASP*	Drive active/slave present
DD<15:0>	Drive data lines for bits 15 to 0
DIOR*	Drive I/O read
DIOW*	Drive I/O write
DMACK*	Drive DMA acknowledge
DMARQ	Drive DMA request
DRESET*	Reset signal to drive
INTRQ	Drive interrupt request
IOCS16*	Indicates a 16-bit register has been decoded
IORDY	Indicates drive is ready for I/O cycles
PDIAG	Output generated from drive 1 and monitored by drive 0
Keyboard/Mouse, TTL Levels	
AUXCLK	Clock for the PS/2 auxilary device (mouse)
AUXDAT	Serial data line for the mouse
KBDCLK	Clock for the PC/AT or PS/2 keyboard
KBDDAT	Serial data line for the PC/AT or PS/2 keyboard
Parallel Port	
ACK*	Pulsed by the peripheral device to acknowledge data was sent
AFD*	Causes the printer to generate a line feed
BUSY	Indicates that the printer cannot accept more data
ERR*	The peripheral device detected an error
INIT*	Initializes the printer
PD<7:0>	Parallel port data lines, bits 7 to 0
PE	Indicates the printer is out of paper
SLCT	The peripheral device indicates that it is selected
SLIN*	Selects the printer
STB*	Indicates data is valid
Serial Ports (a/b), RS232 Levels	
CTSa/CTSb	Clear to send
DCDa/DCDb	Data carrier detected
DSRa/DSRb	Data set ready
DTRa/DTRb	Data terminal ready
RIa/RIb	Ring indicator

Table 7–4 J5 Connector Signal Definitions (Continued)

Signal	Definition
RTSa/RTSb	Request to send
RXDa/RXDb	Serial receive data
TXDa/TXDb	Serial transmit data
USB Ports (0/1), USB Levels	
UDATA0+/UDATA1+	Plus (+) signal of differential data pair for the USB channel
UDATA0–/UDATA0–	Minus (–) signal of differential data pair for the USB channel
Miscellaneous	
DIAG*OC	Diagnostic and alarm output, open collector output
PBRESET*	Pushbutton system reset input (pulled up, filtered, and debounced on the host card)
RESET*	System reset output, TTL totem-pole
SPKR*OC	PC/AT speaker output, open collector output

7.4 Parallel Port Connector and Header

The parallel port is normally used for connecting a printer to the system. On the front panel of the SBC, this port is a 25-pin micro-D connector (J22).

Figure 7–3 shows the pin layout for the parallel port connector. Table 7–5 lists the connector pin assignments. Table 7–6 defines the signals associated with the pins.

Note

An asterisk (*) in a signal name indicates that the signal is active low.

Figure 7–3 Parallel Port Connector Pin Layout

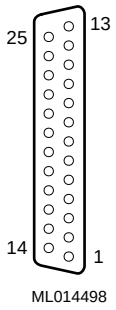


Table 7–5 Parallel Port Connector Pin Assignments

Signal	I/O Direction	Pin	Pin	I/O Direction	Signal
			13	Input	SLCT
GND		25	12	Input	PE
GND		24	11	Input	BUSY*
GND		23	10	Input	ACK*
GND		22	9	Input/Output	D7
GND		21	8	Input/Output	D6
GND		20	7	Input/Output	D5
GND		19	6	Input/Output	D4
GND		18	5	Input/Output	D3
SLIN*	Output	17	4	Input/Output	D2
INIT*	Output	16	3	Input/Output	D1
ERR*	Input	15	2	Input/Output	D0
AFD*	Output	14	1	Output	STB*

Table 7–6 Parallel Port Connector Signal Definitions

Signal	Definition
ACK*	Input is pulsed by the peripheral device to acknowledge data retrieval
AFD*	Causes the printer to add a line feed
BUSY*	Indicates that the printer cannot accept any more data
ERR*	Set low when an error is detected
GND	Ground
INIT*	Initializes the printer
PD<7:0>	Parallel port data lines, bits 7 to 0
PE	Indicates that the printer is out of paper
SLCT	Set high when selected
SLIN*	Selects the printer
STB*	Indicates that data at the parallel port is valid

7.5 PS/2 Keyboard/Mouse Connector

A 6-pin PS/2 keyboard/mouse connector (J15) is on the front panel of the SBC .

Figure 7–4 shows the pin layout for the PS/2 keyboard/mouse connector. Table 7–7 lists the connector pin assignments for the SBC's keyboard/mouse combination connector. Table 7–8 defines the signals associated with the pins.

Notes

An asterisk (*) in a signal name indicates that the signal is active low.

Figure 7–4 PS/2 Keyboard/Mouse Connector Pin Layout

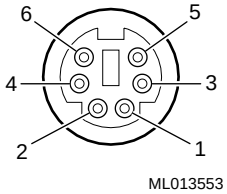


Table 7–7 PS/2 Keyboard/Mouse Combination Connector Pin Assignments

Pin	Signal
1	KBDDAT*
2	MDAT*
3	GND
4	VCC (+5 V)
5	KBDCLK*
6	MCLK*

Note

Power present on a keyboard/mouse connector is only for use by the keyboard or mouse.

Table 7–8 PS/2 Keyboard/Mouse Connector Signal Definitions

Signal	Definition
GND	Ground
KBDCLK	Keyboard clock
KBDDAT	Keyboard data

Table 7–8 PS/2 Keyboard/Mouse Connector Signal Definitions

Signal	Definition
VCC (+5 V)	Keyboard or mouse power
MCLK	Mouse clock
MDAT	Mouse data

Note

Power present on the keyboard/mouse connector is only for use by the keyboard or mouse.

7.6 Serial Port Connectors

The serial ports are used for connecting serial devices, such as a serial mouse or serial printer, to the system. Serial ports are also known as COM or Universal Asynchronous Receiver/Transmitter (UART) ports. On the front panel of the SBC, the serial ports are 9-pin micro D connectors.

Figure 7–5 shows the pin layout for the serial port connectors. Table 7–9 lists the connector pin assignments. Table 7–10 defines the signals associated with the pins.

Note

An asterisk (*) in a signal name indicates that the signal is active low.

Figure 7–5 Serial Port Connector Pin Layout

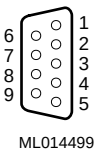


Table 7–9 Serial Port Connector Pin Assignments

Signal	Pin	Pin	Signal
		1	DCD
DRS	6	2	RXD
RTS	7	3	TXD
CTS	8	4	DTR
RI	9	5	GND

Table 7–10 Serial Port Connector Signal Definitions

Signal	Definition
CTS	Indicates that the data set is ready to accept data
DCD	Indicates that the data set has detected the data carrier
DSR	Indicates that the data set is ready to establish a communications link
DTR	Indicates that the data terminal equipment (DTE), is ready to accept a communications link
GND	Ground
RI	Indicates that the modem has received a telephone ringing signal
RTS	Indicates to the data set that the DTE is ready to send data
RXD	Receives serial data from the communications link
TXD	Sends serial data to the communications link

7.7 Universal Serial Bus Port Connectors

Two universal serial bus (USB) port connectors (J18) reside on the front panel of the SBC. The USB jumper on the SBC enables the front access connectors on the SBC or the rear access connectors on a rear transition module (see Section 2.2). The factory setting is for rear access connectors. To use front access connectors, you must remove the jumper as explained in Section 6.4.

Note

Be sure to plug the USB cables into the USB connectors that are enabled.

Figure 7–6 shows the pin layout for the USB connectors. Table 7–11 lists the connector pin assignments. Table 7–12 defines the signals associated with the pins.

Note

An asterisk (*) in a signal name indicates that the signal is active low.

Figure 7–6 USB Port Connector Pin Layout

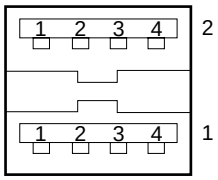


Table 7–11 USB Port Connector Pin Assignments

Pin	Signal
4	GND
3	USBP2/USBP1
2	USBP2*/USBP1*
1	VCC (+5 V)

Table 7–12 USB Port Connector Signal Definitions

Signal	Definition
GND	Ground
USBP2*/USBP2	Differential data pair for serial bus 2
USBP1*/USBP1	Differential data pair for serial bus 1
VCC	Power (+5 V)

7.8 Ethernet Connectors

An Ethernet connector (J16) resides on the front panel of the SBC . The Ethernet jumper on the SBC enables the front access connector on the SBC or a rear access connector on a rear transition module (see Section 2.2). The factory setting enables the rear access connector. To use the front access connector, you must reposition the jumper as explained in Section 6.4.

Note

Be sure to plug the Ethernet cable into the Ethernet connector that is enabled.

Figure 7–7 shows the pin layout for the Ethernet connectors. Table 7–13 lists the connector pin assignments. Table 7–14 defines the signals associated with the pins.

Note

An asterisk (*) in a signal name indicates that the signal is active low.

Figure 7–7 Ethernet Connector Pin Layout

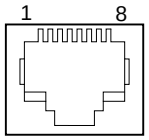


Table 7–13 Ethernet Connector Pin Assignments

Pin	Signal
1	TX
2	TX*
3	RX
4	REF

Table 7–13 Ethernet Connector Pin Assignments (Continued)

Pin	Signal
5	REF
6	RX*
7	NC
8	NC

Table 7–14 Ethernet Connector Signal Definitions

Signal	Definition
NC	No connection
REF	Floating reference signals tied together through 75Ω resistors to a common point
RX	Receive line
TX	Transmit line

7.9 SCSI Connectors

A 68-pin SCSI connector resides on the front panel of the SBC (J19).

Figure 7–8 shows the pin layout for the SCSI connector. Table 7–15 lists the connector pin assignments. Table 7–16 defines the signals associated with the pins.

Note

An asterisk (*) in a signal name indicates that the signal is active low.

Figure 7–8 SCSI Connector Pin Layout

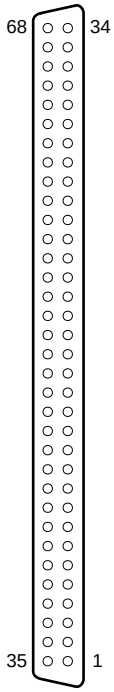


Table 7–15 SCSI Connector Pin Assignments

Signal	Pin	Pin	Signal
SCD11	68	34	GND
SCD10	67	33	GND
SCD9	66	32	GND
SCD8	65	31	GND
IO*	64	30	GND
SREQ*	63	29	GND
CD*	62	28	GND
SEL*	61	27	GND
MSG*	60	26	GND
SRST*	59	25	GND
SACK*	58	24	GND
BSY*	57	23	GND
GND	56	22	GND
ATN*	55	21	GND
GND	54	20	GND
NC	53	19	NC

Table 7–15 SCSI Connector Pin Assignments (Continued)

Signal	Pin	Pin	Signal
TERMPWR	52	18	TERMPWR
TERMPWR	51	17	TERMPWR
GND	50	16	GND
GND	49	15	GND
SCDPL*	48	14	GND
SCD7	47	13	GND
SCD6	46	12	GND
SCD5	45	11	GND
SCD4	44	10	GND
SCD3	43	9	GND
SCD2	42	8	GND
SCD1	41	7	GND
SCD0	40	6	GND
SCDPH*	39	5	GND
SCD15	38	4	GND
SCD14	37	3	GND
SCD13	36	2	GND
SCD12	35	1	GND

Table 7–16 SCSI Connector Signal Definitions

Signal	Definition
ATN*	Driven as an initiator when a special condition exists
BSY*	Driven by an initiator as a hand-shake during arbitration
CD*	Indicates the command or message phase when asserted and the data phase when deasserted
GND	Ground
IO*	Indicates the “in” direction when asserted and the “out” direction when deasserted
MSG*	Indicates the message phase when asserted and the command or data phase when deasserted
NC	No connection
SACK*	An initiator will assert ACK to indicate a byte is ready for or was received from the target
SCD<15:0>	SCSI data lines
SCDPH*	Provides odd parity for SCD<15:8>

Table 7–16 SCSI Connector Signal Definitions (Continued)

Signal	Definition
SCDPL*	Provides odd parity for SCD<7:0>
SEL*	Driven after a successful arbitration to select as an initiator or reselect as a target
SREQ*	A target will assert REQ to indicate that a byte is ready or is needed by the target
SRST*	Interpreted as a hard reset
TERMPWR	Termination power

7.10 Video Connectors

A 15-pin standard D video connector resides on the front panel of the SBC (J17).

Figure 7–9 shows the pin layout for the video connector. Table 7–17 lists the connector pin assignments. Table 7–18 defines the signals associated with the pins.

Note

An asterisk (*) in a signal name indicates that the signal is active low.

Figure 7–9 Video Connector Pin Layout

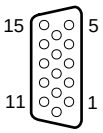


Table 7–17 Video Connector Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal
15	MID3	10	DACVSS	5	DACVSS
14	VSYNC	9	NC	4	MID2
13	HSYNC	8	DACVSS	3	BLUE
12	MID1	7	DACVSS	2	GREEN
11	MID0	6	DACVSS	1	RED

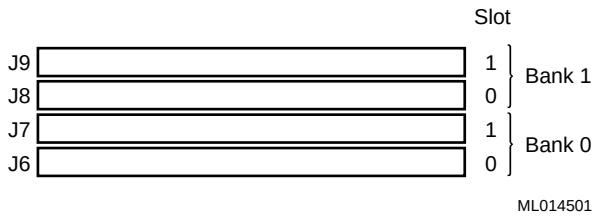
Table 7–18 Video Connector Signal Definitions

Signal	Definition
BLUE	Blue signal
DACVSS	Shielded ground wire
GREEN	Green signal
HSYNC	Horizontal synchronization
MID<3:0>	Bidirectional output that reflects the address into the palette DAC or input that can be used to drive pixel values into the palette DAC
NC	No connection
RED	Red signal
VSYNC	Vertical synchronization

7.11 SIMM Connectors

Four SIMM connectors are on the SBC. These connectors are organized into two banks as shown in Figure 7–10. For information on valid memory configurations, see Section 2.2.

Figure 7–10 SIMM Connectors



8

System Address Mapping and Interrupts

This chapter discusses system address mapping and system interrupts. Topics include:

- PCI I/O Address Map
- Memory Address Map
- DMA Channel Assignments
- System Interrupts

8.1 PCI I/O Address Map

PCI I/O address space is mapped dynamically each time the system boots or through the operating system by way of plug and play capabilities. Regardless of the dynamic mapping, legacy I/O locations remain constant.

Table 8–1 shows the PCI I/O address map. Address functions listed as optional normally are not occupied by onboard resources. You use WINBIOS Setup or special utilities to enable or relocate these features from default values.

Table 8–1 PCI I/O Address Map

Physical Address Range	Function
0000 – 000F	DMA controller 1
0020 – 0021	Interrupt controller 1
0040 – 0043	Counter timer
0060 – 0064	Keyboard, nonmaskable interrupt (NMI), and speaker
0070 – 0071	Real-time clock and NMI mask
0050–0057[1]	LM78 system monitor (optional)
0058–005F[1]	Watchdog timer, ENUM (optional)
0080 – 009F	DMA page register and POST checkpoint
00A0 – 00BF	Interrupt controller 2
00C0 – 0000DF	DMA controller 2
00F0	Reset coprocessor
0170 – 0177[2]	Secondary IDE channel (optional)
01F0 – 01F7[2]	Primary IDE channel
0278 – 027F[3]	Parallel port 2 (optional)
02E8 – 02EF[3]	Serial port 4 (optional)

Table 8–1 PCI I/O Address Map (Continued)

Physical Address Range	Function
02F8 – 02FF[2]	Serial port 2 (default)
0376 – 0377[2]	Secondary IDE port (optional)
0378 – 037F[2]	Parallel port 1 (default)
03BC – 03C3[3]	Parallel port 3 (optional)
03E8 – 03EF[3]	Serial port 3 (optional)
03F0 – 03F5	Diskette channel
03F6 – 03F7	Primary IDE and diskette
03F8 – 03FF[2]	Serial port 1 (default)
040A – 043F	DMA scatter/gather
0480 – 048F	DMA high pages
04D0 – 04D1	Edge/level interrupts
04D6	DMA 2 extended mode
0678 – 067A[3]	Parallel port 2 (optional)
0778 – 077A[3]	Parallel port 1 (optional)
07BC – 07BE[3]	Parallel port 3 (optional)
0CF8 – 0CFF	PCI configuration

[1] The watchdog timer and LM78 normally are disabled, but may be relocated and enabled by way of the PCI configuration.
[2] These ports are available if the listed function is not enabled in WINBIOS Setup.
[3] This is an alternate range that you can select by using WINBIOS Setup.

8.2 Memory Address Map

PCI memory address space is mapped dynamically each time the system boots or through the operating system by way of plug and play capabilities. Regardless of the dynamic mapping, legacy memory locations remain constant.

Table 8–2 shows the memory address map.

Table 8–2 Memory Address Map

Physical Address Range	Function
000000 – 09FFFF	Conventional RAM
0A0000 – 0BFFFF	VGA DRAM[1]
0C0000 – 0C7FFF	VGA ROM[1]
0C8000 – 0DFFFF	Expansion ROM
0E0000 – 0EFFFF	System BIOS extensions
0F0000 – 0FFFFF	AMI system BIOS (AMIBIOS)

[1] Typically on the PCI backplane.

8.3 DMA Channel Assignments

Table 8–3 lists DMA channel assignments.

Table 8–3 DMA Channels

Channel	Function
DMA 0	ISA memory refresh
DMA 1	Reserved
DMA 2	Diskette controller
DMA 3	Reserved
DMA 4	Cascade for DMA 1
DMA 5	Reserved
DMA 6	Reserved
DMA 7	Reserved

8.4 System Interrupts

Table 8–4 lists system interrupt request (IRQ) numbers and associated functions.

Table 8–4 System Interrupts

IRQ#	Function
NMI	Reports parity and system errors
SMI	System management, ECC APM, and so on
0	System timer
1	Keyboard
2	Cascade for IRQs 8 through 15
3	COM 2 (serial port 2)
4	COM 1 (serial port 1)
5	Parallel port 2
6	Diskette controller
7	Parallel port 1
8	Real-time clock
9	Software redirect to IRQ2
10	Reserved
11	Reserved (special features)
12	Reserved (PS/2 mouse)
13	Coprocessor
14	Hard disk controller
15	Reserved

9

System Management

A field programmable gate array (FPGA) and the LM78 Microprocessor System Hardware Monitor on the SBC, provide advanced system management features designed for use in critical industrial control applications. This chapter describes and explains how to use these features. Topics include:

- System Management Features
- Gaining Access to the System Management Features
- FPGA Registers
- Using the Watchdog Timer
- Using the LM78 System Monitor

9.1 System Management Features

Table 9–1 lists the system management features, all of which are accessible through the address programmed into the programmable chip select (PCS) register in the PCI-to-ISA bridge.

Table 9–1 System Management Features

Feature	Description
Watchdog timer	A countdown timer. When the countdown reaches zero, the timer can set a flag in a register, optionally assert an I/O check (IOCHK) signal, and optionally perform an SBC reset.
System monitor	Monitors backplane and CPU voltage, SBC temperature, fan rotation, and intrusion. Errors are reported through the local nonmaskable interrupt (NMI) or system management interrupt (SMI).

9.2 Gaining Access to the System Management Features

You gain access to the system management features through the address programmed in the system's PCS register on the PCI-to-ISA bridge. The BIOS sets the PCS register address to 0050h by default. To read the register and determine the base address, read from PCI-to-ISA bridge device address 07h, function 00h, registers 78h and 79h.

Note

If the default PCS address assignment results in a conflict for your application, you have the option of changing it.

To gain access to the FPGA watchdog timer features, you must do so programmatically by using the PCS port offsets listed in Table 9–2.

Table 9–2 PCS Port Offsets

Port	Register	Description
0Bh	Watchdog strobe register	Controls the watchdog timer.
0Dh	FPGA index register	Determines which FPGA register is accessible from port 0Fh.
0Fh	FPGA data register	Provides access to the watchdog strobe register.

The LM78 system management features are accessible through port offsets 00h to 07h. You also have the option of configuring the voltage, fan, temperature, and intrusion alarms by using WINBIOS Setup (see Section 5.18). Any changes that you make are stored in CMOS memory and take effect the next time the system boots. As the system boots, the BIOS programs the LM78 with the new settings and reports the measurement and status of the various system management features.

9.3 FPGA Registers

To use the watchdog timer features, you must read from and write data to the following set of FPGA registers:

- Watchdog register
- Watchdog strobe register
- FPGA data register
- FPGA index register

9.3.1 Watchdog Register

The watchdog register contains fields for clearing the watchdog timer and controlling the mode and delay of the timer. Figure 9–1 shows the watchdog register. Table 9–3 describes the fields of the register.

Figure 9–1 Watchdog Register

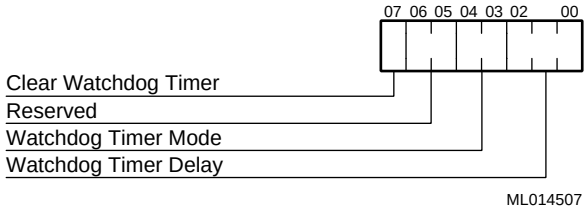


Table 9–3 Watchdog Register Fields

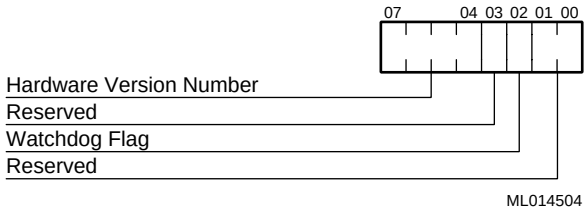
Field	Description
<7>	When set, this bit clears the watchdog timer function. To restart the watchdog timer, this bit must be cleared. This bit must be set before the watchdog flag bit of the card status and watchdog strobe register (see Section 9.3.2) can be cleared.
<6:5>	Reserved
<4:3>	Control the mode of the watchdog timer. Possible values and their associated modes include: 00 – Disable the watchdog timer 01 – Set the watchdog flag in the watchdog strobe register when the timer countdown reaches zeroes 10 – Set the watchdog flag in the watchdog strobe register and assert the I/O channel ready (IOCHRDY) signal when the timer countdown reaches zeroes 11 – Set the watchdog flag in the watchdog strobe register, assert the IOCHRDY signal, start a second counter, and if the second counter reaches zero before the interrupt is cleared, reset the SBC
<2:0>	Control the delay of the watchdog timer until bits <4:3> are activated. Possible delay values include: 000 – 17.8 milliseconds 001 – 71.1 milliseconds 010 – 284 milliseconds 011 – 1.14 seconds 100 – 4.55 seconds 101 – 18.22 seconds 110 – 72.8 seconds 111 – 291 seconds

9.3.2 Watchdog Strobe Register

The watchdog strobe register at port 0Bh is a read/write register. A write operation to the register sets the watchdog timer to the value of the watchdog delay that is programmed in the watchdog register. A read of the register can acquire the status of a watchdog flag bit. The watchdog timer sets this bit when the timer reaches zero. To reset this flag, you must clear the watchdog timer by setting the clear watchdog bit in the watchdog register. Figures 9–2 and 9–3 show the register definitions for write and read operations.

Figure 9–2 Watchdog Strobe Register – Write

Figure 9–3 Watchdog Strobe Register – Read



9.3.3 FPGA Index Register

The FPGA register at port offset 0Dh includes a 3-bit index field that determines which functional FPGA registers are accessible from the FPGA data register. The index is reset to zero following any data port access or after a reset. This feature helps to protect registers that control important option module operations. Figure 9–4 shows the FPGA index register. Table 9–4 lists the possible index values and the registers to which they provide access.

Figure 9–4 FPGA Index Register

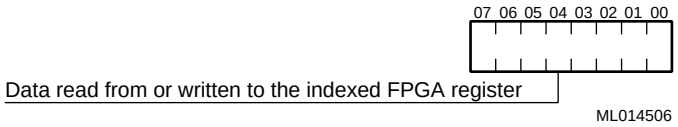
Table 9–4 FPGA Function Index Values

Value	Provides Access To...
00h	Reserved
01h	Reserved
02h	Reserved
03h	Watchdog registers
04h	Reserved
05h	Reserved
06h	Reserved
07h	Reserved
08h	Reserved
09h	Reserved
0Ah	Reserved
0Bh	ENUM status and control (unsupported)
0Ch	ENUM storage (unsupported)

9.3.4 FPGA Data Register

The FPGA data register at port 0Fh serves as the communication mechanism for the FPGA. The function of each bit is dependent on the value set in the function index field of the FPGA index register. Figure 9–5 shows the FPGA data register.

Figure 9–5 FPGA Data Register



9.4 Using the Watchdog Timer

The watchdog timer is designed for use in critical control applications. The timer's function is to stop a program or part of the hardware from going into a run-away or locked mode. Sections 9.4.1 to 9.4.6 explain how to:

- Enable the watchdog timer
- Reset the watchdog timer
- Set the watchdog timer mode and delay
- Reset the watchdog timer delay
- Check the status of the watchdog timer
- Use the watchdog interrupt

9.4.1 Enabling the Watchdog Timer

To enable the watchdog timer for a read or write operation:

1. Set the function index field of the FPGA index register to 03h.
2. Write data to or read data from bits <7:0> of the FPGA data register.

Note

After each read or write operation, the index value is reset to 00h. Thus, you must set the function index to 03h before each operation. This prevents accidental use of the watchdog timer.

9.4.2 Resetting the Watchdog Timer

To reset the watchdog timer after it has been enabled, you must set the clear watchdog bit (bit <7>) in the watchdog register. This clears the timer, making it ready for a restart.

9.4.3 Setting the Watchdog Timer Mode and Delay

To set the watchdog timer mode and delay, write appropriate values to bits <4:3> and <2:0>, respectively. Section 9.3.1 lists the possible values with corresponding modes and delays.

9.4.4 Resetting the Watchdog Timer Delay

To reset the watchdog timer delay to the value programmed in the watchdog register, write to the watchdog strobe register.

9.4.5 Checking the Status of the Watchdog Timer

To check the status of the watchdog timer, read bit <2> of the card status and watchdog strobe register.

9.4.6 Using the Watchdog Interrupt

To use the watchdog interrupt, you must enable it through the SMC Ultra I/O device. The device signal is routed to the GP10 input line, which can generate an interrupt. Table 9–5 shows a sequence of write operations that enable the watchdog interrupt out to interrupt line 11 (INT 11).

Table 9–5 Enabling the Watchdog Interrupt

Step	Operation	Data	Port
Put the SMC Ultra I/O device into configuration mode.	Write	055h	390h
	Write	055h	390h
Index the logical device number	Write	007h	390h
Set the logical device number to 8	Write	008h	391h
Index GP11	Write	0E1h	390h
Enable GP11 to INT 10*	Write	0B9h*	391h
Index GP11	Write	0E1h	390h
Index activate	Write	030h	390h
Activate change	Write	001h	390h
Exit SMC configuration mode	Write	0AAh	390h

* To program another interrupt, set the upper nibble of this byte to the interrupt number. Possible choices are INT 5 (059h), INT 7 (079h), INT 9 (099h), INT 10 (0A9h), INT 11 (0B9h), INT 12 (0C9h), INT14 (0E9h), and INT 15 (0F9h).

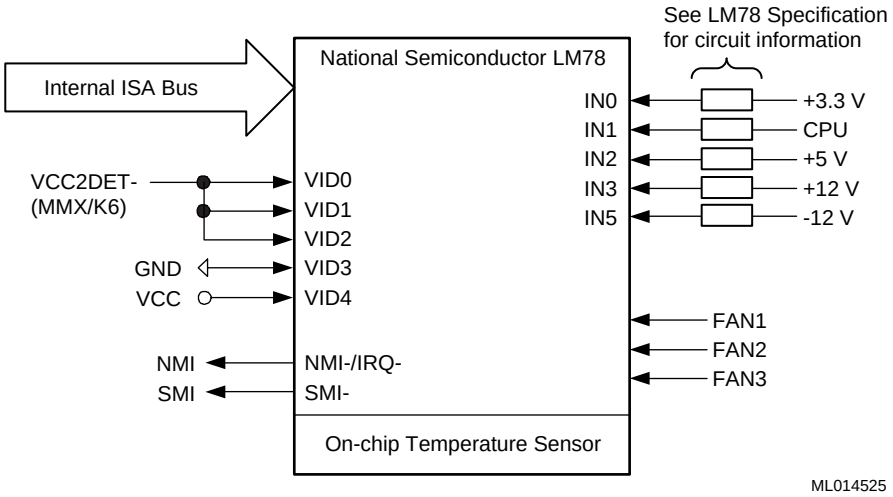
Note

To ensure that the interrupt is not used by PCI devices, you must reserve the interrupt for the ISA device in with WINBIOS Setup, as explained in Section 5.17.4.

9.5 Using the LM78 System Monitor

The LM78 Microprocessor System Hardware Monitor is decoded at the PCS address and uses port offsets 0 to 7. Figure 9–6 shows how the LM78 is connected for monitoring CPU voltages, temperatures, and fan speeds.

Figure 9–6 LM78 Connections



For more information on the LM78 device, see the *LM78 Microprocessor Hardware System Monitor* data sheet.

10
Troubleshooting

This chapter explains how to troubleshoot systems that include the DIGITAL 5/233i CompactPCI SBC. Topics include:

- Basic Troubleshooting Tips
- Troubleshooting Your System
- Responding to Blink Codes and Error Messages

10.1 Basic Troubleshooting Tips

Most computer system failures result from incorrect installation, improper configuration, or incompatible application software or hardware. The following troubleshooting tips can help you solve most system problems:

- Troubleshoot one problem at a time and make only one change at a time. For example, if the hard disk drive fails to boot, do not try all suggested corrective actions at once. Start with one suggestion, such as checking the cables. After securing the cables, try rebooting the system. If it does not work, try another suggestion.
- Look for abnormal LED behavior. For example, make sure the power LED lights when you power on the system and that the drive access indicators light when using the diskette, hard disk, or CD–ROM drive.
- If power-on self test (POST) errors appear on the monitor screen, run WINBIOS Setup and correct the problems identified by the POST error messages.
- If you installed external devices, make sure all cables are correctly and securely connected to the appropriate devices.
- If you installed internal devices, make sure nothing was bumped or jarred loose, and that all cable connections are securely in place.
- Make sure all device drivers are installed correctly.
- If your system hangs, soft boot the system (press the Ctrl, Alt, and Del keys simultaneously). If the system fails to boot, power it off, wait until the disk drives spin down completely, and power the system back on.
- Pay close attention to error messages that appear on the monitor screen. If an error message is system related, see Section B.2 for recommended actions. If an error message is specific to the operating system, refer to the online help and appropriate operating system documentation.
- Watch the speaker LED for blink codes. Record the number of blinks and their pattern. Check the blink code descriptions in Section B.1 for recommended actions.

- After the POST completes, check each line of the system startup and configuration files as appropriate for the operating system being used.
- Read any available README files. README files might be on the CD–ROM disk, or available as printed material. This information can help you set up, configure, and operate your system.

10.2 Troubleshooting Your System

This section will help you troubleshoot problems in systems that include the DIGITAL 5/233i CompactPCI SBC. System problems are usually caused by components being jarred loose during relocation, loose cables, cables connected to the wrong devices, and external device failure.

Table 10–1 lists possible system problems with probable causes and corrective actions to take. If you are not able to solve a problem after consulting the information in this chapter, see the Warranty and Parts Information that shipped with the SBC for information on how to contact customer support.

Table 10–1 Troubleshooting System Problems

Problem	Possible Cause	Action
No response when the system is **powered on**.	System is not plugged in.	Power off the system, plug it in, and power it back on.
	No power at the power outlet.	Use another power outlet.
	Voltage select switch is set incorrectly.	Adjust the voltage select switch.
	Internal system cables are loose.	Check the connections of all internal cables.
	CPU module components were jarred loose during shipping.	Remove the CPU module and check that the CPU and SIMMs are seated properly.
	Pins in a backplane connector are bent or broken.	Contact your service provider.
	Power supply failure.	Contact your service provider.
	SBC failure.	Replace the SBC.
Power is on and a display appears on the monitor screen, but the system does not respond to **keyboard or mouse input**.	Keyboard or mouse is not connected.	Connect the keyboard and mouse to the front panel of the SBC.
	The keyboard or mouse is connected to the wrong port.	If the keyboard and mouse are connected, confirm that they are connected to the correct ports.
Power is on, but no **display** appears on the monitor screen.	Brightness and contrast controls are not set correctly.	Adjust the brightness and contrast controls.
	The monitor-off timer has powered the monitor off.	Press the [Shift] key to reactivate the monitor.
	The monitor is not powered on.	Power on the monitor.
	The monitor cable is installed incorrectly.	Check all monitor cable connections.
	The required video driver is not installed.	Install the required video driver.
	Monitor failure.	Try another monitor.
	Video controller failure.	Replace the SBC.

Table 10–1 Troubleshooting System Problems (Continued)

Problem	Possible Cause	Action
Serial ports are not functional.	A serial port cable is installed incorrectly.	Check all serial port cable connections.
	The serial ports are disabled in the BIOS setup.	Run the BIOS setup utility and enable the serial ports.
	Serial port failure.	Try the other serial port. If the second port fails, contact your service provider.
	Controller failure.	Replace the SBC.
Parallel port is not functional.	The parallel port cable is installed incorrectly.	Check all parallel port cable connections.
	The parallel port is disabled or is not configured correctly in the BIOS setup.	Run the BIOS setup utility and enable the parallel port. Also, make sure the port is configured correctly for the type of printer that is being used.
	Parallel port failure.	Replace the SBC.
	Controller failure.	Replace the SBC.
Ethernet port is not functional.	The Ethernet cable is installed incorrectly.	Check all Ethernet cable connections.
	The onboard Ethernet controller is disabled in the BIOS setup.	Run the BIOS setup utility and enable the onboard Ethernet controller.
	Ethernet port failure.	Replace the SBC.
	Ethernet controller failure.	Replace the SBC.
USB port is not functional.	A USB cable is installed incorrectly.	Check all USB cable connections.
	The USB ports are disabled or are not configured correctly in the BIOS setup.	Run the BIOS setup utility and enable the USB ports. Also, make sure the USB ports are configured correctly for the types of devices being used.
	USB port failure.	Replace the SBC.
	Controller failure.	Replace the SBC.

Table 10–1 Troubleshooting System Problems (Continued)

Problem	Possible Cause	Action
System operates incorrectly after installing optional **SIMMs**.	SIMMs are installed incorrectly.	Remove the CPU module and make sure that both SIMM connectors in each bank are filled with the correct SIMM size, speed, and type.
	SIMM failure.	Remove and reinstall the SIMMs as explained in Section 6.5. Make sure that both SIMM connectors in each bank are filled with the correct SIMM size, speed, and type. Replace the SIMMs, following instructions in Section 6.5.
System fails to retain **setup information**.	System battery failure.	Replace the system battery.
System displays **HIMEM.SYS errors**.	Unstable memory at the specified address.	Run diagnostics. Replace faulty SIMMs as explained in Section 6.5
System displays a System **Error F002** message	Faulty hardware.	Run diagnostic software to identify the faulty hardware. Replace the faulty hardware or contact your service provider.
"**Error 0000001E**"	Your hard disk drive might have corrupted system files.	Run **chkdsk** on your hard disk drive to correct corrupted files. If the problem still exists, contact your service provider.
"**NMI Hardware Error**"	Faulty hardware.	Make sure all SIMM and SBC connectors are clean and properly seated in their respective sockets. Run diagnostic software, such as AMIDIAG, to identify the faulty hardware. Replace the faulty hardware or contact your service provider.
Services or subsystems do not start properly	Improper configuration, required files are missing, or required files are not installed.	Check for status. Also, check the system log for entries relating to the problem. If the problem still exists, contact your service provider.

Table 10–1 Troubleshooting System Problems (Continued)

Problem	Possible Cause	Action
System does not recognize a **SCSI hard disk drive or device**.	SCSI ID conflicts exist.	See the SCSI device kit installation instructions on setting SCSI IDs.
	Terminating resistors have not been removed from the SCSI device.	Remove the terminating resistors. See the SCSI device kit installation instructions.
	SCSI option is not enabled in the BIOS setup.	Run the BIOS setup utility and enable the onboard SCSI controller.
	SCSI cable is not terminated.	Terminate each end of the SCSI cable.
	SCSI device is not plugged in.	Check power and SCSI cable connections.
	Loose SCSI cable connections.	Check and secure all SCSI cable connections.
	Hard disk boot sector is missing.	Repartition and reformat your hard disk drive. **Caution:** This procedure erases what is currently on your hard disk drive. Consider repairing the hard disk drive by using a disk drive repair utility. You can purchase disk drive repair utilities from a local software supplier.
System does not recognize a **SCSI hard disk drive or device**.	A boot sector virus might exist.	Run anti-virus software.
	SCSI adapter failure.	Replace the SBC.
	SCSI ribbon cable failure.	Replace the cable.
	SCSI device failure.	Replace the SCSI device
No response to **keyboard** commands.	Keyboard is password protected.	Enter the keyboard password.
	Keyboard is not connected.	Power off the system and connect the keyboard.
	Keyboard is connected to the mouse port.	Power off the system and connect the keyboard to the keyboard port.
	System halted.	Reboot the system.
	Keyboard failure.	If available, try another keyboard. If the new keyboard operates correctly, replace the old keyboard.
	Keyboard/mouse controller failure.	Replace the SBC.

Table 10–1 Troubleshooting System Problems (Continued)

Problem	Possible Cause	Action
Keyboard keys type incorrectly.	Keyboard failure.	If available, try another keyboard. If the new keyboard operates correctly, replace the old keyboard.
No response to **mouse** activity	Mouse is not connected.	Power off the system and connect the mouse.
	Mouse is connected to the keyboard port.	Power off the system and connect the mouse to the mouse port.
	System halted.	Reboot the system.
	Mouse driver is not installed.	Install the required mouse driver. See your application software documentation.
	Mouse port is disabled or not configured correctly in the BIOS setup.	Run the BIOS setup utility and enable the PS/2 mouse port. If you are using a PS/2 mouse, also make sure the **IRQ12/M Mouse Function** option is enabled.
	Mouse failure.	If available, try another mouse. If the new mouse operates correctly, replace the old mouse.
	Keyboard/mouse controller failure.	Replace the SBC.
Mouse sticks.	Dirty mouse ball.	Remove mouse ball and clean it.

10.3 Responding to Blink Codes and Error Messages

When you power on your system, the BIOS runs power-on self test (POST) routines that initialize the system and compare the defined configuration with hardware that is actually installed. The system monitor or terminal displays codes and initialization messages as the POST routines run.

The BIOS reports errors with blink codes and error messages. A blink code is a series of light blinks on the system's speaker LED, which is identified in Figure 2–1.

Note

The BIOS for DIGITAL 5/233i-8 CompactPCI systems displays blink codes on the speaker LED instead of sounding beep codes, because the systems do not include a speaker.

The method the BIOS uses for reporting an error depends on when the error occurs as indicated in Table 10–2.

Table 10–2 BIOS Error Reporting

If...	Then...
The error occurs before the display device is initialized	A series of blinks appear on the speaker LED. Blink codes indicate that a fatal error has occurred. For a listing of blink codes, see Section B.1.
The error occurs after the display device is initialized	An error message is displayed. A prompt to press the <F1> key might also appear with some error messages. For a listing of error messages, see Section B.2.

10.3.1 Responding to Blink Codes

Table 10–3 lists corrective actions if the system displays blink codes on the speaker LED. For a listing of possible blink codes and descriptions, see Section B.1.

Table 10–3 Troubleshooting Based on Blink Codes

If the LED Blinks...	Then...
1, 2, or 3 times	Reseat the memory SIMMs. If this does not correct the problem, replace the SIMMs.
8 times	The video adapter is not accessible or has a problem. Replace the SBC.
9 times	The BIOS PROM is not accessible or has a problem. Replace the SBC.
11 times	A problem exists in the onboard cache memory. Replace the SBC.
4, 5, 6, 7, or 10 times	Replace the SBC.

10.3.2 Responding to Error Messages

If the BIOS detects an error while the system is powering up and the system monitor has been initialized and is functional, the BIOS displays an error message as follows:

```
ERROR Message Line 1
```

If this message appears, press the F1 key to continue.

The following message might also appear:

```
RUN SETUP UTILITY.
```

If this message appears, press the F1 key to run WINBIOS Setup.

For a listing of BIOS error messages and descriptions, see Section B.2.

A

BIOS Option Summary

Tables A–1 through A–4 summarize the BIOS menu options that are available through the Setup, Security, Utility, and Default WINBIOS windows. Factory (optimal) default settings appear in bold type. Optimal and fail-safe defaults are the same unless noted otherwise.

Table A–1 Setup Options

Options	Settings	Comments
Standard		
Pri Master Pri Slave Sec Master Sec Slave		Configure the system's hard disk drives. All options except **Type** apply to IDE drives.
Type[1]	***Not Installed*** (Secondary Master and Secondary Slave) *1* to *46* ***User*** (Primary Master) *Auto* ***ARMD*** (Primary Slave) *ARMD*	Select a value in the range 43 to 46 for an MFM device. Select ***User*** for a SCSI, MFM, RLL, ARLL or ESDI drive. If you enter ***User***, you must configure all disk drive options manually. For IDE drives, you can select ***Auto*** for automatic device detection and configuration.
LBA/Large Mode	*Off* ***On***	Turn this mode ***On*** for any device between 528 MB and 8.4 GB in size.
Block Mode	*Off* ***On***	Increases the transfer size from 512 bytes per interrupt to 64 KB.
32-Bit Mode	*Off* ***On***	The PCI bus supports 32-bit data transfers.
PIO Mode	***Auto*** *0* - 600 ns *1* - 383 ns *2* - 240 ns *3* - 180 ns *4* - 120 ns	The programmable input/output (PIO) mode represents the timing cycles between IDE drives and the programmable IDE controller. You should set the PIO mode at the highest value that the system allows. To use PIO mode 4, the IDE cable cannot exceed 15 inches long.
Cyl[1]		Specifies the number of cylinders.
Hd[1]		Specifies the number of heads.
WP[1]		Specifies the number of cylinders that have their write timing changed.
Sec[1]		Specifies the number of sectors.
Size[1]		Specifies the capacity of the device in MB.
Date/Time		
Date	*day mmm dd yyyy*	Sets the system data and time.
Time	*hh: mm: ss:*	

Table A–1 Setup Options (Continued)

Floppy A, Floppy B:	***Not Installed*** (B:) *360 KB 5 1/4* *1.2 MB 5 1/4* *720 KB 3 1/2* ***1.44 MB 3 1/2*** (A:) *2.88 MB 3 1/2*	Configures the system's diskette drives.
Advanced		
Quick Boot	***Disabled*** *Enabled*	Powers on to flash ROM within five seconds. The fail-safe default is ***Disabled***.
Pri Master ARMD Emulated as	*Auto* *Floppy* ***Hard Disk***	Specifies whether an ATAPI removeable media device is to be emulated as a diskette or hard disk drive. When set to ***Auto***, the BIOS defaults to hard disk drive emulation.
Pri Slave ARMD Emulated as	***Auto*** *Floppy* *Hard Disk*	Specifies whether an ATAPI removeable media device is to be emulated as a diskette or hard disk drive. When set to ***Auto***, the BIOS defaults to hard disk drive emulation.
Sec Master ARMD Emulated as	***Auto*** *Floppy* *Hard Disk*	Specifies whether an ATAPI removeable media device is to be emulated as a diskette or hard disk drive. When set to ***Auto***, the BIOS defaults to hard disk drive emulation.
Sec Slave ARMD Emulated as	***Auto*** *Floppy* *Hard Disk*	Specifies whether an ATAPI removeable media device is to be emulated as a diskette or hard disk drive. When set to ***Auto***, the BIOS defaults to hard disk drive emulation.
1st Boot Device	*Disabled* *1st IDE-HDD* *2nd IDE-HDD* *3rd IDE-HDD* *4th IDE-HDD* ***Floppy*** *ARMD-FDD* *ARMD-HDD* *ATAPI CDROM* *SCSI* *NETWORK* *I20*	Specifies the first device for which to look and use for booting the system.
2nd Boot Device	*Dissabled* ***1st IDE-HDD*** *2nd IDE-HDD* *3rd IDE-HDD* *4th IDE-HDD* *Floppy* *ARMD-FDD* *ARMD-HDD* *ATAPI CDROM* *SCSI*	Specifies the device for which to look and use for booting the system if the first boot device is not available.

Table A–1 Setup Options (Continued)

3rd Boot Device	*Dissabled* *1st IDE-HDD* *2nd IDE-HDD* *3rd IDE-HDD* *4th IDE-HDD* *Floppy* *ARMD-FDD* *ARMD-HDD* ***ATAPI CDROM***	Specifies the device for which to look and use for booting the system if the first and second boot devices are not available.
Try Other Boot Devices	***Yes*** *No*	Specifies whether the system should boot from other devices in the event that devices in the defined boot sequence are not available.
Initial Display Mode	***BIOS*** *Silent*	Specifies whether BIOS messages are to be displayed on the monitor screen during the boot process.
Display Mode at Add-On ROM Init	*Force BIOS* ***Keep Current***	Specifies the system display mode that is to be used when the BIOS POST initializes an optional adaptor ROM.
Floppy Access Control	***Read-Write*** *Read-Only*	Specifies the type of access control allowed for the diskette drive.
Hard Disk Access Control	***Read-Write*** *Read-Only*	Specifies the type of access control allowed for the hard disk drive.
S.M.A.R.T. for Hard Disks	***Disabled*** *Enabled*	Enables or disables the System Management and Reporting Technologies (S.M.A.R.T.) protocol for reporting server system information over the network.
BootUp Num-Lock	*Off* ***On***	Turns Numlock on or off each time the system boots.
Floppy Drive Swap	***Disabled*** *Enabled*	Specifies whether diskette drives A: and B: can be swapped.
Flopply Drive Seek	***Disabled*** *Enabled*	Specifies whether diskette drive A: is to perform a seek operation at system boot.
PS/2 Mouse Support	*Disabled* ***Enabled***	Enables or disables support for a PS/2 type mouse.
System Keyboard	*Absent* ***Present***	Specifies whether error messages are to be displayed if a keyboard is not attached to the system.
Primary Display	*Absent* ***VGA/EGA*** *CGA 40x25* *CGA 80x25* *Mono*	Specifies the type of video display being used.
Password Check	***Setup*** *Always*	Specifies whether to prompt for a password on every system boot, or only when running WINBIOS Setup.
Boot to OS/2	***No*** *Yes*	Not applicable. The system boots Windows NT.

Table A–1 Setup Options (Continued)

Wait For 'F1' If Error	*Disabled* ***Enabled***	Specifies whether the BIOS is to prompt (and wait for) the user to press <F1> before continuing when an error occurs.
Hit 'DEL' Message Display	*Disabled* ***Enabled***	Specifies whether the BIOS is to display the "Hit <DEL> if you want to run Setup" message when the system boots.
Internal Cache	*Disabled* ***WriteBack***	Disables or enables the system's internal cache to operate in write-back mode. For optimal performance, keep this setting in write-back mode. The fail-safe default is ***Disabled***. **Note:** The system's internal cache is integral to the CPU.
External Cache	*Disabled* ***Enabled***	Disables or enables the system's external cache. For optimal performance, enable caching. The fail-safe default is ***Disabled***.
System BIOS Cacheable	*Disabled* ***Enabled***	Disables or enables system BIOS caching. This increases system performance because the BIOS instructions can execute in cache instead of in RAM. The fail-safe default is ***Disabled***.
C000 , 16 K Shadow C400, 16 K Shadow C800, 16 K Shadow CC00, 16 K Shadow D000, 16 K Shadow D400, 16 K Shadow D800, 16 K Shadow DC00, 16 K Shadow	*Disabled* *Enabled* ***Cached***	Specifies whether the specified area of ROM is to be shadowed and if shadowed, whether it should be written to or read from cache memory. The fail-safe default is ***Disabled***. **Caution:** Some option ROMs do not operate properly when shadowed. **Vorsicht:** Einige optionelle ROM-Speicher funktionieren nicht einwandfrei, wenn sie "schattiert" werden.
Chipset		
USB Function	*Disabled* ***Enabled***	Disables or enables the universal serial bus connectors on the SBC's front panel.
USB KB/Mouse Legacy Support	***Disabled*** *Keyboard* *Auto* *Keyb+Mouse*	Disables or enables support for older keyboards and mouse devices.
USB Passive Release Enable	***Disabled*** *Enabled*	Disables or enables passive release for the USB.
DRAM Timings	***60ns*** *70ns*	Specifies the access speed of the SIMMs. Must be set to ***60ns***.
DRAM Data Integrity Mode	*Disabled* *ECC Level 1* ***ECC Level 2***	Disables or enables error correction code (ECC) Level 1 or Level 2 mode for single-bit error correction.
Power Management		

Table A–1 Setup Options (Continued)

Power Management/APM	***Disabled*** *Enabled*	Disables or enables power management and Advance Power Management (APM) features.
PCI/PNP		
Plug and Play Aware O/S	***No*** *Yes*	Specifies whether the operating system is plug and play aware. You must set this option correctly for installed plug-and-play aware adapter cards to be configured correctly.
PCI Latency Timer (PCI Clocks)	*32* ***64*** *96* *128* *160* *192* *224* *248*	Specifies the latency, in clock pulses, for devices on the PCI bus.
PCI IDE BusMaster	*Disabled* ***Enabled***	Disables or enables the PCI IDE bus as bus master. The fail-safe default is ***Disabled***.
DMA Channel 0, 1, 3, 5, 6, 7	***Pnp*** *ISA/EISA*	Reserves the specified DMA channel for use by a legacy ISA adapter card.
IRQ3, 4, 5, 7, 9, 10, 14, 15	***PCI/PnP*** *ISA/EISA*	Specify the bus on which the named IRQ is to be used. Up to four IRQs can be allocated to the PCI bus.
IRQ11	*PCI/PnP* ***ISA/EISA***	Specify the bus on which the named IRQ is to be used. Up to four IRQs can be allocated to the PCI bus.
Reserved Memory Size	***Disabled*** *16K* *32K* *64K*	Specifies the size of the memory area reserved for legacy ISA adapter cards.
Reserved Memory Address	*C0000* *C4000* ***C8000*** *CC000* *D0000* *D4000* *D8000* *DC000*	Specifies the starting address of a reserved memory area for legacy ISA adapter cards.
Peripheral		
Onboard FDC	***Auto*** *Disabled* *Enabled*	Disables or enables the onboard diskette drive controller. Specify ***Auto*** to auto-detect and configure the device.
Onboard Serial Port 1	***Auto*** *Disabled* *3F8h* *2F8h* *3E8h* *2E8h*	Disables or enables serial port 1and specifies the base I/O address for the port. Specify ***Auto*** to auto-detect and configure the device.

Table A–1 Setup Options (Continued)

Onboard Serial Port 2	***Auto*** *Disabled* *3F8h* *2F8h* *3E8h* *2E8h*	Disables or enables serial port 2 and specifies the base I/O address for the port. Specify ***Auto*** to auto-detect and configure the device.
Serial Port 2 Mode	***Normal*** *IrDA* *Ask IR*	
IR Transmission Mode	***Full Duplex*** *Half Duplex*	
Receiver Polarity	***Active High*** *Active Low*	
Transmitter Polarity	***Active High*** *Active Low*	
Onboard Parallel Port	***Auto*** *Disabled* *378* *278* *3BC*	Disables or enables the parallel port and specifies the base I/O address for the port. Specify ***Auto*** to auto-detect and configure the device.
Parallel Port Mode	*Normal* *EPP* ***ECP***	Specifies the mode to be used by the parallel port.
EPP Version	***1.9*** *1.7*	Specifies the version of the EPP to be used.
Onboard IDE	*Disabled* *Primary* *Secondary* ***Both***	Specifies the onboard IDE controller channels to be used.
Onboard PCI SCSI	*Disabled* ***Enabled***	Disables or enables the onboard SCSI controller.
Onboard Ethernet	*Disabled* ***Enabled***	Disables or enables the onboard Ethernet controller.
Volt Fault Alarm	*Disabled* ***SMI*** *NMI*	Disables or enables LM78 voltage monitoring. The fail-safe default is **Disabled**.
+3.3V Alarm Min Max	 *n*% (**–10%**) *n*% (**+10%**)	Configure the positive and negative limits for the +3.3 V power. If the power supply goes outside the specified limits, a fault can be generated.
CPU Alarm Min Max	 *n*% (**–10%**) *n*% (**+10%**)	Configure the positive and negative limits for the CPU core voltage. If the power supply goes outside the specified limits, a fault can be generated.
+5V Alarm Min Max	 *n*% (**–10%**) *n*% (**+10%**)	Configure the positive and negative limits for the +5 V power. If the power supply goes outside the specified limits, a fault can be generated.

Table A–1 Setup Options (Continued)

+12V Alarm Min Max	 *n*% (**–10%**) *n*% (**+10%**)	Configure the positive and negative limits for the +12 V power. If the power supply goes outside the specified limits, a fault can be generated.
–12V Alarm Min Max	 *n*% (**–10%**) *n*% (**+10%**)	Configure the positive and negative limits for the –12 V power. If the power supply goes outside the specified limits, a fault can be generated.
Intrusion Alarm	***Disabled*** *SMI* *NMI*	Disables or enables the intrusion alarm. If enabled and an intrusion occurs, a fault can be generated.
SBC Fan *n* Alarm	***Disabled*** *SMI* *NMI*	Disables or enables the tachometer input alarm for fan 1, 2, or 3.
Nominal Fan Speed	*n rpm* (**4000 rpm)**	Configures the nominal fan speed. If the fan speed falls below the specified speed, a fault can be generated.
SBC Temp Alarm	*Disabled* ***SMI*** *NMI*	Disables or enables the temperature alarm.
SBC Temp Alarm Min (C) Max (C)	 *nn* C (**00 C)** *nn* C **(55 C)**	Configures the lower and upper limits for temperature monitoring in degrees C. If the temperature goes outside the specified limits, a fault can be generated

[1] Fields that are filled in automatically if the system auto-detects an installed hard disk drive.

Table A–2 Security Options

Options	Settings	Comments
Supervisor		
Password	6 alphanumeric characters	Specifies a supervisor password.
User		
Password	6 alphanumeric characters	Specifies a user password. The supervisor password must be set before a user password can be set.
Anti-Virus	***Disabled*** *Enabled*	Disables or enables anti-virus protection. Enable this option if you want the BIOS to issue a warning when a program or virus issues a Disk Format command or tries to write to the boot sector of the hard disk drive.

Table A–3 Utility Options

Options	Settings	Comments
Detect IDE		
PIO Mode	Auto 0 to **4**	The programmable input/output (PIO) mode represents the timing cycles between IDE drives and the programmable IDE controller. You should set the PIO mode at the highest value that the system allows. To use PIO mode 4, the IDE cable cannot exceed 15 inches long.
Block Mode	*Off* ***On***	Increases the transfer size from 512 bytes per interrupt to 64 KB.
LBA Mode	*Off* ***On***	Turn this mode ***On*** for any device between 528 MB and 8.4 GB in size.
Language	*English*	

Table A–4 Default Options

Options	Settings	Comments
Original	***No*** *Yes*	Returns the system configuration to the values set at the start of the WINBIOS Setup session.
Optimal	***No*** *Yes*	Returns the system configuration to default settings that maximize system performance.
Fail-Safe	***No*** *Yes*	Returns the system configuration to default settings that maximize system stability.

B

Error Messages and Checkpoint Codes

The BIOS reports errors with blink codes and error messages. A blink code is a series of light blinks on the system's speaker LED. For the location of the speaker LED, see Figure 2–1.

Note

The BIOS for DIGITAL 5/233i-8 CompactPCI systems displays blink codes on the speaker LED instead of sounding beep codes, because the systems do not include a speaker.

This appendix lists the blink codes and error messages with descriptions for quick reference.

B.1 BIOS Blink Codes

The BIOS communicates fatal errors that halt the boot process prior to system monitor initialization by using blink codes. Table B–1 lists error messages.

Table B–1 BIOS Blink Codes

Number of Blinks	Error Message	Explanation	Action
1	Refresh failure	The memory refresh circuitry is faulty.	Reseat the memory SIMMs. If this does not correct the problem, replace the SIMMs.
2	Parity error	A parity error occurred in the first 64 KB block of memory.	Reseat the memory SIMMs. If this does not correct the problem, replace the SIMMs.
3	Base 64 KB memory failure	A memory failure occurred in the first 64 KB block of memory.	Reseat the memory SIMMs. If this does not correct the problem, replace the SIMMs.
4	Timer not operational	A memory failure occurred in the first 64 KB block of memory, or a timer is not functioning.	Replace the SBC.
5	Processor error	The CPU generated an error.	Replace the SBC.
6	8042 – gate A20 failure	The system is unable to switch to protected mode.	Replace the SBC.

Table B–1 BIOS Blink Codes (Continued)

Number of Blinks	Error Message	Explanation	Action
7	Processor exception interrupt error	The CPU generated an exception interrupt.	Replace the SBC.
8	Display memory read/write error	The system video adapter is missing or its memory is faulty. This is not a fatal error.	Replace the SBC.
9	ROM checksum error	The ROM checksum value does not match the value encoded in the BIOS.	Update the BIOS in flash ROM.
10	CMOS shutdown register read/write error	The shutdown register for CMOS RAM failed.	Replace the SBC.
11	Cache memory bad — do not enable cache	The cache memory test failed. Cache memory is disabled. Do not press the [Ctrl], [Alt], [Shift] and [+] key combination to enable the cache memory.	Replace the SBC.

B.2 BIOS Error Messages

Table B–2 lists the error messages that the BIOS displays.

Table B–2 Error Messages

Message	Explanation	Action
8042 gate-A20 error	Gate A20 on the keyboard controller is not working.	Replace the SBC.
Address line short!	An error exists in the address decoding circuitry.	Replace the SBC.
C: drive error	Hard disk drive C: does not respond.	Run the BIOS setup utility and check whether the correct disk type is specified for the drive. If necessary, use diagnostics software, such as the AMIDiag Utility, to find and correct the problem.
C: drive failure	Hard disk drive C: does not respond.	Replace the hard disk drive.
Cache memory bad – do not enable cache	Cache memory is defective.	Replace the SBC.
CH–2 timer error	An error exists in timer 2.	Replace the SBC.
CMOS battery state low	The power of the system battery is low.	Replace the battery.
CMOS checksum failure	The CMOS RAM checksum is different than the previous value.	Run the BIOS setup utility.
CMOS system options not set	The BIOS option values stored in the CMOS RAM are destroyed.	Run the BIOS setup utility and reset the values.

Table B–2 Error Messages (Continued)

Message	Explanation	Action
CMOS display type mismatch	The video type found by the BIOS does not match the type detected by the BIOS.	Run the BIOS setup utility and specify the correct video type.
CMOS memory size mismatch	The amount of memory found by the BIOS is different than the amount specified in CMOS RAM.	Run the BIOS setup utility and specify the correct amount of memory.
CMOS time and date not set	The system time and date are not set.	Run the BIOS setup utility and set the time and date.
D: drive error	Drive D: does not respond.	Run the BIOS setup utility and check whether the correct disk type is specified for the drive. If necessary, use diagnostics software, such as the AMIDiag Utility, to find and correct the problem.
D: drive failure	Drive D: does not respond.	Replace the device.
Diskette boot failure	The diskette in drive A: is not a bootable diskette.	Use another boot diskette and follow the instructions that appear on the monitor screen.
Display switch not set properly	The system's video switch is not set correctly.	Power off the system, set the video switch to color or monochrome, as appropriate, and power the system on.
DMA error	An error exists in the DMA controller.	Replace the SBC.
DMA 1 error	An error exists in the first DMA channel.	Replace the SBC.
DMA 2 error	An error exists in the second DMA channel.	Replace the SBC.
FDD controller failure	The BIOS cannot communicate with the diskette drive controller.	Power off the system, remove the rear access panel, and check the diskette drive cable connections. Replace the rear access panel and power on the system.
HDD controller failure	The BIOS cannot communicate with the hard disk drive controller.	Power off the system, remove the rear access panel, and check the IDE disk drive cable connections. Replace the rear access panel and power on the system.
INTR1 error	Interrupt channel 1 failed the POST.	Replace the SBC.
INTR2 error	Interrupt channel 2 failed the POST.	Replace the SBC.
Invalid boot diskette	The BIOS can read the diskette in the diskette drive, but it cannot boot from the diskette.	Use another boot diskette and follow the instructions that appear on the monitor screen.
Keyboard is locked. You must unlock it.	The system's keyboard lock is engaged.	Unlock the keyboard.

Table B–2 Error Messages (Continued)

Message	Explanation	Action
Keyboard error	The keyboard has a timing problem.	Run the BIOS setup utility and make sure a keyboard controller is installed. To skip the POST routines for the keyboard, set the **System Keyboard** option in **Advanced Setup** to ***Absent***.
KB/Interface error	An error exists in the keyboard connector.	Verify that the keyboard is connected correctly. If it is, replace the SBC.
No ROM Basic	The BIOS cannot find a valid bootable sector on either drive A: or C:.	Insert a valid bootable diskette in drive A:.
Off-board parity error	A parity error occurred in memory installed on an adapter card in an expansion slot. The message format is as follows: OFF BOARD PARITY ERROR ADDR = (*xxxx*) The *xxxx* is the hexadecimal address where the error occurred.	Use diagnostics software, such as the AMIDiag Utility, to find and correct the memory problem.
On-board parity error	A parity error occurred in DRAM memory. The message format is as follows: ON BOARD PARITY ERROR ADDR = (*xxxx*) The *xxxx* is the hexadecimal address where the error occurred.	Check that the SIMMs are installed correctly. If the errror persists, use diagnostics software, such as the AMIDiag Utility, to find and correct the memory problem.
Parity error ????	A parity error exists in memory at an unknown address.	Check that the SIMMs are installed correctly. If the error persists, use diagnostics software, such as the AMIDiag Utility, to find and correct the memory problem.

B.3 EISA BIOS Error Messages

The EISA BIOS can generate additional error messages. None of these messages is fatal. Table B–3 lists the error messages.

Table B–3 EISA BIOS Error Messages

Message	Explanation
EISA CMOS Checksum Failure	The checksum for EISA CMOS is bad. The battery for EISA CMOS RAM can be bad.
EISA CMOS Inoperational	A read/write error occurred in extended CMOS RAM. The battery may be bad.
Expansion Board Not Ready at Slot *X, Y, Z*	The BIOS cannot find the expansion board in Slot *x*, *y*, or *z*. Make sure the board is in the correct slot and is correctly seated.
Fail-Safe Timer NMI Inoperational	Devices that depend on the fail-safe NMI timer is not operating correctly.

Table B–3 EISA BIOS Error Messages (Continued)

Message	Explanation
ID Information Mismatch for Slot *X, Y, Z*	The ID of the EISA Expansion Board in Slot *x, y,* or *z* does not match the ID in EISA CMOS RAM.
Invalid Configuration Information for Slot *X, Y, Z*	The configuration information for EISA expansion board *x, y,* or *z* is not correct. The board cannot be configured. Run the ECU.
Software Port NMI Inoperational	The software port NMI is not working.

B.4 ISA NMI Handler Messages

Table B–4 lists ISA non-maskable interrupt (NMI) handler error messages.

Table B–4 ISA NMI Handler Messages

Message	Explanation
Memory parity error at *xxxxx*	Memory failed. If the memory location can be determined, it is displayed as *xxxxx*. If not, the message indicates a memory parity error.
I/O card parity error at *xxxxx*	An option module failed. If the address can be determined, it is displayed as *xxxxx*. If not, the message indicates an I/O card parity error.
DMA bus timeout	A device has driven the bus signal for more than 7.8 microseconds.

B.5 EISA BIOS NMI Error Messages

The EISA BIOS can generate additional NMI messages that are specific to EISA systems. Table B–5 lists these messages.

Table B–5 EISA BIOS NMI Error Messages

Message	Explanation
BUS Timeout NMI at Slot *n*	A bus timeout NMI occurred at slot *n*.
(E)nable (D)isable Expansion Board	Type E to enable the expansion board that had an NMI or D to disable the board.
Expansion Board Disabled at Slot *n*	The expansion board in slot *n* has been disabled.
Expansion Board NMI at Slot *n*	An expansion board NMI was generated from slot *n*.
Fail-Safe Timer NMI	A file-safe timer NMI has been generated.
Software Port NMI	A software port NMI has been generated.

B.6 POST Checkpoint Codes

When AMIBIOS runs the POST diagnostics, it writes checkpoint codes to I/O port 0080h. If the system does not complete the boot process, you can attach diagnostic equipment to the system to read that I/O port. Sections B.6.1 through B.6.3 list the following types of checkpoint codes:

- Uncompressed initialization checkpoint codes
- Runtime checkpoint codes
- Bus checkpoint codes

B.6.1 Uncompressed Initialization Checkpoint Codes

Table B–6 lists the uncompressed initialization checkpoint codes in the order of execution.

Table B–6 Uncompressed Initialization Checkpoint Codes

Code	Explanation
D0h	The NMI is disabled and power on delay is starting. The initialization code checksum will be verified.
D1h	Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh, and entering 4 GB flat mode.
D3h	Determining the amount of memory that is installed.
D4h	Returning to real mode, executing OEM patches, and setting the stack.
D5h	Passing control to the uncompressed code in shadow RAM at address E000:0000h. The initialization code is copied to segment 0 and control will be transferred to segment 0.
D6h	Control is in segment 0. Checking if the [Ctrl] [Home] key combination was pressed and verifying the system BIOS checksum. If either [Ctrl] [Home] was pressed or the system BIOS checksum is bad, jumping to checkpoint code E0h. Otherwise, continue to checkpoint code D7h.
D7h	Passing control to the interface module.
D8h	Decompressing the main system BIOS runtime code.
D9h	Passing control to the main system BIOS in shadow RAM.

B.6.2 Runtime Checkpoint Codes

Runtime checkpoint codes are uncompressed in shadow RAM at address F0000h. Table B–7 lists the runtime checkpoint codes in order of execution.

Table B–7 Runtime Checkpoint Codes

Code	Explanation
03h	The NMI is disabled. Checking for a soft reset or a power on condition.
05h	The BIOS stack has been built. Disabling cache memory.
06h	Uncompressing the POST code.
07h	Initializing the CPU and the CPU data area.
08h	Calculating the CMOS checksum.
0Bh	Performing any required initialization before the keyboard BAT command is issued.
0Ch	The keyboard controller input buffer is free. Issuing the BAT command to the keyboard controller.

Table B–7 Runtime Checkpoint Codes (Continued)

Code	Explanation
0Eh	The keyboard controller BAT command result is verified. Performing any necessary initialization after the keyboard controller BAT command test.
0Fh	Initialization after the keyboard controller BAT command test is complete. Writing the keyboard command byte.
10h	The keyboard controller command byte is written. Issuing the pin 23 and pin 24 blocking and unblocking commands.
11h	Checking whether the [End] or [Ins] keys were pressed when the system was powered on. Initializing CMOS RAM if the AMIBIOS POST option to initialize CMOS RAM in every boot was set in AMIBCP or the [End] key was pressed.
12h	Disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2.
13h	The video display is disabled. Port B is initialized. Initializing the chipset.
14h	Starting the 8254 timer test.
19h	The 8254 timer test is complete. Starting the memory refresh test.
1Ah	The memory refresh line is toggling. Checking the 15 second on/off time.
23h	Reading the 8024 input port and disabling the MEGAKEY Green PC feature. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24h	The configuration required before interrupt vector initialization is complete. Starting interrupt vector initialization.
25h	Interrupt vector initialization complete. Clearing the password if the POST DIAG switch is on.
27h	Completing initialization required before video mode is set.
28h	Initialization required before the video mode is set and is complete. Configuring the monochrome and color mode settings.
2Ah	Initializing bus initialization system, static, and output devices, if present. See Section B.6.3 for more information.
2Bh	Passing control to the video ROM for any required configuration before the video ROM test.
2Ch	All necessary processing before passing control to the video ROM is complete. Looking for and passing control to the video ROM.
2Dh	The video ROM returned control to the BIOS POST. Performing processing that is required after the video ROM had control.
2Eh	Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test.
2Fh	The EGA/VGA controller was not found. Starting the display memory read/write test.
30h	The display memory read/write test passed. Looking for retrace checking.
31h	The display memory read/write test or retrace checking failed. Performing the alternate display memory read/write test.

Table B–7 Runtime Checkpoint Codes (Continued)

Code	Explanation
32h	The alternate display memory read/write test passed. Looking for alternate display retrace checking.
34h	Video display checking is complete. Setting the display mode.
37h	The display mode is set. Displaying the power-on message.
38h	Initializing the bus input, IPL, and general devices, if present. See Section B.6.3 for more information.
39h	Displaying bus initialization error messages. See Section B.6.3 for more information.
3Ah	The new cursor position is read and saved. Displaying the Hit <DEL> message.
40h	Preparing the descriptor tables.
42h	The descriptor tables are prepared. Entering protected mode for the memory test.
43h	Entered protected mode. Enabling interrupts for diagnostics mode.
44h	Interrupts are enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0.
45h	Data is initialized. Checking for memory wraparound at 0:0 and determining the total amount of memory installed.
46h	The memory wraparound test is complete. The total memory calculation is complete. Writing patterns to test memory.
47h	The memory pattern was written to extended memory. Writing patterns to the base 640 KB of memory.
48h	The memory patterns were written to base memory. Determining the amount of memory below 1 MB.
49h	The amount of memory below 1 MB was found and verified. Determining the amount of memory above 1 MB of memory.
4Bh	The amount of memory above 1 MB was found and verified. Checking for a soft reset and clearing the memory below 1 MB for the soft reset. If this is a power-on situation, going to checkpoint 4Eh.
4Ch	The memory below 1 MB was cleared for a soft reset. Clearing the memory above 1 MB.
4Dh	The memory above 1 MB was cleared for a soft reset. Saving the memory size. Going to checkpoint 52h.
4Eh	The memory test started, but not as the result of a soft reset. Displaying the first 64 KB memory size.
4Fh	The memory size display started. The display is updated during the memory test. Performing the sequential and random memory test.
50h	The memory below 1 MB was tested and initialized. Adjusting the displayed memory size for relocation and shadowing.
51h	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1 MB.

Table B–7 Runtime Checkpoint Codes (Continued)

Code	Explanation
52h	The memory above 1 MB was tested and initialized. Saving the memory size information.
53h	The memory size information and the CPU registers are saved. Entering real mode.
54h	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI.
57h	The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing.
58h	The memory size was adjusted for relocation and shadowing. Clearing the Hit <DEL> message.
59h	The Hit <DEL> message is cleared. The <WAIT...> message is displayed. Starting the DMA and interrupt controller test.
60h	The DMA page register test passed. Performing the DMA controller 1 base register test.
62h	The DMA controller 1 base register test passed. Performing the DMA controller 2 base register test.
65h	The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2.
66h	Completed programming DMA controllers 1 and 2. Initializing the 8259 interrupt controller.
7Fh	Extended NMI source enabling is in progress.
80h	The keyboard test started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command.
81h	A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command.
82h	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer.
83h	The command byte was written and global initialization has completed. Checking for a locked key.
84h	Locked key checking is complete. Checking for a memory size mismatch with the CMOS RAM data.
85h	The memory size check is complete. Displaying a soft error and checking for a password or bypassing WINBIOS Setup.
86h	The password was checked. Performing required programming before WINBIOS Setup runs.
87h	The programming before WINBIOS Setup runs is complete. Uncompressing the WINBIOS Setup code and executing WINBIOS Setup.
88h	Returned from WINBIOS Setup and cleared the screen. Performing required programming after WINBIOS Setup runs.
89h	The programming after WINBIOS Setup ran is complete. Displaying the power-on screen message next.

Table B–7 Runtime Checkpoint Codes (Continued)

Code	Explanation
8Bh	The first screen message was displayed. The <WAIT...> message is displayed. Performing the PS/2 mouse check and an extended BIOS data area allocation check.
8Ch	Programming the WINBIOS Setup options.
8Dh	The WINBIOS Setup options are programmed. Resetting the hard disk drive controller.
8Fh	The hard disk drive controller was reset. Configuring the diskette drive controller.
91h	The diskette drive controller was configured. Configuring the hard disk drive controller.
95h	Initializing the bus option ROMs starting at address C800h. For more information, see Section B.6.3.
96h	Initializing before passing control to the adaptor ROM at address C800h.
97h	Initialization before the C800h adaptor ROM gains control completed. Checking the adaptor ROM.
98h	The adaptor ROM had control and returned control to the BIOS POST. Performing any required processing after the option ROM returned control.
99h	Initialization required after the option ROM test completed. Configuring the timer data area and printer base address.
9Ah	Setting the timer and printer base addresses. Setting the RS–232 base address.
9Bh	Returned after setting the RS–232 base address. Performing any required initialization before the coprocessor test.
9Ch	Required initialization before the coprocessor test is complete. Initializing the coprocessor.
9Dh	Coprocessor initialized. Performing required initialization after the coprocessor test.
9Eh	Initialization after the coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key. Issuing the keyboard ID command.
A2h	Displaying soft errors.
A3h	The soft error display completed. Setting the keyboard typematic rate.
A4h	The keyboard typematic rate is set. Programming the memory wait states.
A5h	Memory wait state programming is complete. Clearing the screen and enabling parity and the NMI.
A7h	NMI and parity are enabled. Performing any initialization required before passing control to the adapter ROM at address E000h.
A8h	Initialization before passing control to the adapter ROM at address E000h is complete. Passing control to the adapter ROM at address E000h.
A9h	Returned from the adapter ROM at address E000h. Performing required initialization after the E000h option ROM has control.
AAh	Initialization after E000h option ROM control completed. Displaying the system configuration.

Table B–7 Runtime Checkpoint Codes (Continued)

Code	Explanation
ABh	Building the multiprocessor table, if necessary
ACh	Uncompressing the Device Initialization Manager (DIM) data and initializing the DIM POST.
B0h	Displaying the system configuration.
B1h	Copying code to specific areas.
00h	Copying code to specific areas is complete. Passing control to the boot loader at INT 19h.

B.6.3 Bus Checkpoint Codes

The system BIOS passes control to different buses at various checkpoints. Table B–8 lists the bus checkpoint codes.

Table B–8 Bus Checkpoint Codes

Code	Explanation
2Ah	Initializing the different bus system, static, and output devices, if present.
38h	Initializing bus input, IPL, and general devices, if present.
39h	Displaying bus initialization messages, if there are any.
95h	Initializing the bus adapter ROMs from addresses C8000h through D8000h.

While the bus routines have control, additional checkpoints are written to I/O port address 0080h. These checkpoints identify the routines that are executed and consist of two parts:

- A low nibble (four bits) that represents the system BIOS checkpoint where control is passed to the different bus routines
- A high nibble (four bits) that indicates a routine is being executed on different buses

Table B–9 lists the possible settings for the additional bus checkpoints.

Table B–9 Additional Bus Checkpoint Codes

Bits	Value	Explanation
<7:4>	0000	Function 0. Disable all devices on the bus.
	0001	Function 1. Initialize static devices on the bus.
	0010	Function 2. Initialize output devices on the bus.
	0011	Function 3. Initialize input devices on the bus.
	0100	Function 4. Initialize IPL devices on the bus.
	0101	Function 5. Initiate general devices on the bus.
	0110	Function 6. Initialize error reporting on the bus.
	0111	Function 7. Initialize add-on ROMs for all buses.
<3:0>	0	Generic Device Initialization Manager (DIM)
	1	Onboard system devices
	2	ISA devices
	3	EISA devices
	4	ISA plug and play devices
	5	PCI devices

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