

Olympus III User's Guide

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Revision History

10/31/03	Initial release.
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AMI provides technical support for AMI products purchased directly from AMI or from an AMI-authorized reseller only.

If	Then	
You purchased this product from AMI or	Call AMI technical support at 770-246-	
from a certified AMI reseller,	8645. Please be prepared to specify the	
	serial number of the product.	
This AMI product was installed as part	Call the technical support department of	
of a system manufactured by a company	the computer manufacturer or the	
other than AMI or you purchased an	unauthorized reseller. AMI does not	
AMI product from an unauthorized	provide direct technical support in this	
reseller,	case.	

If your American Megatrends Olympus III motherboard fails to operate as described or you are in doubt about a configuration option, please call technical support at 770-246-8645.

Web Site

We invite you to access the American Megatrends World Wide Web site at:

http://www.ami.com/

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Retail Packing List

You should have received the following:

- an Olympus III motherboard
- a floppy drive cable
- two ATA-100/133 cables
- two Serial ATA cables
- an I/O shield
- a warranty card
- this Olympus III User's Guide (located on the Olympus III CD)
- an Olympus III Quick Installation Guide
- an Olympus III CD

Note:

Your Olympus III (series 875) motherboard may or may not ship with everything listed in the *Retail Packing List*. Contact your AMI authorized reseller to find out what is shipped with your motherboard.

Optional Components

The following component does not come (mounted) with your Olympus III motherboard. You must order these components separately.

Hitachi® BMC chip

Note:

The Hitachi® BMC chip is not mounted on your motherboard. This BMC chip is not described in this manual. This is used strictly for OEM custom configurations. Contact your American Megatrends OEM sales representative for custom OEM design services.

FCC Class A (USA)

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Shielded cables must be used with this unit to ensure compliance with the Class A FCC limits.

Chapter 1 Hardware Specifications and Supported Features

Overview

The AMI Olympus III motherboard utilizes the Intel 875P chipset. It offers support for the latest Intel processors, including 800FSB, 8x AGP, Performance Acceleration Technology (PAT), Hyper Threading technology, Dual-Channel DDR 400/333 SDRAM memory with ECC Support, dual Parallel ATA, dual Serial ATA-150 RAID, Gigabit LAN, and USB 2.0.

One of the biggest features of the Olympus III motherboard is its integration of the onboard Gigabit Ethernet controller. The Gigabit Ethernet controller connects directly to the Intel 875P chipset via a dedicated Communication Streaming Architecture (CSA) bus. In the Olympus II motherboard, the onboard Ethernet controller connected to the south bridge chipset via the PCI bus. The CSA bus is 64 bits wide, while the PCI bus is only 32 bits wide. Theoretically, the CSA bus has twice the bandwidth of a PCI bus. This overcomes the bandwidth limitation found when running off of the PCI bus.

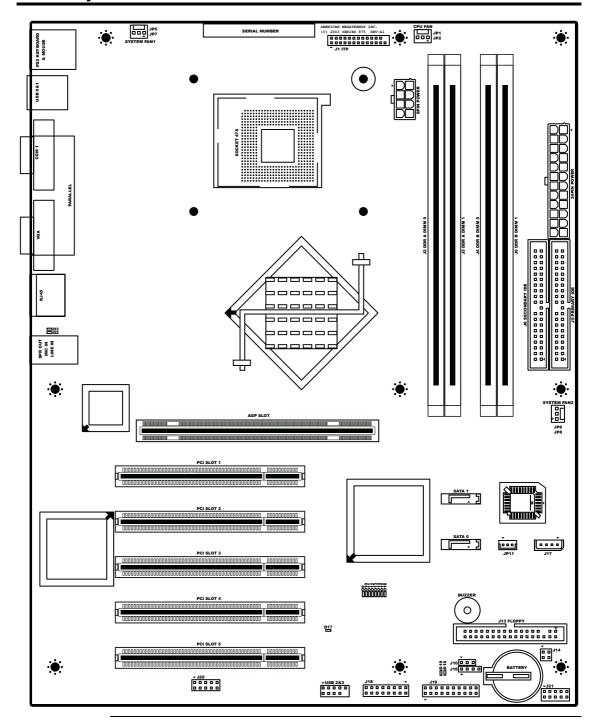
With all these features the Olympus III motherboard is the perfect fit for server appliances such as, Network Attached Storage (NAS) and Mail/Web servers.

Specifications

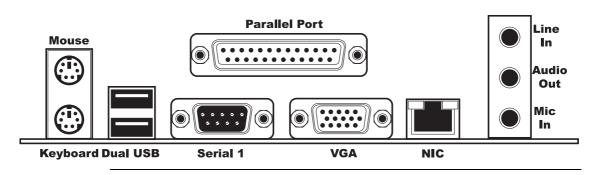
Item	Description	
CPU	Single Pentium 4 and PGA 478 Socket	
	• 533/800 MHz FSB	
	Hyper Threading supported	
i875P	GMCH, Memory Controller Hub, AGP8X Interface	
(Canterwood)	ICH5, I/O Controller Hub	
Intel Chipset	FWH, Firmware Hub Flash Interface	
Memory	Four DIMM Sockets	
	4 GB Max Memory Support	
	Support for Dual Channel DDR333/400 SDRAM with ECC support	
	Maximum Memory Throughout is ~3.2GB/s per channel	
Slots • Five 32-Bit 33 MHz PCI Slots		
	One AGP 8X Slot	
On-Board Video	ATI Rage XL	
On-Board LAN	Gigabit Fast Ethernet Controller: Intel 82547	
	Supports ACPI 1.0b/2.0 Based Power Management	
	Supports Wake on Magic Packet	
	WFM 2.0 Compliant	
	PCI 2.2 Compliant	
	One RJ45 Port for External Connection	

Specifications, Continued

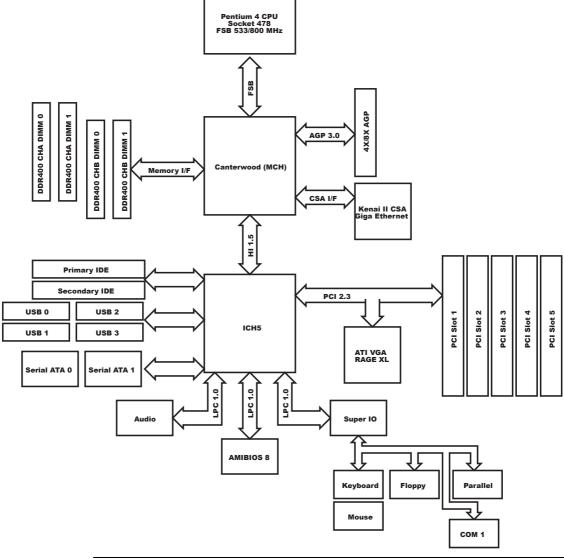
Item	Description					
USB 2.0	Two Ports					
Serial/	Dual Serial ATA Connectors					
Parallel ATA	Dual Parallel IDE Connectors ATA 100/133					
Standard I/O	Port Angeles, Integrated Super I/O with Manageability Functions					
	PS/2 Mouse					
	Floppy, Parallel/Serial HDR					
IPMI BMC	Hardware Monitor: Hitachi H8-2168 BMC (Baseboard Management Controller)					
	IPMI v1.5 Compliant					
	AMI MegaRAC-PM Firmware					
Server	General Purpose Non Volatile (GPNV) Storage					
Management	• Located in the FWH, used to store:					
	BIOS POST Code					
	System Boot Log					
	CPU Temperature, FAN, ECC History					
	Chassis Fan, Temperature History					
	Event Log					
Server	Hardware Monitor: HECETE4					
Management • I2C Master Embedded in the Super I/O						
Hardware	SMBus Controller Embedded in the ICH5					
	System Monitors for the Following Devices:					
	One Chassis Fan, Chassis Door Open Detection, 1 CPU Fan					
	One Ambient Temperature Sensor ONLY CONTROL OF THE MANY AND THE					
	CPU Core Voltages are Individually Monitored					
	Voltage-Safe Operating Ranges Automatically Established for Different CPUs					
13.07.0	Slot Voltages and Chipset Voltages					
AMI Server	System I2C Information Displayed in BIOS Setup Screen					
BIOS	SMBIOS 2.3 Complaint The Court of the					
	Event Logging for System Errors (POST and Runtime) Post Grant Street Control of the Contro					
В В	DMI Compliant, ACPI Compliant					
Form Factor	Standard ATX					
Environmental	Storage Temperature: -20 degrees to 80 Degrees C					
Specifications	Relative Humidity: 5 to 80% Non-Condensing @40 Degrees					
	Operating Temperature: 0 to 55 Degrees C					
	Vibration: 2.5G Acceleration Over 2000 Hz Sine Wave, 2oct/Mian Sine Sweep					
DIOG	Shock: 20G; 11 Msec Duration, Half-Sine Shock Sweep					
BIOS	• AMIBIOS8 TM					



Rear I/O Ports



The block diagram for the Olympus III is shown below:



Supported Processors

The Olympus III motherboard supports the following 478-pin Intel® Pentium® 4 processors:

Processor	Speed	FSB	Cache Size
Intel® Pentium® 4	3.20 GHz	800 MHz	512 KB
processor	3.00 GHz	800 MHz	512 KB
	3.06 GHz	533 MHz	512 KB
	2.80C GHz	800 MHz	512 KB
	2.80 GHz	533 MHz	512 KB
	2.66 GHz	533 MHz	512 KB
	2.60C GHz	800 MHz	512 KB
	2.53 GHz	533 MHz	512 KB
	2.40C GHz	800 MHz	512 KB
	2.40B GHz	533 MHz	512 KB
	2.26 GHz	533 MHz	512 KB

Supported System Memory

The AMI Olympus III motherboard has four DIMM sockets and supports the following memory features:

- 2.5 V 184-pin DDR SDRAM DIMMs
- Unbuffered, single-sided or double-sided DIMMs
- Double-sided DIMMs with 16 chips are not supported
- A maximum of 4 GB of total system memory
- A minimum of 64 MB of total system memory
- ECC and non-ECC DIMMs supported
- Serial Presence Detect (SPD)
- DDR400 and DDR333 SDRAM DIMMs

The following table lists the supported FSB and memory speed combinations.

To use:	the FSB must be:	
DDR400	800 MHz	
DDR333	800 MHz or 533 MHz	

Note:

It is advisable to populate the Olympus III motherboard with DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the AMIBIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the AMIBIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted or the DIMMs may not function under the determined frequency.

Supported System Memory, Continued

The following table is a list of SDRAM types that are supported per bank:

DIMM Capacity	Configuration	DDR SDRAM Density	DDR SDRAM Organization Front-side	DDR SDRAM Organization Back-side	Number of DDR SDRAM Devices
64 MB	Single-Sided	64 Mbit	8 M x 8	empty	8
64 MB	Single-Sided	128 Mbit	8 M x 16	empty	4
128 MB	Double-Sided	64 Mbit	8 M x 8	8 M x 8	16
128 MB	Single-Sided	128 Mbit	16 M x 8	empty	8
128 MB	Single-Sided	256 Mbit	16 M x 16	empty	4
256 MB	Double-Sided	128 Mbit	16 M x 8	16 M x 8	16
256 MB	Single-Sided	256 Mbit	32 M x 8	empty	8
256 MB	Single-Sided	512 Mbit	32 M x 16	empty	4
512 MB	Double-Sided	256 Mbit	32 M x 8	32 M x 8	16
512 MB	Single-Sided	512 Mbit	64 M x 8	empty	8
1024 MB	Double-Sided	512 Mbit	64 M x 8	64 M x 8	16

More Features

Faster, 128-bit dual channel DDR 400 memory support

- DDR 400 memory alone in single channel supports a maximum theoretical bandwidth of 3.2 GB/s; while a dual channel supports 6.4 GB/s, the same bandwidth speed that the 800 MHz FSB P4 can generate
- DDR 400 is implemented with Intel's PAT for incredible performance from the memory interface and provides exceptional performance across a full range of multimedia and 3-D intensive applications
- Flexible memory technology allows a full spectrum of DDR usage from highest performance to more cost-effective systems. ECC ensure data reliability and integrity.

800 MHz FSB CPU support (200 MHz quad-pumped)

- The key factor in enhancing system performance
- All of the 875P's predecessors and current competitors max out at 533 MHz, which should give them a peak bandwidth of 4.2GB/s. The 875P's peak theoretical bus bandwidth is 6.4GB/s.
- Supports platform longevity for the fastest Intel Pentium 4 processor frequencies and delivers greater system bandwidth.

Serial ATA (SATA) support

- A faster and relatively new way to connect the hard drive to the rest of the computer
- Up to now, if you wanted SATA you needed to have a Promise, Highpoint or Silicon Image SATA controller chip. Intel is the first of the chipset manufacturers to have a SATA controller built into its South Bridge
- The SATA specification lists the maximum transfer rate as 15 0MB/s, which is 13 percent more bandwidth than a 32-bit/33 MHz PCI bus can provide!
- Intel brings the SATA controller onto the ICH and bypasses the PCI bus. The SATA controller has a direct link to the Hub Link 2.0 interface in ICH5 and can offer a full 150 MB/s per channel.

ICH

- The Intel I/O Controller Hub version 5 is the newest controller chip designed to work with the I875P and I865 chipsets. There are two major features of ICH5 that separate it from its predecessor, ICH4; the first feature is integrated support for a total of eight USB 2.0 ports.
- ICH5 features two SATA channels (supporting a maximum of two drives) and two Parallel ATA channels (supporting a maximum of four drives), all of which may be enabled and used concurrently.
- Intel also gives another reason to say goodbye to third party SATA controllers with the inclusion of RAID function in the ICH5R version. This allows you to use RAID 0 or 1 on the Serial ATA drives connected to the ICH5R.

AGP 8X

- High-performance AGP 8X graphics interface for an advanced graphics experience
- Offers 2.1 GB/s of dedicated bandwidth
- Highest bandwidth graphics interface enables upgradability to the latest graphics cards.

Integrated hi-speed USB 2.0

• Eight ports offer up to 40x greater bandwidth over USB 1.1 for a variety of today's demanding high-speed I/O peripherals.

Enhanced AC '97 Audio

- Enhanced AC '97 audio implementation with dual independent DMA audio engines
- Delivers improved sound quality and new audio usage models and enables a user to make a PC phone call while playing digital music streams
- Supports Dolby* Digital 5.1 surround sound(1), delivering six channels of enhanced sound quality.

More Features, Continued

Error Correction Code

Error Correction Code is supported for users that demand memory data reliability and integrity

Hyper-Threading Technology

- Optimized to support the Pentium® 4 Processor with Hyper-Threading Technology, the 875P chipset adds intelligence to help manage and prioritize multiple threads received from the microprocessor.
- Delivers increased system responsiveness and performance.

478-pin Processor Package Compatibility

• Supports the highest performance Intel Pentium 4 processors plus, the flexibility to support other 478-pin Intel processors.

Intel Performance Acceleration Technology (PAT)

- Increases memory and system-level performance by optimizing internal data paths.
- PAT speeds data flow between the processor and system memory to increase performance. The 875P chipset also offers a dedicated networking bus based on Intel's new Communications Streaming Architecture

Full-duplex Gigabit Ethernet

• Dedicated 266 MB/s link to a full-duplex Gigabit Ethernet connection

Communications Streaming Architecture (CSA)

- CSA, in conjunction with the new Intel® PRO/1000 CT Desktop Connection gigabit Ethernet controller, doubles the networking bandwidth possible with today's PCI bus based solutions.
- Gigabit Ethernet is slowly becoming the new standard for Ethernet. Most
 motherboard companies are now integrating Gb/E controllers onto their
 motherboards, which allows 1000 megabit along standard Cat5E Ethernet cable
 -- s a great increase in bandwidth.

Low-Power Sleep Mode

Saves Energy

Chapter 2 Hardware Installation

Overview

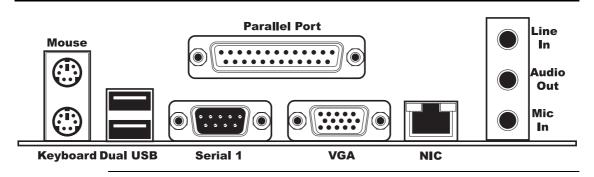
This chapter covers the basic hardware installation of the Olympus III motherboard.

Motherboard Installation

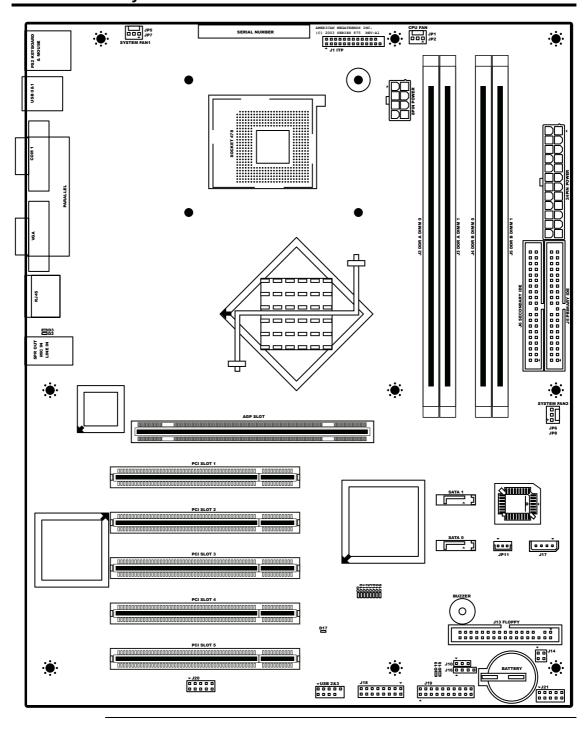
Use the following steps to install the motherboard, memory, CPU, and connectors.

Step	Action
1	Unpack the Motherboard (and check jumper settings)
2	Install Memory
3	Install CPU and Connect CPU Heatsink and Fan
4	Install the Motherboard (and I/O shield)
5	Attach Internal Cables
6	Installing Expansion Boards
7	Connect External Cables
8	Install Drivers
9	Test and Configure

Rear I/O Ports



Motherboard Layout



Step 1 Unpack the Motherboard

Step	Action	
1	Inspect the cardboard carton for obvious damage. If damaged, call 770-246-8600. Leave the motherboard in its original packing.	
2	Perform all unpacking and installation procedures on a ground-connected anti-static mat. Wear an anti-static wristband grounded at the same point as the anti-static mat. Or use a sheet of conductive aluminum foil grounded through a 1-megohm resistor instead of the anti-static mat. Similarly, a strip of conductive aluminum foil wrapped around the wrist and grounded through a 1 megaohm resistor serves the same purpose as the wristband.	
3	Inside the carton, the motherboard is packed in an anti-static bag, and sandwiched between sheets of packaging sponge. Remove the sponge and the anti-static bag. Place the motherboard on a grounded anti-static surface component side up. Save the original packing material.	
4	Inspect the motherboard for damage. Do not apply power to the motherboard if it has been damaged.	
5	If the motherboard is undamaged, it is ready to be installed.	

Avoid Electro-Static Discharge (ESD)



Electro-Static Discharge (ESD) will damage the motherboard and other system components. Keep the motherboard in the anti-static bag until it is to be installed. Wear an anti-static wrist-grounding strap before handling the motherboard. Make sure you stand on an anti-static mat when handling the motherboard.

Avoid contact with any component or connector on any adapter card, printed circuit board, or memory module. Handle these components by the mounting bracket.

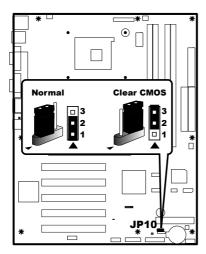
Set Jumpers

Set all jumpers and install the CPU before placing the motherboard in the chassis.

JP10 Clear CMOS

JP10 is a 3-pin berg that can be used to erase the contents of CMOS RAM, where all system configuration information is stored.

Before you change JP10 from the default setting (1-2), turn off the power supply using the mechanical switch (not the soft-off power button.) This switch is normally located on the power supply. If there is no switch, remove the AC cord going to the power supplies.



To drain CMOS RAM power, perform the following steps:

Step	Action	
1	Turn off power to the computer.	
2	Remove the computer cover.	
3	Remove the jumper from pins 1-2 of JP10.	
4	Place a shorting bridge on pins 2-3 of JP10.	
5	Wait for five seconds.	
6	Remove the shorting bridge from pins 2-3 of JP10.	
7	Put the shorting bridge back on pins 1-2 of JP10.	
8	Turn on computer power again.	
	Since you drained power from CMOS RAM, all system configuration information	
	has been erased. You must now re-enter the system configuration information by running AMIBIOS Setup.	

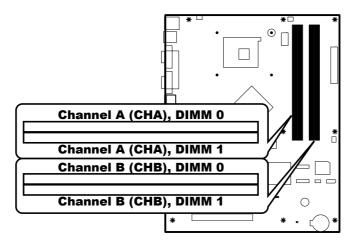
You must then reboot the computer, run AMIBIOS Setup, and restore all system configuration information. The JP10 settings are:

CMOS Drain	Jumper Setting
Normal operation (factory setting).	1-2
The contents of CMOS RAM are destroyed.	2-3

Memory Overview

The AMI Olympus III motherboard has four DIMM sockets and supports the following memory features:

- DIMM modules can be plugged into any slot (or combination of slots)
- 2.5 V 184-pin DDR SDRAM DIMMs
- Unbuffered, single-sided or double-sided DIMMs
- Double-sided DIMMs with 16 chips are not supported
- A maximum of 4 GB of total system memory
- A minimum of 64 MB of total system memory
- ECC and non-ECC DIMMs supported
- Serial Presence Detect (SPD)
- DDR400 and DDR333 SDRAM DIMMs



The following table lists the supported FSB and memory speed combinations.

To use:	the FSB must be:
DDR400	800 MHz
DDR333	800 MHz or 533 MHz

Note:

It is advisable to populate the Olympus III motherboard with DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the AMIBIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the AMIBIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted or the DIMMs may not function under the determined frequency.

Supported Memory

The following table is a list of SDRAM types that are supported per bank:

DIMM Capacity	Configuration	DDR SDRAM Density	DDR SDRAM Organization Front-side	DDR SDRAM Organization Back-side	Number of DDR SDRAM Devices
64 MB	Single-Sided	64 Mbit	8 M x 8	empty	8
64 MB	Single-Sided	128 Mbit	8 M x 16	empty	4
128 MB	Double-Sided	64 Mbit	8 M x 8	8 M x 8	16
128 MB	Single-Sided	128 Mbit	16 M x 8	empty	8
128 MB	Single-Sided	256 Mbit	16 M x 16	empty	4
256 MB	Double-Sided	128 Mbit	16 M x 8	16 M x 8	16
256 MB	Single-Sided	256 Mbit	32 M x 8	empty	8
256 MB	Single-Sided	512 Mbit	32 M x 16	empty	4
512 MB	Double-Sided	256 Mbit	32 M x 8	32 M x 8	16
512 MB	Single-Sided	512 Mbit	64 M x 8	empty	8
1024 MB	Double-Sided	512 Mbit	64 M x 8	64 M x 8	16

Memory Configuration

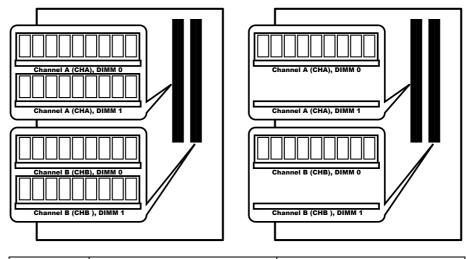
The Olympus III motherboard has the following features for enhancing memory throughput:

- Dual Channel memory interface. The Olympus III motherboard has two memory channels (CHA and CHB), each with two DIMM sockets.
- Dynamic Addressing Mode. Dynamic mode minimizes overhead by reducing memory accesses.

Characteristics of Dual and Single Channel Configuration with and without Dynamic Mode:

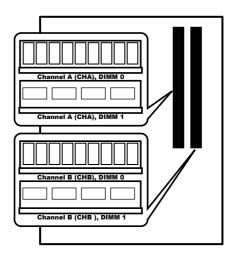
Throughput Level	Configuration	Characteristics
Highest	Dual Channel with Dynamic Mode	All DIMMs matched
Higher	Dual Channel without Dynamic Mode	DIMMs matched from Channel A to Channel B DIMMs not matched within channels
Lower	Single Channel with Dynamic Mode	Single DIMM or DIMMs matched within a channel
Lowest	Single Channel without Dynamic Mode	DIMMs not matched

Highest Throughput Level (RECOMMENDED)



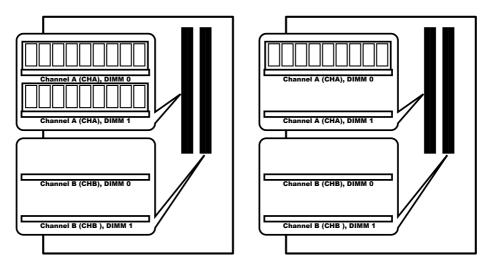
Throughput	Configuration	Characteristics
Level		
Highest	Dual Channel with Dynamic Mode	All DIMMs matched

Second Highest Throughput Level



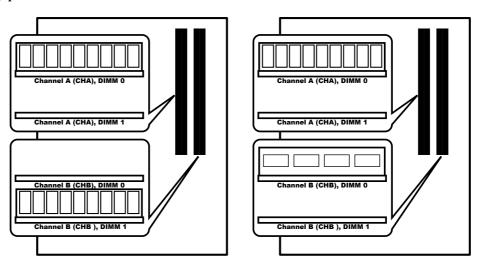
Throughput Level	Configuration	Characteristics
Higher	Dual Channel without Dynamic Mode	 DIMMs matched from Channel A to Channel B DIMMs not matched within channels

Second Lowest Throughput Level



Throughput Level	Configuration	Characteristics
Lower	Single Channel with Dynamic Mode	Single DIMM or DIMMs matched within a channel

Lowest Throughput Level

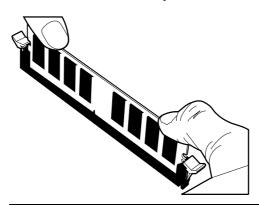


Throughput Level	Configuration	Characteristics
Lowest	Single Channel without Dynamic Mode	DIMMs not matched

Inserting DIMM Modules

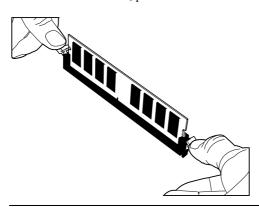
Locate the DIMM slot(s) you will be using. See the *Memory Configuration* section located on the previous pages.

Match the DIMM module and DIMM slot so that the notches align properly. Insert the module by sliding it straight down into the slot. Using your thumbs, press down on the module until the tabs lock in place.



Removing DIMM Modules

To remove the module, press down on the tabs. This will eject the module.

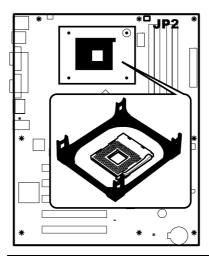


Memory Display

System memory is reported by AMIBIOS as it boots and again when the AMIBIOS System Configuration Screen is displayed just before the operating system boots. The memory displayed by AMIBIOS on the System Configuration Screen is 384 KB less than the total memory installed.

Step 3 Install CPU and Connect Heatsink and Fan

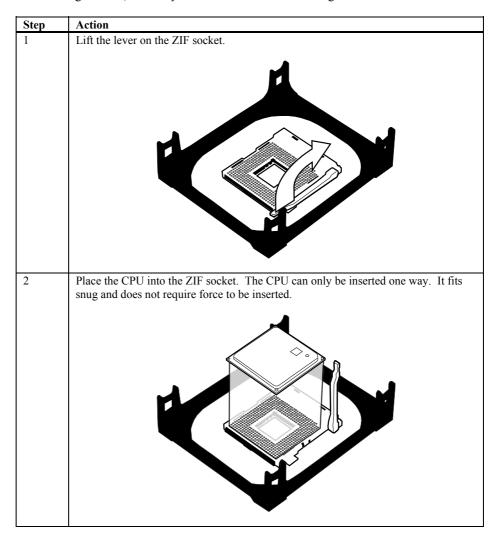
The Olympus III motherboard is equipped with a Socket 478 ZIF (zero insertion force) socket. The CPU socket is located in the shaded are diagramed below along with its CPU cooling fan connector location (JP2 CPU Fan header).



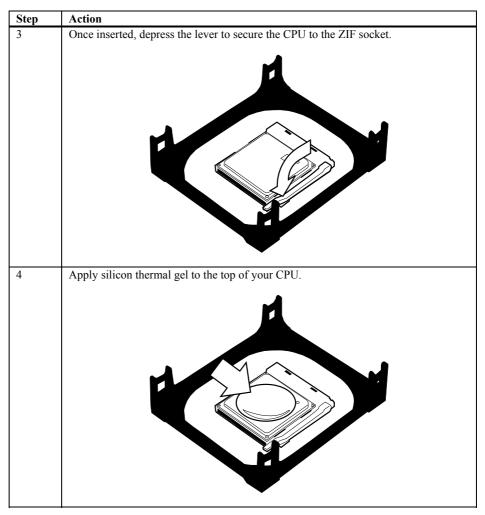
Step 3 Install CPU and Connect Heatsink and Fan, Continued

Note:

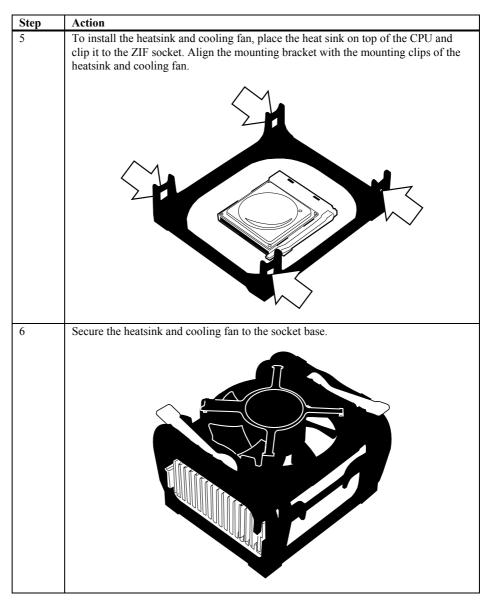
The CPU heatsink/cooling fan installation described in this section is based on the common retail packaged Intel® processor with heatsink/fan combination. For custom OEM configurations, consult your CPU heatsink and cooling fan documentation.



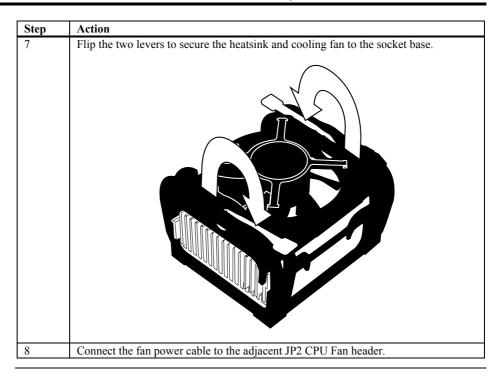
Step 3 Install CPU and Connect Heatsink and Fan, Continued



Step 3 Install CPU and Connect Heatsink and Fan, Continued

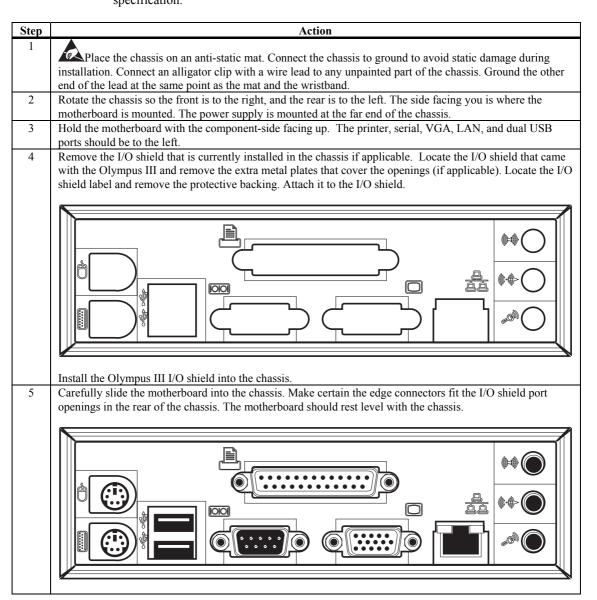


Step 3 Install CPU and Connect Heatsink and Fan, Continued

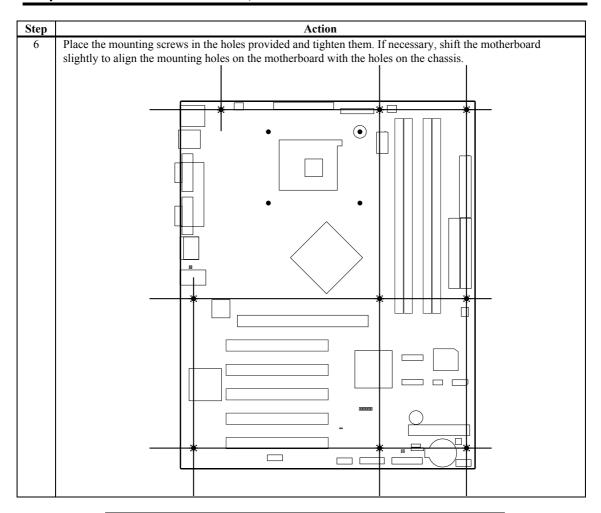


Step 4 Install the Motherboard

Note: We encourage integrators to choose a chassis that complies with the ATX 2.01 (or later) specification.



Step 4 Install the Motherboard, Continued



⚠Warning

If using metallic screws, make sure you use them only in the plated mounting holes.

If using metallic screws, make sure the head of the screw fits completely inside the plated mounting holes.

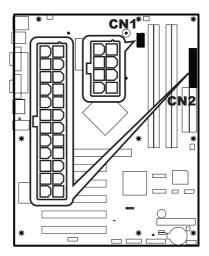
Step 5 Attach Internal Cables

Connectors

The Olympus III motherboard includes many connectors. Connection instructions, illustrations of connectors, and pin-out locations are supplied in the following pages. A list of all connectors described in this manual are as follows:

Location	Connector	Turn to page
CN1	8-pin ATX12V/SSI EPS12V Power Connector	28
CN2	24-pin Main Power Connector	28
CN4	Serial ATA 0 Connector	42
CN5	Serial ATA 1 Connector	42
JP2	CPU Cooling Fan Connector	48
JP5	Auxiliary Cooling Fan Connector	49
JP6	Auxiliary Cooling Fan Connector	49
JP10	Clear CMOS Jumper	14
JP11	Wake On LAN Connector	31
J1	ITP Connector	32
J6	Secondary IDE Connector	40
J7	Primary IDE Connector	40
J13	Floppy Drive Connector	39
J14	OEM BIOS Function Connector	33
J16	External Hard Disk Activity LED Connector	34
J17	IPMB Connector	35
J18	BMC Debug Connector	36
J19	Front Panel Connector	44
J20	External Serial Port Connector	37
J21	BMC Diagnostics & Recover Connector	38

CN1 and CN2 ATX Power Supply Connectors



Attach the power cables from the power supply to the connectors located at CN1 and CN2. The socket is keyed so that the ATX power supply connector can only mount one way.

Note:

Do not use a standard ATX power supply. The Olympus III motherboard will not boot with a standard ATX power supply. Use only ATX12V-compliant or Server System Infrastructure (SSI) Entry-Level Power Supply (EPS) EPS12V power supplies with the Olympus III motherboard. ATX12V and EPS12V power supplies have an additional power lead that provides required supplemental power for the Intel Pentium 4 processor. The Olympus III motherboard will not boot if the ATX12V power supply is not connected to both the CN1 4-pin (or 8-pin) and CN2 20-pin (or 24-pin) power connectors.

For more information on ATX12V power supplies, see the formfactor.org website. For more information on SSI EPS12V power supplies, see the ssiforum.org website.

The main power connector pinout is:

Pin	Signal Name	Pin	Signal Name
1	3.3 V	13	3.3 V
2	3.3 V	14	-12 V
3	Ground	15	Ground
4	+5 V	16	Power Supply On
5	Ground	17	Ground
6	+5 V	18	Ground
7	Ground	19	Ground
8	Power OK	20	-5 V
9	5 VSB	21	+5 V
10	+12 V	22	+5 V
11	+12 V	23	+5 V
12	+3.3 V	24	GND

CN1 and CN2 ATX Power Supply Connectors, Continued

The ATX12V/SSI EPS12V power connector pinout is:

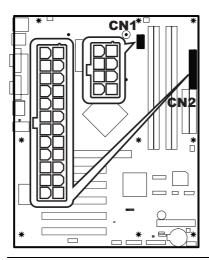
Pin	Signal Name	Pin	Signal Name
1	Ground	5	+12 V
2	Ground	6	+12 V
3	Ground	7	+12 V
4	Ground	8	+12 V

The power supply should match the physical configuration of the chassis. Make sure the power switch is *Off* before assembly.

Before attaching all components, make sure the proper voltage has been selected. Power supplies often can run on a wide range of voltages and must be set (usually via a switch) to the proper range. Use at least a 300-watt ATX power supply, which should have builtin filters to suppress radiated emissions. Power supply voltage depends upon system load. For example, +12V rating should be matched to the amount of the external load.

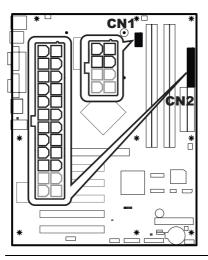
Attach the cables from the power supply to the power connector(s) on the motherboard. ATX-compatible power supplies can have either one or two 20-pin (or 24-pin) connectors. You can use either one or both power connectors.

For 24-pin /8-pin SSI EPS12V power supplies, plug the connectors into CN1 and CN2 as illustrated in the following diagram:

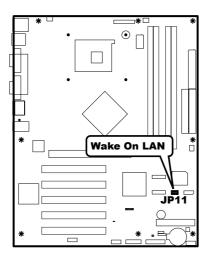


CN1 and CN2 ATX Power Supply Connectors, Continued

For 20-pin /4-pin ATX12V power supplies, plug the connectors into pin one first as illustrated in the following diagram:



JP11 Wake On LAN connector

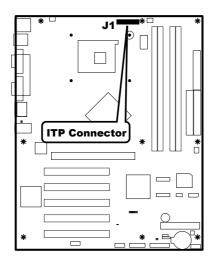


This connector is used to connect to a network adapter card that supports Wake-On-LAN (WOL). WOL is the industry standard term used to describe the technology used to remotely wake a computer system. A network adapter card that supports WOL has a very-low-power mode to monitor the network for a special data packet that can wake up the machine from *standby mode* (commonly known as S3) or *hibernate mode* (commonly known as S4).

Connect your WOL cable from your network adapter card to this connector *only if you* want to remotely wake up your computer system using a WOL compliant network adapter.

Pin	Signal Name
1	+3.3 V stand by
2	Ground
3	Wake on LAN signal

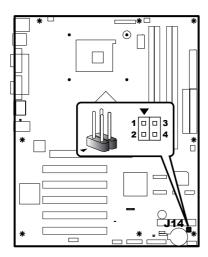
J1 ITP Connector



This is an In-Target Probe (ITP) connector. The physical connector may or may not be mounted on your particular motherboard. This connector is not described in this manual. This connector is used strictly for debugging OEM custom configurations. Contact your American Megatrends OEM sales representative for custom OEM design services.

Pin	Signal Name	Pin	Signal Name
1	Ground	2	Ground
3	H_BPM2-L	4	Not connected
5	H_BPM3-L	6	H_RST_DBR-L
7	H_BPM2-L	8	Ground
9	H_BPM3-L	10	H_TDI
11	H_BPM4-L	12	H_TMS
13	H_BPM5-L	14	H_TRST-L
15	H_CPURST-L	16	H_TCK
17	H_TCK_FB	18	Not connected
19	ITP_100M_T	20	Ground
21	ITP_100M_C	22	Pull up VCCP 1.5K
23	H_BPM5-L	24	H_TDO
25	Ground	26	Not connected

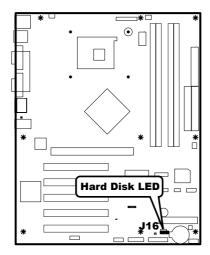
J14 OEM BIOS Function



This is a custom four-pin BIOS driven connector. The physical connector may or may not be mounted on your particular motherboard. This connector is not described in this manual. This connector is used strictly for OEM custom configurations. Contact your American Megatrends OEM sales representative for custom OEM design services.

Pin	Signal Name
1	Must be defined by the OEM. This is a custom OEM design feature.
2	Must be defined by the OEM. This is a custom OEM design feature.
3	Ground
4	Ground

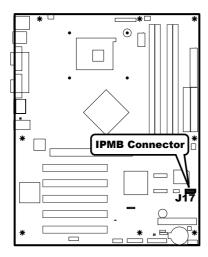
J16 External Hard Disk Activity LED Connector



J16 External Hard Disk Activity LED connector is a 2 x 4-pin connector that allows an expansion card hard disk drive controller to use the same LED as the onboard IDE controller. For proper operation, this connector should be wired to the LED output of the expansion card hard disk drive controller. The LED indicates when data is being read from, or written to, either the expansion card hard disk drive controller or the onboard IDE controller (Parallel ATA or Serial ATA).

Pin	Signal Name
1	Hard Disk Activity
2	NC
3	NC
4	Hard Disk Activity
	•

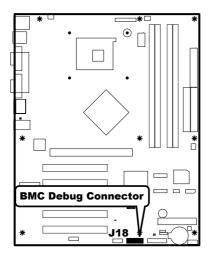
J17 IPMB Connector



This connector can be used to externally monitor FRUs (Field Replaceable Units, such as cooling fans, power supplies, and so on) on the Olympus III motherboard through a management card, such as the MegaRAC remote management card. Attach the IPMB connector from the MegaRAC card into J17 (if applicable).

Pin	Signal Name
1	IPMB_SDA3
2	GND
3	IPMB_SCL3
4	NC

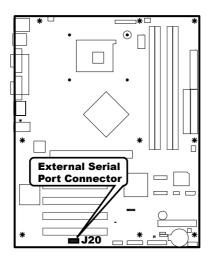
J18 BMC Debug Connector



This is the BMC Debug connector used to debug the Hitachi® BMC chip. The physical connector and Hitachi® BMC chip may or may not be mounted on your particular motherboard. This connector and BMC chip is not described in this manual. This connector is used strictly for debugging OEM custom configurations. Contact your American Megatrends OEM sales representative for custom OEM design services.

Pin	Signal Name	Pin	Signal Name
1	ETCK	2	GND
3	ETRST#	4	GND
5	ETDO	6	GND
7	RST_BMC	8	+3.3 V Stand by
9	ETMS	10	GND
11	ETDI	12	GND
13	Connected to Pin 7	14	GND
15	NC	16	NC

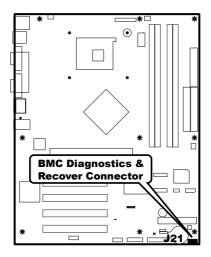
J20 External Serial Port Connector



Attach the external nine-pin serial cable with a D-type connector to jumper J20.

Pin	Signal Name	Pin	Signal Name
1	DSRB	2	DCDB
3	RTSB	4	RXDB
5	CTSB	6	TXDB
7	RIB	8	DTRB
9	NC	10	GND(Connect L28,C479)

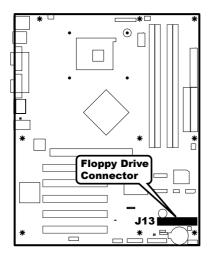
J21 BMC Diagnostics and Recover Connector



This connector is used in conjunction with the Hitachi® BMC chip. The physical connector and Hitachi® BMC chip may or may not be mounted on your particular motherboard. This connector and BMC chip is not described in this manual. This connector is used strictly for OEM custom configurations. Contact your American Megatrends OEM sales representative for custom OEM design services.

Pin	Signal Name	Pin	Signal Name
1	MD0	2	GND
3	MD1	4	GND
5	MD2	6	GND
7	BMC Diag	8	GND
9	BMC Recovery	10	GND

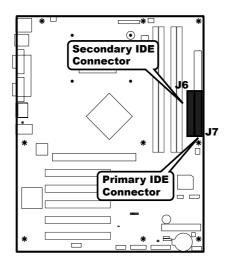
J13 Floppy Drive Connector



Attach your floppy disk drive to this connector.

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	FDINDX# (Index)
9	Ground	10	FDM00# (Motor Enabled A)
11	Ground	12	No Connect
13	Ground	14	FDDS0# (Drive Select A)
15	Ground	16	No Connect
17	No Connect	18	FDDIR# (Stepper Motor Direction)
19	Ground	20	FDSTEP# (Step Pulse)
21	Ground	22	FDWD# (Write Data)
23	Ground	24	FDWE# (Write Enable)
25	Ground	26	FDTRK0# (Track 0)
27	No Connect	28	FDWPD# (Write Protect)
29	Ground	30	FDRDATA# (Read Data)
31	Ground	32	FDHEAD# (Side 1 Select)
33	Ground	34	DSKCHG# (Diskette Change)

J6 and J7 IDE Connectors



Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key
21	DDRQ0	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	P ALE (Cable Select Pull-up)
29	DDACK0#	30	Ground
31	IRQ 14	32	Reserved
33	DAG1 (Address 1)	34	ATA 6 Detect
35	DAG0	36	DAG2
	(Address 0)		(Address 2)
37	Chip Select 1P#	38	Chip Select 3P#
39	Activity#	40	Ground

J7 is the primary IDE (Integrated Drive Electronics) hard disk drive connector. Both the primary master and the primary slave IDE drives must be connected by cable to J7.

J6 is the secondary IDE hard disk connector.

J7 is a 40-pin dual-inline berg that connects an IDE drive to the primary onboard IDE connector. This motherboard supports the following:

	Data Transfer Rate (max.)	Cable	Conductors	CRC
DMA M 1 1		40 . IDE	40 .	
DMA Mode 1	11.1 MBs	40-pin IDE	40-pin	no
Multi-word DMA	13.3 MBs	40-pin IDE	40-pin	no
Mode 1				
Multi-word DMA	16.6 MBs	40-pin IDE	40-pin	no
Mode 2				
Ultra ATA Mode 2	33.3 MBs	40-pin IDE	40-pin	yes
ATA-33				·
Ultra ATA Mode 4	66.6 MBs	40-pin IDE	80-pin	yes
ATA-66				·
Ultra ATA Mode 4	99.9 MBs	40-pin IDE	80-pin	yes
ATA-100				·
Ultra ATA Mode 4	133.3 MBs	40-pin IDE	80-pin	yes
ATA-133				·

These IDE features can be configured in the AMIBIOS Setup utility from the *IDE Configurations* submenu in the *Advanced* section.

The IDE cable that is included with the Olympus III motherboard is a color-coded, 80 conductor/40 pin, ATA-100/133 IDE cable. Connect the blue connector to J7 and the black connector to the primary master IDE device. The white connector is reserved for the primary slave IDE device.

Ultra ATA-100/133

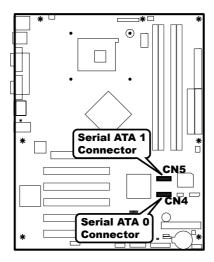
The Olympus III motherboard supports Ultra DMA-100/133. In order to take advantage of this feature, you must have the following:

- DMA-aware operating system
- Ultra ATA-100/133 compatible IDE device
- 40-pin 80-conductor cable (included)

Note:

Some IDE devices that are ATA-33 (and lower) cannot be used with the Ultra ATA-100/133 cable. This is very rare. If the device is not recognized, you must use a standard IDE cable. The Olympus III motherboard does not include a standard IDE cable.

CN4 and CN5 Serial ATA Connectors



The Olympus III motherboard has two independent Serial ATA ports. Serial ATA has a theoretical maximum transfer rate of 150 MBs per Serial ATA port. One Serial ATA device can be installed on each Serial ATA port for a maximum of two Serial ATA devices.

For compatibility, the underlying Serial ATA functionality is transparent to the operating system. The Serial ATA controller can operate in both legacy and native Serial ATA modes. In legacy mode, standard resources are assigned, such as IRQ 14 and IRQ 15. In Native Serial ATA mode, standard PCI resource steering is used. Native Serial ATA mode is recommended for use with the Microsoft® Windows XP and Microsoft® Windows 2000/2003 operating systems.

Pin	Signal Name
1	Ground
2	TXP
3	TXN
4	Ground
5	RXN
6	RXP
7	Ground

Note:

Serial ATA hard disk drives use new low-voltage power connectors and require adapters or power supplies equipped with low-voltage power connectors. See serialata.org for more information.

Step 5 Attach Internal Cables, Continued

Serial ATA RAID

The Olympus III motherboard supports RAID level 0 (disk striping) on the onboard Serial ATA ports. Two physical hard disk drives, of identical size, can be teamed together to create one logical drive. As data is written or retrieved from the logical drive, both drives operate in parallel, thus increasing the throughput.

Note:

The Olympus III motherboard provides support for RAID level 0 and RAID boot in Microsoft $\mbox{\it Windows}$ XP only.

RAID Boot

A RAID array can be created by using the existing Serial ATA ports, correctly configuring the BIOS, and installing drivers. The following steps are required to successfully establish a RAID configuration.

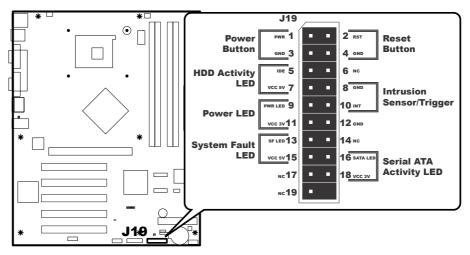
Step	Description
1	Enable RAID Support in BIOS
2	Create a RAID array using the Intel® Application Accelerator (IAA) utility
3	Install the IAA 3.0 RAID driver
4	Format the RAID array

J19 Front Panel Connector

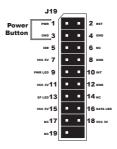
The JP19 Front Panel Connector provides front panel chassis connections for the following connectors:

Connector	Pins	Turn to
ATX Power Supply Soft ON/OFF	1 and 3	
Reset Button	2 and 4	
Parallel ATA Activity LED	5 and 7	
Intrusion Sensor	8 and 10	
Power LED	9 and 11	
System Fault LED	13 and 15	
Serial ATA Activity LED	16 and 18	

The following is a diagram of the J19 header:



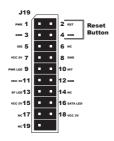
J19 ATX Power Supply Soft ON/OFF Connector



Attach your chassis power on/off button/switch to this section of the header.

Pin	Signal Name
1	#power
3	ground

J19 Reset Button Connector



Attach your chassis reset button/switch to this section of the header.

Pin	Signal Name
2	#reset
4	ground

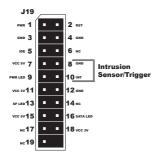
J19 Parallel ATA Activity LED Connector



Attach your chassis HDD activity LED to this section of the header. Check for the correct polarity.

Pin	Signal Name
5	#IDE LED
7	VCC +5 V

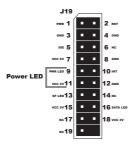
J19 Intrusion Sensor Connector



Attach your chassis intrusion sensor/trigger to this section of the header.

Pin	Signal Name
8	ground
10	#intrusion sensor/trigger

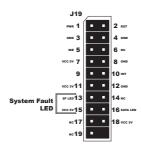
J19 Power LED Connector



Attach your chassis power LED to this section of the header. Check for the correct polarity.

Pin	Signal Name
9	#power LED
11	VCC +3 V

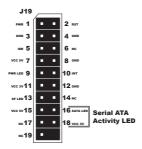
J19 System Fault LED Connector



Attach your chassis system fault/warning LED to this section of the header (if applicable). Check for the correct polarity.

Pin	Signal Name
13	#system fault LED
15	VCC +5 V

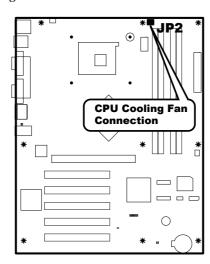
J19 Serial ATA Activity LED Connector



Attach your chassis Serial ATA HDD activity LED to this section of the header (if applicable). Check for the correct polarity.

Pin	Signal Name
16	#SATA LED
18	VCC +3 V

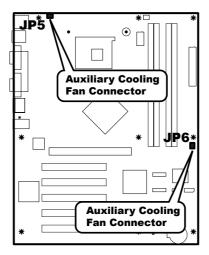
JP2 CPU Cooling Fan Connector



Attach the CPU cooling fan to JP2.

Pin	Signal Name
1	Ground
2	+ 12 V
3	Tachometer Output

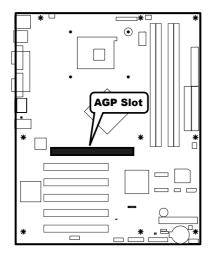
JP5 and JP6 Auxiliary Cooling Fan Connector



If your chassis has an internal chassis-cooling fan, you can attach the chassis-cooling fan to either JP5 or JP6.

Pin	Signal Name
1	Ground
2	+ 12 V
3	Tachometer Output

AGP Slot



The Olympus III incorporates one AGP slot for a video graphics adapter. The Olympus III AGP slot can accept the following:

- 4x, 8x AGP 3.0 expansion boards with 0.8 V I/O
- 1x, 4x AGP 2.0 expansion boards with 1.5 V I/O

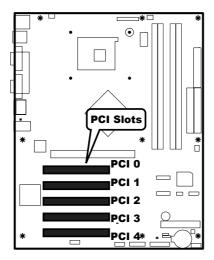
Note:

- AGP 2x expansion boards are **NOT** supported.
- Read the documentation for the expansion board before installing it into the
- For easier installation of your system memory, install your system memory first before installing an AGP expansion board.
- The AGP connector is keyed for Universal 0.8 V AGP 3.0 expansion boards or 1.5 V AGP 2.0 expansion boards only.

!Warning

Do not attempt to install a legacy 3.3 V AGP expansion board. The AGP connector is not mechanically compatible with legacy 3.3 V AGP expansion boards.

PCI Slots



The Olympus III incorporates five PCI slots for a various expansion boards. The Olympus III PCI slots can accept standard 32 bit PCI expansion boards. All of the PCI bus connectors are bus master capable.

Note: Read the documentation for the expansion board before installing it into the system.

PCI IRQ Routing Table

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all expansion boards that require only one interrupt are in this category. For almost all expansion boards that require more than one interrupt, the first interrupt on the expansion board is also classified as INTA.
- INTB: Generally, the second interrupt on expansion boards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on expansion boards is classified as INTC and a fourth interrupt is classified as INTD.

The ICH has eight programmable interrupt request (PIRQ) input signals. All PCI interrupt sources either onboard or from a PCI expansion board connect to one of these PIRQ signals. Some PCI interrupt sources are electrically tied together on the Olympus III motherboard and therefore share the same interrupt. The following table shows an example of how the PIRQ signals are routed.

Step 6 Install Expansion Boards, Continued

PCI IRQ Routing Table, Continued

For example, using the following table as a reference, assume an expansion card using INTA is plugged into PCI slot 2. In PCI slot 2, INTA is connected to PIRQB, which is already connected to the ICH audio controller. The expansion board in PCI slot 2 now shares an interrupt with the onboard interrupt source.

PCI Interrupt	ICH PIRQ Signal Name							
Source	PIRQA	PIRQB	PIRQC	PIRQD	PIRQE	PIRQF	PIRQG	PIRQH
AGP Connector	INTA	INTB						
USB Controller 1	INTA							
SMBus Controller		INTB						
AC'97 ICH Audio		INTB						
Controller								
USB Controller 2				INTB				
USB 2.0 Controller								INTD
PCI 0					INTD	INTA	INTB	INTC
PCI 1					INTC	INTB	INTA	INTD
PCI 2	INTD	INTA	INTB	INTC				
PCI 3			INTB	INTA		INTC	INTD	
PCI 4	INTC		INTA		INTD			INTB
Serial ATA/Serial						INTA		
ATA RAID								

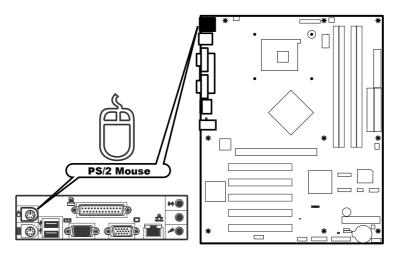
Note:

In PIC mode, the ICH can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

Caution

Only the back panel I/O connectors of the motherboard have overcurrent protection. The internal motherboard connectors are not overcurrent protected, and should connect only to devices inside the system chassis, such as fans and internal peripherals. Do not use these connectors for powering devices external to the system chassis. A fault in the load presented by the external devices could cause damage to the system, the interconnecting cable, and the external devices themselves.

PS/2 Mouse Connector

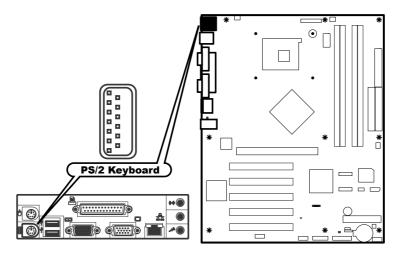


Connect your PS/2 mouse into this port (if applicable).

Pin	Signal Name
1	Mouse Data
2	Not Connected
3	Ground
4	Fused + 5 V
5	Mouse Clock
6	Not Connected

Step 7 Connecting External Cables, Continued

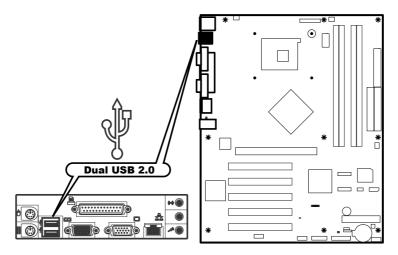
PS/2 Keyboard Connector



Connect your PS/2 keyboard into this port (if applicable).

Pin	Signal Name
1	Keyboard Data
2	Not Connected
3	Ground
4	Fused + 5 V
5	Keyboard Clock
6	Not Connected

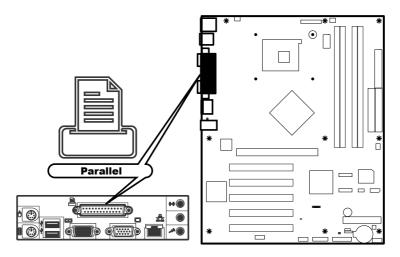
Dual USB Connectors



Connect your USB devices into this port (if applicable).

Pin	Signal Name
1	Fused + 5 V
2	USBP0# / USBP1#
3	USBP0 / USBP1
4	Ground

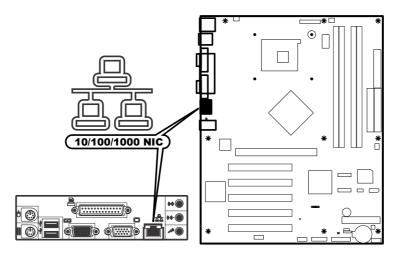
Parallel Port Connector



Connect your parallel device into this port (if applicable).

Pin	Signal Name	Signal Name				
	STD	ECP	EPP			
1	Strobe #	Strobe #	Strobe #			
2	PD0	PD0	PD0			
3	PD1	PD1	PD1			
4	PD2	PD2	PD2			
5	PD3	PD3	PD3			
6	PD4	PD4	PD4			
7	PD5		PD5			
8	PD6	PD6	PD6			
9	PD7	PD7	PD7			
10	ACK #	ACK#	INTR			
11	BUSY	BUSY #, PERIPHACK	WAIT #			
12	PERROR	PE, ACKREVERSE#	PE			
13	Select	Select	Select			
14	AUDOFD#	AUDOFD #, HOSTACK	DATASTB#			
15	FAULT #	FAULT #, PERIPHREQST #	FAULT #			
16	INIT #	INIT #, REVERSERQST #	RESET#			
17	SLCTIN#	SLCTIN #	ADDRSTB#			
18	Ground	Ground	Ground			
19	Ground	Ground	Ground			
20	Ground	Ground	Ground			
21	Ground	Ground	Ground			
22	Ground	Ground	Ground			
23	Ground	Ground	Ground			
24	Ground	Ground	Ground			
25	Ground	Ground	Ground			

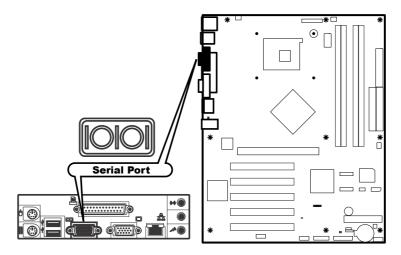
LAN Connector



Connect your network cable into this jack (if applicable).

Pin	Signal Name
1	TX+
2	TX-
3	RX+
4	Ground
5	Ground
6	RX-
7	Ground
8	Ground

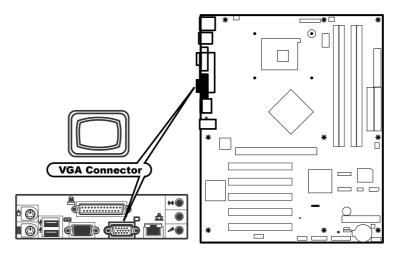
Serial Port Connector



Connect your serial device into this port (if applicable).

Pin	Signal Name
1	DCD (Data Carrier Detect)
2	DSR (Data Set Ready)
3	SIN# (Serial Data In)
4	RTS (Request to Send)
5	SOUT# (Serial Data Out)
6	CTS (Clear to Send)
7	DTR (Data Terminal Ready)
8	RI (Ring Indicator)
9	Ground
10	Key

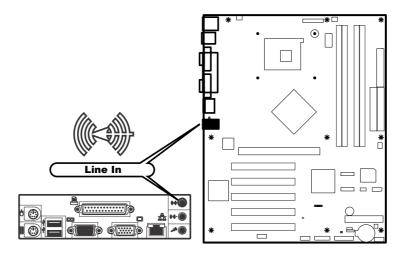
VGA Connector



Connect your monitor into this connector (if applicable).

Pin	Signal Name
1	Red
2	Green
3	Blue
4	+5V
5	Ground
6	Ground
7	Ground
8	Ground
9	+5V
10	Ground
11	+5V
12	5VDDCDA
13	5VHSYNC
14	5VVSYNC
15	5VDDCCL

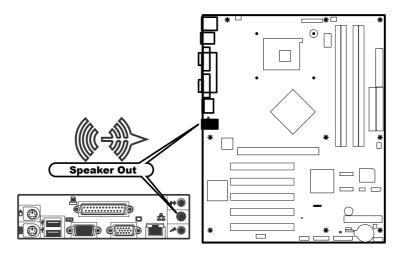
Line In Audio Jack



Connect your audio device into this jack (if applicable).

Pin	Signal Name
1	Line Right
2	Ground
3	Ground
4	Line Left
5	Ground

Speaker Out Audio Jack

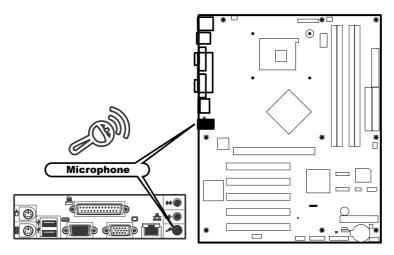


Connect your speaker into this jack (if applicable).

Pin	Signal Name
1	Audio Right
2	Ground
3	Ground
4	Audio Left
5	Ground

Step 7 Connecting External Cables, Continued

Microphone Audio Jack



Connect your microphone into this jack (if applicable).

Pin	Signal Name
1	+5V
2	Ground
3	Ground
4	Mic
5	Ground

Step 8 Install Drivers

Install the software drivers.

Step 9 Test and Configure

Test the board and make sure the configurations are correct.

AMIBIOS Setup Chapter 3

Overview

In PCI servers, the system parameters (such as amount of memory, type of disk drives and video displays, and many other elements) are stored in CMOS RAM. Unlike the system memory that is used for standard system memory, CMOS RAM requires very little power. When the server is powered off, a back-up battery provides power to CMOS RAM that retains the system parameters. Every time the server is powered on, the server is configured with the values stored in CMOS RAM by the system BIOS, which gains control when the server is powered on.

The system parameters are configured by a system BIOS Setup utility. Historically, BIOS setup utilities have been character-based, required keyboard input, and have had user interfaces that were not very intuitive. The BIOS chips acts as an interface between the processor and the rest of the server board's components. This chapter describes the parameters in the AMIBIOS Setup Utility and explains how to modify the settings for the configuration of your Olympus III motherboard.

Caution

The default settings are sufficient for most system operations. Changes to the default settings can affect the performance/reliability/stability of your Olympus III motherboard.

Starting AMIBIOS Setup



As POST executes, press the key to enter the AMIBIOS Setup Utility.

AMIBIOS Setup Menu

The AMIBIOS Setup Utility appears as shown below. Each menu item is described in this chapter.



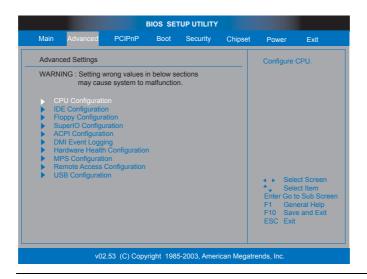
Select *Main* from the main menu of the *AMIBIOS Setup Utility*. All *Main* setup options are described in this section. The *Main* setup screen is displayed below:



Field	Description
AMIBIOS Version	This field displays the AMIBIOS version number. This field cannot be modified and is grayed out.
BIOS Build Date	This field displays the AMIBIOS build date. This field cannot be modified and is grayed out.
BIOS ID	This field displays the AMIBIOS identification number. This field cannot be modified and is grayed out.
Processor Type	This field displays the processor manufacturer information. This field cannot be modified and is grayed out.
Processor Speed	This field displays the speed of the processor. This field cannot be modified and is grayed out.
Processor Count	This field displays the number of physical processors are on the motherboard. This field cannot be modified and is grayed out.
System Memory	This field displays the amount of system memory that is physically installed in the Olympus III motherboard. This field cannot be modified and is grayed out.
System Time	Use this option to change the system time. Highlight <i>Time</i> using the arrow keys. Enter new values through the keyboard. Press the <tab> key or the arrow keys to move between fields. The time is entered in HH:MM:SS format. The time is in 24-hour format. For example, 5:30 a.m. appears as 05:30:00, and 5:30 p.m. as 17:30:00.</tab>
	Press <pgup> or <pgdn> after you have selected an option to display the complete list of valid settings in the bottom section of the screen.</pgdn></pgup>
System Date	Use this option to change the system date. Highlight <i>Date</i> using the arrow keys. Enter new values through the keyboard. Press the <tab> key or the arrow keys to move between fields. The date must be entered in MM/DD/YYYY format.</tab>
	Press <pgup> or <pgdn> after you have selected an option to display the complete list of valid settings in the bottom section of the screen.</pgdn></pgup>

Chapter Three: AMIBIOS Setup 65

Select Advanced from the main menu of the AMIBIOS Setup Utility. All Advanced setup options are described in this section. The *Advanced* setup screen is displayed below:



CPU Configuration



Field	Description
Manufacturer	This field displays the manufacturer of the processor that is installed on the motherboard.
Brand String	This field displays the hard coded text string the is contained in the processor.
Frequency	This field displays the operating frequency of the processor.
FSB Speed	This field displays the front side bus speed of the processor.
Cache L1	This field displays the level one cache that is reported by the processor. Typically, the
	higher this number the greater the performance.
Cache L2	This field displays the level two cache that is reported by the processor. Typically, the
	higher this number the greater the performance.

CPU Configuration, Continued

Field	Description
Cache L3	This field displays the level three cache that is reported by the processor. Typically, the
	higher this number the greater the performance.
Ratio Status	This field displays the current setting of the CPU clock multiplier ratio. Typically this
	setting is locked by the processor and cannot be changed. However, over-clocking the
	processor is very common and it is very desirable to change this setting.
Ratio Actual Value	This field displays the CPU clock multiplier ratio.
Ratio CMOS Settings	This field displays the CPU Ratio in CMOS. If an invalid ratio is set in CMOS, then
	actual and setpoint values may differ.
VID CMOS Settings	This field displays the CPU Voltage Identification code (VID) configuration as set in the
	CMOS.

L3 Cache

Option	Description
Disabled	Set this value to prevent the BIOS from using level three cache. This value is typically
	used to troubleshoot a problem.
Enabled	Set this value to turn on level three cache. This is the default setting.

Hyper Threading Technology

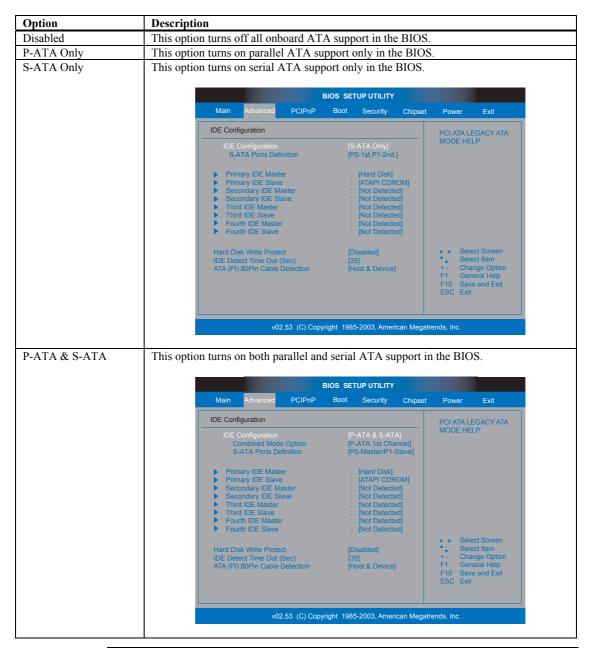
Hyper Threading Technology is the technology being built into many of Intel® Pentium® 4 processors. It allows a single processor to act as two independent processors.

Option	Description
Disabled	Set this value to turn off Hyper Threading technology in your processor.
Enabled	Set this value to turn on Hyper Threading technology in your processor. This is the default setting.

IDE Configuration



IDE Configuration, Continued



S-ATA Running Enhanced Mode

Option	Description
Yes	This value turns on Native mode support for your serial ATA controller. This is the
	default value.
No	This value turns off Native mode support for your serial ATA controller.

P-ATA Channel Selection

Option	Description
Primary	This value turns on parallel ATA support only on the Primary IDE connector and not the
	Secondary connector.
Secondary	This value turns on parallel ATA support only on the Secondary IDE connector and not
	the Primary connector.
Both	This value turns on parallel ATA support on the Primary IDE connector and the
	Secondary connector. This is the default value.

Combined Mode

Option	Description
P-ATA 1st Channel	This setting allows the motherboard to boot off the parallel ATA connectors first. This is the default value.
S-ATA 1st Channel	This setting allows the motherboard to boot off the serial ATA connectors first.

S-ATA Ports Definition

This setting allows you to assign the serial ATA port locations.

Option	Description
P0-3rd./P1-4th.	This setting assigns CN4 (SATA 0) as the third hard disk location and CN5 (SATA 1) as
	the forth hard disk location. For the location of these two connectors, see the <i>Board</i>
	Layout diagram in Chapter One, Hardware Specifications and Supported Features. This
	is the default value.
P0-4th./P1-3rd.	This setting assigns CN5 (SATA 1) as the third hard disk location and CN4 (SATA 0) as
	the forth hard disk location. For the location of these two connectors, see the <i>Board</i>
	Layout diagram in Chapter One, Hardware Specifications and Supported Features.

Configure S-ATA as RAID

Option	Description
No	This value turns off the BIOS level RAID level 0 boot support on the serial ATA
	connectors located at CN4 (SATA 0) and CN5 (SATA 1). This is the default value.
Yes	This value turns on the BIOS level RAID level 0 boot support on the serial ATA
	connectors located at CN4 (SATA 0) and CN5 (SATA 1).

Hard Disk Write Protect

Option	Description
Disabled	This value allows you to write to the hard disk drive. This is the default value.
Enabled	This value prevents you from making any changes to the hard disk drive. Essentially, the
	hard disk drive acts as a CD-ROM disc would.

IDE Detect Time Out (Sec)

Option	Description
0	This value prevents the system from waiting any amount of time when trying to detect
	the hard disk drives.
5	This value allows the system to wait five seconds when trying to detect the hard disk
	drives.
10	This value allows the system to wait ten seconds when trying to detect the hard disk
	drives.
15	This value allows the system to wait fifteen seconds when trying to detect the hard disk
	drives.
20	This value allows the system to wait twenty seconds when trying to detect the hard disk
	drives.
25	This value allows the system to wait twenty-five seconds when trying to detect the hard
	disk drives.
30	This value allows the system to wait thirty seconds when trying to detect the hard disk
	drives.
35	This value allows the system to wait thirty-five seconds when trying to detect the hard
	disk drives. This is the default value.

ATAPI 80 Pin Cable Detection

Option	Description
Host & Device	This setting allows the parallel ATA controller and ATA device to detect the type of
	ATA cable being used. This is the default value.
Host	This setting allows the parallel ATA controller to detect the type of ATA cable being
	used.
Device	This setting allows the ATA device to detect the type of ATA cable being used.

Primary and Secondary IDE Master: Hard Disk Drive



Field	Description
Device	Type of device, such as hard disk drive.
Vendor	Manufacturer of the device.
Size	The size of the device.
LBA Mode	LBA (Logical Block Addressing) is a method of addressing data on a disk drive. In LBA mode, the maximum drive capacity is 137 GB. For drive capacities over 137 GB, your AMIBIOS is equipped with 48-bit LBA mode addressing.
Block Mode	Block mode boosts IDE drive performance by increasing the amount of data transferred. Only 512 bytes of data can be transferred per interrupt if block mode is not used. Block mode allows transfers of up to 64 KB per interrupt.
PIO Mode	IDE PIO mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases.
Async DMA	This indicates the highest Asynchronous DMA Mode that is supported.
Ultra DMA	This indicates the highest Synchronous DMA Mode that is supported.
SMART	Self-Monitoring Analysis and Reporting Technology protocol used by IDE drives of some manufacturers to predict drive failures.

Primary and Secondary IDE Master: ATAPI CD ROM



Field	Description
Device	Type of device, such as hard disk drive.
Vendor	Manufacturer of the device.
LBA Mode	LBA (Logical Block Addressing) is a method of addressing data on a drive.
PIO Mode	IDE PIO mode programs timing cycles between the IDE drive and the programmable IDE
	controller. As the PIO mode increases, the cycle time decreases.
Async DMA	This indicates the highest Asynchronous DMA Mode that is supported.
Ultra DMA	This indicates the highest Synchronous DMA Mode that is supported.

Type

This option sets the type of device that the AMIBIOS attempts to boot from after the Power-On Self-Test (POST) has completed. The Optimal and Fail-Safe default setting is Auto.

Option	Description
Not Installed	Set this value to prevent the BIOS from searching for an IDE disk drive on the specified
	channel.
Auto	Set this value to allow the BIOS auto detect the IDE disk drive type attached to the specified
	channel. This setting should be used if an IDE hard disk drive is attached to the specified
	channel. This is the default setting.
CDROM	This option specifies that an IDE CD-ROM drive is attached to the specified IDE channel. The
	BIOS will not attempt to search for other types of IDE disk drives on the specified channel.
ARMD	This option specifies an ATAPI Removable Media Device.
	This includes, but is not limited to:
	• ZIP
	• LS-120

LBA/Large Mode

LBA (Logical Block Addressing) is a method of addressing data on a disk drive. In LBA mode, the maximum drive capacity is 137 GB. The Optimal and Fail-Safe default setting is Auto.

Note:

For hard disk drive capacities over 137 GB, your AMIBIOS is equipped with 48-bit LBA mode addressing.

Option	Description
Disabled	Set this value to prevent the BIOS from using Large Block Addressing mode control on the
	specified channel.
Auto	Set this value to allow the BIOS to auto detect the Large Block Addressing mode control on the
	specified channel. This is the default setting.

Block (Multi-Sector Transfer)

This option sets the block mode multi sector transfers option. The Optimal and Fail-Safe default setting is Auto.

Option	Description
Disabled	Set this value to prevent the BIOS from using Multi-Sector Transfer on the specified channel. The data to and from the device will occur one sector at a time.
Auto	Set this value to allow the BIOS to auto detect device support for Multi-Sector Transfers on the specified channel. If supported, set this value to allow the BIOS to auto detect the number of sectors per block for transfer from the hard disk drive to the memory. The data transfer to and from the device will occur multiple sectors at a time. This is the default setting.

PIO Mode

IDE PIO (Programmable I/O) mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases. The Optimal and Fail-Safe default setting is Auto.

Option	Description
Auto	Set this value to allow the BIOS to auto detect the PIO mode. Use this value if the IDE disk
	drive support cannot be determined. This is the default setting.
0	Set this value to allow the BIOS to use PIO mode 0. It has a data transfer rate of 3.3 MBs.
1	Set this value to allow the BIOS to use PIO mode 1. It has a data transfer rate of 5.2 MBs.
2	Set this value to allow the BIOS to use PIO mode 2. It has a data transfer rate of 8.3 MBs.
3	Set this value to allow the BIOS to use PIO mode 3. It has a data transfer rate of 11.1 MBs.
4	Set this value to allow the BIOS to use PIO mode 4. It has a data transfer rate of 16.6 MBs.
	This setting generally works with all hard disk drives manufactured after 1999. For other disk
	drive, such as IDE CD-ROM drives, check the specifications of the drive.

DMA Mode

This setting allows you to adjust the DMA mode options. The Optimal and Fail-Safe default setting is Auto.

Option	Description
Auto	Set this value to allow the BIOS to auto detect the DMA mode. Use this value if the IDE disk drive support cannot be determined. This is the default setting.
SWDMA0	Set this value to allow the BIOS to use Single Word DMA mode 0. It has a data transfer rate of 2.1 MBs.
SWDMA1	Set this value to allow the BIOS to use Single Word DMA mode 1. It has a data transfer rate of 4.2 MBs.
SWDMA2	Set this value to allow the BIOS to use Single Word DMA mode 2. It has a data transfer rate of 8.3 MBs.
MWDMA0	Set this value to allow the BIOS to use Multi Word DMA mode 0. It has a data transfer rate of 4.2 MBs.
MWDMA1	Set this value to allow the BIOS to use Multi Word DMA mode 1. It has a data transfer rate of 13.3 MBs.
MWDMA2	Set this value to allow the BIOS to use Multi Word DMA mode 2. It has a data transfer rate of 16.6 MBs.
UDMA0	Set this value to allow the BIOS to use Ultra DMA mode 0. It has a data transfer rate of 16.6 MBs. It has the same transfer rate as PIO mode 4 and Multi Word DMA mode 2.
UDMA1	Set this value to allow the BIOS to use Ultra DMA mode 1. It has a data transfer rate of 25 MBs.
UDMA2	Set this value to allow the BIOS to use Ultra DMA mode 2. It has a data transfer rate of 33.3 MBs.
UDMA3	Set this value to allow the BIOS to use Ultra DMA mode 3. It has a data transfer rate of 44.4 MBs.
UDMA4	Set this value to allow the BIOS to use Ultra DMA mode 4. It has a data transfer rate of 66.6 MBs.
UDMA5	Set this value to allow the BIOS to use Ultra DMA mode 5. It has a data transfer rate of 99.9 MBs.
UDMA6	Set this value to allow the BIOS to use Ultra DMA mode 6. It has a data transfer rate of 133.3 MBs.

S.M.A.R.T. for Hard Disk Drives

Self-Monitoring Analysis and Reporting Technology (SMART) feature can help predict impending drive failures. The Optimal and Fail-Safe default setting is Auto.

Option	Description
Auto	Set this value to allow the BIOS to auto detect hard disk drive support. Use this setting if the
	IDE disk drive support cannot be determined. This is the default setting.
Disabled	Set this value to prevent the BIOS from using the SMART feature.
Enabled	Set this value to allow the BIOS to use the SMART feature on all supported hard disk drives.

32Bit Data Transfer

This option sets the 32-bit data transfer option. The Optimal and Fail-Safe default setting is *Enabled*.

Option	Description
Disabled	Set this value to prevent the BIOS from using 32-bit data transfers.
Enabled	Set this value to allow the BIOS to use 32-bit data transfers on supported hard disk drives. This is the default setting.

ARMD Emulation Type

ATAPI Removable Media Device (ARMD) is a device that uses removable media, such as the LS120, MO (Magneto-Optical), or Iomega Zip drives. If you want to boot up from media on an ARMD, it is required that you emulate boot up from a floppy or hard disk drive. This is especially necessary when trying to boot to DOS. You can select the type of emulation used if you are booting from such a device. The Optimal and Fail-Safe default setting is *Auto*.

Note: This option only appears when an ARMD device is installed.

Option	Description
Auto	Set this value to allow the BIOS to automatically set the emulation used by ARMD. This is the default setting.
Floppy	Set this value for ARMD to emulate a floppy disk drive during boot up.
Hard Disk	Set this value for ARMD to emulate a hard disk drive during boot up.

Third and Forth IDE Slave

Not supported by the Olympus III hardware.

Floppy Configuration

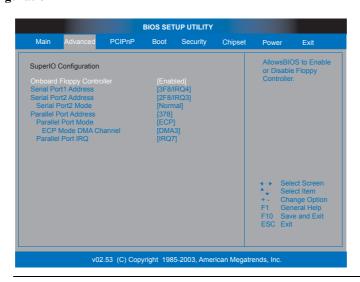


Floppy A Floppy B

Floppy disk drives are slowly being phased out of most systems. Since it is a relatively slow and low storage medium, most do not find a need to install it. However, the Olympus III motherboard still retains this legacy feature. It is especially useful when you are trying to boot to DOS. The Optimal and Fail-Safe default setting is Disabled.

Option	Description
Disabled	Set this value to prevent the system from using the selected Floppy Drive location.
360 KB 5.25"	Set this value to allow the system to address the selected Floppy Drive location as a 360 KB 5.25" floppy drive.
1.2 MB 5.25"	Set this value to allow the system to address the selected Floppy Drive location as a 1.2 MB 5.25" floppy drive.
720 KB 3.5"	Set this value to allow the system to address the selected Floppy Drive location as a 720 KB 3.5" floppy drive.
1.44 MB 3.5"	Set this value to allow the system to address the selected Floppy Drive location as a 1.44 MB 3.5" floppy drive.
2.88 MB 3.5"	Set this value to allow the system to address the selected Floppy Drive location as a 2.88 MB 3.5" floppy drive.

SuperIO Configuration



Onboard Floppy Controller

This field allows you to enable or disable the floppy disk drive controller on the Olympus III motherboard. The default value for this setting is *Enabled*.

Option	Description
Enabled	Set this value to allow the system to use the onboard floppy disk drive controller. This is the
	default value.
Disabled	Set this value to prevent the system from using the onboard floppy disk drive controller.

Serial Port1 Address

This option specifies the base I/O port address and Interrupt Request address of serial port 1. The Optimal setting is *3F8/IRQ4*. The Fail-Safe default setting is *Disabled*.

Option	Description
Disabled	This option prevents the serial port from accessing any system resources. It is not made
	available.
3F8/IRQ4	This option allows the serial port to use 3F8 as its I/O port address and IRQ 4 for the interrupt address. This is the default setting. The majority of serial port 1 or COM1 ports on computer systems use IRQ4 and I/O Port 3F8 as the standard setting. The most common serial device connected to this port is a mouse. If the system will not use a serial device, it is best to set this port to <i>Disabled</i> .
3E8/IRQ4	This option allows the serial port to use 3E8 as its I/O port address and IRQ 4 for the interrupt address. If the system will not use a serial device, it is best to set this port to <i>Disabled</i> .
2E8/IRQ3	This option allows the serial port to use 2E8 as its I/O port address and IRQ 3 for the interrupt address. If the system will not use a serial device, it is best to set this port to <i>Disabled</i> .

Serial Port2 Address

This option specifies the base I/O port address and Interrupt Request address of serial port 2. The Optimal setting is *2F8/IRQ3*. The Fail-Safe setting is *Disabled*.

Option	Description
Disabled	This option prevents the serial port from accessing any system resources. It is not made available.
2F8/IRQ3	This option allows the serial port to use 2F8 as its I/O port address and IRQ 3 for the interrupt address. This is the default setting. The majority of serial port 2 or COM2 ports on computer systems use IRQ3 and I/O Port 2F8 as the standard setting. If the system will not use a serial device, it is best to set this port to <i>Disabled</i> .
3E8/IRQ4	This option allows the serial port to use 3E8 as its I/O port address and IRQ 4 for the interrupt address. If the system will not use a serial device, it is best to set this port to <i>Disabled</i> .
2E8/IRQ3	This option allows the serial port to use 2E8 as its I/O port address and IRQ 3 for the interrupt address. If the system will not use a serial device, it is best to set this port to <i>Disabled</i> .

Serial Port2 Mode

This option specifies the mode of the secondary onboard serial port I/O port. The Optimal and Fail-Safe setting is Normal. When selecting settings other than Normal, more choices become available under it. The options are all related to Infrared settings.

IrDA (Infrared Data Association)Error! Bookmark not defined. has about the same transfer rate as that of a parallel port.

Option	Description
Normal	This option allows the motherboard to set the secondary onboard serial port to standard serial
Sharp IR	Sharp IR or ASK IR is a protocol developed by Sharp for use with its range of electronic organizers. Sharp was a manufacturing partner for the Apple MessagePad and released a similar model at the same time. Apple adopted the Sharp protocol, and included an application in the Newton OS 1.x to connect via infrared to Sharp organizers and exchange data. This Infrared protocol is widely used in Japan.
SIR	SIR or Serial IR operates at higher rates. It is meant for long-range transmission where you need more than a few characters to pass through.
Consumer	Consumer IR can be used in long distance, but the transfer rate is very slow.

IR Duplex Mode

This option specifies the Infrared transfer used when any infrared option is enabled on serial port 2. The Optimal and Fail-Safe settings hide this option completely. The default setting is Full Duplex.

Option	Description
Full Duplex	This option allows the Infrared port to send and receive at the same time.
Half Duplex	This option allows the Infrared port to send or receive information, then send or receive
	information after the infrared port is clear. It cannot perform both a send and receive at the
	same time.

IR Receiver Pin

This option allows you to specify the receiver pin used to receive IR signals.

Option	Description
IRRX1	This option allows you to specify the IRRX1 pin to be used for receiving IR signals.
IRRX2	This option allows you to specify the IRRX2 pin to be used for receiving IR signals.

Parallel Port Address

This option specifies the I/O address used by the parallel port. The Optimal setting is 378. The Fail-Safe setting is *Disabled*.

Option	Description
Disabled	This option prevents the parallel port from accessing any system resources. It is not made available.
378	This option allows the serial port to use 378 as its I/O port address. This is the default setting. The majority of parallel ports on computer systems use IRQ7 and I/O Port 378H as the standard setting.
278	This option allows the serial port to use 278 as its I/O port address.
3BC	This option allows the serial port to use 3BC as its I/O port address.

Parallel Port Mode

This option specifies the parallel port mode. The Optimal setting is Normal. The Fail-Safe setting is *Disabled*.

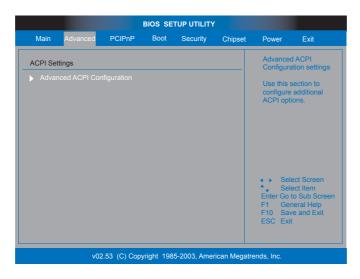
Option	Description
Normal	This option allows the standard parallel port mode to be used. This is the default setting.
Bi-Directional	This option allows data to be sent to and received from the parallel port.
ЕРР	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bi-directional data transfer driven by the host device.
	When EPP is selected, you can select the EPP Version as either 1.7 or 1.9.
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits per second. ECP provides symmetric bi-directional communication.
	When ECP is selected, you can change the value of the ECP Mode DMA Channel. It can be set to 0, 1, or 3.

Parallel Port IRQ

This option specifies the IRQ used by the parallel port. The Optimal and Fail-Safe default setting is 7.

Option	Description
5	This option allows the serial port to use Interrupt 3.
7	This option allows the serial port to use Interrupt 7. This is the default setting. The majority of
	parallel ports on computer systems use IRQ7 and I/O Port 378H as the standard setting.

ACPI Configuration



Option	Description
Advanced ACPI	This option allows you to enable or disable various ACPI (Advanced Configuration and Power
Configuration	Interface) support.

Advanced ACPI Configuration



ACPI 2.0 Support

This option allows you to enable or disable ACPI (Advanced Configuration and Power Interface) 2.0 support.

Option	Description
No	This option turns off ACPI 2.0 support and is the default setting.
Yes	This option turns on ACPI 2.0 support.

ACPI APIC Support

This option allows you to enable or disable ACPI APIC (Advanced Programmable Interrupt Controller) support.

Option	Description
Disabled	This option turns off ACPI APIC support.
Enabled	This option turns on ACPI APIC support and is the default setting.

APIC SCI IRQ

This option allows you to enable or disable APIC SCI IRQ.

Option	Description
Disabled	This option turns off APIC SCI IRQ support and is the default setting.
Enabled	This option turns on APIC SCI IRQ support.

BIOS-->AML ACPI Table

This option allows you to enable or disable the BIOS-->AML ACPI table function.

Option	Description
Disabled	This option turns off the BIOS> AML ACPI table function.
Enabled	This option turns on the BIOS> AML ACPI table function and is the default setting.

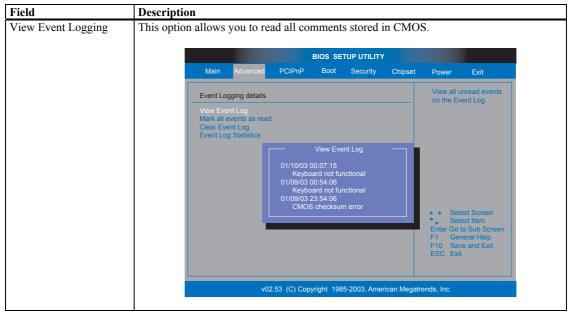
Headless Mode

This option allows you to enable or disable headless operation mode through ACPI.

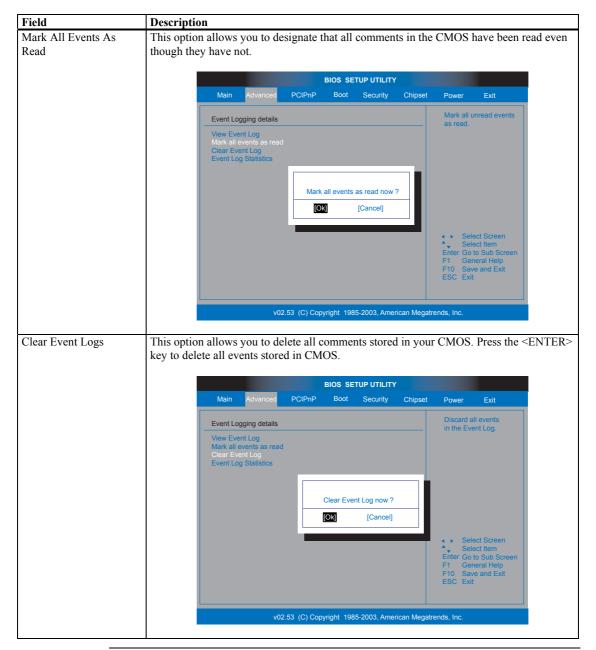
Option	Description
Disabled	This option turns off headless operation mode through ACPI and is the default setting.
Enabled	This option turns on headless operation mode through ACPI.

DMI Event Logging

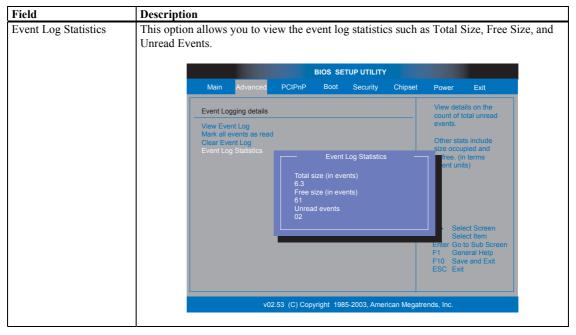




DMI Event Logging, Continued



DMI Event Logging, Continued



Hardware Health Configuration



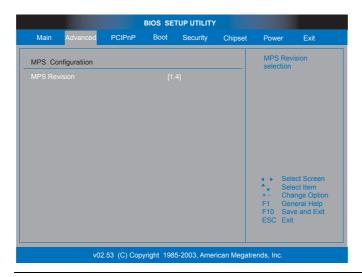
HW Health Function

Option	Description
Disabled	This option turns off hardware health monitoring
Enabled	This option turns on hardware health monitoring and is the default setting.

Hardware Health Event Monitoring

Field	Description
System	Displays the current internal system ambient temperature.
Temperature	
CPU	Displays the current CPU internal temperature.
Temperature	
Fan1/2/3 Speed	Displays the current speed of CPU cooling fan at JP2 and Auxiliary Fans at JP5 and JP6.
CPU Core	Displays the current CPU core actual voltage value.
1.5V/3.3V/+12V	Displays the current voltage against the 1.5V/3.3V/+12V/+5V/5VSB/Battery power supply.
/+5.00V/5VSB/	
Battery	

MPS Configuration



MPS Revision

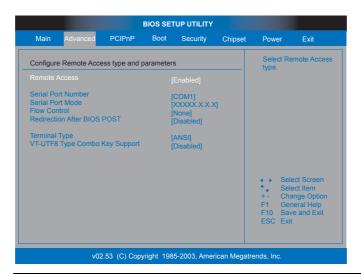
The AMIBIOS Setup allows you to select whether to use Multi-Processor Specification (MPS) 1.1 or 1.4. The MPS is a specification by which PC manufacturers design and build Intel architecture (IA) systems with two or more processors.

MPS version 1.4 added extended configuration tables to improve support for multiple PCI bus configurations and improve future expandability. Most newer versions of server operating systems support MPS 1.4 and, as such, you should not change the BIOS Setup default of 1.4 to 1.1 if your operating system supports the 1.4 version.

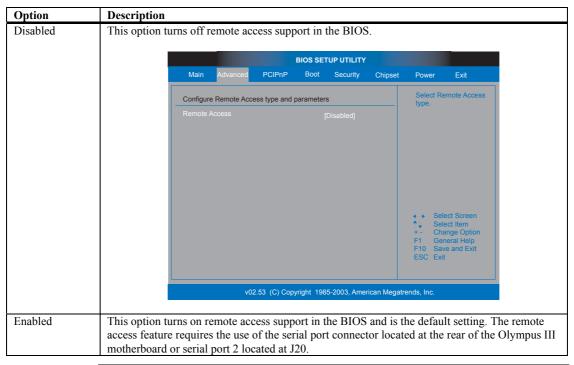
Check with the vendor of your operating system to find out which version to use if you are unsure. Some operating systems may require version 1.1 for compatibility reasons.

Option	Description
1.4	This option allows the BIOS to use MultiProcessor Specification version 1.4. This is the default
	setting.
1.1	This option allows the BIOS to use MultiProcessor Specification version 1.1.

Remote Access Configuration



Remote Access



Serial Port Number

Option	Description
COM1	This setting allows you to use the serial port connector located at the rear of the Olympus III
	motherboard. This is the default value.
COM2	This setting allows you to use the internal serial port connector located at J20 on the Olympus
	III motherboard.

Serial Port Mode

You can use any mode you want. Just keep in mind that the bits per second, data bits, parity, and stop bits must match your terminal setting.

Option	Description
115200 8,n,1	This value allows the serial port to transfer data at 115200 bits per second using eight data bits, no parity bit, and one stop bit.
57600 8,n,1	This value allows the serial port to transfer data at 57600 bits per second using eight data bits, no parity bit, and one stop bit.
19200 8,n,1	This value allows the serial port to transfer data at 19200 bits per second using eight data bits, no parity bit, and one stop bit. This is the default value.

Flow Control

Option	Description
None	This value turns off data flow control (handshaking). Flow control is not used. This is the
	default value.
Software	This value allows software handshaking to be used to control data flow.
Hardware	This value allows hardware handshaking to be used to control data flow.

Redirection After BIOS POST

Option	Description
Disabled	This value turns off redirection after POST. This is the default value.
Boot Loader	This value turns on redirection during POST and during the time when the operating system is
	booting.
Always	This value allows redirection to be on at all times. Some operating systems may not work if this
	value is used.

Terminal Type

Option	Description
ANSI	Use this value if your target terminal uses a standard US (United States) ANSI keyboard. This is
	the default value.
VT-UTF8	Use this value if your target terminal uses VT-UTF8 combination keys.

VT-UTF8 Type Combo Key Support

Option	Description
Disabled	This option turns off VT-UTF8 combination key support for ANSI/VT100 terminals.
Enabled	This option turns on VT-UTF8 combination key support for ANSI/VT100 terminals. This is the default value.

USB Configuration



Field	Description
Module Version	This field displays the version of the USB module.
USB Devices Enabled	This field lists all USB devices that are attached and functioning properly on the Olympus III motherboard.

USB Function

Option	Description
Disabled	Set this value to prevent the system from using any of the onboard USB ports.
	BIOS SETUP UTILITY
	Main Advanced PCIPnP Boot Security Chipset Power Exit
	USB Configuration Enables USB host controllers.
	Module Version - 2.23.0-7.4
	USB Devices Enabled : None
	USB Function [Disabled]
	Select Screen Select Item + Change Option F1 General Help F10 Save and Exit ESC Exit
	v02.53 (C) Copyright 1985-2003, American Megatrends, Inc.
2 USB Ports	Set this value to allow the system to address up to two USB ports.
4 USB Ports	Set this value to allow the system to address up to four USB ports. This is the defau

Legacy USB Support

Option	Description
Enabled	Set this value to allow the system to use legacy USB devices such as a USB keyboard and a
	USB mouse. This is the default value.
Disabled	Set this value to prevent the system from using legacy USB devices such as a USB keyboard
	and a USB mouse.
Auto	Set this value to allow the BIOS to automatically detect the correct settings.

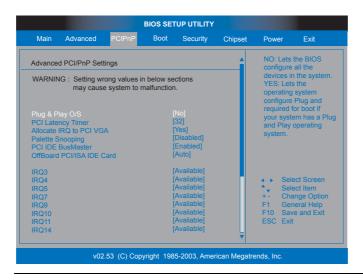
USB 2.0 Controller

Option	Description
Enabled	Set this value to allow the system to use the onboard USB 2.0 controller. This is the default
	value.
Disabled	Set this value to prevent the system from using the onboard USB 2.0 controller.

USB 2.0 Controller Mode

Option	Description
FullSpeed	Set this value to force the BIOS to use the onboard USB 2.0 controller at the USB 1.1 speeds.
HiSpeed	Set this value to force the BIOS to use the onboard USB 2.0 controller at full USB 2.0 speeds. This is the default value.

Choose PCI/PnP Setup from the AMIBIOS Setup main menu. All PCI/PnP Setup options are described in this section. The PCI/PnP Setup screen is shown below:



Plug and Play O/S

Option	Description
No	This value allows the BIOS to configure the devices in the system. This is the default value.
Yes	This value allows the operating system to configure all Plug and Play devices not required during boot. Use this setting if your operating system supports plug and play devices.

PCI Latency Timer

This option allows the PCI Latency Timer to be adjusted. Basically, it allows you to set a delay to allow the BIOS to find all PCI devices. This option sets the latency of all PCI devices on the PCI bus. The settings are in units equal to PCI clocks. The Optimal and Fail-Safe default settings is 64.

Option	Description
32	This option sets the PCI latency to 32 PCI clocks.
64	This option sets the PCI latency to 64 PCI clocks. This is the default setting.
96	This option sets the PCI latency to 96 PCI clocks.
128	This option sets the PCI latency to 128 PCI clocks.
160	This option sets the PCI latency to 160 PCI clocks.
192	This option sets the PCI latency to 192 PCI clocks.
224	This option sets the PCI latency to 224 PCI clocks.
248	This option sets the PCI latency to 248 PCI clocks.

Section 3 PCI/PnP Setup, Continued

Allocate IRQ to VGA

This option allows the system to adjust the Allocate IRQ to VGA setting. The Optimal and Fail-Safe default settings is Yes.

Option	Description
Yes	This option allows the allocation of an IRQ to a VGA adapter card that uses the PCI local bus.
	This is the default setting.
No	This option prevents the allocation of an IRQ to a VGA adapter card that uses the PCI local bus.

Palette Snooping

This option allows the system to modify the Palette Snooping settings. The Optimal and Fail-Safe default settings is *Disabled*.

Option	Description
Disabled	This is the default setting and should not be changed unless the VGA card manufacturer requires Palette Snooping to be Enabled.
Enabled	This setting informs the PCI devices that an ISA based Graphics device is installed in the system so the card will function correctly. This does not necessarily indicate a physical ISA adapter card. The graphics chipset can be mounted on a PCI card. Always check with your adapter card manuals first, before modifying the default settings in the BIOS.

PCI IDE BusMaster

This option allows the PCI IDE busmastering to be set. The Optimal and Fail-Safe default settings is Disabled.

Option	Description
Disabled	This option prevents PCI busmastering. This is the default setting.
Enabled	This option specifies that the IDE controller on the PCI local bus has mastering capabilities.

Section 3 PCI/PnP Setup, Continued

Onboard PCI IDE Card

This option allows you to select which physical PCI slot a PCI IDE expansion board is installed. Some PCI IDE expansion boards require this. The Optimal and Fail-Safe default settings is Auto.

Option	Description
Auto	This value allows the BIOS to locate any PCI IDE expansion boards installed on the motherboard. This is the default value.
PCI Slot 1	Use this value if you have installed a PCI IDE expansion board in PCI slot labeled PCI0 on your motherboard.
PCI Slot 2	Use this value if you have installed a PCI IDE expansion board in PCI slot labeled PCI1 on your motherboard.
PCI Slot 3	Use this value if you have installed a PCI IDE expansion board in PCI slot labeled PCI2 on your motherboard.
PCI Slot 4	Use this value if you have installed a PCI IDE expansion board in PCI slot labeled PCI3 on your motherboard.
PCI Slot 5	Use this value if you have installed a PCI IDE expansion board in PCI slot labeled PCI4 on your motherboard.

IRQ 3, 4, 5, 9, 10, 11, 14, and 15

Option	Description
Available	This setting specifies that this IRQ is available to be used by PCI/PnP devices. This is the
	default value.
Reserved	This setting specifies that this IRQ is reserved to be used by legacy ISA devices.

DMA Channel 0, 1, 3, 5, 6, and 7

Option	Description
Available	This setting specifies that this DMA is available to be used by PCI/PnP devices. This is the default value.
Reserved	This setting specifies that this DMA is reserved to be used by legacy ISA devices.

Section 3 PCI/PnP Setup, Continued

Reserved Memory Size



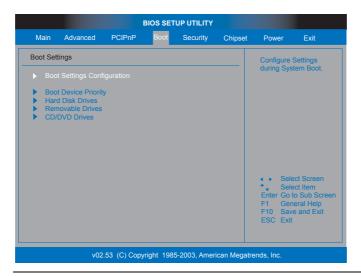
Option	Description
Disabled	This value prevents the BIOS from reserving any memory for legacy ISA devices. This is the
	default value.
16K	Set this value to reserve a 16K block of memory for use with legacy ISA devices.
32K	Set this value to reserve a 32K block of memory for use with legacy ISA devices.
64K	Set this value to reserve a 64K block of memory for use with legacy ISA devices.

Section 4 Boot Setup

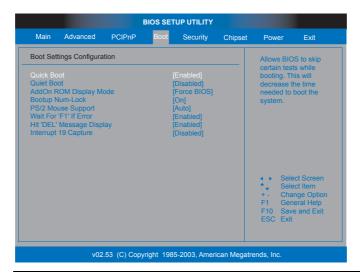
Choose Boot Setup from the AMIBIOS Setup main menu. All Boot Setup options are described in this section. Select an item on the Boot Setup screen to access the sub screen for:

- **Boot Settings Configuration**
- **Boot Device Priority**
- Hard Disk Drives
- Removable Devices
- CD/DVD Drives

The Boot Setup screen is shown below:



Boot Settings Configuration



Section 4 Boot Setup, Continued

Quick Boot

Option	Description
Enabled	This value allows the BIOS to skip some POST tests to speed up the boot process. This is the
	default value.
Disabled	This value runs all BIOS POST tests.

Quiet Boot

Option	Description
Enabled	This value displays an OEM logo instead of the BIOS boot screens during POST.
Disabled	This value displays the BIOS boot screens during POST. This is the default value.

AddOn ROM Display Mode

Option	Description
Force BIOS	This value displays the option ROM even if the option ROM is set to not display during boot.
	This is the default value.
Keep Current	This value allows the option ROM to determine whether or not it is displayed.

Bootup Num-Lock

Option	Description
On	This value turns on the NUM-LOCK at boot. This is the default value.
Off	This value turns off the NUM-LOCK at boot. The number lock can be instated at anytime after the motherboard is powered on by simply pressing the NUM LOCK key (if applicable).

PS/2 Mouse Support

Option	Description
Disabled	This value turns off PS/2 mouse support at the BIOS level.
Enabled	This value turns on PS/2 mouse support at the BIOS level.
Auto	This value allows the BIOS to determine if a PS/2 mouse is being used. If a PS/2 mouse is detected, the BIOS enables the PS/2 mouse support. This is the default value.

Wait For 'F1' If Error

Option	Description
Disabled	This value prevents the system from waiting for you to press the <f1> key if the BIOS detects an error during POST.</f1>
Enabled	This value allows the system to halt on errors while it waits for you to press the <f1> key if the BIOS detects an error during POST. This is the default value.</f1>

Section 4 Boot Setup, Continued

Hit 'DEL' Message Display

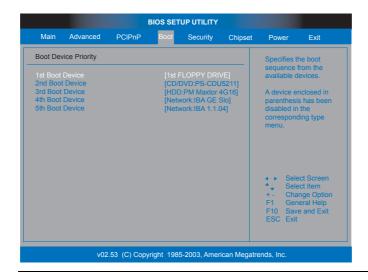
Option	Description
Disabled	This value turns off the <i>Press DEL to run Setup</i> message.
Enabled	This value turns on the <i>Press DEL to run Setup</i> message. This is the default value.

Interrupt 19 Capture

Option	Description
Disabled	This value prevents option ROMs to trap IRQ 19. This is the default value.
Enabled	This value allows option ROMs to trap IRQ 19.

Boot Device Priority

Use this screen to specify the order in the system checks for the device to boot from. To access this screen, select Boot Device Priority on the Boot Setup screen and press <Enter>. The following screen displays:

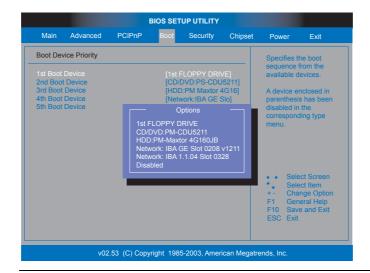


Section 4 Boot Setup, Continued

- 1st Boot Device
- 2nd Boot Device 3rd Boot Device
- 4th Boot Device 5th Boot Device

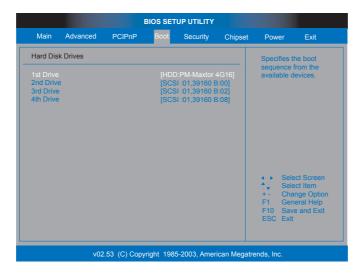
Set the boot device options to determine the sequence in which the computer checks which device to boot from. The settings are Removable Dev., Hard Drive, or CD/DVD. The Optimal and Fail-Safe settings are:

- 1st boot device 1st Removable Device
- 2nd boot device CD/DVD
- 3^{rd} boot device I^{st} HDD
- 4th boot device *Network*
- 5th boot device *Network*



Hard Disk Drives Boot Priority

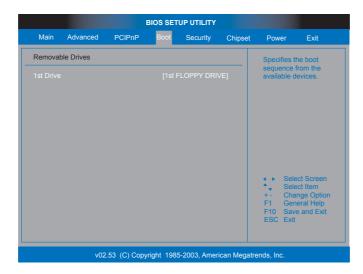
Use this screen to view the hard disk drives in the system. To access this screen, select Hard Disk Drives on the Boot Setup screen and press <Enter>. The following screen displays examples of hard disk drives:





Removable Drives Boot Priority

Use this screen to view the removable drives in the system. To access this screen, select Removable Devices on the Boot Setup screen and press <Enter>. The following screen displays examples of removable devices:

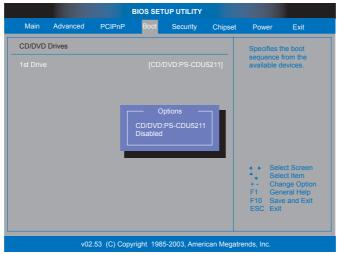




CD/DVD Drives Boot Priority

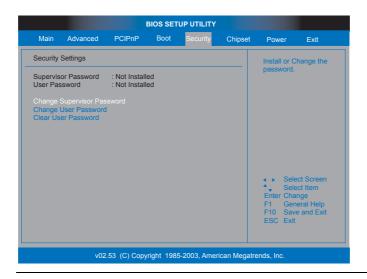
Use this screen to view the ATAPI DVD and CD-ROM drives in the system. To access this screen, select CD/DVD Drives on the Boot Setup screen and press <Enter>. The following screen displays examples of ATAPI CD-ROM and DVD Drives screen:





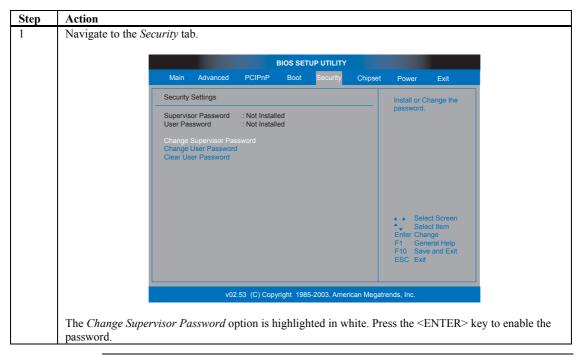
Chapter Three: AMIBIOS Setup 101

Select Security from the main menu of the AMIBIOS Setup Utility. The Security setup screen is displayed below:

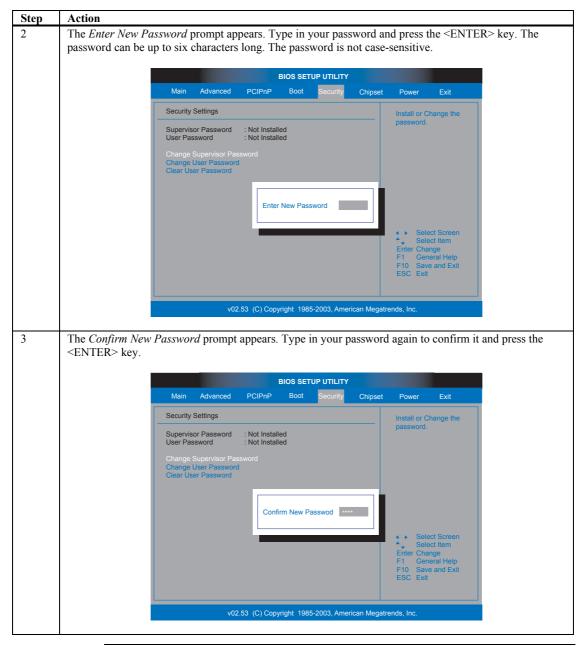


Setting Up a Supervisor Password

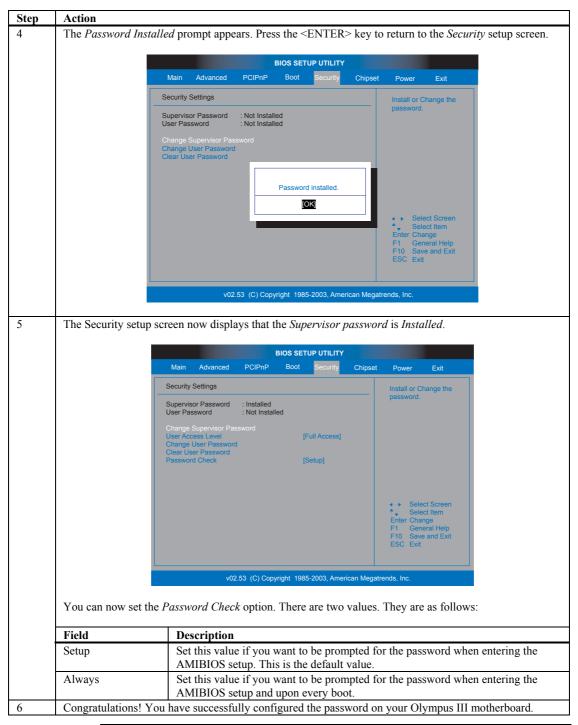
Follow the instructions below to setup a supervisor level password on your Olympus III motherboard.



Setting Up a Supervisor Password, Continued

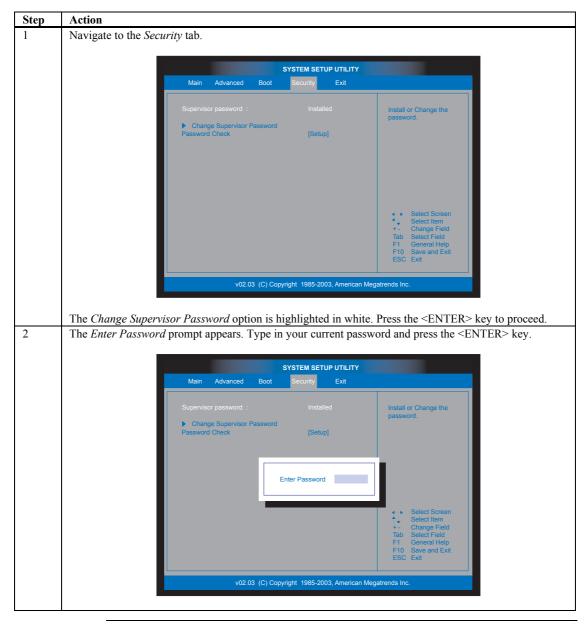


Setting Up a Supervisor Password, Continued

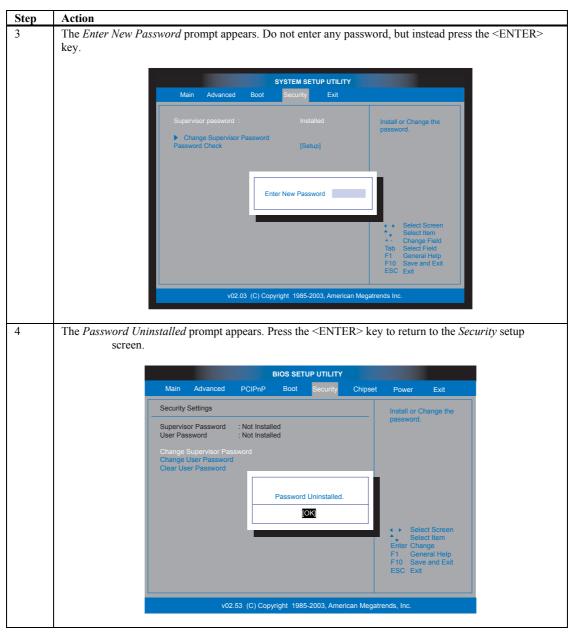


Clearing the Password (via BIOS)

Follow the instructions below to clear the supervisor level password from your Olympus III motherboard.

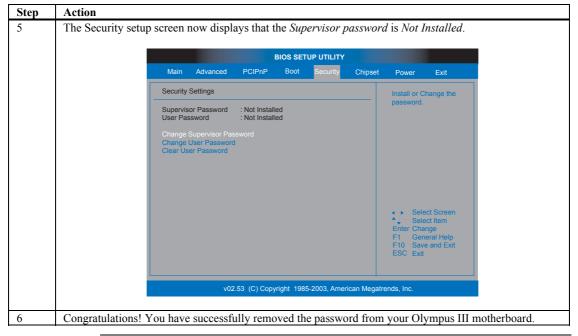


Clearing the Password (via BIOS), Continued



Section 5 Security Setup, Continued

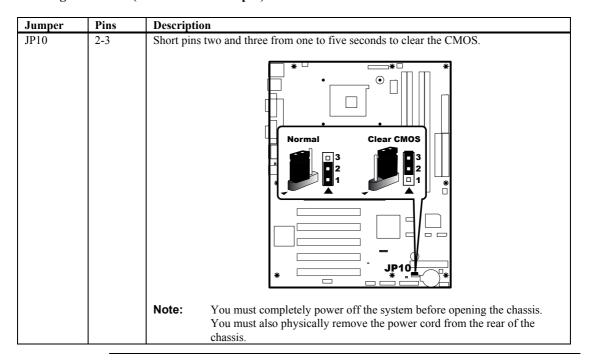
Clearing the Password (via BIOS), Continued



Cont'd

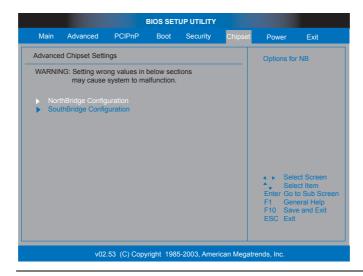
Chapter Three : AMIBIOS Setup 107

Clearing the CMOS (via Hardware Jumper)



Section 6 Chipset Setup

Choose Chipset Setup from the AMIBIOS Setup Utility main menu. The screen is shown below. All Chipset Setup options are described following the screen. This menu allows you to configure the NorthBridge or SouthBridge chipset.



NorthBridge Chipset Configuration



DRAM Frequency

The value represents the performance parameters of the installed memory chips (DRAM). Do not change the value from the factory setting unless you install new memory that has a different performance rating.

Option	Description
266 MHz	This value changes the DRAM frequency to 266 MHz.
333 MHz	This value changes the DRAM frequency to 333 MHz.
400 MHz	This value changes the DRAM frequency to 400 MHz.
Auto	This value allows the BIOS to auto detect the DRAM frequency. This is
	the default value.

Configure DRAM Timing by SPD

SPD (Serial Presence Detect) is located on the memory module. The BIOS can read information coded in SPD during system boot up.

Option	Description
Disabled	This value prevents the SDRAM Timing to be set by the SPD.
Enabled	This value allows the SDRAM Timing to be set by the SPD. This is the
	default value.

Section 6 Chipset Setup, Continued

DRAM Integrity Mode

Option	Description
Disabled	This value prevents ECC (Error Check and Correction) mode from checking DRAM integrity. This is the default value. This can speed the system up if left disabled.
ECC	This value allows ECC (Error Check and Correction) mode to check DRAM integrity. This can impact the system performance.

Memory Hole

Option	Description
Disabled	This value prevents a memory hole being reserved in system memory
	between 15 MB – 16 MB for ISA adapter ROMs. This is the default value.
15 MB – 16 MB	This value reserves the area of system memory between 15 MB – 16 MB
	for ISA adapter ROMs. When this area is reserved, it cannot be cached.

Primary Graphics Adapter

Option	Description
AGP	This value allows the monitor connected to the AGP graphics card to be
	the first monitor to display in multiple monitor situations.
PCI	This value allows the monitor connected to the PCI graphics card to be the
	first monitor to display in multiple monitor situations.

Graphics Aperture Size

Memory mapped and graphics data structures can reside in a Graphics Aperture. This area is similar to a buffer. The BIOS will automatically report the starting address of this buffer to the operating system.

Option	Description
4MB	This value allows 4 MB of memory to be mapped and graphics data
	structures stored in the Graphics Aperture.
8MB	This value allows 8 MB of memory to be mapped and graphics data
	structures stored in the Graphics Aperture.
16MB	This value allows 16 MB of memory to be mapped and graphics data
	structures stored in the Graphics Aperture.
64MB	This value allows 64 MB of memory to be mapped and graphics data
	structures stored in the Graphics Aperture. This is the default value.
128MB	This value allows 128 MB of memory to be mapped and graphics data
	structures stored in the Graphics Aperture.
256MB	This value allows 256 MB of memory to be mapped and graphics data
	structures stored in the Graphics Aperture.

Section 6 Chipset Setup, Continued

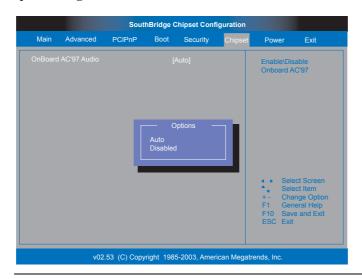
CSA Gigabit Ethernet

Option	Description
Disabled	This value turns off the onboard 10/100/1000 Ethernet port.
Auto	This value allows the use of the onboard 10/100/1000 Ethernet port. It also allows the operating system to turn on and off this port (if applicable). This is the default value.

Onboard VGA Configuration

Option	Description
Disabled	This value prevents the onboard VGA to be used by the system. All system
	resources are freed.
Enabled	This value turns on the onboard VGA chip. This is the default value.

South Bridge Chipset Configuration



Onboard AC'97 Audio

Option	Description
Disabled	This option prevents the use of the onboard audio.
Auto	This option allows the BIOS to determine if the onboard audio is enabled or disabled.

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Section 7 Power Management

Choose Power from the AMIBIOS Setup main menu. All Power Management Setup options are described in this section.



Power Management/APM

This option allows Power Management/APM support. The Optimal and Fail-Safe default settings is Enabled.

Option	Description
Disabled	This option prevents the chipset power management and APM (Advanced
	Power Management) features.
Enabled	This option allows the chipset power management and APM (Advanced
	Power Management) features. This is the default setting.

Video Power Down Mode

This option specifies the power state that the video subsystem enters when the BIOS places it in a power saving state after the specified period of display inactivity has expired. The Optimal and Fail-Safe settings is *Suspend*.

Option	Description
Disabled	This setting prevents the BIOS from initiating any power saving modes
	concerned with the video display or monitor.
Standby	This option places the monitor into standby mode after the specified period
	of display inactivity has expired. This means the monitor is not off. The
	screen will appear blacked out. The standards do not cite specific power
	ratings because they vary from monitor to monitor.
Suspend	This option places the monitor into suspend mode after the specified period of display inactivity has expired. This means the monitor is not off. The screen will appear blacked out. The standards do not cite specific power ratings because they vary from monitor to monitor, but this setting uses less power than Standby mode. This is the default setting.

Hard Disk Power Down Mode

This option specifies the power conserving state that the hard disk drive enters after the specified period of hard drive inactivity has expired. The Optimal and Fail-Safe settings is *Suspend*.

Option	Description
Disabled	This setting prevents hard disk power down mode.
Standby	This option stops the hard disk drives from spinning during a system standby.
Suspend	This option cuts the power to the hard disk drives during a system suspend. This is the default setting.

Standby Time Out

This option specifies the length of time the length of time the system needs to be inactive before it enters standby mode. The Optimal and Fail-Safe default settings is *Disabled*.

Option	Description
Disabled	This option prevents the computer system from entering standby mode.
	This is the default setting.
1Min	This option allows the computer system to enter standby mode after being
	inactive for 1 minute.
5Min	This option allows the computer system to enter standby mode after being
	inactive for 5 minutes.
10Min	This option allows the computer system to enter standby mode after being
	inactive for 10 minutes.

Suspend Time Out (Minute)

This option specifies the length of time the length of time the system needs to be inactive before it enters suspend mode. The Optimal and Fail-Safe default settings is *Disabled*.

Option	Description
Disabled	This setting prevents the system from entering suspend mode. This is the
	default setting.
1Min	This option allows the computer system to enter suspend mode after being
	inactive for 1 minute.
5Min	This option allows the computer system to enter suspend mode after being
	inactive for 5 minutes.
10Min	This option allows the computer system to enter suspend mode after being
	inactive for 10 minutes.

Throttle Slow Clock Ratio

In power management state, BIOS can throttle the CPU clock to reduce power consumption. For example, a throttle ratio of 50% means the clock is turned off 50 percent of the time. The Optimal and Fail-Safe default settings is 50%.

Option	Description
87.5%	This setting allows the BIOS to throttle back the CPU clock to operate 87.5
	percent of the time.
75.0%	This setting allows the BIOS to throttle back the CPU clock to operate 75
	percent of the time.
62.5%	This setting allows the BIOS to throttle back the CPU clock to operate 62.5
	percent of the time.
50%	This setting allows the BIOS to throttle back the CPU clock to operate 50
	percent of the time. This is the default setting.
37.5%	This setting allows the BIOS to throttle back the CPU clock to operate 37.5
	percent of the time.
25%	This setting allows the BIOS to throttle back the CPU clock to operate 25
	percent of the time.
12.5%	This setting allows the BIOS to throttle back the CPU clock to operate 12.5
	percent of the time.

Keyboard & PS/2 Mouse FDC/LPT/COM Ports Primary Master IDE Primary Slave IDE Secondary Master IDE Secondary Slave IDE

Option	Description
Monitor	This value allows the Olympus III motherboard to wake up when one of
	the device selected is used. This is the default value.
Ignore	This value prevents the Olympus III motherboard from waking up when
	the selected device is used.

Section 7 Power Management, Continued

System Thermal

Option	Description
Enabled	This value allows an out-of-threshold thermal reading to generate a power
	management event.
Disabled	This value prevents an out-of-threshold thermal reading to generate a
	power management event.

System Thermal Active Temperature

Option	Description
40C/104F	A temperature reading higher that 40 degrees C and 104 degrees F will generate a power management event. The CPU clock will throttle back a certain percentage as dictated by the value in the Thermal Slow Clock Ratio field.
45C/113F	A temperature reading higher that 45 degrees C and 113 degrees F will generate a power management event. The CPU clock will throttle back a certain percentage as dictated by the value in the Thermal Slow Clock Ratio field.
50C/122F	A temperature reading higher that 50 degrees C and 122 degrees F will generate a power management event. The CPU clock will throttle back a certain percentage as dictated by the value in the Thermal Slow Clock Ratio field.
55C/131F	A temperature reading higher that 55 degrees C and 131 degrees F will generate a power management event. The CPU clock will throttle back a certain percentage as dictated by the value in the Thermal Slow Clock Ratio field.
60C/140F	A temperature reading higher that 60 degrees C and 140 degrees F will generate a power management event. The CPU clock will throttle back a certain percentage as dictated by the value in the Thermal Slow Clock Ratio field. This is the default value.
65C/149F	A temperature reading higher that 65 degrees C and 149 degrees F will generate a power management event. The CPU clock will throttle back a certain percentage as dictated by the value in the Thermal Slow Clock Ratio field.
70C/158F	A temperature reading higher that 70 degrees C and 158 degrees F will generate a power management event. The CPU clock will throttle back a certain percentage as dictated by the value in the Thermal Slow Clock Ratio field.
75C/167F	A temperature reading higher that 75 degrees C and 167 degrees F will generate a power management event. The CPU clock will throttle back a certain percentage as dictated by the value in the Thermal Slow Clock Ratio field.

Cont'd

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Thermal Slow Clock Ratio

This option allows the Thermal Throttle Ratio to be selected. This type of throttling is used to lower power consumption and reduce thermals. The Optimal and Fail-Safe default settings is 50%.

Option	Description
87.5%	This setting allows the BIOS to throttle back the CPU clock to operate 87.5 percent of the time.
75.0%	This setting allows the BIOS to throttle back the CPU clock to operate 75 percent of the time.
62.5%	This setting allows the BIOS to throttle back the CPU clock to operate 62.5 percent of the time.
50%	This setting allows the BIOS to throttle back the CPU clock to operate 50 percent of the time. This is the default setting.
37.5%	This setting allows the BIOS to throttle back the CPU clock to operate 37.5 percent of the time.
25%	This setting allows the BIOS to throttle back the CPU clock to operate 25 percent of the time.
12.5%	This setting allows the BIOS to throttle back the CPU clock to operate 12.5 percent of the time.

Power Button Mode

This option specifies how the power button mounted externally on the computer chassis is used. The Optimal and Fail-Safe default settings is *On/Off*.

Option	Description
On/Off	Pushing the power button turns the computer on or off. This is the default setting. This is the default setting.
Suspend	Pushing the power button places the computer in Suspend mode or Full On power mode.

Restore on AC Power Loss

This function allows you to set whether or not to restart the system after power interruptions.

Option	Description
Power Off	Use this value if you want the system to always power off after a power interruption.
Power On	Use this value if you want the system to always power on after a power interruption.
Last State	Use this value if you want the system to power on if the system was on before a power interruption. If the system was not on, it will stay off when power is restored. This is the default value.

Section 7 Power Management, Continued

Resume on Ring, LAN, PME#, and RTC Alarm

Option	Description
Enabled	This value allows the selected signal to generate a wake event.
Disabled	This value prevents the selected signal to generate a wake event. This is the default value.

Section 8 Exit

Select *Exit* from the main menu of the *AMIBIOS Setup Utility*. All *Exiting* options are described in this section. The *Exit* screen is displayed below:



Cont'd

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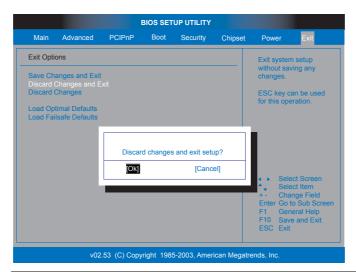
Exit Saving Changes

When you have completed the system configuration changes, select this option to leave the AMIBIOS Setup Utility and reboot the Olympus III motherboard so the new configuration parameters can take effect. Select Exit Saving Changes from the Exit menu and press the <ENTER> key.



Exit Discarding Changes

Select this option to quit the AMIBIOS Setup Utility without making any permanent changes to the configuration. Select Exit Discarding Changes from the Exit menu and press the <ENTER> key.



Discard Changes

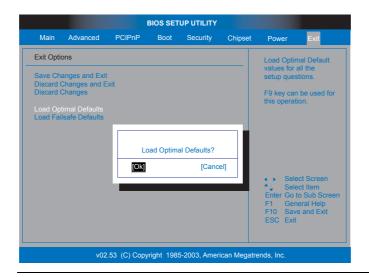
Select *Discard Changes* from the *Exit* menu and press the <ENTER> key.



Load Optimal Defaults

The AMIBIOS Setup Utility automatically sets all options to a complete set of default settings when you select this option. The Optimal settings are designed for maximum system performance, but may not work best for all applications. In particular, do not use the Optimal options if your Olympus III motherboard is experiencing system configuration problems.

Select *Load Optimal Defaults* from the *Exit* menu and press the <ENTER> key.



Load Failsafe Defaults

AMIBIOS automatically sets all AMIBIOS Setup options to a complete set of default settings when you choose this option. The Fail-Safe settings are designed for maximum system stability, but not maximum performance. Choose the Fail-Safe AMIBIOS Setup options if your computer is experiencing system configuration problems. Select Load Fail-Safe Defaults from the Exit menu and press <Enter>.

Click on Ok to load Fail-Safe defaults.



Chapter 4 Programming Flash ROM

All versions of the AMIBIOS use Flash EPROM to store the system BIOS. The advantage of Flash EPROM is the EPROM chip does not have to be replaced to update the BIOS. The end user can actually reprogram the BIOS, using a ROM file supplied by American Megatrends.

This chapter contains two procedures for programming Flash ROM:

- A) Using the <Ctrl> <Home> keys
- B) Using the AMIFlash utility

A) Programming the Flash EPROM Using <Ctrl> <Home>

Step	Action
1	Turn power off.
2	Insert the floppy disk with the S875P.ROM file in the root directory into drive A:.
3	Press and hold the <ctrl> and <home> keys down while turning the power on. Continue to hold the <ctrl> and <home> keys down until the access light on the floppy drive comes on. It may take 10 seconds or more before this light turns on. Since AMIBIOS uses a 4 megabit BIOS, the flashing process may take up to 3 minutes.</home></ctrl></home></ctrl>
4	Release the <ctrl> and <home> keys. AMIBIOS issues a series of beep codes that indicate that the system BIOS ROM file is being updated.</home></ctrl>
5	When the flash ROM has successfully been programmed, the motherboard will reboot.
6	When the motherboard reboots, check the BIOS Release text at the bottom of the first boot screen to make sure that the correct BIOS has been used. Note: Use the <tab> key to switch between the POST screen and the boot logo.</tab>
7	The error message: CMOS Checksum Bad will appear during the first boot after a successful BIOS ROM update. This message indicates that the NVRAM area in the system BIOS has been cleared. AMIBIOS will reconstruct the NVRAM area before the system boots completely, so you can safely ignore this message.
8	<u>Load</u> the optional default and save.

Bootblock Actions

When you reprogram from system boot, the bootblock code performs the following:

Step	Action
1	Reads S875P.ROM from the root directory of the floppy disk in drive A:.
2	Erases the Flash EPROM.
3	Programs the Flash EPROM with the data read from the floppy disk in drive A:.
4	Generates a CPU reset, rebooting the system.

The bootblock part of the Flash EPROM is not programmed. Should you inadvertently open the disk drive door or turn power off to the system while programming the Flash EPROM, the bootblock will be unaffected. Simply turn power back on and begin the Flash ROM programming process again.

Programming the Flash ROM, Continued

S875P.ROM

S875P.ROM resides on a floppy disk and contains the updated main BIOS code. American Megatrends will provide this file when the AMIBIOS for the AMIBIOS must be updated.

 ${\tt S875P.ROM}$ must be present in the root directory of the floppy disk before the onboard Flash EPROM can be reprogrammed. The file that has the main BIOS code must be named S875P.ROM.

Beep Codes

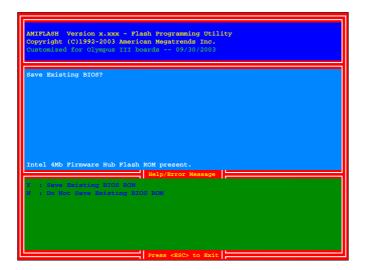
The bootblock code produces a series of beeps during Flash ROM programming to: signify completion of a step (as shown on the previous page), or to signal an error. Error beeps are arranged in a coded sequence and have different meanings depending on when they occur. The error beep codes and when they can occur are:

Number of	Description
Beeps	
1	Insert diskette in floppy drive A:.
2	The S875P.ROM file was not found in the root directory of the diskette in floppy drive A:.
3	Base memory error.
4	Flash program successful.
5	Floppy read error.
6	Keyboard controller BAT command failed.
7	No Flash EPROM detected.
8	Floppy controller failure.
9	Boot Block BIOS checksum error.
10	Flash erase error.
11	Flash Program error.
12	S875P.ROM file size error.

B) Programming the Flash EPROM Using the AMIFlash Utility

AMIFlash utility runs in DOS only.

The main menu screen is shown below. You are prompted to save or delete the existing BIOS. Enter *Y* if you want to save the existing BIOS ROM, or *N* if you do not.



B) Programming the Flash EPROM Using the AMIFlash Utility, cont'd

Enter the filename, ${\tt S875P.ROM}$, that you want to save the existing BIOS to and press <Enter>.

```
AMIFLASH Version x.xxx - Flash Programming Utility
Copyright (0)1992-2003 American Megatrends Inc.
Customized for Olympus III boards -- 89/30/2003

Save Existing BIOS? y
Enter Filename : s875p.bak

Intel 4Mb Fixmware Hub Flash ROM present.

Help/Error Message

Intel 4Mb Fixmware Hub Flash ROM present.

Help/Error Message

Intel 4Mb Fixmware Hub Flash ROM present.

Help/Error Message

Intel 4Mb Fixmware Hub Flash ROM present.

Help/Error Message

Intel 4Mb Fixmware Hub Flash ROM present.

Help/Error Message

Intel 4Mb Fixmware Hub Flash ROM present.

Help/Error Message

Intel 4Mb Fixmware Hub Flash ROM present.

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Intel 4Mb Fixmware Hub Flash ROM present.

Help/Error Message

Intel 4Mb Fixmware Hub Flash ROM present.

Help/Error Message

Intel 4Mb Fixmware Hub Flash ROM present.

Help/Error Message

Intel 4Mb Fixmware Hub Flash ROM present.
```

Enter the BIOS filename from which the Flash ROM will be programmed and press <Enter>.

```
AMIFLASH Version x.xxx - Flash Programming Utility
Copyright (c)1992-2003 American Magatrends Inc.
Customized for Olympus III boards -- 09/30/2003

Save Existing BIOS? y
Enter Filename : s875p.bak
Enter BIOS Filename:

Intel 4Mb Firmware Hub Flash ROM present.

Help/Error Message

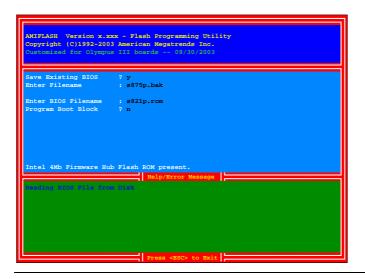
Linear tars Exist Filename; November Wiles Will be groupedmann.
The Polympus International Vilename National Company.
The Polympus and With A CHARLEY.
```

B) Programming the Flash EPROM Using the AMIFlash Utility, cont'd

To enable this program to update bootblock code, perform the following procedure:

Step	Action
1	Turn the system off.
2	Turn the system on.
3	Boot to DOS using a bootable DOS disk or go to DOS mode directly from the
	operating system.
4	Run AMIFlash.
5	At the prompt "Program Boot Block?", type Y and press <enter>.</enter>
6	After the boot block is programmed, reboot the system.
7	Turn the power off.

Enter Y if you want to program the boot block or N if you do not want to program the boot block.



Bootblock Code Checkpoint Codes

Code	Description
E0h	Verify the Boot Block BIOS checksum. Disable the internal cache, DMA, and interrupt controllers.
	Initialize the system timer. Start memory refresh.
E1h	Initialize the chipset registers. Set the BIOS size to 128K. Make the 512 KB base memory available.
E2h	Test the base 64 KB of system memory. Send the BAT command to the keyboard controller. Make sure that <ctrl> <home> was pressed. Verify the main system BIOS checksum.</home></ctrl>
E3h	The main system BIOS is good. Transfer control to the main system BIOS.
E4h	Start the memory test.
E5h	The memory test is over. Initialize the interrupt vector table.
E6h	Initialize the DMA and interrupt controllers.
E7h	Determine the CPU internal clock frequency.
E8h	Initialize the I/O chipset, if any.
E9h	Program the CPU clock-dependent chip set parameters.
EAh	Enable the timer and the floppy diskette interrupt. Enable the internal cache. Copy the boot block BIOS and pass control to the boot block BIOS in the 0000h segment.
EDh	Initialize the floppy drive.
EEh	Look for a diskette in drive A:. Read the first sector of the diskette.
EFh	Floppy read error.
F0h	Search for S875P.ROM in the root directory of the floppy diskette in drive A:.
F1h	The S875P.ROM file is not in the root directory.
F2h	Read the FAT table. Analyze the FAT to find the clusters occupied by the S875P.ROM .
F3h	Start reading the S875P.ROM file, cluster by cluster.
F4h	The S875P.ROM file is not the correct size.
F5h	Disable the internal cache. Raise the Vpp. Enable Flash write and reset the Flash ROM.
FBh	Detect the flash type.
FCh	Start erasing flash blocks.
FDh	Program the Flash ROM in the E0000-EFFFFh region.
FEh	Start programming Flash at F0000-FFFFF region.
FFh	Flash programming is successful. The system reboots.

Chapter 5 Deleting a Password

Overview

If you forget the passwords you setup through AMIBIOS Setup, the only way you can restart the system is to erase the system configuration information where the passwords are stored. System configuration data is stored in CMOS RAM, a type of memory that consumes very little power.

Erase Old Password

You can drain CMOS RAM power via JP10 on the motherboard. JP10 is a 3-pin berg with a default setting of pins 1 and 2 shorted by a jumper. Perform the following steps to erase the old password.

<u> ∕!</u> Important

Make sure you are properly grounded before performing the following procedure. You must be certain that no electrostatic discharge (ESD) occurs. ESD can ruin your motherboard. Wear an antistatic wristband attached to a ground. See "Avoid Static Electricity" on the following page.



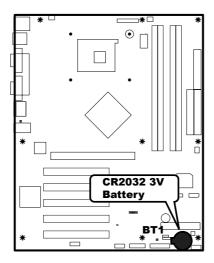
Step	Action
1	Turn the system power off and remove the system cover.
2	Short pins two and three on JP10 from one to five seconds to clear the CMOS. Normal Clear CMOS 2 2 1 3 1 3 1 3 1 4 1 1 1 1 1 1 1 1 1 1 1 1
3	Turn on system power again. Since you drained power from CMOS RAM, all system configuration information has been erased. You must now re-enter the system configuration information by running AMIBIOS Setup.

Appendix A Battery Replacement

Battery

The Olympus III motherboard BIOS retains CMOS settings when powered off. It does this by power supplied from a Lithium battery. The operating life of the battery ranges from two (2) to five (5) years, depending on how you use the system.

This battery location is shown in the illustration below:



American Megatrends suggests that you replace this battery with a coin-type CR2032 Lithium Manganese Dioxide battery.

Caution

Danger of explosion if the battery is incorrectly replaced. Replace only with a coin-type CR2032 Lithium Manganese Dioxide battery. Dispose of the battery according to the battery manufacturer's instructions.

Appendix B AMIBIOS Beep Codes

Number of Beeps	Error Type
1	Refresh Failure
2	Parity Error
3	Base 64K Memory Failure
4	Timer Not Operational
5	Processor Error
6	Not Available. Usually, 8042 – Gate A20 Failure
7	Processor Exception Interrupt Error
8	Display Memory Read/Write failure
9	ROM Checksum Error
10	CMOS Shutdown Register Read/Write
11	Cache Memory Bad

Except for beep code #8, these codes are always fatal.

Troubleshooting AMIBIOS Beep Codes

- For 1 beep, 2 beeps, or 3 beeps try reseating the memory first. If the error still occurs, replace the memory with known good chips.
- For 4 beeps, 5 beeps, 7 beeps, or 10 beeps the system board must be sent in for repair.
- 8 beeps indicate a memory error on the video adapter. Replace the video card or the memory on the video card.
- 9 beeps indicate faulty BIOS chip(s). It is not likely that this error can be corrected by reseating the chips. Consult the motherboard supplier or an AMI product distributor for replacement part(s).

Troubleshooting AMIBIOS Beep Codes, Continued

- If no beeps are heard and no display is on the screen, The first thing to check is the power supply. Connect an LED to the POWER LED connection on the motherboard. If this LED lights and the drive(s) spin up then the power supply will usually be good.
- Next, inspect the motherboard for loose components. A loose or missing CPU, BIOS chip, or Chipset chip will cause the motherboard not to function.
- Next, eliminate the possibility of interference by bad or improperly setup I/O cables by removing all cards and cables except the video debug cable. The system should at least power up and wait for a drive time-out. Insert the card and cables back into the system one at a time until the problem happens again. When the system does nothing, the problem will be with the last expansion card or cable that was put in.
- If the above suggestions fail to cause any change in the dysfunction of the system, the motherboard must be returned for repair.

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