

# CHAPTER 1 INTRODUCTION

## SYSTEM OVERVIEW

The S4967 Rev:2B.31 486 Cache system board is 2/3 Baby AT-sized, fully PC/AT compatible and offers outstanding performance and features.

With 128K/256K/512K/1M cache memory on board, this system board is really a high speed machine that is well suited for building advanced personal computers or workstations.

The S4967 Rev:2B.31 486 Cache system board is designed with the SiS 85C496/85C497 chipset which are highly integrated. With this chipset, there are only a few discrete devices required, which allows 4 memory banks to be placed on the board. The size of the memory can be scaled from 1 MB up to 255 MB.

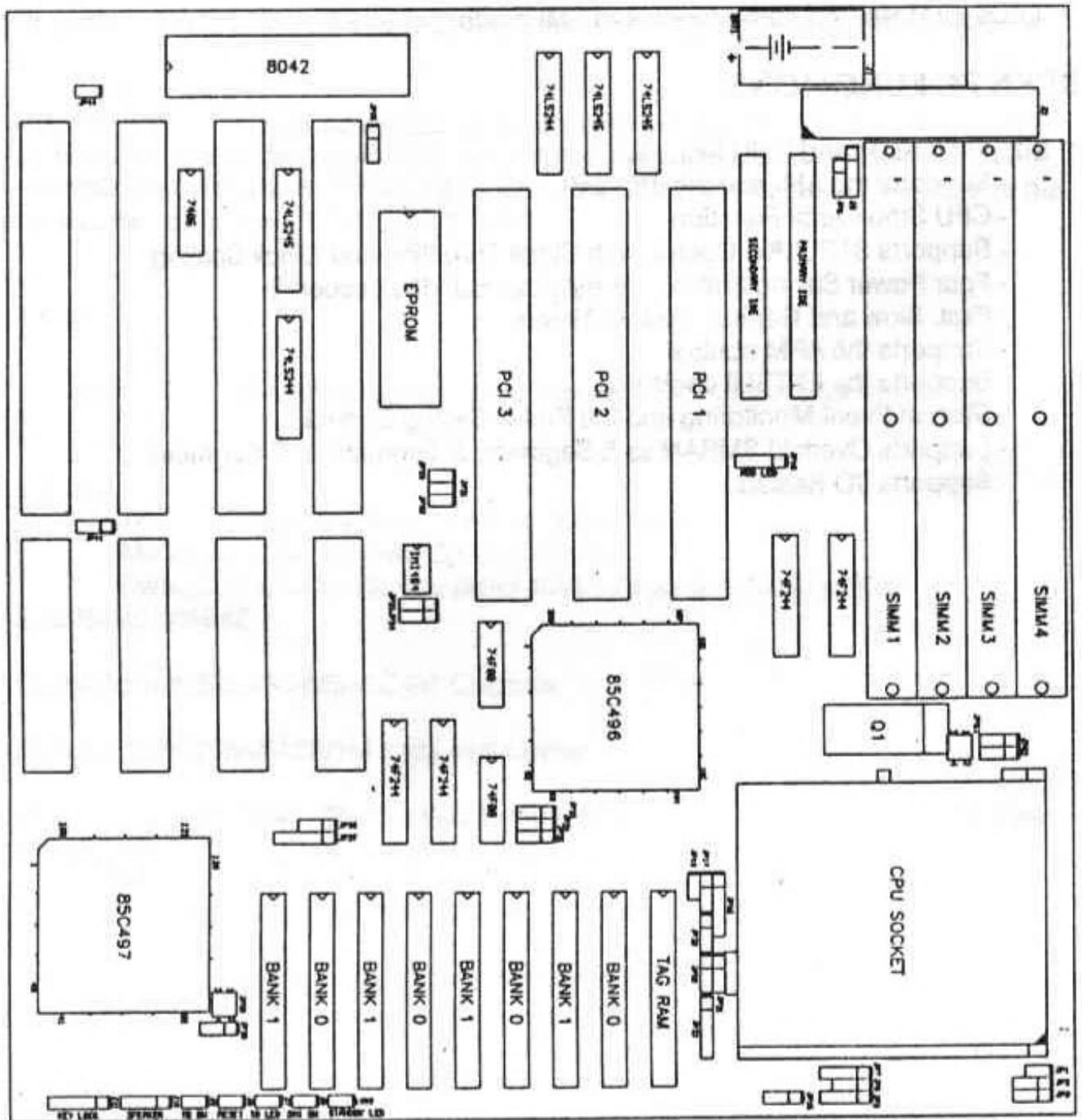
## FEATURES

The S4967 Rev:2B.31 486 Cache system board supports (or includes) the following features:

- \* Support  
Intel 486SX/SX2/DX/DX2,DX4(3.45V),P24D,P24T  
AMD DX,DX2/DX4(NV8T),DX2/DX4(SV8B)  
Cyrix SX/DX/DX2,DX2-V66/V80(3.45V),DX4(3.45V),I5x86(3.45V)  
in 25/33/40/50MHZ
- \* Designed with SiS 85C496/85C497 Chipsets
- \* Support 128K/256K/512K/1M 2nd Level Cache
- \* Support 4 DRAM Banks. The DRAM can be built with either Single-Sided or Double-Sided SIMMs. The maximum memory is up to 255MB
- \* Software-controlled shadow RAM for system and/or video BIOS
- \* Three 32-bit PCI local bus slots, four 16-bit expansion slots

# CHAPTER 2 SYSTEM BOARD LAYOUT

## Placement of the S486 Rev:2B.31



SILKSCREEN FOR COMPONENT SIDE

# CHAPTER 3 HARDWARE CONFIGURATION

Before the system is ready to operate, the hardware must be configured to allow for various functions within the system. To configure the S4967 Rev:2B.31 Cache system board is a simple task, only a few jumpers, connectors, and sockets needs to be selected.

## CACHE MEMORY SOCKETS

The S4967 Rev:2B.31 Cache system board supports 2 banks of SRAM which provides either 128/256K/512K/1MB of cache memory. The following table lists the detailed information.

Cache Size	Bank 0	Bank 1	Tag
128 K	four 32K x 8		one 8K x 8
256 K	four 32K x 8	four 32K x 8	one 16K x 8 or 32K x 8
256 K	four 64K x 8		one 16K x 8 or 32K x 8
512 K	four 64K x 8	four 64K x 8	one 32K x 8
512 K	four 128K x 8		one 32K x 8
1MB	four 128K x 8	four 128K x 8	one 64K x 8

The corresponding bank to part identification are as follows:

- Bank 0 -- U9, U11, U19, U24
- Bank 1 -- U10, U14, U20, U25
- Tag -- U8

CACHE Size Select						
	128K	256K	256K	512K	512K	1MB
JP23 JP24 JP25						
JP36 JP37						
TAG	8KX8	32KX8	32KX8	32KX8	32KX8	64KX8
BANK 0 U9,U11, U19,U24	32KX8	32KX8	64KX8	64KX8	128KX8	128KX8
BANK 1 U10,U14, U20,U25	X	32KX8	X	64KX8	X	128KX8

Table 3-1 Cache Size Select

Cache size	Cacheable DRAM size (8 bit tag)	Cacheable DRAM size (7 bit tag)
64K byte	16M byte	8M byte
128K byte	32M byte	16M byte
256K byte	64M byte	32M byte
512K byte	128M byte	64M byte
1M byte	255M byte	128M byte

**Table 3-2 Cache Size Options**

Processor Type	L1 Cache Mode	L2 Cache Mode
486SX/DX/DX2/ DX4/SL-Enhanced	WT	WT/WB
P24D/P24T	WT/WB	WT/WB
Cyrix M7/DX4/M1sc	WT/WB	WT/WB
Am486DXL/DX2 DX4-100 NV8T	WT	WT/WB
Am486DX4-100/120 SV8B	WT/WB	WT/WB

**Table 3-3 L1/L2 Cache Configurations**

Cycle Definition	Total Clocks at Host Interface			
	25MHz	33MHz	40MHz	50MHz
Host-to-Memory				
Single-Read (L2 Cache Hit)	2	2	2	2
Single-Read (L2 Cache Miss)	3	4	5	6
*Burst-Read (L2 Cache Hit)	2-1-1-1	2-1-1-1	3-2-2-2	3-2-2-2
Burst-Read (L2 Cache Miss)	3-2-2-2	4-3-3-3	5-4-4-4	6-5-5-5
Single-Write (L2 Cache Hit)	2	2/WB,3/WT	3/WB,4/WT	3/WB,5/WT
Single-Write (L2 Cache Miss)	2	3	4	5
*Burst-Write (L2 Cache Hit)	2-1-1-1/WB 3-2-2-2/WT	2-1-1-1/WB 3-2-2-2/WT	3-2-2-2/WB 4-3-3-3/WT	3-2-2-2/WB 5-4-4-4/WT
Burst-Write (L2 Cache Miss)	3-2-2-2	3-2-2-2	4-3-3-3	5-4-4-4

**Table 3-4 L2 Cache/DRAM Performance Options**

## SHADOW CACHEABLE

UMB (Upper Memory Block) which is not main memory area is by default non-cacheable. However, once shadowed, the RAM segments 0C0000-0FFFFFFh can be further cached in Level 2 and Level 1 cache. Each 32K memory segments can be individually enabled to be cacheable by both 85C496's secondary level cache and CPU's internal cache.



# RAM SIMM SOCKETS

The S4967 Rev:2B.31 Cache system board will support 4 DRAM banks, Bank 0 and Bank 1 Bank 2 and Bank 3 in SIMM sockets use 72-pin SIMM. DRAM type can be 256K, 512K, 1M, 2M, 4M, or 16M by 32/36 bits Single side or Double side Fast Page Mode and faster than 80ns.

With the use of 256K, 512K, 1M, 2M, 4M or 16M DRAM modules, 1M and upto 255 M of local memory can be attained. The installation of DRAM SIMMs is "Table-free", which allows the SIMMs be installed into any slot location and any combinations.

## CPU INSTALLATION :

### CPU Voltage Select

CPU Voltage Select					
	3.3V	3.45V	3.6V	4.0V	5V
JP61					
JP62					


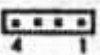

































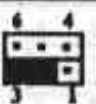
### CPU CLK Select

CPU CLK Select				
	25MHZ	33MHZ	40MHZ	50MHZ
JP29 JP31 JP32				

# CPU Type Select

Intel CPU								
	486SX	486DX	SL Enhance 486SX	SL Enhance 486DX	SL Enhance 486DX2	P24T	P24D	P24C
JP7								
JP8								
JP9								
JP15								
JP16								
JP17								
JP18								
JP20								
JP21								
JP22								
JP61								
JP62								

# AMD CPU

	Am486DXL	Am486DX2/DX4 -66/80/100 NV8T	Am486DX2/DX4 -66/80/100/120 SV8B
JP7			
JP8			
JP9			
JP15			
JP16			
JP17			
JP18			
JP20			
JP21			
JP22			
JP61			
JP62			

# Cyrrix CPU

	486DX (5V)	486DX2 (5V)	486DX2 (3V)	486DX4 (3V)	Misc (CX5X86)
JP7					
JP8					
JP9					
JP15					
JP16					
JP17					
JP18					
JP20					
JP21					
JP22					
JP61					
JP62					



## JUMPER :

(1) JP1 CX486S2 Select

<u>Pin #</u>	<u>Assignment</u>
SHORT	CX486S2 only
OPEN	OTHER CPU

(2) JP2 CLKMUL/WB\_WT Select

\* FOR AMD CPU :

<u>Pin #</u>	<u>Assignment</u>
1 - 2	3X
2 - 3	2X
OPEN	3X

\* FOR P24D CPU :

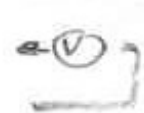
<u>Pin #</u>	<u>Assignment</u>
1 - 2	Write-Back
2 - 3	Write-Through

(3) JP3 P24T WB\_WT Select

<u>Pin #</u>	<u>Assignment</u>
1 - 2	Write-Back
2 - 3	Write-Through

? (4) JP28 BIOS Type Selection

<u>Pin#</u>	<u>Assignment</u>
1 - 2,5 - 6	FLASH BIOS
2 - 3,4 - 5	EPROM BIOS




(5) JP33 PCI CLK Select

<u>Pin #</u>	<u>Assignment</u>
1 - 2	PCICLK = CPUCLK
2 - 3	PCICLK = 1/2 CPUCLK

(6) JP34 CPU CLK Delay Select

<u>Pin #</u>	<u>Assignment</u>
1 - 2	Normal
2 - 3	CPUCLK Delay



(7) JP6/JP35 RTC Discharge Select

<u>Pin #</u>	<u>Assignment</u>
1 - 2	Normal
2 - 3	Discharge RTC CMOS

**NOTE :** When you can't enter system setup, you must use JP6/JP35 to discharge RTC CMOS.

(8) JP38 GREEN control (SMOUT connector)

<u>Pin#</u>	<u>Assignment</u>
1 - 2	GREEN Outlet connector 1 (For Green Power-Supply)
3 - 4	GREEN Outlet connector 2 (For Green Power-Supply)

(9) JP39 Stop CPU Clock control

<u>Pin#</u>	<u>Assignment</u>
1 - 2	CPUCLK down by chipset
2 - 3	CPUCLK down by CPU (AMD486DXL is not included)

(10) JP41 DREQ signal control

<u>Pin #</u>	<u>Assignment</u>
1 - 2	DREQ pull-up
2 - 3	DREQ pull-down

(11) JP44 MONITOR Type selection

<u>Pin#</u>	<u>Assignment</u>
SHORT	COLOR Monitor
OPEN	MONO Monitor

(12) JP50 DX4/5x86/AmDX4 SV8B CLKMUL

<u>Pin#</u>	<u>Assignment</u>
1 - 2	2.5X(For DX4 only)
2 - 3	2X(DX4/5x86/AmDX4 SV8B)
OPEN	3X(DX4/5x86/AmDX4 SV8B)

## CONNECTORS :

### (1) BT1A Rechargeable Battery

<u>Pin #</u>	<u>Assignment</u>
1	Battery Positive
2	Ground

### (2) J1 Keyboard

<u>Pin #</u>	<u>Assignment</u>
1	Keyboard Clock
2	Keyboard Data
3	No Connection
4	Ground
5	+ 5V DC

### (3) J2 Power Connector

<u>Pin #</u>	<u>Assignment</u>
1	Power Good
2	+ 5V DC
3	+ 12V DC
4	- 12V DC
5	Ground
6	Ground
7	Ground
8	Ground
9	- 5V DC
10	+ 5V DC
11	+ 5V DC
12	+ 5V DC

### (4) J3 4.5V External Battery

<u>Pin #</u>	<u>Assignment</u>
1	Battery Positive
2	No Connection
3	Ground
4	Ground

### (5) J6 Hardware SMI Break Switch

<u>Pin#</u>	<u>Assignment</u>
SHORT	Immediately into SMI mode
OPEN	Normal operation