SUPERO®

SUPER S2DL3 SUPER 370DL6 SUPER 370DL3 SUPER 370DLE

USER'S MANUAL

Revision 1.0

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Preface

About This Manual

This manual is written for system integrators, PC technicians and knowledgeable PC users. It provides information for the installation and use of the SUPER S2DL3/370DL6/370DL3/370DLE motherboard. The SUPER S2DL3 supports single or dual Pentium® III Xeon 400-800 MHz processors with a 133/100 MHz front side bus. The SUPER 370DL6/370DL3/370DLE supports single or dual Pentium® III 500-933 MHz FCPGA processors with a 133/100 MHz front side bus. Please refer to the support section of our web site (http://www.supermicro.com/TechSupport.htm) for a complete listing of supported processors.

Pentium III FCPGA (Flip Chip Pin Grid Array) processors are housed in a 370-pin socket, which is the new standard that will support future Intel processors. Xeon processors are based on the "Slot 2" architecture.

Manual Organization

Chapter 1 includes a checklist of what should be included in your mainboard box, describes the features, specifications and performance of the SUPER S2DL3/370DL6/370DL3/370DLE mainboard and provides detailed information about the chipset.

Chapter 2 begins with instructions on handling static-sensitive devices. Read this chapter when you want to install the processor and DIMM memory modules and when mounting the mainboard in the chassis. Also refer to this chapter to connect the floppy and hard disk drives, SCSI drives, the IDE interfaces, the parallel and serial ports and the twisted wires for the power supply, the reset button, the keylock/power LED, the speaker and the keyboard.

If you encounter any problems, see **Chapter 3**, which describes troubleshooting procedures for the video, the memory and the setup configuration stored in CMOS. For quick reference, a general FAQ [Frequently Asked Questions] section is provided. Instructions are also included for contacting technical support. In addition, you can visit our web site at www.supermicro.com/techsupport.htm for more detailed information.

Chapter 4 includes an introduction to BIOS and provides detailed information on running the CMOS Setup utility.

Appendix A gives information on BIOS error beep codes and messages.

Appendix B provides post diagnostic error messages.

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Chapter 1 Introduction

1-1 Overview

Checklist

Congratulations on purchasing your computer motherboard from an acknowledged leader in the industry. Supermicro boards are designed with the utmost attention to detail to provide you with the highest standards in quality and performance.

Please check that the following items have all been included with your motherboard. If anything listed here is damaged or missing, contact your retailer

- One (1) Supermicro Mainboard
- One (1) ribbon cable for IDE devices
- One (1) floppy ribbon cable for (1) 5.25-inch floppy and (2) 3.5-inch floppy drives
- One (1) I/O backpanel shield

SCSI Accessories (S2DL3, 370DL6 and 370DL3 only)

- One (1) 50-pin Ultra SCSI cable
- One (1) 68-pin LVD SCSI cable
- One (1) set of SCSI driver diskettes
- One (1) SCSI manual
- One (1) Supermicro CD or diskettes containing drivers and utilities
- One (1) User's/BIOS Manual

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Notes

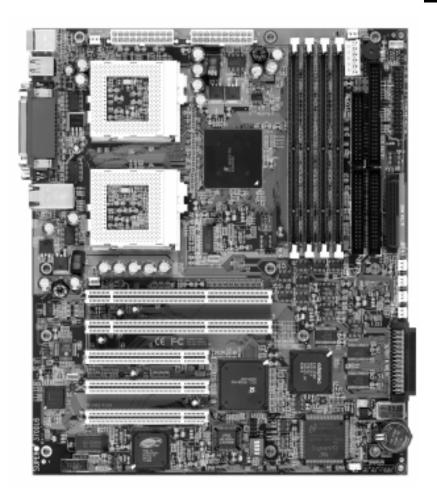
SUPER S2DL3

Figure 1-1. SUPER S2DL3 Image



SUPER 370DL6

Figure 1-2. SUPER 370DL6 Image



SUPER 370DL3

Figure 1-3. SUPER 370DL3 Image



SUPER 370DLE

Figure 1-4. SUPER 370DLE Image

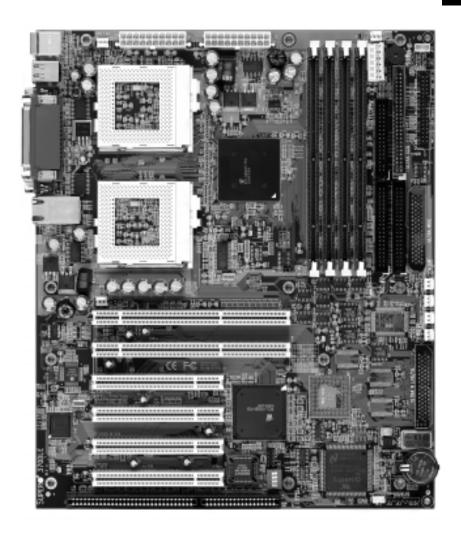
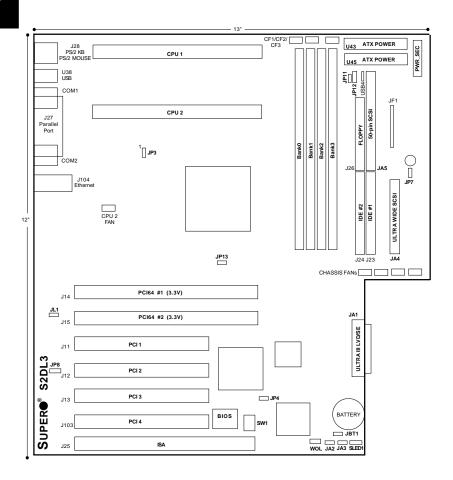


Figure 1-5. SUPER S2DL3 Layout (not drawn to scale)



Also see the figure on page 2-7 for the locations of the I/O ports and 2-8 for the Front Control Panel (JF1) connectors.

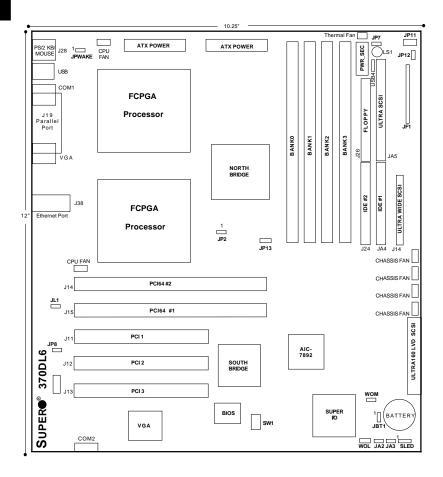
S2DL3 Quick Reference

<u>Jumpers</u>	<u>Description</u>	Default Setting
JA2	SCSI Term. (p. 2-17)	Open (Enabled)
JA3	SCSI Term. (p. 2-17)	Open (Enabled)
JBT1	CMOS Clear (p. 2-16)	Pin 1-2 (Normal)
JP2	Front Side Bus Speed (p. 2-16)	Pin 1-2 (CPU Select
JP4	Manufacturer's Setting	Open
JP7	Overheat Alarm (p. 2-17)	Closed (Enabled)
JP8	LAN Enable/Disable (p. 2-17)	Open (Enabled)
JP12	3rd P/S Failure Alarm (p. 2-18)	Open (Disabled)
JP13	Speed for 64-bit PCI	Open (66 MHz)

DIP Switches	<u>Description</u>	Default Setting
SW1 (1-4)	CPU Core/Bus Ratio	(see p. 2-15)
SW2	Manufacturer's Setting	(Open)

<u>Connectors</u>	<u>Description</u>
BANK0-BANK3	Memory (RAM) Slots (p. 2-6)
CHASSIS FAN (4 ea)	Chassis Fan Header (p. 2-12)
COM1/COM2	COM1/COM2 Serial Port Connector (p. 2-12)
CF1/CF2	CPU1/CPU2 Fan Header (p. 2-12)
CF3	Thermal Control Fan Header (p. 2-12)
J23, J24	IDE Hard Disk Drive Connectors (p. 2-19)
J26	Floppy Disk Drive Connector (p. 2-19)
J27	Parallel Printer Port (p. 2-18)
J28	PS/2 Keyboard/Mouse (p. 2-12)
J104	Ethernet Port
JA1	Ultra160 LVD SCSI Connector (p. 2-21)
JA4	Ultra Wide SCSI Connector (p. 2-20)
JA5	Ultra SCSI Connector (p. 2-20)
JF1	Front Control Panel (p. 2-7)
JP11	Power Supply Fail Header (p. 2-14)
P1	Primary ATX Power Connector (p. 2-9)
P2	Primary ATX Power Connector (p. 2-9)
PWR_SEC	Secondary ATX Power Connector (p. 2-9)
SLED1	SCSI LED header (p. 2-14)
U38	Universal Serial Bus Ports (p. 2-13)
USB4 (J105)	Extra USB Header(p.2-13)
WOL	Wake-on-LAN Header (p. 2-13)
WOM	Wake-on-Modem Header (p. 2-13)

Figure 1-6. SUPER 370DL6 Layout (not drawn to scale)



Also see the figure on page 2-7 for the locations of the I/O ports and 2-8 for the Front Control Panel (JF1) connectors.

370DL6 Quick Reference

<u>Jumpers</u>	<u>Description</u>	Default Setting
JA2	SCSI Term. (p. 2-17)	Open (Enabled)
JA3	SCSI Term. (p. 2-17)	Open (Enabled)
JBT1	CMOS Clear (p. 2-16)	Pin 1-2 (Normal)
JP2	Front Side Bus Speed (p. 2-16)	Pin 1-2 (CPU Select)
JP4	Manufacturer's Setting	Open
JP7	Overheat Alarm (p. 2-17)	Closed (Enabled)
JP8	LAN Enable/Disable (p. 2-17)	Open (Enabled)
JP12	3rd P/S Failure Alarm (p. 2-18)	Open (Disabled)
JP13	Speed for 64-bit PCI	Open (66 MHz)

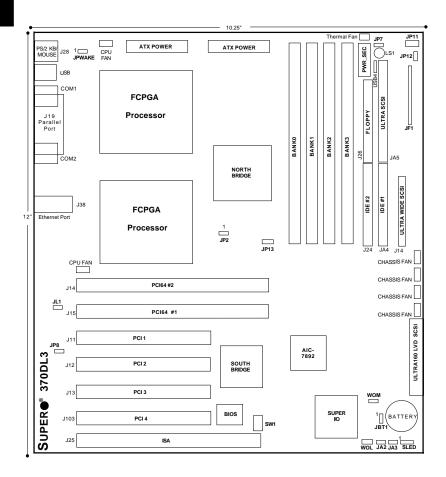
DIP Switches	<u>Description</u>	Default Setting
SW1 (1-4)	CPU Core/Bus Ratio	(see p. 2-15)
SW2	Manufacturer's Setting	(Open)

Description

Connectors

BANK0-BANK3	Memory (RAM) Slots (p. 2-6)
CF3	Thermal Control Fan Header (p. 2-12)
CHASSIS FAN (4 ea)	Chassis Fan Header (p. 2-12)
COM1	COM1 Serial Port Connector (p. 2-12)
COM2	COM2 Serial Port Header (p. 2-12)
CPU FAN (2 ea)	CPU1/CPU2 Fan Header (p. 2-12)
J23, J24	IDE Hard Disk Drive Connectors (p. 2-19)
J26	Floppy Disk Drive Connector (p. 2-19)
J27	Parallel Printer Port (p. 2-18)
J28	PS/2 Keyboard/Mouse (p. 2-12)
J104	Ethernet Port
JA1	Ultra160 LVD SCSI Connector (p. 2-21)
JA4	Ultra Wide SCSI Connector (p. 2-20)
JA5	Ultra SCSI Connector (p. 2-20)
JF1	Front Control Panel (p. 2-7)
JP11	Power Supply Fail Header (p. 2-14)
P1	Primary ATX Power Connector (p. 2-9)
P2	Primary ATX Power Connector (p. 2-9)
PWR_SEC	Secondary ATX Power Connector (p. 2-9)
SLED1	SCSI LED header (p. 2-14)
U38	Universal Serial Bus Ports (p. 2-13)
USB4(J105)	Extra USB Header (p. 2-13)
VGA	Onboard VGA Monitor Connector
WOL	Wake-on-LAN Header (p. 2-13)
WOM	Wake-on-Modem Header (p. 2-13)

Figure 1-7. SUPER 370DL3 Layout (not drawn to scale)



Also see the figure on page 2-7 for the locations of the I/O ports and 2-8 for the Front Control Panel (JF1) connectors.

370DL3 Quick Reference

<u>Jumpers</u>	<u>Description</u>	Default Setting
JA2	SCSI Term. (p. 2-17)	Open (Enabled)
JA3	SCSI Term. (p. 2-17)	Open (Enabled)
JBT1	CMOS Clear (p. 2-16)	Pin 1-2 (Normal)
JP2	Front Side Bus Speed (p. 2-16)	Pin 1-2 (CPU Select
JP4	Manufacturer's Setting	Open
JP7	Overheat Alarm (p. 2-17)	Closed (Enabled)
JP8	LAN Enable/Disable (p. 2-17)	Open (Enabled)
JP12	3rd P/S Failure Alarm (p. 2-18)	Open (Disabled)
JP13	Speed for 64-bit PCI	Open (66 MHz)

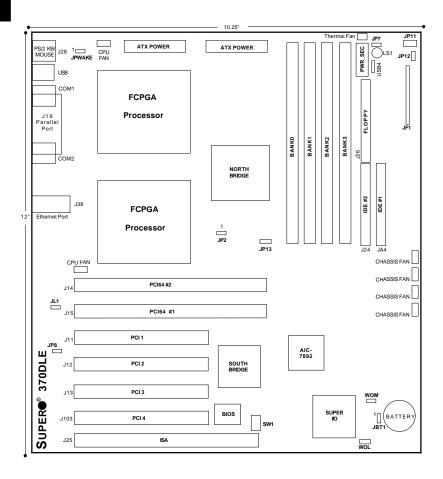
DIP Switches	<u>Description</u>	Default Setting
SW1 (1-4)	CPU Core/Bus Ratio	(see p. 2-15)
SW2	Manufacturer's Setting	(Open)

Description

Connectors

<u> </u>	<u>=</u>
BANK0-BANK3	Memory (RAM) Slots (p. 2-6)
CF3	Thermal Control Fan Header (p. 2-12)
CHASSIS FAN (4 ea)	Chassis Fan Header (p. 2-12)
COM1	COM1/COM2 Serial Port Connector (p. 2-12)
CPU FAN (2 ea)	CPU1/CPU2 Fan Header (p. 2-12)
J23, J24	IDE Hard Disk Drive Connectors (p. 2-19)
J26	Floppy Disk Drive Connector (p. 2-19)
J27	Parallel Printer Port (p. 2-18)
J28	PS/2 Keyboard/Mouse (p. 2-12)
J104	Ethernet Port
JA1	Ultra160 LVD SCSI Connector (p. 2-21)
JA4	Ultra Wide SCSI Connector (p. 2-20)
JA5	Ultra SCSI Connector (p. 2-20)
JF1	Front Control Panel (p. 2-7)
JP11	Power Supply Fail Header (p. 2-14)
P1	Primary ATX Power Connector (p. 2-9)
P2	Primary ATX Power Connector (p. 2-9)
PWR_SEC	Secondary ATX Power Connector (p. 2-9)
SLED1	SCSI LED header (p. 2-14)
U38	Universal Serial Bus Ports (p. 2-13)
USB4 (J105)	Extra USB Header (p. 2-13)
WOL	Wake-on-LAN Header (p. 2-13)
WOM	Wake-on-Modem Header (p. 2-13)

Figure 1-8. SUPER 370DLE Layout (not drawn to scale)



Also see the figure on page 2-7 for the locations of the I/O ports and 2-8 for the Front Control Panel (JF1) connectors.

370DLE Quick Reference

<u>Jumpers</u>	<u>Description</u>	Default Setting
JBT1	CMOS Clear (p. 2-16)	Pin 1-2 (Normal)
JP2	Front Side Bus Speed (p. 2-16)	Pin 1-2 (CPU Select)
JP4	Manufacturer's Setting	Open
JP7	Overheat Alarm (p. 2-17)	Closed (Enabled)
JP8	LAN Enable/Disable (p. 2-17)	Open (Enabled)
JP12	3rd P/S Failure Alarm (p. 2-18)	Open (Disabled)
JP13	Speed for 64-bit PCI	Open (66 MHz)

DIP Switches	<u>Description</u>	Default Setting
SW1 (1-4)	CPU Core/Bus Ratio	(see p. 2-15)
SW2	Manufacturer's Setting	(Open)

<u>Connectors</u>	<u>Description</u>
BANK0-BANK3	Memory (RAM) Slots (p. 2-6)
CF3 (1 ea)	Thermal Control Fan Header (p. 2-12)
CHASSIS FAN (4 ea)	Chassis Fan Header (p. 2-12)
COM1/COM2	COM1,COM2 Serial Port Connector (p. 2-12)
CPU FAN (2 ea)	CPU1/CPU2 Fan Header (p. 2-12)
J23, J24	IDE Hard Disk Drive Connectors (p. 2-19)
J26	Floppy Disk Drive Connector (p. 2-19)
J27	Parallel Printer Port (p. 2-18)
J28	PS/2 Keyboard/Mouse (p. 2-12)
J104	Ethernet Port
JF1	Front Control Panel (p. 2-7)
JP11	Power Supply Fail Header (p. 2-14)
P1	Primary ATX Power Connector (p. 2-9)
P2	Primary ATX Power Connector (p. 2-9)
PWR_SEC	Secondary ATX Power Connector (p. 2-9)
U38	Universal Serial Bus Ports (p. 2-13)
USB4 (J105)	Extra USB Header (p. 2-13)
WOL	Wake-on-LAN Header (p. 2-13)
WOM	Wake-on-Modem Header (p. 2-13)

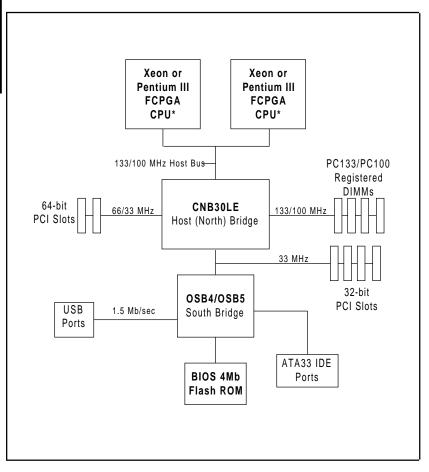


Figure 1-9. ServerWorks LE Chipset: System Block Diagram

*Note: See next page for details on processor support.

Features of the S2DL3/370DL6/370DL3/370DLE

CPU

S2DL3:

 Single or dual Pentium III Xeon 400-800 MHz processors at 133 or 100 MHz front side bus (FSB)

370DL6/370DL3/370DLE:

 Single or dual Pentium III FCPGA 500-933 MHz processors at 133 or 100 MHz front side bus

Note: Please refer to the support section of our web site for a complete listing of supported processors. (http://www.supermicro.com/TechSupport.htm)

Memory

 Four 168-pin DIMM sockets supporting up to 4 GB registered ECC DIMMs (133/100 MHz memory bus speed depends on processor front side bus speed)

Chipset

ServerWorks ServerSet III LE (see page 1-19 for details)

Expansion Slots

S2DL3/370DL3/370DLE:

370DL6:

- Two 64-bit, 66/33 MHz PCI slots
- Two 64-bit, 66/33 MHz PCI slots
- Four 32-bit, 33 MHz PCI slots
- · Three 32-bit, 33 MHz PCI slots

· One ISA slot

BIOS

- 4 Mb AMI® Flash BIOS
- APM 1.2, DMI 2.1, PCI 2.2, ACPI 1.0, Plug and Play (PnP)

PC Health Monitoring

- Seven onboard voltage monitors for CPU core, chipset voltage, +5V and +12V
- Fan status monitor with firmware/software on/off control
- Environmental temperature monitor and control
- · CPU fan auto-off in sleep mode
- Power-up mode control for recovery from AC power loss
- · System overheat LED and control
- · System resource alert

ACPI/PC 98 Features

- Microsoft OnNow
- · Slow blinking LED for suspend state indicator
- · Main switch override mechanism
- · External modem ring-on

Onboard I/O

- · AIC-7899 for dual channel Ultra160 SCSI (370DL6 only)
- AIC-7892 for single channel Ultra160 SCSI (S2DL3/370DL3)
- Integrated ATI Rage XL Graphics Controller (370DL6 only)
- Intel 82559 for integrated onboard Ethernet
- 2 EIDE bus master interfaces support Ultra DMA/33
- 1 floppy port interface (up to 2.88 MB)
- · 2 Fast UART 16550A compatible serial ports
- 1 EPP (Enhanced Parallel Port) and ECP (Extended Capabilities Port) supported parallel port
- PS/2 mouse and PS/2 keyboard ports
- · 2 USB (Universal Serial Bus) ports

Other

- Selectable CPU and chassis fan speed control (set in BIOS)
- · Internal/external modem ring-on
- · Recovery from AC power loss control
- Wake-on-LAN (WOL)
- Multiple FSB clock frequency selections (set in BIOS)

CD/Diskette Utilities

- · BIOS flash upgrade utility
- · Device Drivers

Dimensions

- SUPER S2DL3 Extended ATX: 12" x 13" (305 x 330 mm)
- SUPER 370DL6 Extended ATX: 12" x 10.50" (305 x 267 mm)
- SUPER 370DL3 Extended ATX: 12" x 10.25" (305 x 260 mm)
- SUPER 370DLE Extended ATX: 12" x 10.25" (305 x 260 mm)

1-2 Chipset Overview

The ServerWorks ServerSet™ III LE is a high-performance core logic chipset that consists of a North Bridge and a South Bridge.

The North Bridge includes an integrated main memory subsystem and a dual channel PCI bus that bridges the processor bus to a 64-bit PCI bus and a 32-bit PCI bus. The North Bridge also packs and unpacks data for PCI accesses, which reserves more processor bandwidth for multiprocessor motherboards.

The South Bridge provides various integrated functions, including the PCI to ISA bridge and support for UDMA33, security (passwords and system protection), Plug & Play, USBs, power management, interrupt controllers and the SMBus.

The North and South Bridges communicate over a serial bus that uses the PCI clock as a timing reference. This serial bus uses a single pin on both bridges to send a 4-bit word for transmitting commands back and forth.

1-3 Special Features

ATI Graphics Controller (370DL6 only)

The 370DL6 has an integrated ATI video controller based on the Rage XL graphics chip. The Rage XL is the first accelerator in the world to provide integrated support for digital flat panel monitors and fully supports the AGP 2X mode, sideband addressing and AGP texturing. Working with system memory, this onboard graphics package can provide a bandwidth of up to 1 GB/sec over a 64-bit interface.

BIOS Recovery

The BIOS Recovery function allows you to recover your BIOS image file if the BIOS flashing procedure fails (see Section 3-3).

Recovery from AC Power Loss

BIOS provides a setting for you to determine how the system will respond when AC power is lost and then restored to the system. You can choose for the system to remain powered off (in which case you must hit the power switch to turn it back on) or for it to automatically return to a power on state. See the Power Lost Control setting in BIOS on page 4-11 of this manual to change this setting. The default setting is Always OFF.

1-4 PC Health Monitoring

This section describes the PC health monitoring features of the SUPER S2DL3/370DL6/370DL3/370DLE. Both have an onboard System Hardware Monitor chip that supports PC health monitoring.

Seven Onboard Voltage Monitors for the CPU Core, Chipset Voltage, +5V and +12V

The onboard voltage monitor will scan these seven voltages continuously. Once a voltage becomes unstable, it will give a warning or send an error message to the screen. Users can adjust the voltage thresholds to define the sensitivity of the voltage monitor.

Fan Status Monitor with Firmware/Software On/Off Control

The PC health monitor can check the RPM status of the cooling fans. The onboard 3-pin CPU and chassis fans are controlled by the power management functions. The thermal fan is controlled by the overheat detection logic.

Environmental Temperature Control

The thermal control sensor monitors the CPU temperature in real time and will turn on the thermal control fan whenever the CPU temperature exceeds a user-defined threshold. The overheat circuitry runs independently from the CPU. It can continue to monitor for overheat conditions even when the CPU is in sleep mode. Once it detects that the CPU temperature is too high, it will automatically turn on the thermal control fan to prevent any overheat damage to the CPU. The onboard chassis thermal circuitry can monitor the overall system temperature and alert users when the chassis temperature is too high.

CPU Fan Auto-Off in Sleep Mode

The CPU fan activates when the power is turned on. It can be turned off when the CPU is in sleep mode. When in sleep mode, the CPU will not run at full power, thereby generating less heat.

CPU Overheat LED and Control

This feature is available when the user enables the CPU overheat warning function in the BIOS (see page 4-17). This allows the user to define an overheat temperature. When this temperature is exceeded, both the overheat fan and the warning LED are triggered.

System Resource Alert

This feature is available when used with Intel's LANDesk Client Manager (optional). It is used to notify the user of certain system events. For example, if the system is running low on virtual memory and there is insufficient hard drive space for saving the data, you can be alerted of the potential problem.

Hardware BIOS Virus Protection

The system BIOS is protected by hardware so that no virus can infect the BIOS area. The user can only change the BIOS content through the flash utility provided by SUPERMICRO. This feature can prevent viruses from infecting the BIOS area and destroying valuable data.

Auto-Switching Voltage Regulator for the CPU Core

The auto-switching voltage regulator for the CPU core can support up to 20A current and auto-sense voltage IDs ranging from 1.4V to 3.5V. This will allow the regulator to run cooler and thus make the system more stable.

1-5 ACPI/PC 98 Features

ACPI stands for Advanced Configuration and Power Interface. The ACPI specification defines a flexible and abstract hardware interface that provides a standard way to integrate power management features throughout a PC system, including its hardware, operating system and application software. This enables the system to automatically turn on and off peripherals such as CD-ROMs, network cards, hard disk drives and printers. This also includes consumer devices connected to the PC such as VCRs, TVs, telephones and stereos.

In addition to enabling operating system-directed power management, ACPI provides a generic system event mechanism for Plug and Play and an operating system-independent interface for configuration control. ACPI leverages the Plug and Play BIOS data structures while providing a processor architecture-independent implementation that is compatible with both Windows 98 and Windows NT

5.0. **Note:** To utilize ACPI, you must reinstall Windows 98. To reinstall Windows 98 with ACPI, enter DOS and type "setup /p J" at the CDROM prompt (usually D:\) with the Windows 98 CD loaded. (Make sure you include the spaces after "setup" and "p".) Then hit <Enter>. You can check to see if ACPI has been properly installed by looking for it in the Device Manager, which is located in the Control Panel in Windows.

Microsoft OnNow

The OnNow design initiative is a comprehensive, system-wide approach to system and device power control. OnNow is a term for a PC that is always on but appears to be off and responds immediately to user or other requests.

Slow Blinking LED for Suspend-State Indicator

When the CPU goes into a suspend state, the chassis power LED will start blinking to indicate that the CPU is in suspend mode. When the user presses any key, the CPU will wake-up and the LED will automatically stop blinking and remain on.

Main Switch Override Mechanism

When an ATX power supply is used, the power button can function as a system suspend button. When the user depresses the power button, the system will enter a SoftOff state. The monitor will be suspended and the hard drive will spin down. Depressing the power button again will cause the whole system to wake-up. During the SoftOff state, the ATX power supply provides power to keep the required circuitry in the system alive. In case the system malfunctions and you want to turn off the power, just depress and hold the power button for 4 seconds. The power will turn off and no power will be provided to the motherboard.

External Modem Ring-On

Wake-up events can be triggered by a device such as the external modem ringing when the system is in the SoftOff state. Note that external modem ring-on can only be used with an ATX 2.01 (or above) compliant power supply.

Wake-On-LAN (WOL)

Wake-On-LAN is defined as the ability of a management application to remotely power up a computer that is powered off. Remote PC setup, updates and asset

tracking can occur after hours and on weekends so that daily LAN traffic is kept to a minimum and users are not interrupted. The motherboards have a 3-pin

header (WOL) to connect to the 3-pin header on a Network Interface Card (NIC) that has WOL capability. Wake-On-LAN must be enabled in BIOS. Note that Wake-On-Lan can only be used with an ATX 2.01 (or above) compliant power supply.

1-6 Power Supply

As with all computer products, a stable power source is necessary for proper and reliable operation. It is even more important for processors that have CPU clock rates.

The SUPER S2DL3/370DL6/370DL3/370DLE accommodates ATX power supplies. Although most power supplies generally meet the specifications required by the CPU, some are inadequate. You should use one that will supply at least 300W of power - an even higher wattage power supply is recommended for high-load configurations. Also your power supply must provide a +5V standby voltage that supplies at least 720 mA of current.

It is strongly recommended that you use a high quality power supply that meets ATX power supply Specification 2.02 or above. Additionally, in areas where noisy power transmission is present, you may choose to install a line filter to shield the computer from noise. It is recommended that you also install a power surge protector to help avoid problems caused by power surges.

1-7 Super I/O

The disk drive adapter functions of the Super I/O chip include a floppy disk drive controller that is compatible with industry standard 82077/765, a data separator, write pre-compensation circuitry, decode logic, data rate selection, a clock generator, drive interface control logic and interrupt and DMA logic. The wide range of functions integrated onto the Super I/O greatly reduces the number of components required for interfacing with floppy disk drives. The Super I/O supports four 360 K, 720 K, 1.2 M, 1.44 M or 2.88 M disk drives and data transfer rates of 250 Kb/s, 500 Kb/s or 1 Mb/s.It also provides two high-speed, 16550 compatible serial communication ports (UARTs), one of which supports serial infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability and a processor interrupt system.

Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability and a processor interrupt system. Both UARTs provide legacy speed with baud rate of up to 115.2 Kbps as well as an advanced speed with baud rates of 250 K, 500 K, or 1 Mb/s, which support higher speed modems.

The Super I/O supports one PC-compatible printer port (SPP), Bi-directional Printer Port (BPP), Enhanced Parallel Port (EPP) or Extended Capabilities Port (ECP).

The Super I/O provides functions that comply with ACPI (Advanced Configuration and Power Interface), which includes support of legacy and ACPI power management through an SMI or SCI function pin. It also features auto power management to reduce power consumption.

The IRQs, DMAs and I/O space resources of the Super I/O can flexibly adjust to meet ISA PnP requirements, which suppport ACPI and APM (Advanced Power Management).

Chapter 2 Installation

2-1 Static-Sensitive Devices

Static-sensitive electrical discharge can damage electronic components. To prevent damage to your system board, it is important to handle it very carefully. The following measures are generally sufficient to protect your equipment from static discharge.

Precautions

- · Use a grounded wrist strap designed to prevent static discharge.
- Touch a grounded metal object before removing the board from the antistatic bag.
- Handle the board by its edges only; do not touch its components, peripheral chips, memory modules or gold contacts.
- When handling chips or modules, avoid touching their pins.
- Put the motherboard and peripherals back into their antistatic bags when not in use.
- For grounding purposes, make sure your computer chassis provides excellent conductivity between the power supply, the case, the mounting fasteners and the motherboard.

Unpacking

The motherboard is shipped in antistatic packaging to avoid static damage. When unpacking the board, make sure the person handling it is static protected.

2-2 Pentium III/II Xeon Processor Installation (S2DL3)

Please Note: These instructions are for the retail pack with a passive heatsink. OEM Pentium II/III Xeon processors require a heatsink.



When installing the Pentium II/III Xeon processor, the DRM (Dual Retention Module) must be bolted to the chassis to support the processor against shock and vibration.



When handling the Pentium II/III Xeon processor, avoid placing direct pressure to the label area of the fan.

IMPORTANT: Always connect the power cord last and always remove it before adding, removing or changing any hardware components.

1. Installing the metal standoffs:

Attach the metal standoffs to the motherboard tray. Make sure the location of all the mounting holes for both the motherboard and the chassis match. When installing, make sure the metal standoffs click in or are screwed in tightly. There are three additional metal standoffs, specifically for the Slot 2 motherboard, that are required for mounting the DRM (Dual Retention Module). See Figure 2-1 for mounting hole locations.

2. Mounting the motherboard onto the motherboard tray: Except for the four Slot 2 mounting holes, use a Philips screwdriver to first secure the motherboard onto the motherboard tray.

3. Mounting the fans and the DRM (See Figure 2-2): Before mounting the retention base, you first need to mount the fans (if needed) in their proper locations. Screw the base retention parts into the four Slot 2 mounting holes. Note: The DRM must be bolted through the motherboard and into the motherboard tray.

4. Installing caps on the Xeon processor as a handlebar: When attaching the caps for each Xeon processor, make sure the directions of the mounting screw holes on each cap face inside so that the unit can easily slide in. Please test the configuration of the units before mounting the caps.

5. Securing the processor:

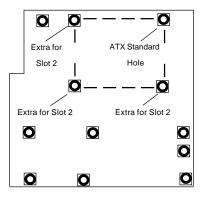
Slide in the processor(s) making sure it sits on the Slot 2 socket. Then, push down to fully seat the processor in the socket. Finish by using screws from the DRM kit to secure the caps to the DRM base.

Removing the Pentium II/III Xeon Processor

To remove the Pentium II/III processor from the motherboard, follow the reverse of the installation process.



When removing the Pentium II/III Xeon processor, avoid pressing down on the motherboard or any of its components.



*Back view of motherboard

When mounting the motherboard to the chassis, please note there are three holes specifically for mounting the Slot 2 DRM as well as an ATX Standard hole that serves to secure the Slot 2 DRM.

Figure 2-1. Dual Retention Module Mounting holes



Figure 2-2. DRM (with Caps and Screws)

2-3 FCPGA Processor Installation (370DL6/DL3/DLE)



When handling the FCPGA processor package, avoid placing direct pressure on the label area of the fan.

This section covers the installation procedure for FCPGA (Flip Chip Plastic Grid Array) type processors. You should install the processor first and then install the motherboard in the chassis. Following the installation procedures in the order they appear in this section should eliminate the most common problems encountered when installing a system.

<u>IMPORTANT</u>: Always connect the power cord last and always remove it before adding, removing or changing any hardware components.

Heat Sink

Follow the instructions that came with your processor or heat sink to attach a heat sink to the processor. Your heat sink should have a 3-pin fan, which connects to the CPU FAN header. Make sure that good contact is made between the CPU chip (the die) and the heat sink. Insufficient contact or inproper types of heat sinks and fans can cause the processor to overheat, which may crash the system. (You can check the CPU temperature readings in the "Periperal Setup" Section of BIOS.)

Processor

Your motherboard has two 370-pin sockets, which support Intel FCPGA processors. Lift the lever on the FCPGA socket and insert the processor with the notched corner oriented toward pin one on the socket. Make sure the processor is fully seated in the socket and and then close the lever. You can also install a single 370-pin FCPGA CPU on a dual-processor motherboard without changing any jumper settings. See Figure 2-3 for views of the 370-pin FCPGA socket before and after processor installation.

Mounting the Motherboard in the Chassis

All motherboards have standard mounting holes to fit different types of chassis. Make sure the location of all the mounting holes for both the motherboard and the chassis match. Although a chassis may have both plastic and metal mounting fasteners, metal ones are highly recommended because they ground the motherboard to the chassis. Make sure the metal standoffs click in or are

screwed in tightly. Then use a screwdriver to secure the motherboard onto the motherboard tray.

Figure 2-3. FCPGA Socket: Empty and with Processor Installed





2-4 Installing DIMMs

CAUTION

Exercise extreme care when installing or removing DIMM modules to prevent any possible damage.

DIMM Installation (See Figure 2-4)

- 1. Insert DIMMs as required for the desired system memory.
- Insert each DIMM module vertically into its slot. Pay attention to the two notches along the bottom of the module to prevent inserting the DIMM module incorrectly.
- Gently press down on the DIMM module until it snaps into place in the slot. As stated in 1 above, you must populate either two or four banks of memory.

Support

The S2DL3/370DL6/370DL3/370DLE only supports registered DIMMs with ECC memory. Both PC133 and PC100 memory are fully supported.

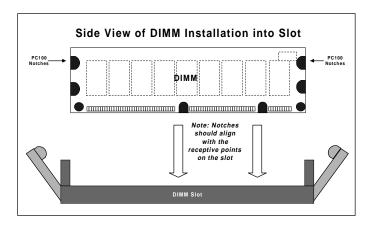
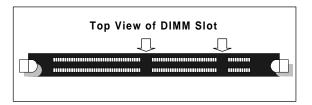


Figure 2-4. DIMM Installation

To Install: Insert module vertically and press down until it snaps into place. Pay attention to the two notches.



To Remove:

Use your thumbs to gently push near the edge of both ends of the module. This should release it from the slot.

2-5 Port/Control Panel Connector Locations

The I/O ports are color coded in conformance with the PC 99 specification. See Figure 2-5 below for the colors and locations of the various I/O ports.

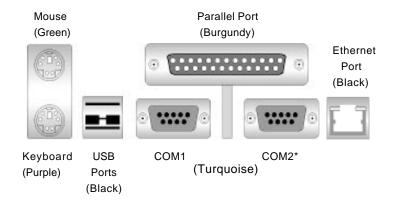


Figure 2-5. I/O Port Locations and Definitions

*Note: On the 370DL6, the COM2 connector as shown in Figure 2-5 is replaced by a VGA connector.

Front Control Panel

JF1 contains header pins for various front control panel connectors. See Figure 2-6 for the pin definitions of the speaker, overheat LED, keyboard lock, I²C, USB3, reset, power on, hard drive LED and power LED headers, which are all located on JF1. Please note that even and odd numbered pins are on opposite sides. Refer to pages 2-8 to 2-13 for details.

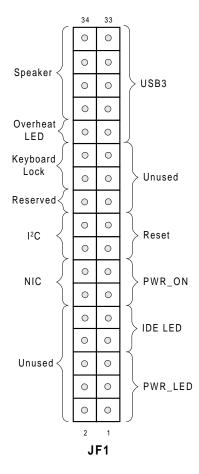


Figure 2-6. Front Control Panel Connectors

2-6 Connecting Cables (see previous page for JF1 connection locations)

Power Supply Connector

After you have securely mounted the motherboard, memory and add-on cards, you are ready to connect the cables. Attach an ATX power supply cable to U45 (and also to U43 for heavy load configurations). See Table 2-1 for the pin definitions of these ATX power supply connectors.

Table 2-1 ATX Power Supply Connector Pin Definitions (P1, P2)

20 (, . 2)				
Pin Number	Definition	Pin Number	Definition	
1	3.3V	11	3.3V	
2	3.3V3	12	-12V	
3	Ground	13	Ground	
4	5 V	14	PS-ON	
5	Ground	15	Ground	
6	5 V	16	Ground	
7	Ground	17	Ground	
8	PW-OK	18	-5V	
9	5VSB	19	5 V	
10	12V	20	5 V	

Secondary Power Connector

Use of the Secondary Power connector (PWR_SEC) is recommended when a heavy load of peripherals has been added to the motherboard. Note: Be sure to use a 6-pin connector and check the power supply layout before attaching it. See Table 2-2 for pin definitions.

Table 2-2 Secondary Power Connector

(PWK_SEC)		
Pin		
Number	Definition	
1	Ground	
2	Ground	
3	Ground	
4	+3.3V	
5	+3.3V	
6	+5V (keyed)	

Power LED

The Power LED connection is located on pins 1, 3 and 5 of JF1. See Table 2-3 for pin definitions.

Table 2-3 PWR_LED Pin Definitions (JF1)

Pin	
Number	Definition
1	+5V
3	Key
5	GND

Hard Drive LED

The Hard Drive LED connection is located on pins 7 and 9 of JF1. Attach the IDE hard drive LED cable to these pins to display disk activity. See Table 2-4 for pin definitions.

Table 2-4 IDE_LED Pin Definitions (JF1)

Pin Number	Definition
7	+5V
9	HD Active

PWR ON

The PWR_ON connection is located on pins 11 and 13 of JF1. Momentarily contacting both pins will power on/off the system. The user can also configure this button to function as a suspend button. (See the Power Button Mode setting in BIOS.) To turn off the power when set to suspend mode, hold down the power button for at least 4 seconds. See Table 2-5 for pin definitions.

Table 2-5
PWR_ON Connector
Pin Definitions
(JF1)

Pin	
Number	Definition
11	PW_ON
13	Ground

NIC_LED

The Network Interface Controller LED connection is located on pins 12 and 14 of JF1. Attach the NIC LED cable to these pins to display network activity. See Table 2-6 for pin definitions.

Table 2-6 NIC_LED Pin Definitions (JF1)

	-
Pin	
Number	Definition
12	+5V
14	GND
1	1

Reset

The Reset connection is located on pins 15 and 17 of JF1. This connector attaches to the hardware reset switch on the computer case. See Table 2-7 for pin definitions.

I²C

The I²C connection is located on pins 16 and 18 of JF1. See Table 2-8 for pin definitions.

Table 2-7 Reset Pin Definitions (JF1)

Pin	
Number	Definition
15	Reset
17	Ground

Table 2-8 I²C Pin Definitions (JF1)

Pin Number	Definition
16	SDA
18	SCL

Chassis Intrusion

A Chassis Intrusion connection is located on pin 20 of JF1. See Table 2-9 for pin definitions. Note: An extra chassis intrusion header is provided at JL1.

Keyboard Lock

The Keyboard Lock connection is located on pins 22 and 24 of JF1. See Table 2-10 for pin definitions. Pins 5 through 7 are for the power LED. Pins 8 and 9 are for the keylock.

Overheat LED (OH)

Connect an LED to the OH connection on pin 26 of JF1 to provide advanced warning of chassis overheating. Refer to Table 2-11 for pin definitions.

Extra Universal Serial Bus Connection (USB3)

An additional connection for USB3 is included on pins 25, 27, 29 and 31 of JF1 for front side USB access. You will need a USB cable (not included) to use this connection.

Note: The USB4 (J105) connector is described on page 2-13.

Table 2-9 Chassis Intrusion (IT) Pin Definitions (JF1)

Pin	
Number	Definition
20	Intrusion Input

Table 2-10 Keyboard Lock (KL) Pin Definitions (JF1)

Pin	
lumber	Definition
22	+5V
24	GND
	lumber 22

Table 2-11 Overheat LED (OH) Pin Definitions (JF1)

Pin	
Number	Definition
10	OH Active

Table 2-12 USB3 Pin Definitions (JF1)

Pin	
Number	Definition
1	+5V
2	Key
3	IRRX
4	Ground

Speaker

The speaker connection is located on pins 28, 30, 32 and 34 of JF1. See Table 2-13 for pin definitions.

Table 2-13 Speaker Connector Pin Definitions (JF1)

Pin		
Number	Function	Definition
28	+	Red wire, Speaker data
30	Key	No connection
32		Key
34		Speaker data

Fan Headers*

The thermal control fan header is designated THERMAL FAN on your board. The CPU (2 ea.) and chassis fan headers (4 ea.) are designated CPU FAN and CHASSIS FAN, respectively. Refer to Table 2-14 for pin definitions.

Table 2-14
Fan Header Pin Definitions
(THRMAL, CPU and CHASSIS

FANS)			
Pin			
Number	Definition		
1	Ground (black)		
2	+12V (red)		
3	Tachometer		

^{*} Caution: These fan headers are DC power.

Serial Ports

Two connectors, for the COM1 and COM2 serial ports, are located under the parallel port on your motherboard (see Figure 2-3). See Table 2-15 for pin definitions. For the 370DL6, COM2 is a 10-pin header. An additional COM port cable is need to use this COM port.

Table 2-15 Serial Port Pin Definitions (COM1, COM2)

Definition	Pin Number	Definition
DCD	6	CTS
DSR	7	DTR
Serial In	8	RI
RTS	9	Ground
Serial Out	10	NC
	DCD DSR Serial In RTS	DSR 7 Serial In 8 RTS 9

ATX PS/2 Keyboard and PS/2 Mouse Ports

The ATX PS/2 keyboard and the PS/2 mouse are located on J28. See Table 2-16 for pin definitions. (The mouse port is above the keyboard port. See Figure 2-5.)

Table 2-16 PS/2 Keyboard and Mouse Port Pin Definitions (J28)

Pin	
Number	Definition
1	Data
2	NC
3	Ground
4	VCC
5	Clock
6	NC
	Number 1 2 3 4 5

Universal Serial Bus (USB)

Two Universal Serial Bus connectors are located on U38. USB0 is the bottom connector and USB1 is the top connector. See Table 2-17 for pin definitions.

USB4: Extra USB Connection (J105)

J105 is a five-pin headers for the USB4 port. The pin definitions are the same as those for USB0 (see Table 2-17.) You will need a USB cable (not included) to use this connection.

Wake-On-LAN

The Wake-On-LAN header is designated as WOL. Refer to Table 2-18 for pin definitions. You must enable the LAN Wake-Up setting in BIOS to use this feature. You must also have a LAN card with a Wake-on-LAN connector and cable.

Wake-On-Modem

The Wake-On-Modem header is designated as WOM. This function allows your computer to receive and be "woken up" by an incoming call when in the suspendstate. Refer to Table 2-19 for pin definitions. You must also have a modem card and cable to use WOM.

Table 2-17 Universal Serial Bus Pin Definitions U38 U38

Pin		Pin	
Number	Definition	Number	Definition
1	+5V	1	+5V
2	P0-	2	P0-
3	P0+	3	P0+
4	Ground	4	Ground
5	N/A	5	Key

Table 2-18 Wake-On-LAN Pin Definitions (WOL)

Pin	
Number	Definition
1	+5V Standby
2	Ground
3	Wake-up

Table 2-19 Wake-On-Modem Pin Definitions (WOM)

Pin	
Number	Definition
1	+5V Standby
2	Ground
3	Wake-up

Power Supply Fail Header

Connect a cable from your power supply to the header at JP11 to provide warning of power supply failure. This warning signal is passed through the PWR_LED pin on JL1 to provide indication of a power failure on the chassis. This feature is only available when using Supermicro power supplies. See Table 2-20 for pin definitions.

Table 2-20 Power Supply Fail Header Pin Definitions (JP11)

	• •
Pin	
Number	Definition
1	P/S 1 Fail Signal
2	P/S 2 Fail Signal
3	P/S 3 Fail Signal
4	Reset (from MB)

SLED1 (SCSI LED) Indicator (not on 370DLE)

The SLED connector is used to provide an LED indication of SCSI activity. Refer to Table 2-21 for connecting the SCSI LED.

Table 2-21 SLED1 Pin Definitions

Pin	
Number	Definition
1	Positive
2	Negative
3	Negative
4	Positive

2-7 DIP Switch Settings

DIP Switch 1: Core/Bus Ratio

Two "DIP" switches labeled SW1 and SW2 are located on the S2DLE/370DL6/370DL3/370DLE. Each has four individual switches. The four on Dip Switch 1 are used to set the core/bus ratio.

The example on the right will show you which CPU Core/Bus Ratio to use. The general rule is to divide the CPU speed by the bus speed. If you have a 550 MHz CPU, dividing it by a 100 Mhz front side bus will give you a CPU Core/BUS Ratio of 5.5. After determining the CPU Core/Bus Ratio, refer to Table 2-22 for the correct settings of DIP Switch 1.

Note:

Most Intel processors have a fixed Core/Bus ratio that will overwrite the setting of DIP Switch 1.

DIP Switch 2

Only DIP switch 1 is functional at this time. DIP switch 2 should be left as set by the manufacturer.

Table 2-22 CPU Core/Bus Ratio Selection

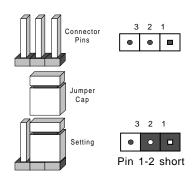
(DIP Switch1)					
CPU Core/	SW1	SW1	SW1	SW1	
Bus Ratio	#1	#2	#3	#4	
2.0	ON	ON	ON	ON	
3.0	ON	OFF	ON	ON	
4.0	ON	ON	OFF	ON	
4.5	OFF	ON	OFF	ON	
5.0	ON	OFF	OFF	ON	
5.5	OFF	OFF	OFF	ON	
6.0	ON	ON	ON	OFF	
6.5	OFF	ON	ON	OFF	
7.0	ON	OFF	ON	OFF	
7.5	OFF	OFF	ON	OFF	
8.0	ON	ON	OFF	OFF	
8.5	OFF	ON	OFF	OFF	
9.0	ON	OFF	OFF	OFF	

550 (MHz) / 100 (MHz) = 5.5 CPU Speed / Bus Freq. = Ratio

2-8 Jumper Settings

Explanation of Jumpers

To modify the operation of the motherboard, jumpers can be used to choose between optional settings. Jumpers create shorts between two pins to change the function of the connector. Pin 1 is identified with a square solder pad on the printed circuit board. See the motherboard layout pages for jumper locations.



CMOS Clear

Refer to Table 2-23 for the jumper settings to clear CMOS. Always remove the AC power cord from the system before clearing CMOS. NOTE: For an ATX power supply, you must completely shut down the system, remove the AC power cord and *then* use JBT1 to clear CMOS. Replace JBT1 back to the pin 1-2 position before powering up the system again. Do not use the PW_ON connector to clear CMOS.

Table 2-23 CMOS Clear Jumper Settings (JBT1) Jumper Position Definition 1-2 Normal 2-3 CMOS Clear Position Position 1-2 2-3 CMOS Clear Vorma

Front Side Bus Speed

CPU speed = FSB x Core/Bus ratio

Core/Bus Ratio settings are described in Section 2-7.

Table 2-24 Front Side Bus Speed Jumper Settings (JP2)

Jumper Position	Definition
1-2	Auto
2-3	100 MHz
OFF	133 MHz

* Note: The Auto setting allows the CPU to set the speed.

SCSI Termination Enable/ Disable (not on 370DLE)

370DL6 (dual channel Ultra160): JA2 and JA3.

<u>S2DL3 and 370DL3</u> (single channel Ultra160): JA2.

370DLE: N/A.

Jumpers JA2 and JA3 allow you to enable or disable termination for the SCSI connectors. The normal (default) position is open to enable SCSI termination. See Table 2-25 for jumper settings.

Table 2-25 SCSI Termination Enable/Disable Jumper Settings (JP8)

Jumper Position	Definition
Open	Enabled
Closed	Disabled

Overheat Alarm (Buzzer) Enable/Disable

You may want to disable the audio alarm signal that notifies you of overheat condtions. Jumper JP7 gives you this option. See Table 2-26 for jumper settings.

Table 2-26 Overheat Alarm Enable/Disable Jumper Settings (JP7)

Jumper	
Position	Definition
Open	Disabled
Closed	Enabled

Onboard LAN/NIC Enable/Disable

Change the setting of jumper JP8 to enable or disable the onboard LAN or NIC (Network Interface Card) on your motherboard. See Table 2-27 for jumper settings.

Table 2-27 Onboard LAN/NIC Enable/Disable Jumper Settings (JP8)

Jumper	
Position	Definition
Open	Enabled
Closed	Disabled

Third Power Supply Failure Alarm Enable/Disable

The system will notify you in the event of a power supply failure. This feature assumes that three power supply units are installed in the chassis, with one acting as a backup. If you only have one or two power supply units installed, you should disable this with JP12 to prevent false alarms. See Table 2-28 for jumper settings.

Table 2-28 Power Supply Failure Alarm Enable/Disable Jumper Settings (JP12)

Jumper Position	Definition
Open Closed	Disabled Enabled

2-9 Parallel Port, Floppy/Hard Disk Drive and SCSI Connections

Note the following when connecting the floppy and hard disk drive cables:

- · The floppy disk drive cable has seven twisted wires.
- A red mark on a wire typically designates the location of pin 1.
- A single floppy disk drive ribbon cable has 34 wires and two connectors to provide for two floppy disk drives. The connector with twisted wires always connects to drive A, and the connector that does not have twisted wires always connects to drive B.

Parallel Port Connector

The parallel port is located on J22. See Table 2-29 for pin definitions.

Table 2-29
Parallel (Printer) Port Pin Definitions
(J22)

Pin Number	Function	Pin Number	Function
1	Strobe-	2	Auto Feed-
3	Data Bit 0	4	Error-
5	Data Bit 1	6	Init-
7	Data Bit 2	8	SLCT IN-
9	Data Bit 3	10	GND
11	Data Bit 4	12	GND
13	Data Bit 5	14	GND
15	Data Bit 6	16	GND
17	Data Bit 7	18	GND
19	ACK	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SLCT	26	NC

Floppy Connector

The floppy connector is located on J26. See Table 2-30 for pin definitions.

Table 2-30 Floppy Connector Pin Definitions (JP26)

Pin Number	Function	Pin Number	Function
1	GND	2	FDHDIN
3	GND	4	Reserved
5	Key	6	FDEDIN
7	GND	8	Index-
9	GND	10	Motor Enable
11	GND	12	Drive Select B-
13	GND	14	Drive Select A-
15	GND	16	Motor Enable
17	GND	18	DIR-
19	GND	20	STEP-
21	GND	22	Write Data-
23	GND	24	Write Gate-
25	GND	26	Track 00-
27	GND	28	Write Protect-
29	GND	30	Read Data-
31	GND	32	Side 1 Select-
33	GND	34	Diskette

IDE Connectors

There are no jumpers to configure the onboard IDE connectors J23 and J24. Refer to Table 2-31 for pin definitions.

Table 2-31 IDE Connector Pin Definitions (J23, J24)

(020)		
Function	Pin Number	Function
Reset IDE	2	GND
Host Data 7	4	Host Data 8
Host Data 6	6	Host Data 9
Host Data 5	8	Host Data 10
Host Data 4	10	Host Data 11
Host Data 3	12	Host Data 12
Host Data 2	14	Host Data 13
Host Data 1	16	Host Data 14
Host Data 0	18	Host Data 15
GND	20	Key
DRQ3	22	GND
I/O Write-	24	GND
I/O Read-	26	GND
IOCHRDY	28	BALE
DACK3-	30	GND
IRQ14	32	IOCS16-
Addr 1	34	GND
Addr 0	36	Addr 2
Chip Select 0	38	Chip Select 1-
Activity	40	GND
	Function Reset IDE Host Data 7 Host Data 6 Host Data 5 Host Data 3 Host Data 2 Host Data 1 Host Data 1 Host Data 0 GND DRQ3 I/O Write- I/O Read- IOCHRDY DACK3- IRQ14 Addr 1 Addr 0 Chip Select 0	Function

50-pin Legacy SCSI Connector

Refer to Table 2-32 for pin definitions for the 50-pin Legacy SCSI connector located at JA5.

Table 2-32 50-pin Legacy SCSI Connector Pin Definitions (JA5)

(JA5)					
Pin Number	Function	Pin Number	Function		
1	GND	26	-DB (0)		
2	GND	27	-DB (1)		
3	GND	28	-DB (2)		
4	GND	29	-DB (3)		
5	GND	30	-DB (4)		
6	GND	31	-DB (5)		
7	GND	32	-DB (6)		
8	GND	33	-DB (7)		
9	GND	34	-DB (P)		
10	GND	35	GND		
11	GND	36	GND		
12	Reserved	37	Reserved		
13	Open	38	Termpwr		
14	Reserved	39	Reserved		
15	GND	40	GND		
16	GND	41	-ATN		
17	GND	42	GND		
18	GND	43	-BSY		
19	GND	44	-ACK		
20	GND	45	-RST		
21	GND	46	-MSG		
22	GND	47	-SEL		
23	GND	48	-C/D		
24	GND	49	-REQ		
25	GND	50	-I/O		

Ultra Wide SCSI Connector

Refer to Table 2-33 for the Ultra Wide SCSI pin definitions. The connector is located at JA5.

Table 2-33 Ultra Wide SCSI Connector (JA4)

Pin Number	Function	Pin Number	Function
1	GND	35	-DB (12)
2	GND	36	-DB (13)
3	GND	37	-DB (14)
4	GND	38	-DB (15)
5	GND	39	Parity H
6	GND	40	-DB (0)
7	GND	41	-DB (1)
8	GND	42	-DB (2)
9	GND	43	-DB (3)
10	GND	44	-DB (4)
11	GND	45	-DB (5)
12	GND	46	-DB (6)
13	GND	47	-DB (7)
14	GND	48	Parity L
15	GND	49	GND
16	GND	50	Termpwrd
17	Termpwrd	51	Termpwrd
18	Termpwrd	52	Termpwrd
19	GND	53	NC
20	GND	54	GND
21	GND	55	-ATTN
22	GND	56	GND
23	GND	57	-BSY
24	GND	58	-ACK
25	GND	59	-RST
26	GND	60	-MSG
27	GND	61	-SEL
28	GND	62	-CD
29	GND	63	-REQ
30	GND	64	-10
31	GND	65	-DB (8)
32	GND	66	-DB (9)
33	GND	67	-DB (10)
34	GND	68	-DB (11)

Ultra160 SCSI Connector

Refer to Table 2-34 for pin definitions for the Ultra160 SCSI connector located at JA1.

Table 2-34 68-pin Ultra160 SCSI Connectors (JA1)

		1		
Connector			Connector	
Contact			Contact	
Number	Signal Names		Number	Signal Names
	•			·
1	+DB(12)		35	-DB(12)
2	+DB(13)		36	-DB(13)
3	+DB(14)		37	-DB(14)
4	+DB(15)		38	-DB(15)
5	+DB(P1)		39	-DB(P1)
6	+DB(0)		40	-DB(0)
7	+DB(0) +DB(1)		41	-DB(0) -DB(1)
8	+DB(1) +DB(2)		42	-DB(1)
9	+DB(2) +DB(3)		43	-DB(2)
10	+DB(3) +DB(4)		44	-DB(3) -DB(4)
11			44	
	+DB(5)			-DB(5)
12	+DB(6)		46	-DB(6)
13	+DB(7)		47	-DB(7)
14	+DB(P)		48	-DB(P)
15	GROUND		49	GROUND
16	DIFFSENS		50	GROUND
17	TERMPWR		51	TERMPWR
18	TERMPWR		52	TERMPWR
19	RESERVED		53	RESERVED
20	GROUND		54	GROUND
21	+ATN		55	-ATN
22	GROUND		56	GROUND
23	+BSY		57	-BSY
24	+ACK		58	-ACK
25	+RST		59	-RST
26	+MSG		60	-MSG
27	+SEL		61	-SEL
28	+C/D		62	-C/D
29	+REQ		63	-REQ
30	+1/0		64	-1/0
31	+DB(8)		65	-DB(8)
32	+DB(9)		66	-DB(9)
33	+DB(10)		67	-DB(10)
34	+DB(11)		68	-DB(11)
"	.55(,			55(,

2-10 Installing Software Drivers

After all the hardware has been installed you must install the software drivers. The necessary drivers are all included on the Supermicro CD that came packaged with your motherboard. After inserting this CD into your CDROM drive, the display shown in Figure 2-7 should appear. (If this display does not appear, click on the My Computer icon and then on the icon representing your CDROM drive. Finally, double click on the S "Setup" icon.)

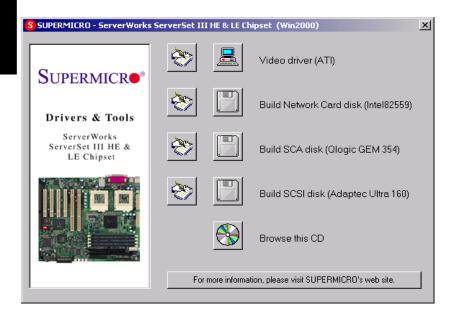


Figure 2-7. Driver/Tool Installation Display Screen

Click the icons showing a hand writing on paper to view the readme files for each item. The bottom icon with a CD on it allows you to view the entire contents of the CD.

Video driver (ATI): For the 370DL6 only.

Build Netword Card disk: For the S2DL3/370DL6/370DL3/370DLE.

<u>Build SCA disk (QLogic GEM 354):</u> For integration with the SuperServer SC850 and SC860 chassis.

Build SCSI disk (Ultra160): For the S2DL3/370DL6/370DL3 only.

Chapter 3 Troubleshooting

3-1 Troubleshooting Procedures

Use the following procedures to troubleshoot your system. If you have followed all of the procedures below and still need assistance, refer to the 'Technical Support Procedures' and/or 'Returning Merchandise for Service' section(s) in this chapter.

Note: Always disconnect the power cord before adding, changing or installing any hardware components.

Before Power On

- Make sure no short circuits exist between the motherboard and chassis.
- Disconnect all ribbon/wire cables from the motherboard, including those for the keyboard and mouse.
- 3. Remove all add-on cards.
- Install one CPU (making sure it is fully seated) and connect the chassis speaker and the power LED to the motherboard. (Check all jumper settings as well.)

No Power

- Make sure no short circuits exist between the motherboard and the chassis
- 2. Verify that all jumpers are set to their default positions.
- 3. Check that the 115V/230V switch on the power supply is properly set.
- 4. Turn the power switch on and off to test the system.
- 5. The battery on your motherboard may be old. Check to verify that it still supplies ~3VDC. If it does not, replace it with a new one.

No Video

- If the power is on but you have no video, remove all the add-on cards and cables.
- Use the speaker to determine if any beep codes exist. Refer to Appendix A for details on beep codes.

NOTE

If you are a system integrator, VAR or OEM, a POST diagnostics card is recommended. For I/O port 80h codes, refer to App. B.

Memory Errors

- 1. Make sure the DIMM modules are properly and fully installed.
- Determine if different speeds of DIMMs have been installed and verify that the BIOS setup is configured for the fastest speed of RAM used. It is recommended to use the same RAM speed for all DIMMs in the system.
- Make sure you are using PC133 or PC100 compliant, registered ECC, unbuffered SDRAM. EDO SDRAM is not supported.
- Check for bad DIMM modules or slots by swapping a single module between two slots and noting the results.
- 5. Make sure all memory modules are fully seated in their slots.
- 6. Check the power supply voltage 115V/230V switch.

Losing the System's Setup Configuration

- Check the setting of jumper JBT1. Ensure that you are using a high quality power supply. A poor quality power supply may cause the system to lose the CMOS setup information. Refer to page 1-19 for details on recommended power supplies.
- The battery on your motherboard may be old. Check to verify that it still supplies ~3VDC. If it does not, replace it with a new one.
- If the above steps do not fix the Setup Configuration problem, contact your vendor for repairs.

3-2 Technical Support Procedures

Before contacting Technical Support, please take the following steps. Also, note that as a motherboard manufacturer, Super Micro does not sell directly to end-users, so it is best to first check with your distributor or reseller for troubleshooting services. They should know of any possible problem(s) with the specific system configuration that was sold to you.

 Please go through the 'Troubleshooting Procedures' and 'Frequently Asked Question' (FAQ) sections in this chapter or see the FAQs on our web site (http://www.supermicro.com/techsupport.htm) before contacting Technical Support.

BIOS upgrades can be downloaded from our web site at http://www.supermicro.com/techsupport/download.htm.

Note: Not all BIOS can be flashed depending on the modifications to the boot block code.

- 3. If you still cannot resolve the problem, include the following information when contacting Super Micro for technical support:
 - Motherboard model and PCB revision number
 - •BIOS release date/version

(this can be seen on the initial display when your system first boots up)

System configuration

An example of a Technical Support form is on our web site at http://www.supermicro.com/techsupport/contact_support.htm.

4. Distributors: For immediate assistance, please have your account number ready when placing a call to our technical support department. We can be reached by e-mail at support@supermicro.com or by fax at (408) 895-2012.

3-3 Frequently Asked Questions

Question: What are the various types of memory that the S2DL3/370DL6/370DL3/370DLE motherboard can support?

Answer: The S2DL3/370DL6/370DL3/370DLE has four DIMM slots that support 168-pin, registered DIMMs with ECC only. Note that since the motherboard has a 133 MHz memory bus, both PC133 and PC100 memory are fully supported. **Note:** Unbuffered SDRAM or non-ECC memory is not supported.

Question: How do I update my BIOS?

Answer: It is recommended that you <u>do not</u> upgrade your BIOS if you are experiencing no problems with your system. Updated BIOS files are located on our web site at http://www.supermicro.com. Please check our BIOS warning message and the info on how to update your BIOS on our web site. Also, check the current BIOS revision and make sure it is newer than your BIOS before downloading. Select your motherboard model and download the BIOS file to your computer. Unzip the BIOS update file and you will find the readme.txt (flash instructions), the fwhflash.com (BIOS flash utility) and

the BIOS image (xxxxxx.rom) files. Copy these files onto a bootable floppy and reboot your system. It is not necessary to set BIOS boot block protection jumpers on the motherboard. At the DOS prompt, enter the command "fwhflash." This will start the flash utility and give you an opportunity to save your current BIOS image. Flash the boot block and enter the name of the update BIOS image file.

Note: It is important to save your current BIOS and rename it "super.rom" in case you need to recover from a failed BIOS update. Select flash boot block, then enter the update BIOS image. Select "Y" to start the BIOS flash procedure and do not disturb your system until the flash utility displays that the procedure is complete. After updating your BIOS, please clear the CMOS then load Optimal Values in the BIOS.

Question: After flashing the BIOS my system does not have video. How can I correct this?

Answer: If the system does not have video after flashing your new BIOS, it indicates that the flashing procedure failed. To remedy this, first clear CMOS per the instructions in this manual and retry the BIOS flashing procedure. If you still do not have video, please use the following BIOS Recovery Procedure. First, make sure jumper JP6 is disabled. Then, turn your system off and place the floppy disk with the saved BIOS image file (see above FAQ) in drive A. Press and hold <CTRL> and <Home> at the same time, then turn on the power with these keys pressed until your floppy drive starts reading. Your screen will remain blank until the BIOS program is done. If the system reboots correctly, then the recovery was successful. The BIOS Recovery Procedure will not update the boot block in your BIOS.

Question: Do I need the CD that came with your motherboard?

Answer: The supplied compact disc has quite a few drivers and programs that will greatly enhance your system. We recommend that you review the CD and install the applications you need. Applications on the CD include chipset drivers for Windows and security and audio drivers.

Question: Why can't I turn off the power using the momentary power on/off switch?

Answer: The instant power off function is controlled in BIOS by the Power Button Mode setting. When the On/Off feature is enabled, the motherboard

will have instant off capabilities as long as the BIOS has control of the system. When the Standby or Suspend feature is enabled or when the BIOS is not in control such as during memory count (the first screen that appears when the system is turned on), the momentary on/off switch must be held for more than four seconds to shut down the system. This feature is required to implement the ACPI features on the motherboard.

3-4 Returning Merchandise for Service

A receipt or copy of your invoice marked with the date of purchase is required before any warranty service will be rendered. You can obtain service by calling your vendor for a Returned Merchandise Authorization (RMA) number. When returning to the manufacturer, the RMA number should be prominently displayed on the outside of the shipping carton, and mailed prepaid or hand-carried. Shipping and handling charges will be applied for all orders that must be mailed when service is complete.

This warranty only covers normal consumer use and does not cover damages incurred in shipping or from failure due to the alternation, misuse, abuse or improper maintenance of products.

During the warranty period, contact your distributor first for any product problems.

Notes

Chapter 4 BIOS

4-1 Introduction

This chapter describes the AMIBIOS for the S2DL3/370DL6/370DL3/370DLE. The AMI ROM BIOS is stored in a Flash EEPROM and can be easily upgraded using a floppy disk-based program.

Configuration Data

The original IBM AT had 64 kbytes of non-volatile memory storage in CMOS RAM. All AT-compatible systems have at least 64 kbytes of CMOS RAM, which is usually part of the Real Time Clock. Many systems have 128 kbytes of CMOS RAM.

How Data Is Configured

AMIBIOS provides a Setup utility in ROM that is accessed by pressing at the appropriate time during system boot. Setup configures data in CMOS RAM.

POST Memory Test

Normally, the only visible POST routine is the memory test. The screen that appears when the system is powered on is shown on the next page.

A BIOS identification string is displayed at the left bottom corner of the screen below the copyright message.

4-2 BIOS Features

- Supports Plug and Play V1.0A and DMI 2.3
- Supports Intel PCI 2.2 (Peripheral Component Interconnect) local bus specification
- Supports Advanced Power Management (APM) specification v 1.2
- Supports ACPI
- Supports Flash ROM

AMIBIOS supports the LS120/zip drive:

- Can be used as a boot device.
- Is accessible as the next available floppy drive

AMIBIOS supports PC Health Monitoring chips. When a failure occurs in a monitored activity, AMIBIOS can sound an alarm and display a message. The PC Health Monitoring chips monitor:

- Four CPU temperatures
- System Overheat
- Chassis intrusion
- Four positive voltage inputs
- Four fan-speed monitor inputs

4-3 Running Setup

*Optimal default settings are in bold text unless otherwise noted.

The BIOS setup options described in this section are selected by choosing the appropriate text from the Standard Setup screen. All displayed text is described in this section, although the screen display is often all you need to understand how to set the options (see on next page).

AMIBIOS HIFLEX SETUP UTILITY VERSION 1.18

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STANDARD CMOS SETUP
ADVANCED CMOS SETUP
ADVANCED CHIPSET SETUP
POWER MANAGEMENT SETUP
PCI / PLUG AND PLAY SETUP
PERIPHERAL SETUP
AUTO-DETECT HARD DISKS
CHANGE USER PASSWORD
CHANGE SUPERVISOR PASSWORD
CHANGE LANGUAGE SETTING

AUTO CONFIGURATION WITH OPTIMAL SETTINGS
AUTO CONFIGURATION WITH FAIL-SAFE SETTINGS
SAVE SETTINGS AND EXIT
EXIT WITHOUT SAVING

Standard CMOS setup for changing time, date, hard disk type, etc.

Esc:Exit ↑↑↓↓:Sel F2/F3:Color F10:Save & Exit

AMIBIOS SETUP-STANDARD CMOS SETUP
(C)1998 American Megatrends, Inc. All Rights Reserved

Date mm/dd/yyyy):Thurs March 2,2000 Base Memory: 640KB Time (hh/mm/ss) :16:05:13 Extd Memory: 127MB

Floppy Drive A: 1.44MB 3½ Floppy Drive B: Not Installed

Type Size Cyln Head Wpcom Sec Mode Mode Mode Mode

Pri Master: Auto

Pri Slave: Not Installed Sec Master: Not Installed Sec Slave: Not Installed

Boot Sector Virus Protection Disabled

Standard CMOS Setup

Date and Time Configuration

Select the Standard option. Select the *Date/Time* icon. The current values for each category are displayed. Enter new values through the keyboard.

Floppy A Floppy B

Choose the Floppy Drive A or B icon to specify the floppy drive type. The settings are Not Installed, 360 KB 5½ inch, 1.2 MB 5½ inch, 720 KB 3½ inch,1.44 MB 3½ inch or 2.88 MB 3½ inch. Note: The Optimal and Fail-Safe settings for Floppy Drive A are 1.44 MB 3 1/2 inch and for Floppy Drive B are Not Installed.

Pri Master Pri Slave Sec Master Sec Slave

Type

How to Configure

Type

Select *Type*. The options are 1-46, User, Auto, CDROM, ARMD. 1-46 indicates the prefined type of the parameters. Select Enter to enter the parameter type manually. If Auto is selected, the parameter type will be set automatically on each boot. Select CDROM when ATAPI CDROM drives are used. Select ARMD if LS120, MO, Iomega Zip drives are used, or Press enter to let the BIOS autodetect the parameter type.

Entering Drive Parameters

You can also enter the hard disk drive parameters. The drive parameters are:

Parameter	Description
Туре	The number for a drive with certain identification parameters.
Cylinders	The number of cylinders in the disk drive.
Heads	The number of heads.
WPCOM	The size of a sector gets progressively smaller as the track diameter diminishes. Yet each sector must still hold 512 bytes. WPCOM circuitry on the hard disk compensates for the physical difference in sector size by boosting the write current for sectors on inner tracks. This parameter is the track number where WPCOM begins.
Sectors	The number of sectors per track. MFM drives have 17 sectors per track. RLL drives have 26 sectors per track. ESDI drives have 34 sectors per track. SCSI and IDE drive may have even more sectors per track.

Boot Sector Virus Protection

This setting allows you to prevent any data from being written the boot sector of the hard drive. While this may prevent viruses from infecting your system, you may need to change information here when installing new programs. The options for this setting are *Enabled* or *Disabled*.

Advanced CMOS Setup

Quick Boot

The Settings are *Disabled* or *Enabled*. Set to *Enabled* to permit AMIBIOS to boot quickly when the computer is powered on. This option replaces the old Above 1 MB Memory Test Advanced Setup option. The settings are:

<u>Setting</u>	Description
Disabled	AMIBIOS tests all system memory. AMIBIOS waits up to 40
	seconds for a READY signal from the IDE hard disk drive.
	AMIBIOS waits for .5 seconds after sending a RESET
	signal to the IDE drive to allow the IDE drive time to get
	ready again. AMIBIOS checks for a key press and
	runs AMIBIOS setup if the key has been pressed.

Enabled

AMIBIOS does not test system memory above 1 MB.

AMIBIOS does not wait up to 40 seconds for a

READY signal from the IDE hard disk drive. If a READY
signal is not received immediately from the IDE drive,

AMIBIOS does not configure that drive. AMIBIOS does not
wait for .5 seconds after sending a RESET signal to the
IDE drive to allow the IDE drive time to get ready again. In
Enabled, the keyboard will be bypassed.

Note: The AMIBIOS Setup can be run at system boot but no display is given.

Pri Master ARMD Emulated as Pri Slave ARMD Emulated as Sec Master ARMD Emulated as Sec Slave ARMD Emulated as

The settings for these options are *Auto*, *Floppy* or *Hard disk*. If set to Auto, the default emulation type depends on the ARMD drive. The default emulation type is floppy for LS120, Hard Disk for MO and Hard Disk for lomega Zip.

1st Boot Device 2nd Boot Device 3rd Boot Device

The options for the 1st Boot Device are Disabled, 1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD, 4th IDE-HDD, Floppy, ARMD-FDD, ARMD-HDD, ATAPI CDROM, SCSI, Network or I_2O . The options for the 2nd Boot Device are Disabled, 1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD, 4th IDE-HDD, Floppy, ARMD-FDD, ARMD-HDD, ATAPI CDROM or SCSI. The options for the 3rd Boot Device are Disabled, 1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD, 4th IDE-HDD, Floppy, ARMD-FDD, ARMD-HDD or ATAPI CDROM.

1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD and 4th IDE-HDD are the four hard disks that can be installed by the BIOS. 1st IDE-HDD is the first hard disk installed by the BIOS, 2nd IDE-HDD is the second hard disk, and so on. For example, if the system has a hard disk connected to Primary Slave and another hard disk to Secondary Master, then 1st IDE-HDD will be referred to as the hard disk connected to Primary Slave and 2nd IDE-HDD will be referred to as the hard disk connected to the Secondary Master. 3rd IDE-HDD and 4th IDE-HDD are not present. Note that the order of the initialization of the devices connected to the primary and secondary channels are Primary Master first, Primary Slave second, Secondary Master third, and Secondary Slave fourth.

The BIOS will attempt to read the boot record from 1st, 2nd, 3rd and 4th boot device in the selected order until it is successful in reading the booting record. The BIOS will not attempt to boot from any device which is not selected as the boot device.

Try Other Boot Devices

This option controls the action of the BIOS if all the selected boot devices failed to boot. The settings for this option are **Yes** or **No**. If **Yes** is selected, the BIOS will try to boot from the other boot devices that are present in the setup but not selected if all selected Boot Devices failed to boot. If **No** is selected, the BIOS will <u>not</u> try to boot from the other boot devices when all selected boot devices failed to boot.

Initialize I2O Devices

The settings for this option are **Yes** or *No.* If **Yes** is selected, the BIOS will initialize I2O processor(s), I2O storage devices and provide INT13 support for I2O storage devices. If *No is* selected, the BIOS will not initialize I2O processor(s) and I2O storage devices.

Initial Display Mode

This option determines the display screen with which the POST is going to start the display. The settings for this option are *BIOS* or *Silent*. If selected as *BIOS*, the POST will start with the normal sign-on message screen. If *Silent* is selected, the POST will start with the Supermicro screen.

Display Mode at Add-On ROM Init

The settings for this option are *Force BIOS* or *Keep Current*. If *Force Bios* is selected, the Add-on ROM will take control of the POST screen.

Floppy Access Control

The settings for this option are *Read-Write* or *Read-Only*. This option will be effective only if the device is accessed through BIOS.

Hard Disk Access Control

The settings for this option are *Read-Write* or *Read-Only*. This option will be effective only if the device is accessed through BIOS.

S.M.A.R.T. for Hard Disks

S.M.A.R.T. (Self-Monitoring, Analysis and Reporting Technology) is a technology developed to manage the reliability of the hard disk by predicting future device failures. The hard disk needs to be S.M.A.R.T. capable. The settings for this option are *Disabled* or *Enabled*. Note: **S.M.A.R.T.** cannot predict all future device failures. **S.M.A.R.T.** should

be used as a warning tool, not as a tool to predict the device reliability.

Boot Up Num-Lock

Settings for this option are **On** or **Off**. When this option is set to **On**, the BIOS turns off the Num Lock key when the system is powered on. This will enable the end user to use the arrow keys on both the numeric keypad and the keyboard.

PS/2 Mouse Support

Settings for this option are *Enabled* or *Disabled*. When this option is set to *Enabled*, AMIBIOS supports a PS/2-type mouse.

Primary Display

The settings for this option are Absent, VGA/EGA, CGA 40x25, CGA 80x25 or Mono.

Password Check

This option enables the password check option every time the system boots or the end user runs WinBIOS Setup. If *Always* is chosen, a user password prompt appears every time the computer is turned on. If *Setup* is chosen, the password prompt appears if WinBIOS Setup is executed.

Boot to OS/2

If DRAM size is over 64 MB, set this option to *Yes* to permit AMIBIOS to run with IBM OS/2. The settings are *No* or *Yes*.

CPU Microcode Updation

This option allows the BIOS to update the CPU Microcode. The settings for this option are *Disabled and Enabled*.

Processor Serial Number

Intel included a serial number in their Pentium III/Pentium III Xeon Processors as a unique system identifier. Select *Enabled* to allow Processor's Serial Number to be detected by the application software programs. For privacy reasons, you can disable this setting to prevent the release of this identifier. The settings for this option are *Enabled* or *Disabled*.

Internal Cache (L1 Cache)

This option is for enabling or disabling the internal cache memory. The settings for this option are *Disabled*, *WriteThru* or *WriteBack*.

External Cache (L2 Cache)

This option is for enabling or disabling the external cache memory. The settings for this option are *Disabled*, *WriteThru* or *WriteBack*.

System BIOS Cacheable

When set to *Enabled*, the contents of the F0000h system memory segment can be read from or written to cache memory. The contents of this memory segment are always copied from the BIOS ROM to system RAM for faster execution. The settings are *Enabled* or *Disabled*. *Note: The Optimal default setting is Enabled and the Fail-Safe default*

setting is Disabled. Set this option to Enabled to permit the contents of F0000h RAM memory segment to be written to and read from cache memory.

C000 Shadow (16K) (Cached)

C400 Shadow (16K) (Cached)

C800 Shadow (16K) (Cached)

CC00 Shadow (16K) (Cached)

D000 Shadow (16K)

D400 Shadow (16K)

D800 Shadow (16K)

DC00 Shadow (16K)

These options specify how the 16 KB of video ROM at C0000h (or D0000h) is treated. The settings are: *Disabled, Enabled or Cached.* The default is *Disabled* for all settings except C000, C400, C8000, CC00 which are *Cached* for default. When set to *Disabled,* the contents of the video ROM are not copied to RAM. When set to *Enabled,* the contents of the video ROM area from C0000h-CFFFFh (or D0000h-D7FFFh) are copied (shadowed) from ROM to RAM for faster execution. When set to *Cached,* the contents of the video ROM area from C0000h-C7FFFh (or D0000h-D7FFFh) are copied from ROM to RAM, and can be written to or read from cache memory.

Advanced Chipset Setup

USB Function

The settings for this option are *Enabled* or *Disabled*. Set this option to *Enabled* to enable the USB (Universal Serial Bus) functions.

Port 64/60 Emulation:

The settings for this option are *Enabled* or *Disabled*.

The main memory system of the CNB30 supports various clock speeds and memory speeds. The MTCR (Memory Timing Control Register) dictates the memory controller to generate the DRAM timing accordingly.

Act to Deact

The settings for this option are 6CLKS or 5CLKS.

Act to Read/Write

The settings for this option are 3CLKS or 2CLKS.

RAS Precharge Time

This option defines the RAS Precharge Time. The settings are 3 CLKS or 2 CLKS.

RAS Cycle Time

This option defines the RA Cycle Time. The settings are 10CLKS, 9CLKS, 8CLKS, 7CLKS.

Write to DeAct

The settings for this option are 2CLKS and 1CLKS.

SDRAM CAS Latency

The settings for this option are CAS Latency3 and CAS Latency2.

ISA IO Cycle Delay

The settings for this option are Full Delay, 1.5 BCLK, 2.5 BCLK and 3.5 BLK

MPS 1.4 Support

The settings for this option are *Enabled* and *Disabled*. Select "Enabled" to activate Multi-Processor System Support.

Power Management

ACPI Aware O/S

The settings for this option are *No* or *Yes*. Available with ACPI only. The operating system has the built-in ACPI features. Select "Yes" to permit the OS to detect the ACPI functions in the system.

Power Management/APM

The settings for this option are *Enabled* and *Disabled*. If "enabled" is selected, the Power Management/Advanced Power Management mode (and the following options) will be activated.

Video Power Down Mode

When in the AMP mode, this option specifies the power conserving state that the VGA video subsystem enters after the specified period of display inactivity has expired. The settings are *Disabled* and *Suspend*. *Note:* The Optimal default setting for this option is Suspend and the Fail-Safe default setting is Disabled.

Hard Disk Power Down Mode

When in the AMP mode, this option specifies the power conserving state that the hard disk drive enters after the specified period of hard drive inactivity has expired. The settings are *Disabled* and *Suspend*. *Note:* The Optimal default setting for this option is Suspend and the Fail-Safe default setting is Disabled.

Hard Disk Time Out (Minutes)

When in the AMP mode, this option specifies the length of a period of hard disk drive inactivity. When this length of time expires, the computer enters the power-conserving state specified in the Hard Disk Power Down Mode option. The settings are *Disabled* and *1 Min* through *14 Min* in 1 minute increments.

Suspend Time Out

When in the AMP mode, this option specifies the length of a period of system inactivity while in the suspend state. When this length of time expires, the computer enters a suspend power. The settings are Disabled and 1 Min through 14 Min in 1 minute increments. The default setting is 5.

Power Button Enable

When in the AMP mode, this in the AMP mode, this option specifies how the power button mounted externally on the computer chassis is used. The settings are: Suspend, PowerOn and PowerOff. When set to PowerOn or PowerOff, pushing the power button turns the computer on or off. The Suspend setting places the computer in Suspend mode or Full On power mode.

Suspend State

The settings for this option are C3 State and S1State.

Sleep Button Enable

The settings for this option are Suspend and Disable.

The BIOS has the capability to detect the IRQ events. When the BIOS detects an IRQ trigger event being activated, then, the system will "wake up" and resumes its activities.

IRQ1:

The settings are: Ignore, and Monitor.

IRQ3:

The settings are: Ignore, and Monitor.

IRQ4:

The settings are: Ignore, and Monitor.

IRQ5:

The settings are: Ignore, and Monitor.

IRQ6:

The settings are: Ignore, and Monitor.

IRQ7:

The settings are: Ignore, and Monitor.

IRQ9:

The settings are: Ignore, and Monitor.

IRQ10:

The settings are: Ignore, and Monitor.

IRQ11:

The settings are: Ignore, and Monitor.

IRQ12:

The settings are: Ignore, and Monitor.

IRQ14:

The settings are: Ignore, and Monitor.

IRQ15:

The settings are: Ignore, and Monitor.

USB Resume

When in the AMP mode, this option allows you to wake up the system from a USB device. The settings for this option are *Enabled* and *Disabled*.

PME Resume

When in the AMP mode, this option allows you to wake up the system from a PME device. The settings for this option are *Enabled* and *Disabled*.

R1 Resume

When in the AMP mode, this option allows you to wake up the system from a R1 device. The settings for this option are *Enabled* and *Disabled*.

PCI/Plug and Play Setup

Plug and Play-Aware OS

The settings for this option are $\it No$ or $\it Yes$. Set this option to $\it Yes$ to allow the operating system to detect ISA Plug and Play devices. (Since the S2QR6 has no ISA slots, this should always be set to $\it No$.

PCI Latency Timer (PCI Clocks)

This option specifies the latency timings in PCI clocks for all PCI devices. The settings are 32, 64, 96, 128, 160, 192, 224, or 248.

PCI VGA Palette Snoop

The settings for this option are *Disabled* or *Enabled*. When set to *Enabled*, multiple VGA devices operating on different buses can handle data from the CPU on each set of palette registers on every video device. Bit 5 of the command register in the PCI device configuration space is the VGA Palette Snoop bit (0 is disabled). For example: if there are two VGA devices in the computer (one PCI and one ISA) and this option is disabled, data read and written by the CPU is only directed to the PCI VGA device's palette registers. If enabled, data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA palette registers. This will permit the palette registers of both devices to be identical. This option must be set to *Enabled* if any ISA adapter card installed in the system requires VGA palette snooping.

PCI IDE Busmaster

The settings for this option are *Disabled* or *Enabled*. Set to *Enabled* to specify the IDE Controller on the PCI bus has bus mastering capabilities. Under Windows 95, you should set this option to *Disabled* and install the Bus Mastering driver.

Offboard PCI IDE Card

This option specifies if an offboard PCI IDE controller adapter card is installed in the computer. The PCI expansion slot on the motherboard where the offboard PCI IDE controller is installed must be specified. If an offboard PCI IDE controller is used, the onboard IDE controller is automatically disabled. The settings are *Auto* (AMIBIOS automatically determines where the offboard PCI IDE controller adapter card is installed), *Slot 1*, *Slot 2*, *Slot 3*, *Slot 4*, *Slot 5* and *Slot 6*.

This option forces IRQ14 and IRQ15 to a PCI slot on the PCI local bus. This is necessary to support non-compliant ISA IDE controller adapter cards. If an offboard PCI IDE controller adapter card is installed in the computer, you must also set the Offboard PCI IDE Primary IRQ and Offboard PCI IDE Secondary IRQ options.

Offboard PCI IDE Primary IRQ Offboard PCI IDE Secondary IRQ

These options specify the PCI interrupt used by the primary (or secondary) IDE channel on the offboard PCI IDE controller. The settings are **Disabled**, Hardwired, INTA, INTB, INTC, and INTD.

Onboard USB IRQ

Use these options to specify the IRQ priority for Onboard USB devices installed in the PCI expansion slots. The settings are *Auto*, (IRQ) 3, 4, 5, 7, 9, 10, and 11, in priority order.

PCI Slot 1 through Slot 4 IRQ

Use these options to specify the IRQ priority for PCI devices installed in the PCI expansion slots. The settings are **Auto**, (IRQ) 3, 4, 5, 7, 9, 10, and 11 in priority order.

Onboard LAN IRQ

Use these options to specify the IRQ priority for Onboard LAN devices installed in the PCI expansion slots. The settings are *Auto*, (IRQ) 3, 4, 5, 7, 9, 10, and 11 in priority order.

PCI Slot 5, PCI Slot 6 and Onboard SCSI IRQ

Use these options to specify the IRQ priority for PCI Slots 5 and 6 and Onboard SCSI devices installed in the PCI expansion slots. The settings are *Auto*, (IRQ) 3, 4, 5, 7, 9, 10, and 11 in priority order.

PCI Slot 4 IRQ

PCI Slot 5 IRQ

PCI Slot 6 IRQ

PCI Slot 7 IRQ

PCI Slot 8 IRQ

Use these options to specify the IRQ priority for PCI devices installed in the PCI expansion slots. The settings are **Auto**, (IRQ) 3, 4, 5, 7, 9, 10, and 11 in priority order.

DMA Channel 0

DMA Channel 1

DMA Channel 3

DMA Channel 5

DMA Channel 6

DMA Channel 7

These DMA channels control the data transfers between the I/O devices and the system memory. The chipset allows the BIOS to choose which channels to do the job. The settings are *PnP* or *ISA/EISA*.

IRQ3

IRQ4

IRQ5

IRQ7

IRQ9

IRQ10

IRQ11 IRQ14

IRQ15

These options specify which bus the specified IRQ line is used on and allow you to reserve IRQs for legacy ISA adapter cards. If more IRQs must be removed from the pool, the end user can use these options to reserve the IRQ by assigning an *ISA/EISA* setting to it. Onboard I/O is configured by AMIBIOS. All IRQs used by onboard I/O are configured as PCI/PnP.

IRQ14 and 15 will not be available if the onboard PCI IDE is enabled. If all IRQs are set to *ISA/EISA* and IRQ14 and 15 are allocated to the onboard PCI IDE, IRQ 9 will still be available for PCI and PnP devices. This is

because at least one IRQ must be available for PCI and PnP devices. The settings are *PCI/PnP* or *ISA/EISA*. (See Chapter 3 for information on shared IRQs.)

Reserved Memory Size

This option specifies the size of the memory area reserved for legacy ISA adapter cards. The settings are *Disabled*, 16K, 32K or 64K.

Reserved Memory Address

This option specifies the beginning address (in hex) of the reserved memory area. The specified ROM memory area is reserved for use by legacy ISA adapter cards. The settings are *C0000*, *C4000*, *C8000*, *CC000*, *D0000*, *D4000*, *D8000* or *DC000*.

Peripheral Setup

Onboard SCSI

This setting enables or disables the onboard SCSI. The settings are *Enabled* and *Disabled*.

Onboard LAN

This setting enables or disables the onboard LAN. The settings are **Enabled** and **Disabled**.

Power Lost Control

This setting determines how the system will respond when lost power is restored. The settings are *Always On* and *Always Off*.

Reset Button

This setting enables or disables the system reset button. The settings are *Enabled* and *Disabled*.

CPU1 Current Temperature

The current temperature of CPU1 is displayed here.

CPU2 Current Temperature

The current temperature of CPU2 is displayed here.

System Overheat Warning

The settings for this option are *Enabled* or *Disabled*. When set to *Enabled* this option allows the user to set an overheat warning temperature.

Overheat Warning Temperature

Use this option to set the CPU overheat warning temperature. The settings are 25 °C through 75 °C in 1 °C intervals. Note: The Optimal and Fail-Safe default settings are 55 °C.

H/W Monitor CPU H/W H/WMonitor (+5V) H/W Monitor (+12V) CPU1 Fan CPU2 Fan

The above features are for PC Health Monitoring. The motherboards with W83781D have seven onboard voltage monitors for the CPU core, CPU I/O, +3.3V, +5V, -5V, +12V, and-12V, and for the four-fan status monitor.

OnBoard FDC

This option enables the FDC (Floppy Drive Controller) on the motherboard. The settings are *Auto, Disabled* and *Enabled*.

OnBoard Serial Port1

This option specifies the base I/O port address of serial port 1. The settings are *Disabled*, *3F8h*, *2F8h*, *3E8h* and *2E8h*.

OnBoard Serial Port2

This option specifies the base I/O port address of serial port 2. The settings are *Disabled*, *3F8h*, *2F8h*, *3E8h* and *3BC*.

Onboard Parallel Port

This option specifies the base I/O port address of the parallel port on the motherboard. The settings are *Auto* (AMIBIOS automatically determines the correct base I/O port address), *Disabled*, *378h*, *278h* and *38Ch*.

Parallel Port Mode

This option specifies the parallel port mode. The settings are *Normal*, *Bi-Dir*, *EPP* and *ECP*. When set to *Normal*, the normal parallel port mode is used. Use *Bi-Dir* to support bidirectional transfers. Use *EPP* (Enhanced Parallel Port) to provide asymmetric bidirectional data transfer driven by the host device. Use *ECP* (Extended Capabilities Port) to achieve data transfer rates of up to 2.5 Mbps. ECP uses the DMA protocol and provides symmetric bidirectional communication.

EPP Version

The settings are Enabled and Disabled. Note: The Optimal and Fail-Safe default settings are N/A.

Parallel Port IRQ

This option specifies the IRQ to be used by the parallel port. The settings are 5 and 7.

Parallel Port ECP DMA Channel

This option is only available if the setting of the parallel port mode option is *ECP*. The settings are 0, 1, 2, 3, 5, 6 and 7.

Onboard IDE

This option enables the IDE (Hard Disk Drive Controller) device(s) on the motherboard. The options are *Enabled* and *Disabled*.

Auto-Detect Hard Disks

This section allows BIOS to look for and configure any hard disk drives on your system. After highlighting this option, hit <Enter> and wait momentarily while BIOS performs the auto-detect. You will soon see the disk drives appear properly configured.

Change User Password

Change Supervisor Password

The system can be configured so that all users must enter a password every time the system boots or when the AMIBIOS setup is executed. You can set either a Supervisor password or a User password. If you do not want to use a password, just press <Enter> when the password prompt appears.

The password check option is enabled in the Advanced Setup by choosing either *Always* or *Setup*. The password is stored in CMOS RAM. You can enter a password by typing it out on the keyboard or by selecting each letter via the mouse or a pen stylus. Pen access must be customized for each specific hardware platform.

When you select to change the Supervisor or User password, AMIBIOS prompts you for the new password. You must set the Supervisor password before you can set the User password. Enter a 1-6 character password. (It will not appear on the screen when typed.) Retype the new password as prompted and press <Enter>. Make sure you write it down. If you forget it, you must clear CMOS RAM and reset the password.

Change Language Setting

Because this version of BIOS only supports English at this time, this setting cannot be chosen. Future releases may support other languages.

Auto Configuration with Optimal Settings

The Optimal default settings provide optimum performance settings for all devices and system features.

Auto Configuration with Fail Safe Settings

The Fail-Safe default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance characteristics.

Save Current Settings and Exit

Highlight this and hit <Enter> when you wish to save any changes made to settings in BIOS and exit back to the system boot-up procedure.

Exit Without Saving

Highlight this and hit <Enter> when you wish to exit back to the system boot-up procedure without saving any changes.

Notes

Appendix A BIOS Error Beep Codes & Messages

During the POST (Power-On Self-Test) routines, which are performed each time the system is powered on, errors may occur.

Non-fatal errors are those which, in most cases, allow the system to continue the boot-up process. The error messages normally appear on the screen.

Fatal errors are those which will not allow the system to continue the boot-up procedure. If a fatal error occurs, you should consult with your system manufacturer for possible repairs.

These fatal errors are usually communicated through a series of audible beeps. The numbers on the fatal error list, on the following page, correspond to the number of beeps for the corresponding error. All errors listed, with the exception of #8, are fatal errors.

AMIBIOS Error Beep Codes

1 beep: System needs to update BIOS. Insert the diskette in that has the system BIOS file (SUPER.ROM) in the root directory.

2 beeps: BIOS file (SUPER.ROM) absent or not in root directory.

4 beeps: Flash program successful.

5 beeps: Floppy read error.

7 beeps: No flash part detected. The BIOS cannot be updated.

8 beeps: The ROM checksum value does not match the value encoded in the BIOS.

10 beeps: Flash erase error.

11 beeps: Flash program error.

12 beeps: Wrong BIOS file size.

13 beeps: ROM image mismatch.

If you hear	it's because
5 short and 1 long beeps	no memory is installed
6 short and 1 long beeps	EDO memory detected
7 short and 1 long beeps	SMBUS (System Manage- ment Bus) error

Notes

Appendix B

AMIBIOS POST Diagnostic Error Messages

This section describes the power-on self-tests (POST) port 80 codes for the AMIBIOS.

Check <u>Point</u>	Description
00	Code copying to specific areas is done. Passing control to INT 19h boot loader next.
03	NMI is Disabled. Next, checking for a soft reset or a power-on condition.
05	The BIOS stack has been built. Next, disabling cache memory.
06	Uncompressing the post code unit next.
07	Next, initializing the CPU init and the CPU data area.
08	The CMOS checksum calculation is done next.
0B	Next, performing any required initialization before keyboard BAT command is issued.
0C	The keyboard controller I/B is free. Next, issuing the BAT command to the keyboard controller.
0E	The keyboard controller BAT command result has been verified. Next, performing any necessary initialization after the keyboard controller BAT command test.
0F	The initialization after the keyboard controller BAT command test is done. The keyboard command byte is written next.

Check <u>Point</u>	Description
10	The keyboard controller command byte is written. Next, issuing the pin 23 and 24 blocking and unblocking commands.
11	Next, checking if the <end <ins="" or=""> keys were pressed during power on. Initializing CMOS RAM if the Initialize CMOS RAM in every boot AMIBIOS POST option was set in AMIBCP or the <end> key was pressed.</end></end>
12	Next, disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2.
13	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.
14	The 8254 timer test will begin next.
19	The 8254 timer test is over. Starting the memory refresh test next.
1A	The memory refresh test line is toggling. Checking the 15 second on/off time next.
23	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24	The configuration required before interrupt vector initialization has completed. Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.
25	Interrupt vector initialization is done. Clearing the password if the POST DIAG Switch is on.
27	Any initialization before setting video mode will be done next.

Check Point	Description
28	Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.
2A	Bus initialization system, static, output devices will be done next, if present.
2B	Passing control to the video ROM to perform any required configuration before the video ROM test.
2C	All necessary processing before passing control to the video ROM is done. Looking for the video ROM next and passing control to it.
2D	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control.
2E	Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2F	The EGA/VGA controller was not found. The display memory read/write test is about to begin.
30	The display memory read/write test passed. Look for retrace checking next.
31	The display memory read/write test or retrace checking failed. Performing the alternate display memory read/write test next.
32	The alternate display memory read/write test passed. Looking for alternate display retrace checking next.
34	Video display checking is over. Setting the display mode next.
37	The display mode is set. Displaying the power on message next.

Check <u>Point</u>	Description
38	Initializing the bus input, IPL, and general devices next, if present.
39	Displaying bus initialization error messages.
3A	The new cursor position has been read and saved. Displaying the Hit message next.
40	Preparing the descriptor tables next.
42	The descriptor tables are prepared. Entering protected mode for the memory test next.
43	Entered protected mode. Enabling interrupts for diagnostics mode next.
44	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.
46	The memory wraparound test has completed. The memory size calculation has been completed. Writing patterns to test memory next.
47	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory next.
48	Patterns written in base memory. Determining the amount of memory below 1 MB next.
49	The amount of memory below 1 MB has been found and verified. Determining the amount of memory above 1 MB memory next.
4B	The amount of memory above 1 MB has been found and verified. Checking for a soft reset and clearing the memory below 1 MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.

Check Point	Description
4C	The memory below 1 MB has been cleared via a soft reset. Clearing the memory above 1 MB next.
4D	The memory above 1 MB has been cleared via a soft reset. Saving the memory size next. Going to checkpoint 52h next.
4E	The memory test started, but not as the result of a soft reset. Displaying the first 64 KB memory size next.
4F	The memory size display has started. The display is updated during the memory test. Performing the sequential and random memory test next.
50	The memory below 1 MB has been tested and initialized. Adjusting the displayed memory size for relocation and shadowing next.
51	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1 MB next.
52	The memory above 1 MB has been tested and initialized. Saving the memory size information next.
53	The memory size information and the CPU registers are saved. Entering real mode next.
54	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57	The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.
58	The memory size was adjusted for relocation and shadowing. Clearing the Hit message next.
59	The Hit message is cleared. The <wait> message is displayed. Starting the DMA and interrupt controller test next.</wait>

Check <u>Point</u>	Description
60	The DMA page register test passed. Performing the DMA Controller 1 base register test next.
62	The DMA controller 1 base register test passed. Performing the DMA controller 2 base register test next.
65	The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
66	Completed programming DMA controllers 1 and 2. Initializing the 8259 interrupt controller next.
7F	Extended NMI source enabling is in progress.
80	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
81	A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
82	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83	The command byte was written and global data initialization has been completed. Checking for a locked key next.
84	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85	The memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next.
86	The password was checked. Performing any required programming before WINBIOS Setup next.

Check <u>Point</u>	Description
87	The programming before WINBIOS Setup has been completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next.
88	Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next.
89	The programming after WINBIOS Setup has been completed. Displaying the power-on screen message next.
8B	The first screen message has been displayed. The <wait> message is displayed. Performing the PS/2 mouse check and extended BIOS data area allocation check next.</wait>
8C	Programming the WINBIOS Setup options next.
8D	The WINBIOS Setup options are programmed. Resetting the hard disk controller next.
8F	The hard disk controller has been reset. Configuring the floppy drive controller next.
91	The floppy drive controller has been configured. Configuring the hard disk drive controller next.
95	Initializing the bus option ROMs from C800 next.
96	Initializing before passing control to the adaptor ROM at C800.
97	Initialization before the C800 adaptor ROM gains control has been completed. The adaptor ROM check is next.
98	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.

Check <u>Point</u>	<u>Description</u>
99	Any initialization required after the option ROM test has been completed. Configuring the timer data area and printer base address next.
9A	Set the timer and printer base addresses. Setting the RS-232 base address next.
9B	Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next.
9C	Required initialization before the Coprocessor test is over. Initializing the Coprocessor next.
9D	Coprocessor initialized. Performing any required initialization after the Coprocessor test next.
9E	Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.
A2	Displaying any soft errors next.
A3	The soft error display has completed. Setting the keyboard typematic rate next.
A4	The keyboard typematic rate is set. Programming the memory wait states next.
A5	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7	NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.
A8	Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next.

Check <u>Point</u>	Description
A9	Returned from adaptor ROM at E000h control. Next, performing any initialization required after the E000 option ROM had control.
AA	Initialization after E000 option ROM control has completed. Displaying the system configuration next.
AB	Building the multiprocessor table, if necessary. POST next.
В0	The system configuration is displayed.
AC	Uncompressing the DMI data and initializing DMI.
B1	Copying any code to specific areas.
D0h	The NMI is disabled. Power on delay is starting. Next, the initialization cade checksum will be verified.
D1h	Initializing the DMA controller. Performing the keyboard controller BAT test. Starting memory refresh, and entering 4 GB flat mode next.
D3h	Starting memory sizing next.
D4h	Returning to real mode. Executing any OEM patches and setting the stack next.
D5h	Passing control to the uncompressed code in shadow RAM at E000:0000h. The initialization code is copied to segment 0 and control will be transferred to segment 0.
D6h	Control is in segment 0. Next, checking if <ctrl><home>was pressed and verifying the system BIOS checksum.</home></ctrl>
	If either <ctrl><home> was pressed or the system BIOS checksum is bad, next the system will go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.</home></ctrl>

Notes