USER'S MANUAL

RHINO 5

Pentium PCI Local Bus Motherboard

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Version 1.0 August 1995

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Preface

About the Rhino 5

Thank you for purchasing the Rhino 5, Ocean's new top-of-the-line Pentium motherboard. The Rhino 5 utilizes advanced PCI architecture that takes personal computing to a new level of performance.

About the Manual

The content of this manual is for reference only and is intended to provide basic information for the general user. Technical information is also included in the Appendix for hardware and software engineers.

This manual provides information about the installation and maintenance of the Octek Rhino 5 motherboard.

Table of Contents

Preface

Chapter 1: System Overview

Chapter 2: Installation and Upgrade

Appendix-A: Advanced Technical Information

Appendix-B: Connectors Pinout

Appendix-C: Hardware Settings

CHAPTER 1

SYSTEM OVERVIEW

OCTEK RHINO 5 is a powerful PC machine offering unparalleled performance. The advanced external cache system implemented meets the demand of the most memory-intensive applications today. With the Pentium processor and a high bandwidth 32-bit PCI expansion bus, the I/O bottleneck that plagues most PC systems is now removed.

All of the I/O is integrated inside the mainboard to further facilitate system installation. The built-in IDE can support up to 4 fast Enhanced IDE devices whereas it can also support up to two floppy drives. The mainboard also includes two serial ports and one parallel port as the basic configuration for end user. All that is needed is just a VGA card plugged into a PCI or ISA slot to complete the whole system.

1.1 General Specifications Overview

Processor:

◆ Processor Type	Intel Pentium CPU including P54C, P54CQS, P54CS, P55C and future upgrades CPU
◆ External CPU clock	50/60/66 Mhz

Chipset:

◆ Motherboard chipset	Opti Viper-M PCI/ISA Pentium motherboard chipset
◆ Super I/O chipset	SMC 665/669 super I/O chipset

Cache Architecture:

◆ Internal Cache	8KB data cache 8KB code cache
◆ External Cache	256KB/ 512KB/ 1MB asynchronous 3V/Mixed voltage SRAM

Memory Subsystem:

◆ DRAM SIMM sockets	4 x 72 pin 4MB / 8MB / 16MB / 32MB DRAM modules
◆ Max. Memory Size	128MB
◆ Enhancement	Fast Page Mode or EDO DRAM supported

Input/Output Subsystem

◆ PCI bus slots	3 x 32-bit PCI Bus slots (3 masters)
◆ ISA bus slots	3 x 16-bit ISA slots
◆ shared bus slots	1 x 32 bit PCI bus slot (master) OR 1 x 16-bit ISA slot
◆ I/O bus speed	Up to 33MHz (PCI bus)

Integrated IDE, Super I/O Subsystem

◆ IDE support to	Chipset built-in PCI IDE support up 4 IDE Drives
◆ On board I/O	One Floppy Port supporting 2 floppy drives of 360 / 720 / 1.44M/ 2.88M capacity. Two serial ports (16550 Fast UART compatibles) One parallel Port (Standard, ECP, EPP support)

PS/2 Mouse

◆ PS/2 Mouse	Supports PS/2 Mouse through a 2x4 header

Power Management

◆ Green functions	Support various Power Management schemes

BIOS Subsystem

◆ BIOS Type	AWARD
◆ BIOS Shadowing	Shadow RAM for System and Video BIOS
◆ BIOS Features	Built-in setup, Power-on self test, Drive table optimization, User-definable drive types, Password protection, Shadowing options

Plug & Play / BIOS Update

◆ Plug & Play BIOS	Support Plug & Play for easy installation
◆ Flash EEPROM	Use Flash EEPROM (1M bits) to allow easy BIOS update

System Support Functions

◆ System functions	7 DMA channels, 16 level interrupts, Programmable timers
◆ Support functions	Fast A20 gate and Fast Reset
◆ Clock	Enhanced real time clock/calendar with battery back-up

Other Features

◆ Power good	On board power good signal generation
◆ 3.3V supply	On board 3.3V supply to eliminate the need for special power supply for 3.3V component e.g. CPU, SRAM. Maximum rating : 30 W.
◆ Switches	EPMI, Reset, Keylock switches
◆ Size	8.5" (W) x 13" (L)

1.2 Central Processing Unit

The Pentium processor is a superscalar, pipelined CPU that provides next generation performance for the existing PC compatible software.

The processor is equipped with an 8K code cache and an 8K data cache . Each cache is organized in a 2-way set-associative architecture, offering higher hit rates. The data cache can be configured in write-back or write-through modes.

The internal numeric coprocessor is redesigned to give three times the performance of the 80486 FPU. It is backward compatible with i486DX math coprocessor and complying to ANSI/IEEE standard 754-1985.

1.3 External Cache Subsystem

The external cache of RHINO 5 is organized in a direct-mapped configuration with sizes of 256KB, or 512KB or 1MB. It can operate in write-through mode or write-back mode
.
Either 3.3V asynchronous SRAM or mixed mode voltage asynchronous SRAM can be used in RHINO 5.

1.4 DRAM Subsystem

The main memory in RHINO 5 is organized as a 64-bit memory pool. Both fast-page mode and EDO DRAMs are supported.

EDO DRAM stands for Extended Data Out DRAM and is designed to improve the DRAM read performance. EDO DRAM holds the memory data valid until the next CAS# falling edge, unlike standard fast page mode DRAM which tri-states the memory data when CAS# is deasserted to precharge for the next cycle. As a result, the CAS# precharge can now overlap

with the data valid time to allow CAS# to negate earlier while still satisfying the memory data valid window time.

In addition, Advanced Posted-Write buffers are implemented to improve memory write timing. Shadow RAM is available as an option . System BIOS and video BIOS residing in slow EPROM can be copied to local DRAM to speed up accesses to BIOS code.

1.5 PCI Bus

The Peripheral Component Interconnect (PCI) local bus was specified to establish a high performance local bus standard. It is a 32-bit wide bus supporting burst transactions. PCI local bus devices residing in add-on cards can be configured automatically.

The PCI local bus implemented in RHINO 5 is fully compliant to v2.0 specification. Up to four PCI bus masters are supported. Advanced PCI bus buffer management logic speeds to the transfer rate.

1.6 Super I/O Subsystem

To facilitate system implementation, included in RHINO 5 are two fast Enhanced IDE ports that can dramatically boost the system performance if fast IDE drives are used.

Furthermore, floppy drives supporting various format are also supported through the floppy connector on board. The motherboard is also equipped with two serial ports (16550 Fast UART compatibles) and one parallel port that operates in standard, ECP or EPP mode.

In addition, RHINO 5 is designed to support the PS/2 mouse using specialized keyboard controller and the use of interrupt

IRQ 12. Nevertheless, user can disable the PS/2 mouse function by means of jumpers.

1.7 Input/Output Subsystem

To allow greater system feasibility, RHINO 5 has four ISA bus expansion connectors and four PCI expansion connectors. One of the expansion slots is shared by connectors that will accommodate either an ISA or a PCI expansion, but not both at the same time. Therefore, up to seven expansion slots can be populated on RHINO 5 . Furthermore, all the PCI slots can accept PCI bus master cards.

1.8 BIOS Subsystem

RHINO 5 uses Award ROM BIOS and is stored in Flash EEPROM (1 M bits) which allows easy upgrade through the utility found inside the diskette shipped with RHINO 5.

Inside the diskette you can find the BIOS update utility as well as the most updated version of the BIOS for RHINO 5, together with the BIOS reference manual in TEXT format. The BIOS contains Setup utility, Power-On Self Tests (POST), and PCI auto-configuration utility during boot-up.

CHAPTER 2

INSTALLATION AND UPGRADE

2.1 Setup

Before installing the Rhino 5 motherboard in your system, you must attach the peripheral connectors. Follow the instructions outlined in this chapter for proper installation.

2.2 Installation Precautions

- Turn off the power whenever installing or removing any connectors, memory module or add-on cards.
- Before turning on the power, make sure that all the connectors, memory modules and add-on cards are secured.
- Eliminate any static electricity when handling the motherboard or any peripherals to prevent damage to electrical components. To eliminate electricity, touch a grounded metal object before removing the board from the anti-static bag and wear a grounded wrist or ankle strap when handling the components.
- Put the board and peripherals back into the anti-static bags when you are not using them.
- Always handle the board by its edges, taking care not to touch any of its components.

2.3 Operation and Maintenance

- Keep the system cool. The motherboard contains many high-speed components and they will generate heat during operation. Other add-on cards and the hard disk can also produce a lot of heat. The temperature inside the computer system may be very high. In order to keep the system running stable, the temperature must be kept at a low level. An easy way to do this is to keep the cool air circulating inside the case. If the temperature is still very high, install another fan inside the case. Using a larger case is

recommended if there a number of add-on cards and disk drives in the system.

- Clean the "Gold Finger." Whenever inserting an add-on card to the motherboard, make sure that there is no dirt on the "gold finger" of the add-on card. If dirt is present, the contact between the "golden finger" and the slot may be poor, causing the add-on card to work improperly. Use a pencil eraser to clean the "gold finger" if dirt is found.
- Clean the motherboard. The computer system should be kept clean . Dust and dirt are harmful to electronic devices. To prevent from accumulating on the motherboard, install all mounting plates on the rear of the case. Regularly examine your system and , if necessary, vacuum the interior of the system with a miniature vacuum.

2.4 CPU Installation

The CPU is composed of pins that can easily be bent during installation, causing permanent damage to the processor. It is therefore very important that you make sure the pins are straight before installing the CPU onto the SPGA socket located on RHINO 5 (refer to layout for exact location). To properly align the CPU with the socket, align pin 1 of the CPU (with a notch at the corner) with pin 1 of the CPU socket as demonstrated below.

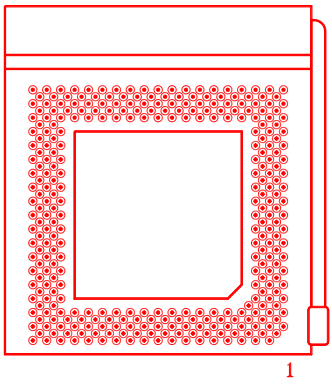


Figure 1 Socket 7 for Pentium CPU

2.5 CPU Upgrade/ VRM Header

In case that you would like to upgrade your CPU, make sure that you have followed the hardware setting described in Appendix-C for new CPU setting. If you upgrade your Pentium with CPU such as P55C , care must be taken to install the VRM used in connection with the CPU.

VRM stands for Voltage Regulator Module and is specially designed to provide a steady power source (with voltage of around 2.5V) for use by P55C CPU. CPU such as P54C, P54CT, P54CS, P54CQS do not need to use the VRM as all the voltage required (about 3.3.V) has already provided by the mainboard.

Inside RHINO 5 motherboard, you will find the VRM header (Header 7) which is stuffed with four jumper shunts. To install the VRM , remove the four jumper shunts and insert the VRM into the header. Make sure that it is securely stuffed by the header.

Never change the jumper shunts in the VRM header if you are not upgrading the P55C CPU.

2.6 Fast Page mode / EDO DRAM Installation

There are four memory banks located on the RHINO 5 motherboard, marked SM1, SM2, SM3 and SM4. The SM1, SM2, SM3 and SM4 are counted starting from right to left consecutively. Start to install the SIMM modules (IN PAIRS) from the right hand side first (SM1/SM2). Depending on how your memory is configured, you may not need to use all the memory banks. Either X32 or X36 of 72 pins SIMM can be installed.

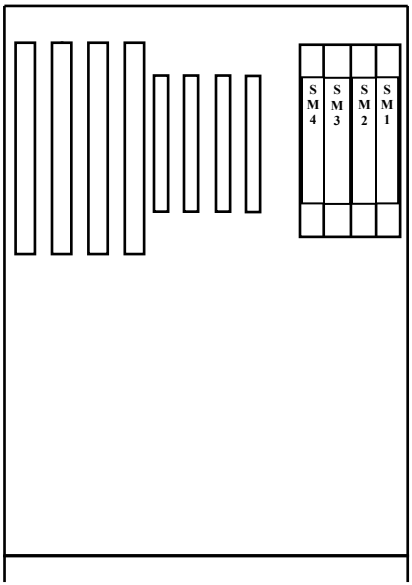


Figure 2 SIMM Sockets Location

Never force the SIMM modules into the SIMM sockets. The sockets are fragile and the locking latches may break.

To insert the modules into the banks follow these steps:

- Locate the notch (near pin 1) on the corner of the module.
- Hold the module so that the notch is at the bottom left corner.
- Insert the bottom edge of the module into the bank at an angle, then pull the module in the direction towards yourself so that it is locked into place by the latches located on the sides of the bank. The latches should be locked tightly and the holes in the module should be aligned with the tabs on the bank.

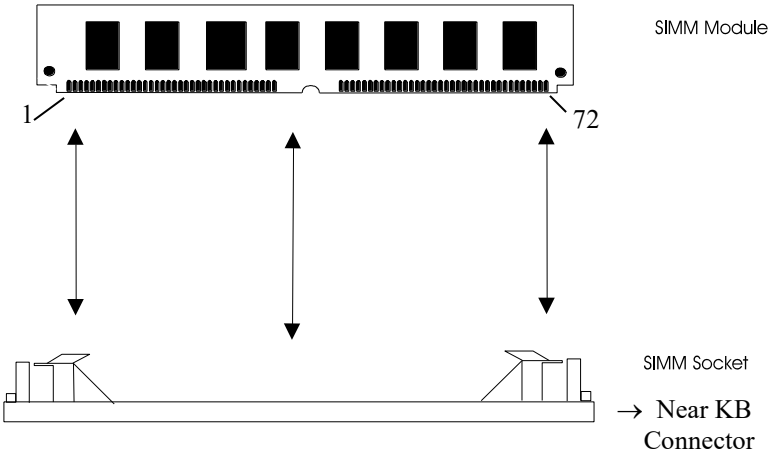


Figure 3 Proper Memory Module Installation

Below is the memory configuration table for RHINO 5.

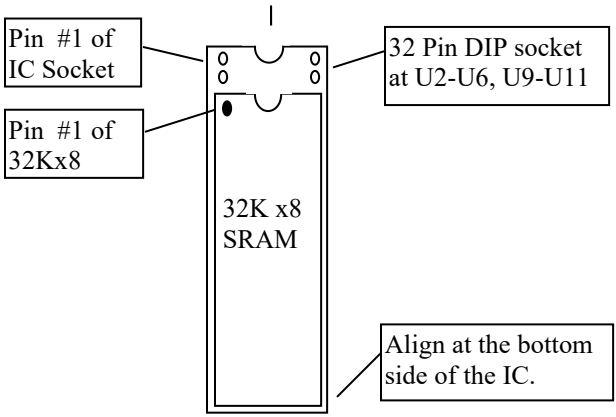
SM4	SM3	SM2	SM1	Total
--------	--------	256Kx32	256Kx32	2MB
--------	--------	512Kx32	512Kx32	4MB
--------	--------	1Mx32	1Mx32	8MB
--------	--------	2Mx32	2Mx32	16MB
--------	--------	4Mx32	4Mx32	32MB
--------	--------	8Mx32	8Mx32	64MB
256Kx32	256Kx32	256Kx32	256Kx32	4MB
512Kx32	512Kx32	256Kx32	256Kx32	6MB
512Kx32	512Kx32	512Kx32	512Kx32	8MB
1Mx32	1Mx32	256Kx32	256Kx32	10MB
1Mx32	1Mx32	512Kx32	512Kx32	12MB
1Mx32	1Mx32	1Mx32	1Mx32	16MB
2Mx32	2Mx32	256Kx32	256Kx32	18MB
2Mx32	2Mx32	512Kx32	512Kx32	20MB
2Mx32	2Mx32	1Mx32	1Mx32	24MB
2Mx32	2Mx32	2Mx32	2Mx32	32MB
4Mx32	4Mx32	256Kx32	256Kx32	34MB
4Mx32	4Mx32	512Kx32	512Kx32	36MB
4Mx32	4Mx32	1Mx32	1Mx32	40MB
4Mx32	4Mx32	2Mx32	2Mx32	48MB
4Mx32	4Mx32	4Mx32	4Mx32	64MB
8Mx32	8Mx32	256Kx32	256Kx32	66MB
8Mx32	8Mz32	512Kx32	512Kx32	68MB
8Mx32	8Mx32	1Mx32	1Mx32	72MB
8Mx32	8Mx32	2Mx32	2Mx32	80MB
8Mx32	8Mx32	4Mx32	4Mx32	96MB
8Mx32	8Mx32	8Mx32	8Mx32	128MB

Table 1 Memory Configuration Table

2.7 Asynchronous Cache RAM Installation

RHINO 5 provides the option for changing the size of the asynchronous cache RAM from cacheless up to 1M bytes cache RAM. To do this, besides the jumper settings mentioned in the Appendix C has to be set properly, care must be taken to stuff the cache RAM in the proper place and orientation.

Cache size of 256K bytes requires 8 pieces of 32Kx8 data RAM. As they are 28 pin DIP IC, they should be stuffed at U2-U6 and U9-U11 as shown below :



For cache size of 512K bytes or 1M bytes, 8 pieces of 64Kx8 or 128Kx8 data SRAM should be used respectively. As both of them are 32-pin DIP IC, just stuff them at U2-U6 and U9-U11.

2.8 Control of System Speed

System speed can be controlled by keyboard. To change the speed by keyboard, use the minus sign (-) and the plus sign (+). Press <control> + <alt> + <"-"> for slow speed and <control> + <alt> + <"+"> for fast speed.

2.9 Fan voltage

There are two different voltages available for CPU fans; +5 volts and + 12 volts. Select a proper setting for jumper JP1 before you turn on the computer.

2.10 Fan Connector

This Fan connector (P4) allows the CPU fan to draw current directly from the motherboard, without having to rely on a separate power connector.

A CPU fan is highly recommended for today's high speed CPUs. Extreme high CPU temperature are generated during system operations, and may cause abnormal hardware behaviour if system is not cool down.

2.11 Reset CMOS

If the setting of the system setup is done improperly, it may make the system malfunction. If this happens, turn off the power and set jumper JP21 to 1-2 to clear the internal CMOS status register. Next, set the jumper JP21 back to 2-3 and turn on the power. The BIOS will find the CMOS status register is reset and will regard the setup information invalid, so it will prompt you to correct the information.

APPENDIX-A

ADVANCED TECHNICAL INFORMATION

A.1 Memory Address Map

Address	Size	Function
0000000- 009FFFF	640 KB	System board memory
00A0000- 00BFFFF	128 KB	Video RAM display buffer
00C0000- 00DFFFF	128 KB	Reserved for add-on cards ROM BIOS
00E0000-00EFFFF	64 KB	System ROM BIOS expansion
00F0000-00FFFFF	64 KB	System ROM BIOS
0100000-7FFFFFF	127MB	Extended memory

A.2 I/O Address Map

I/O Address Hex 000 to 0FF are reserved for the system board and Hex 100 to 3FF are for I/O channels.

Address (Hex)	Device
000-01F	DMA Controller 1, 8237A-5
020-021	Interrupt Controller 1, 8237A-5
022-023	Chip set Address
040-04F	Timer 1, 8254
050-05F	Timer 2, 8254
060-06F	8042 Keyboard/Controller
070-07F	Real Time Clock, Non-Maskable Interrupt Mask
080-09F	DMA Page Registers
0A0-0BF	Interrupt Controller 2,8259A
0C0-0DF	DMA Controller 2, 8237A-5
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor
1F0-1F8	Fixed Disk
200-207	Game Ports
278-27F	Parallel Printer Port 2 (PIO-2)
2F8-2FF	Serial Port 2 (SIO-2)
300-31F	Prototype Card/Streaming Tape Adapter
360-363	PC Network, Low Address
368-36B	PC Network, High Address
378-37F	Parallel Printer Port 1 (PIO-1)
380-38F	SDLC, Bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome Display and Primer Adapter
3C0-3CF	EGA Adapter
3D0-3DF	Color/Graphics Monitor Adapter
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1 (SIO-1)

A.3 I/O Extension Pinout

A.3i 8-Bit ISA Pinout

Ground	GND	B1	A1	-I/O CHCK	I
O	RSTDRV	B2	A2	SD7	I/O
Power	+5 VDC	B3	A3	SD6	I/O
I	IRQ9	B4	A4	SD5	I/O
Power	-5 VDC	B5	A5	SD4	I/O
I	DRQ2	B6	A6	SD3	I/O
Power	-12 VDC	B7	A7	SD2	I/O
I	OWS	B8	A8	SD1	I/O
Power	+12 VDC	B9	A9	SD0	I/O
Ground	GND	B10	A10	-I/O CHRDY	I
O	-SMEMW	B11	A11	AEN	O
O	-SMEMR	B12	A12	SA19	I/O
I/O	-IOW	B13	A13	SA18	I/O
I/O	-IOR	B14	A14	SA17	I/O
O	-DACK3	B15	A15	SA16	I/O
I	DRQ3	B16	A16	SA15	I/O
O	-DACK1	B17	A17	SA14	I/O
I	DRQ1	B18	A18	SA13	I/O
I/O	-Ref	B19	A19	SA12	I/O
O	CLK	B20	A20	SA11	I/O
I	IRQ7	B21	A21	SA10	I/O
I	IRQ6	B22	A22	SA9	I/O
I	IRQ5	B23	A23	SA8	I/O
I	IRQ4	B24	A24	SA7	I/O
I	IRQ3	B25	A25	SA6	I/O
O	-DACK2	B26	A26	SA5	I/O
O	T/C	B27	A27	SA4	I/O
O	BALE	B28	A28	SA3	I/O
Power	+5 VDC	B29	A29	SA2	I/O
O	OSC	B30	A30	SA1	I/O
Ground	GND	B31	A31	SA0	I/O

A.3ii 16-Bit ISA Extension Pinout

I	-MEMCS16	D1	C1	-BHE	I/O
I	-I/OCS16	D2	C2	LA23	I/O
I	IRQ10	D3	C3	LA22	I/O
I	IRQ11	D4	C4	LA21	I/O
I	IRQ12	D5	C5	LA20	I/O
I	IRQ15	D6	C6	LA19	I/O
I	IRQ14	D7	C7	LA18	I/O
0	-DACK0	D8	C8	LA17	I/O
I	DRQ0	D9	C9	-MEMR	I/O
0	-DACK5	D10	C10	-MEMW	I/O
I	DRQ5	D11	C11	SD08	I/O
0	-DACK6	D12	C12	SD09	I/O
I	DRQ6	D13	C13	SD10	I/O
0	-DACK7	D14	C14	SD11	I/O
I	DRQ7	D15	C15	SD12	I/O
Power	+5 VDC	D16	C16	SD13	I/O
I	-MASTER	D17	C17	SD14	I/O
Ground	GND	D18	C18	SD15	I/O

A.4 PCI Bus Pinout

-12V	B1	A1	TRST#
TCK	B2	A2	+12V
GROUND	B3	A3	RESERVED
RESERVED	B4	A4	RESERVED
+5V	B5	A5	+5V
+5V	B6	A6	INTA#
INTB#	B7	A7	INTC#
INTD#	B8	A8	+5V
PRSNT1#	B9	A9	RESERVED
RESERVED	B10	A10	+5V
PRSNT2#	B11	A11	RESERVED
GROUND	B12	A12	GROUND
GROUND	B13	A13	GROUND
RESERVED	B14	A14	RESERVED
GROUND	B15	A15	RST#
CLK	B16	A16	+5V
GROUND	B17	A17	GNT#
REQ#	B18	A18	GROUND
+5V	B19	A19	RESERVED
AD[31]	B20	A20	AD[30]
AD[29]	B21	A21	RESERVED
GROUND	B22	A22	AD[28]
AD[27]	B23	A23	AD[26]
AD[25]	B24	A24	GROUND
RESERVED	B25	A25	AD[24]
C/BE[3]#	B26	A26	IDSEL
AD[23]	B27	A27	RESERVED
GROUND	B28	A28	AD[22]
AD[21]	B29	A29	AD[20]
AD[19]	B30	A30	GROUND
RESERVED	B31	A31	AD[18]
AD[17]	B32	A32	AD[16]
C/BE[2]#	B33	A33	RESERVED
GROUND	B34	A34	FRAME#
IRDY#	B35	A35	GROUND
RESERVED	B36	A36	TRDY#
DEVSEL#	B37	A37	GROUND
GROUND	B38	A38	STOP#
LOCK#	B39	A39	RESERVED
PERR#	B40	A40	SDONE
RESERVED	B41	A41	SBO#
SERR#	B42	A42	GROUND
RESERVED	B43	A43	PAR
C/BE[1]#	B44	A44	AD[15]
AD[14]	B45	A45	RESERVED
GROUND	B46	A46	AD[13]
AD[12]	B47	A47	AD[11]
AD[10]	B48	A48	GROUND
GROUND	B49	A49	AD[09]
AD[08]	B50	A50	C/BE[0]#
AD[07]	B51	A51	RESERVED
RESERVED	B52	A52	AD[06]

AD[05]	B53	A53	AD[04]
AD[03]	B54	A54	GROUND
GROUND	B55	A55	AD[02]
AD[01]	B56	A56	AD[00]
RESERVED	B57	A57	+5V
ACK64#	B58	A58	REQ64#
+5V	B59	A59	+5V
+5V	B60	A60	+5V

PCI Bus Pinout (Cont.)

A.5 Direct Memory Access Channels

Channel	Function	8-Bit	16-Bit	Transfer Block Size
0	Spare	8-bit		64
1	SDLC	8-bit		64
2	Floppy Disk	8-bit		64
3	Spare	8-bit		64
4	Cascade for DMA controller 1			
5	Spare		16-bit	128
6	Spare		16-bit	128
7	Spare		16-bit	128

A.6 DMA Controller Registers

Address (Hex)	Command Code
C0	CH-0 base and current address
C2	CH-0 base and current word count
C4	CH-1 base and current address
C6	CH-1 base and current word count
C8	CH-2 base and current address
CA	CH-2 base and current word count
CC	CH-3 base and current address
CE	CH-3 base and current word count
D0	Read Status Register/Write Command Register
D2	Write Request Register
D4	Write Single Mask Register Bit
D6	Write Mode Register
D8	Clear Byte Pointer Flip-Flop
DA	Read Temporary Register/Write Master Clear
DC	Clear Master Register
DE	Write All Mask Register Bits

A.7 Page Register Address

Page Register	I/O Address (Hex)
DMA Channel 0	0087
DMA Channel 1	0083
DMA Channel 2	0081
DMA Channel 3	0082
DMA Channel 5	008B
DMA Channel 6	0089
DMA Channel 7	008A
Refresh	008F

A.8 System Interrupts

Interrupt	Parity or I/O Channel Check

Controllers (NMI level)		
CTLR 1	**CTLR 2**	
IRQ0		Timer Output 0
IRQ1		Keyboard (Output Buffer Full)
IRQ2		Interrupt from CTLR 2
	IRQ8	Real-time Clock Interrupt
	IRQ9	Software Redirected to INT 0AH (IRQ2)
	IRQ10	Reserved
	IRQ11	Reserved
	IRQ12	PS/2 Mouse
	IRQ13	Coprocessor
	IRQ14	Fixed Disk Controller
	IRQ15	Reserved
IRQ3		Serial Port 2
IRQ4		Serial Port 1
IRQ5		Parallel Port 2
IRQ6		Diskette Controller
IRQ7		Parallel Port 1

APPENDIX-B

CONNECTORS PINOUT

B.1 Reset Connector (P1)

Pin	Signal Name
1	Reset
2	Ground

B.2 Turbo LED Connector (P2)

Pin	Signal Name
1	Pull_Up_150
2	LED_Turbo-

B.3 Keylock Connector (P3)

Pin	Signal Name
1	+5Vdc
2	Mechanical Key
3	Ground
4	Keyboard Inhibit
5	Ground

B.4 Fan Connector (P4)

Pin	Signal Name
1	+5/+12dc Power
2	Ground

B.5 EPMI/T.B. Switch (P5)

Pin	Signal Name
1	EPMI
2	Ground

B.6 Speaker Connector (P6)

Pin	Signal Name
1	Speaker Data_Out
2	N.C.
3	Ground
4	+5Vdc

B.7 Header 7 (P8)

Signal Name	Pin	Pin	Signal Name
Ground	1	2	Ground
Ground	3	4	Ground
+12Vdc	5	6	V/IO
V/IO	7	8	V/IO
+3.3Vdc	9	10	+3.3Vdc
+3.3Vdc	11	12	+3.3Vdc
VCORE	13	14	VCORE
VCORE	15	16	VCORE
Ground	17	18	VCORE
VCORE	19	20	VCORE
N.C.	21	22	UPVRM#
Sense	23	24	N.C.
Ground	25	26	Ground
+5Vdc	27	28	+5Vdc
+5Vdc	29	30	+5Vdc

B.8 External Battery Connector (P9)

Pin	Signal Name

1	+3.6Vdc
2	N.C.
3	Ground
4	Ground

B.9 IDE LED Connector (P10)

Pin	Signal Name
1	+5Vdc
2	HD_LED-

B.10 IDE Connector (P11,P12)

Signal Name	Pin	Pin	Signal Name
Reset	1	2	Ground
Data 7	3	4	Data 8
Data 6	5	6	Data 9
Data 5	7	8	Data 10
Data 4	9	10	Data 11
Data 3	11	12	Data 12
Data 2	13	14	Data 13
Data 1	15	16	Data 14
Data 0	17	18	Data 15
Ground	19	20	Key
DRQx	21	22	Ground
I/O Write-	23	24	Ground
I/O Read-	25	26	Ground
IOCHRDY	27	28	BALE
DACKx	29	30	Ground
IRQ14/15*	31	32	IOCS16-
Signal Name	**Pin**	**Pin**	**Signal Name**
Address 1	33	34	N.C.
Address 0	35	36	Address 2
Chip Select 0-	37	38	Chip Select 1-
Activity	39	40	Ground

IDE Connector Pinout (Cont.)

* Note : For Primary IDE, IRQ 14 is used whereas for Secondary IDE, IRQ 15 is used.

B.11 Floppy Connector (P13)

Signal Name	Pin	Pin	Signal Name
Ground	1	2	FDHDIN
Ground	3	4	Reserved
Key	5	6	FDEDIN
Ground	7	8	Index-
Ground	9	10	Motor Enable 0
Ground	11	12	Drive Select 1
Ground	13	14	Drive Select 0
Ground	15	16	Motor Enable 1
Ground	17	18	DIR-
Ground	19	20	STEP-
Ground	21	22	Write Data-
Ground	23	24	Write Gate-
Ground	25	26	Track 00-
Ground	27	28	Write Protect-
Ground	29	30	Read Data-
Ground	27	28	Write Protect-
Ground	29	30	Read Data-
Ground	31	32	Side 1 Select-
Ground	33	34	Disk Change

B.12 Printer Port Connector (P14)

Signal Name	Pin	Pin	Signal Name
STROBE-	1	14	AUTO FEED-
Data bit 0	2	15	ERROR-
Data bit 1	3	16	INIT-
Data bit 2	4	17	SLCT IN-

Data bit 3	5	18	Ground
Data bit 4	6	19	Ground
Data bit 5	7	20	Ground
Data bit 6	8	21	Ground
Data bit 7	9	22	Ground
ACK-	10	23	Ground
BUSY	11	24	Ground
PE (Paper End)	12	25	Ground
SLCT	13	26	N.C.

B.13 Serial Port Connector (P15,P16)

Signal Name	**Pin**	**Pin**	**Signal Name**
DCD	1	2	RXD
TXD	3	4	DTR
Ground	5	6	DSR
RTS	7	8	CTS
RI	9	10	N.C.

B.14 Power Connector (P17,P18)

Pin	Signal Name
1	Power Good
2	+5Vdc
3	+12Vdc
4	-12V dc
5	Ground
6	Ground
7	Ground
8	Ground
9	-5Vdc
10	+5Vdc
11	+5Vdc
12	+5Vdc

B.15 PS/2 Mouse Connector (P19)

Signal Name	Pin	Pin	Signal Name
+5V dc	1	2	N.C.
N.C.	3	4	N.C.
Data	5	6	N.C.
Ground	7	8	Clock

B.16 Keyboard Connector (KB1)

Pin	Signal Name
1	Keyboard clock
2	Keyboard data
3	Not used
4	Ground
5	VCC

Note: KB1 is a DIN5 socket.

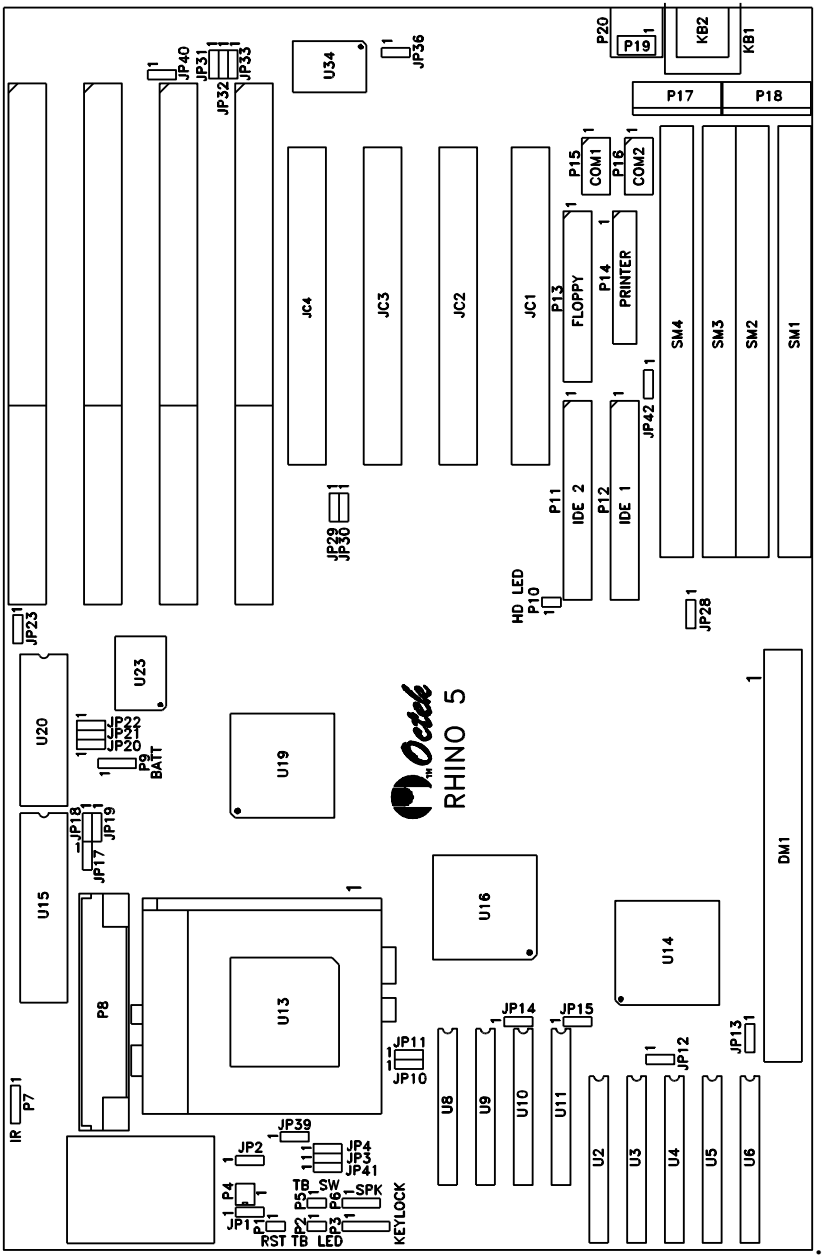
APPENDIX-C

HARDWARE SETTINGS

C.1 System Component Map

Jumper Connectors	Function
P1	Reset
P2	Turbo LED
P3	Keylock
P4	Fan connector
P5	EPMI/TB Switch
P6	Speaker
P8	Header 7
P9	External Battery Connector
P10	IDE LED Connector
P11	Secondary IDE Connector
P12	Primary IDE Connector
P13	Floppy Drive Connector
P14	Printer Port
P15	Serial Port 1
P16	Serial Port 2
P17	Power Connector
P18	Power Connector
P19	PS/2 Mouse Connector
KB1	Keyboard Connector

C.2 Layout of RHINO 5 Main Board



C.3 Jumper Settings

All factory settings are marked by * in the following sections.

C.3.1 CPU related settings

Header 7 setting
The factory settings are as follows:

P8 (7-9)
P8 (8-10)
P8 (11-13)
P8 (12-14)

The four pieces of shunt connectors are to be left in factory setting. This configuration works well with all Pentium CPUs P54C, P54CQS and P54CS.

For P55C CPU, the processor will be used in connection with an Voltage Regulator Module (VRM). All the four shunt connectors installed in P8 should be removed. An VRM should be plugged in P8 instead.

TOP VIEW OF HEADER 7 (BESIDE THE CPU SOCKET)

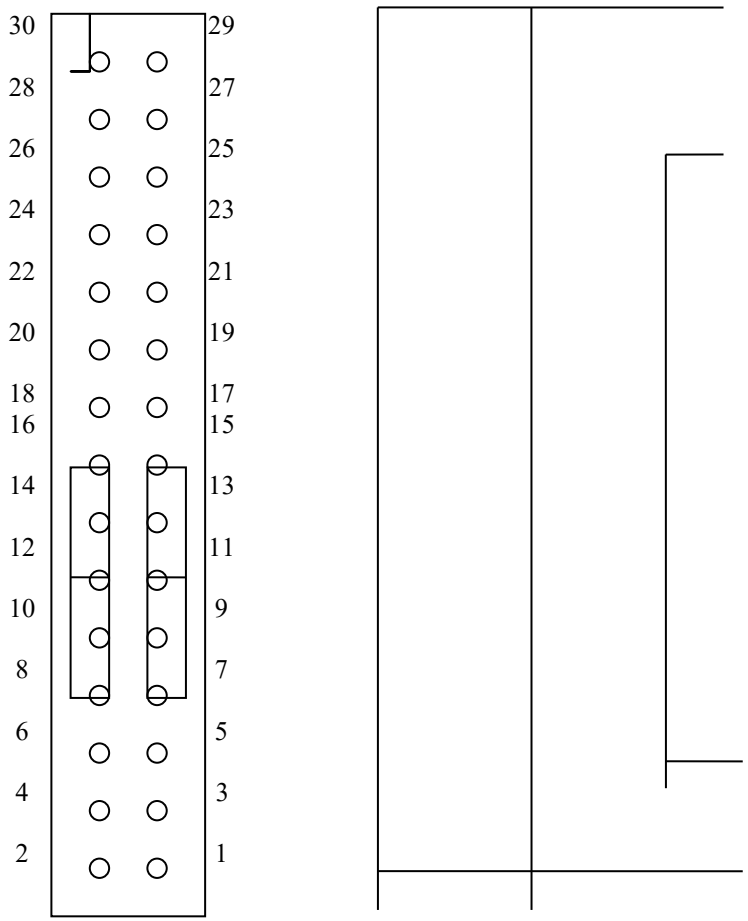


Figure 4 Top View of Header 7

CPU Clock

JP29	JP30	CPU Clock	CPU
1-2	2-3	50MHz	Intel P54C-75 Cyrix M1
2-3	1-2	60MHz	Intel P54C-90 Intel P54C-120 Intel P54CS-150
1-2	1-2	66MHz	Intel P54C-100 Intel P54C-133

Clock multiplier

JP2	JP39	P54C P54CQS	P54CS B-STEP	P54CS C-STEP	P55C
1-2	1-2	reserved	reserved	x2.5	x2.5
2-3	1-2	reserved	reserved	reserved	reserved
1-2	2-3	x2	x2	x2	x2
2-3	2-3	x1.5	x1.5	x1.5	reserved

Multiplier selection based on CPU type

		JP2	JP39
Intel	P54C-75	2-3	2-3
Intel	P54C-90	2-3	2-3
Intel	P54C-100	2-3	2-3
Intel	P54C-120	1-2	2-3
Intel	P54C-133	1-2	2-3
Cyrix	M1	1-2	2-3

Power saving mode

CPU	**JP11**
Intel	1-2
Cyrix	2-3

CPU Fan voltage select

	JP1
+5V	1-2 *
+12V	2-3

C.3.2 External cache (L2 cache) setting

Async Cache/ Sync Cache selection

	JP42
Asynchronous Cache	1-2
Synchronous Cache	2-3

Asynchronous L2 cache size

	JP3	**JP4**	**JP10**
256KB	2-3	1-2	2-3
512KB	1-2	1-2	1-2
1MB	1-2	2-3	1-2

Voltage source for asynchronous L2 cache

	JP12	**JP13**	**JP14**	**JP15**
+5V supply	2-3	2-3	2-3	2-3
+3.3V supply	1-2	1-2	1-2	1-2

Async SRAM device requirement

256KB cache

SRAM	location	type	speed	voltage
tag RAM	U8	32Kx8	15ns	5V I/0
data RAM	U2 - U6, U9 - U11	32Kx8	15ns	3.3V I/O

512KB cache

SRAM	location	type	speed	voltage
tag RAM	U8	32Kx8	15ns	5V I/0
data RAM	U2 - U6, U9 - U11	64Kx8	15ns	3.3V I/O

1MB cache

SRAM	location	type	speed	voltage
tag RAM	U8	32Kx8	15ns	5V I/0
data RAM	U2 - U6, U9 - U11	128Kx8	15ns	3.3V I/O

Synchronous SRAM module
Install a 32Kx8 5V tag SRAM at location U8**.**

C.3.3 DRAM

DRAM Type

	JP28
Fast page mode DRAM(60ns or 70ns)	1-2
EDO DRAM(60ns or 70ns)	2-3

EDO DRAM SIMMs are NOT allowed to be mixed with Fast-page mode DRAM SIMMs.

C.3.4 Peripheral setup

PS/2 MOUSE support

	JP17	**JP18**	**JP19**
Enabled	1-2 *	2-3 *	2-3 *
Disabled	2-3	1-2	1-2

Printer port interrupt

	JP31
IRQ5	1-2
IRQ7	2-3 *

DMA request for printer port ECP mode

	JP32
DRQ1	1-2 *
DRQ3	2-3

DMA acknowledge for printer port ECP mode

	JP33
DACK1	1-2 *
DACK3	2-3

Installation of a 2nd FLOPPY drive in PS/2 mode

	JP36
2nd drive absent	1-2 *
2nd drive present	2-3

C.3.5 Miscellaneous

Power Good Signal select

	JP40
External Power Good	1-2 *
On-board Power Good	2-3

CMOS discharge

	JP21
Clear CMOS	1-2
Preserve CMOS	2-3 *

Battery select

	JP20
External Battery	1-2
On-board Battery	2-3 *

Reserved Jumpers

JP22	2-3
JP27	2-3 PCI clock = CPUclock/2