Raptor MicroATX

Motherboard
Installation Guide

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First Edition.

©March, 2002

Introduction

Thank you for your purchase of the Raptor MicroATX industrial embedded motherboard. The Raptor MicroATX design was based on the Intel 815E chipset providing the ideal platform to industrial applications. The Raptor MicroATX design is based on the Intel Celeron (FC-PGA) and Pentium III (FC-PGA and FC-PGA2) processors.

With proper installation and maintenance, your Raptor MicroATX will provide years of high performance and trouble free operation.

This manual provides a detailed explanation into the installation and use of the Raptor MicroATX industrial embedded motherboard. This manual is written for the novice PC user/installer. However, as with any major computer component installation, previous experience is helpful and should you not have prior experience, it would be prudent to have someone assist you in the installation. This manual is broken down into 3 chapters and 4 appendixes.

Chapter 1 - System Board Pre-Configuration

This chapter provides all the necessary information for installing the Raptor MicroATX. Topics discussed include: installing the CPU (if necessary), DRAM installation and jumper settings. Connecting all the cables from the system board to the chassis and peripherals is also explained.

Chapter 2 - BIOS Configuration

This chapter shows the final step in getting your system firmware setup.

Chapter 3 - Upgrading

The Raptor MicroATX provides a number of expansion options including memory. All aspects of the upgrade possibilities are covered.

Appendix A - Technical Specifications

A complete listing of all the major technical specifications of the Raptor MicroATX is provided.

Appendix B - Flash BIOS Programming (optional) and Codes

Provides all information necessary to program your optional General Software Embedded 2000 Flash BIOS. POST Codes and beep codes are described in details.

Appendix C - Communication Devices

Two on-board 10/100 Ethernet controllers and four serial ports (Two RS232 + Two RS232 or RS422/485(optional)).

Appendix D - On-Board Video Controller (LCD Optional)

On-board CRT video controller/LCD (optional).

Static Electricity Warning!

The Raptor MicroATX has been designed as rugged as possible but can still be damaged if jarred sharply or struck. Handle the motherboard with care.
The Raptor MicroATX also contains delicate electronic circuits that can be damaged or weakened by static electricity. Before removing the Raptor MicroATX from its protective packaging, it is strongly recommended that you use a grounding wrist strap. The grounding strap will safely discharge any static electricity build up in your body and will avoid damaging the motherboard. Do not walk across a carpet or linoleum floor with the bare board in hand.

Warranty

This product is warranted against material and manufacturing defects for two years from the date of delivery. Buyer agrees that if this product proves defective the manufacturer is only obligated to repair, replace or refund the purchase price of this product at manufacturer's

discretion. The warranty is void if the product has been subjected to alteration, misuse or abuse; if any repairs have been attempted by anyone other than the manufacturer; or if failure is caused by accident, acts of God, or other causes beyond the manufacturer's control.

Raptor MicroATX - An Overview

The Raptor MicroATX represents the ultimate in industrial embedded motherboard technology. No other system board available today provides such impressive list of features:

CPU Support

- Supports full series of Intel Celeron (FC-PGA 66MHz PSB, FC-PGA 100MHz PSB and FC-PGA2 (0.13u) 100MHz PSB) and Pentium III (FC-PGA 100MHz PSB, FC-PGA 133 PSB and FC-PGA2 (0.13u) 133MHz PSB) PGA370 processors.

Supported Bus Clocks

- 66MHz, 100MHz and 133MHz.

Memory

- Two DIMM sockets up to 512MB (unbuffered) SDRAM, PC100 and PC133 (recommended for higher performance when using 133MHz PSB processors).

On-Board I/O

- 2 Floppies up to 2.88 MB.
- Dual channel PCI 32-bit EIDE controller – UDMA 66/100 supported. One extra connector (mini-Header 44 pin) in parallel to IDE1 for Solid State IDE disk or any 44 pin IDE device support.
- Four high speed RS-232 (or two RS-232 and two RS-422/485 (optional)) serial ports 16 Bytes FIFO (16550/16550D). RS-422/485 Full duplex or Half-duplex (RTS flow control), termination resistors on/off, transient suppression on transmitter lines.

- One Centronics™ compatible bi-directional parallel port. EPP/ECP mode compatible.
- One PS/2 mouse and one PS/2 keyboard connectors.
- Auxiliary Keyboard/Mouse header for front panel access.
- Two Universal Serial Bus connectors.
- Four 32-bit PCI slots.
- Two RJ45 Ethernet connectors.
- Power Button – advanced management support.
- SMBus/I2C header.
- Automatic CPU voltage & temperature monitoring device (optional).

ROM BIOS

- General Software Embedded 2000 BIOS with optional FLASH ROM.

On-Board Ethernet

- Two On-board 10/100 Ethernet.

On-Board CRT/LCD(Optional) video controller

- Standard CRT video controller (Intel 815E chipset).
- DVO connector (optional).
- LCD support (optional) (SmartASIC SP1015).

Conventions Used in this Manual

Notes - Such as a brief discussion of memory types.

Important Information - such as static warnings, or very important instructions.

When instructed to enter keyboard keystrokes, the text will be noted by this graphic.

Chapter 1 Pre-Configuration

This chapter provides all the necessary information for installing the Raptor MicroATX into a standard PC chassis. Topics discussed include: installing the CPU (if necessary), DRAM installation and jumper settings.

Handling Precautions

The Raptor MicroATX has been designed to be as rugged as possible but it can be damaged if dropped, jarred sharply or struck. Damage may also occur by using excessive force in performing certain installation procedures such as forcing the system board into the chassis or placing too much torque on a mounting screw.

Take special care when installing or removing the system memory DIMMs. Never force a DIMM into a socket. Screwdrivers slipping off a screw and scraping the board can break a trace or component leads, rendering the board unusable. Always handle the Raptor MicroATX with care.

Special Warranty Note:
Products returned for warranty repair will be inspected for damage caused by improper installation and misuse as described in the previous section and the static warning below. Should the board show signs of abuse, the warranty will become void and the customer will be billed for all repairs and shipping and handling costs.

Static Warning

The Raptor MicroATX contains delicate electronic semiconductors that are highly sensitive to static electricity. These components, if subjected to a static electricity discharge, can be weakened thereby reducing the serviceable life of the system board. BEFORE THE BOARD IS

REMOVED FROM ITS PROTECTIVE ANTISTATIC PACKAGING, TAKE PROPER PRECAUTIONS! Work on a conductive surface that is connected to the ground. Before touching any electronic device, ground yourself by touching an unpainted metal object or, and highly recommended, use a grounding strap.

Step 1 Setting the Jumpers

Your Raptor MicroATX is equipped with a large number of peripherals. As such, there are a large number of configuration jumpers on the board. Taken step by step, setting these jumpers is easy. We suggest you review each section and follow the instructions.

Special note about operating frequency:
The Raptor Micro ATX has the ability to run at a variety of speeds without the need to change any crystal, oscillator or jumper.

Jumper Types

Jumpers are small copper pins attached to the system board. Covering two pins with a shunt closes the connection between them. The Raptor MicroATX examines these jumpers to determine specific configuration information. There are two different categories of jumpers on the Raptor MicroATX.

A. Two pin jumpers are used for binary selections such as enable, disable. Instructions for this type of jumper are open, for no shunt over the pins or closed, when the shunt covers the pins.

B. Three or four pin jumpers are used for multiple selections. Instructions for these jumpers will indicate which two pins to cover. For example: for JP*x* 2-3 the shunt will be covering pins 2 and 3 leaving pins 1 and 4 exposed.

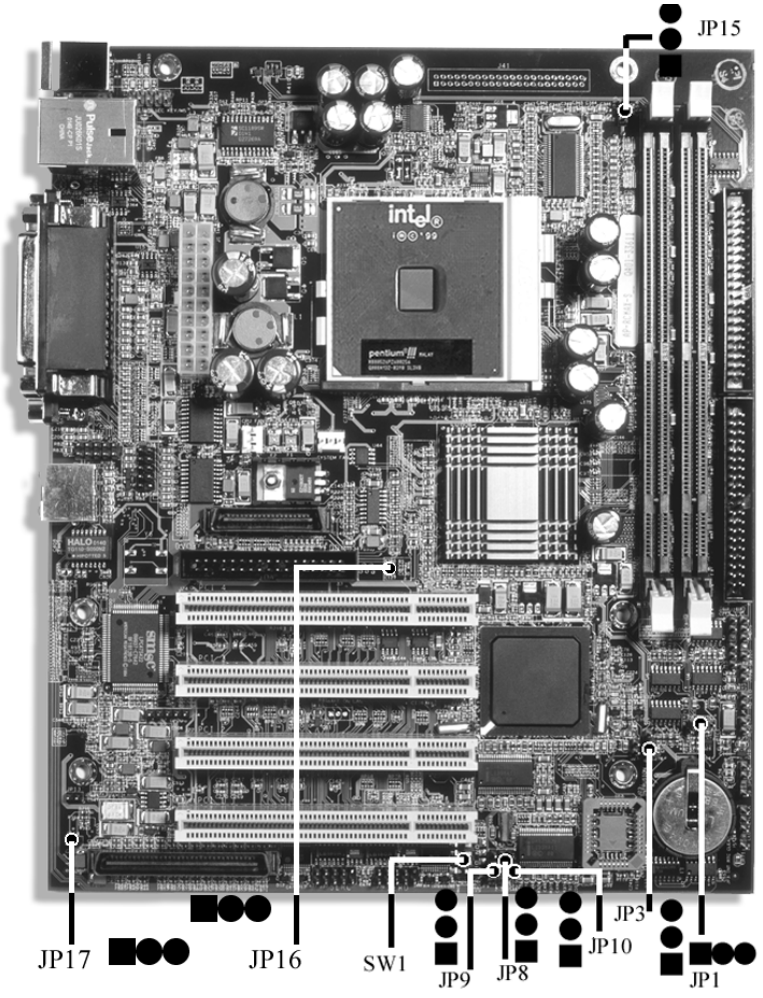
Some jumpers are actually a set of micro-switches. Moving the micro-switch to the position assigned "ON" will have the same effect as closing a regular jumper.

How to identify pin number 1 on *Figure 1-1*: Looking to the solder side (The board side without components) of the PCB (Printed Circuit Board), pin number 1 will have a squared pad ■. Other pins will have a circular pad ●. They are numbered sequentially.

Jumper Locations

Use the diagram below and the tables on the following pages to locate and set the on-board configuration jumpers.

Figure 1-1 Jumper Locations



CMOS Reset

This option is provided as a convenience for those who need to reset the CMOS registers. It should always be set to "Normal" for standard operation. If the CMOS needs to be reset, turn off the system, move JP3 to 2-3, turn the system on, move jumper to 1-2 and press reset.

Table 1-1 CMOS Reset

Reset CMOS	Normal	Clear CMOS
JP3	1-2*	2-3

** Manufacturer's Settings.*

MicroATX Power Supply Enhancements

The Raptor MicroATX has a Power on mode selection. The jumper JP1 selects the power on mode.

Table 1-2 POWER ON Mode Select

Power on mode	Power on immediately	Power on upon PWR_SW signal (Button press)
JP1	1-2*	2-3

** Manufacturer's Settings.*

SER C and SER D RS-232/RS-422/485 Selection (Optional Feature)

To Select SER C and SER D operation mode use JP9. For RS-232 mode set 1-2, for RS-422/485 mode set 3-4. Both serial channels will be changed by the same jumper, they cannot be selected independently.

Table 1-3 SER C and SER D RS-232/RS-422/485 Selection

SER C & SER D Mode	RS-232	RS-422/485
JP9	1-2*	2-3

**Manufacturer's Settings.*

SER C RS-422/485 Receiver Mode (Optional Feature)

The Receiver of SER C has two operating modes when used as RS-422/485. The jumper JP8 either selects receiver always on (1-2) for RS-422 operation or receiver controlled by the RTS signal (2-3). For Half Duplex operation (RS-485) the option controlled by RTS signal must be selected. For more information please refer to Appendix C.

Table 1-4 SER C RS-485 Receiver Mode Selection

SER C RS-485 Receiver[1] Mode	Always On	Controlled by RTS
JP8	1-2*	2-3

** Manufacturer's Settings.*

SER D RS-422/485 Receiver Mode (Optional Feature)

The Receiver of SER D has two operating modes when used as RS-422/485. The jumper JP10 either selects receiver always on (1-2) for RS-422 operation or receiver controlled by the RTS signal (2-3). For Half Duplex operation (RS-485) the option controlled by RTS signal must be selected. For more information please refer to Appendix C.

Table 1-5 SER D RS-485 Receiver Mode Selection

SER D RS-485 Receiver[1] Mode	Always On	Controlled by RTS
JP10	1-2*	2-3

** Manufacturer's Settings.*

[1] The receiver may be always on or controlled by RTS, but the transmitter is always controlled by RTS. Therefore, when using RS-422, the software application must enable RTS.

SER C and SER D RS-422/485 Termination Resistor Option (Optional Feature)

The switch SW1 allows the insertion of the termination resistors in the Receiver and Transmitter lines of the Serial C and Serial D when operating in RS-422/485 mode.

Table 1-6 SER C RS-422/485 Tx Termination Resistor Selection

SER C RS-422/485 Tx Termination Resistor	On	Off
SW1 - 1	On	Off*

** Manufacturer's Settings.*

Table 1-7 SER C RS-422/485 Rx Termination Resistor Selection

SER C RS-422/485 Rx Termination Resistor	On	Off
SW1 - 2	On	Off*

** Manufacturer's Settings.*

Table 1-8 SER D RS-422/485 Tx Termination Resistor Selection

SER D RS-422/485 Tx Termination Resistor	On	Off
SW1 - 3	On	Off*

** Manufacturer's Settings.*

Table 1-9 SER D RS-422/485 Rx Termination Resistor Selection

SER D RS-422/485 Rx Termination Resistor	On	Off
SW1 – 4	On	Off*

** Manufacturer's Settings.*

ATA-Disk Connector Voltage Selection

The ATA-Disk Connector J41 can provide either 5Vcc or 3.3Vcc. The jumper JP15 selects the voltage.

Table 1-10 ATA-Disk Connector Voltage Select

ATA-Disk Voltage	5Vcc	3.3Vcc
JP15	1-2*	2-3

**Manufacturer's Settings.*

LCD Panel Voltage Selection

The LCD panel connector J40 can provide either 5Vcc or 3.3Vcc to the LCD panel. The jumper JP17 selects the voltage.

Table 1-11 LCD Panel Connector Voltage Select

LCD Panel Voltage	5Vcc	3.3Vcc
JP17	1-2	2-3*

** Manufacturer's Settings.*

On-Board Chipset I2C Connection to EDID EEPROM

The On-Board EEPROM that contains EDID information of LCD Panels may be Enabled or Disabled. The jumper JP16 selects the option.

Table 1-12 On-Board EDID EEPROM Select

On-Board EDID	Enabled	Disabled
JP16	1-2*	2-3

** Manufacturer's Settings.*

Step 2 SDRAM, CPU, and Cables Installation

Depending upon how your Raptor MicroATX is configured you may need to install the following:

- SDRAM (DIMMs)
- CPU

Raptor MicroATX Memory Configuration

The Raptor MICROATX offers 2 DIMM memory sockets (Locations J27 and J26 – *Figure 1-3*). They can be configured with 3.3V unbuffered SDRAM modules. It is very important that the quality of the DIMMs is good. Unreliable operation of the system may result if poor quality DIMMs are used. Always purchase your memory from a reliable source. We strongly recommend using PC133 memory module for higher performance when using 133MHz PSB processors.

The Raptor MICROATX uses standard DIMMs. To determine the actual capacity of a 1 by 64 DIMM, simply multiply the 1MB by 8.

CPU Installation

The Raptor MICROATX currently supports the following CPUs:

- Full series of Intel Celeron (FC-PGA 66MHz PSB, FC-PGA 100MHz PSB and FC-PGA2 (0.13u) 100MHz PSB) and Pentium III (FC-PGA 100MHz PSB, FC-PGA 133 PSB and FC-PGA2 (0.13u) 133MHz PSB) PGA370 processors

1. Improper installation of the CPU may cause permanent damage to both the system board and the CPU. -- Void of warranty
2. Always handle the CPU by the edges, never touch the pins.
3. Always use a heat-sink and a CPU fan.

Locate the CPU socket on your Raptor MicroATX system board (PGA Socket – Location U1 – *Figure 1-3*). To install the processor, lift the lever of the ZIF socket and gently insert the CPU. The CPU will fit only in the right alignment. Make sure the CPU is inserted all the way. Lower the lever. Install the CPU fan. Make sure it is locked and connected to J3 (see pin-out in Appendix A).

The continued push of technology to increase performance levels (higher operating speeds) and packaging density (more transistors) is aggravating the thermal management of the CPU. As operating frequencies increase and packaging sizes decreases, the power density increases and the thermal cooling solution space and airflow become more constrained. The result is an increased importance on system design to ensure that thermal design requirements are met for the CPU.

The objective of thermal management is to ensure that the temperature of the processor is maintained within functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet their specified performance requirements. Operation outside the functional limit can degrade system performance, cause logic errors or cause component and/or system damage. Temperatures exceeding the maximum operating limits may result in irreversible changes in the operating characteristics of the component.

If the Raptor MicroATX industrial embedded motherboard is acquired without the CPU and the thermal solution, extremely care must be taken to avoid improper thermal management. All Intel thermal solution specifications, design guidelines and suggestions to the CPU being used must be followed. The Raptor MicroATX warranty is void if the thermal management does not comply with Intel requirements.

Designing for thermal performance
In designing for thermal performance, the goal is to keep the processor within the operational thermal specifications. The inability to do so will shorten the life of the processor.

Fan Heatsink
An active fan heatsink can be employed as a mechanism for cooling the Intel processors. This is the acceptable solution for most chassis.
Adequate clearance must be provided around the fan heatsink to ensure unimpeded air flow for proper cooling.

Airflow management
It is important to manage the velocity, quantity and direction of air that flows within the system (and how it flows) to maximize the volume of air that flows over the processor.

Thermal interface management
To optimize the heatsink design for the Celeron/Pentium III processor, it is important to understand the impact of factors related to the interface between the processor and the heatsink base. Specifically, the bond line thickness, interface material area, and interface material thermal conductivity should be managed to realize the most effective thermal solution.

This completes the installation of the CPU. Now is it a good time to double check both the CPU and DIMM installation to make sure that these devices have been properly installed.

Installing Cables

Power and Control Panel Cables

The Raptor MicroATX gets power from the power connector J1 (*Figure 1-3*).

Installing Peripheral Cables

Now it is a good time to install the internal peripherals such as floppy and hard disk drives. Do not connect the power cable to these peripherals, as it is easier to attach the bulky ribbon cables before the smaller power connectors. If you are installing more than one IDE drive double check your master/slave jumpers on the drives. Review the information supplied with your drive for more information on this subject.

Connect the floppy cable (not included) to the system board. Then connect remaining ends of the ribbon cable to the appropriate peripherals. Connect the Ethernet cable (not included) if using the header connector. Connect the serial port cables and the auxiliary Keyboard/Mouse cable (not included) if using the alternative Keyboard/Mouse header connector. Finally, connect the IDE cable (not included) to the system. If using a Solid State Device, connect it to the

mini-ATA connector. Then connect remaining ends of the ribbon cable to the appropriate peripherals. This concludes the hardware installation of your Raptor MicroATX system. Now it is a good time to re-check all of the cable connections to make sure they are correct.

The connector hole layouts on the Raptor MicroATX I/O Gasket (included) are designed according to Intel ATX specifications.

Figure 1-2 MicroATX I/O Gasket

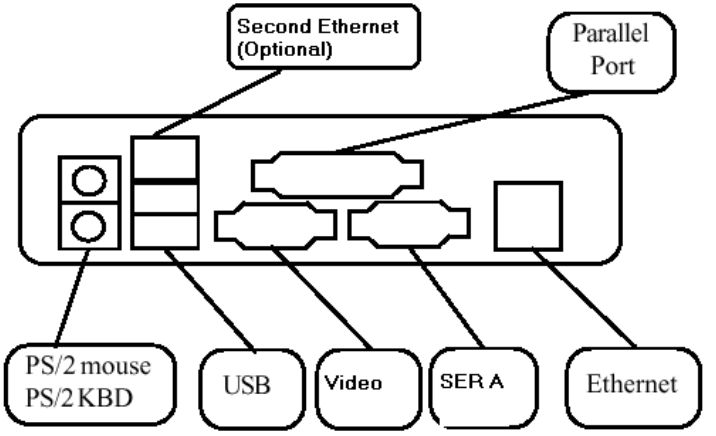
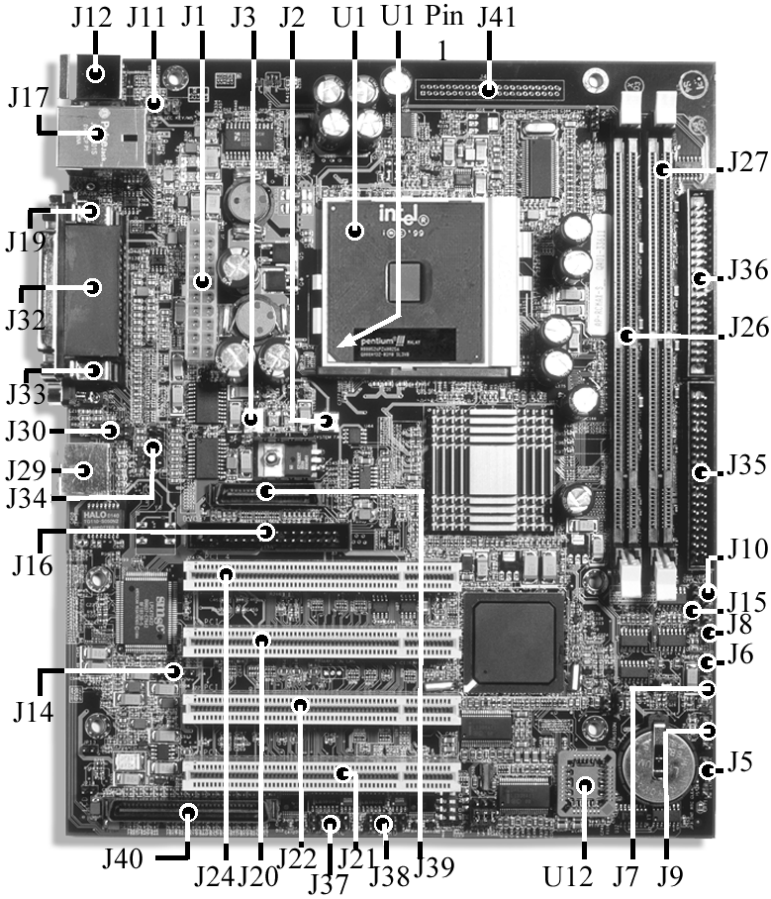


Figure 1-3 Location of Components and Connectors



Index of Connectors

Please refer to Appendix A for pin-out descriptions.

Table 1-11 Connectors descriptions

Connector	Description
J1	ATX Power
J2	Sys. Fan
J3	CPU Fan
J5	Power LED/Keylock
J6	HDD LED
J7	RESET
J8	Soft Power Switch
J9	Speaker
J10	SMBUS Header
J11	Keyboard/Mouse Header
J12	(Bottom)Keyboard – PS/2 (Top)Mouse – PS/2
J14	GPIO Header
J15	Infra Red
J16	FDD
J17	(Bottom) USB (2x) - (Top) Ethernet 2 (Device 245Dh) (Optional)
J19	VGA DB15
J20	PCI Connector 3
J21	PCI Connector 1
J22	PCI Connector 2
J23	PCI Connector 4
J29	Ethernet 1 (Device 2459h) RJ45
J30	Ethernet 1 (Device 2459h) Header
J32	LPT - Parallel
J33	SER A
J34	SER B
J35	Primary IDE
J36	Secondary IDE
J37	SER C
J38	SER D

J39	DVO Connector
J40	LCD Connector (Optional)
J41	Alt. Secondary IDE

User's Notes:

Chapter 2 Embedded BIOS 2000 Setup

Your Raptor MicroATX features General Software Embedded BIOS 2000. The system configuration parameters are set via the BIOS setup. Since the BIOS Setup resides in the ROM BIOS, it is available each time the computer is turned on.

General Software's EMBEDDED BIOS brand BIOS (Basic Input/Output System) pre-boot firmware is the industry's standard product used by most designers of embedded X86 computer equipment in the world today. Its superior combination of configurability and functionality enables it to satisfy the most demanding ROM BIOS needs for embedded designers. Its modular architecture and high degree of configurability make it the most flexible BIOS in the world.

When your platform is powered on, Embedded BIOS tests and initializes the hardware and programs the chipset and other peripheral components. During this time, Power On Self Test (POST) progress codes are written by the system BIOS to I/O port 80h, allowing the user to monitor the progress with a special monitor. Appendix B lists the POST codes and their meanings.
During early POST, no video is available to display error messages should a critical error be encountered; therefore, POST uses beeps on the speaker to indicate the failure of a critical system component during this time. Consult Appendix B for a list of Beep codes used by the BIOS.

Starting BIOS Setup

When a keyboard and video device are attached, the MicroATX can display either a traditional character-based PC BIOS display with memory count-up, or it can display a graphical POST with splash screen and progress icons. Both POST displays accept a <DEL> key press to enter the setup screen, and both display boot-time progress activity displays. The graphical display shows the status of file system devices, but omits character-based PCI resource display. The text-based POST displays the memory count-up and the PCI resource assignment table.

BIOS Setup Main Menu

The MicroATX is configured from within the Setup Screen System, a series of menus that can be invoked from POST by pressing the <DEL> key.

Once in the Setup Screen System, the user can navigate with the UP and DOWN arrow keys from the main. TAB and ENTER are used to advance to the next field, and '+' and '-' keys cycle through values, such as those in the Basic Setup Screen.

The BIOS Setup main menu is organized into 14 windows. Each window is discussed in this chapter.

Each window contains several options. Clicking on each option activates a specific function. The BIOS Setup options and functions are described in this chapter. Some options may not be available in your BIOS. The windows are:

- Basic CMOS Configuration
- Features Configuration
- Custom Configuration
- Shadow Configuration
- Reset CMOS to Last Known Values
- Reset CMOS to Factory Defaults
- Write to CMOS and Exit
- Exit Without Saving CMOS

Basic CMOS Configuration Setup Screen

The drive types, boot activities, and POST optimizations are configured from the Basic Setup Screen (Figure 2-1). In order to use disk drives with your system, you must select appropriate assignments of drive types in the left-hand column. Then, if you are using true floppy and IDE drives (not memory disks that emulate these drives), you need to configure the drive types themselves in the Floppy Drive Types and IDE Drive Geometry sections. Finally, you'll need to configure the boot sequence in the middle of the screen. Once these selections have been made, your system is ready to use.

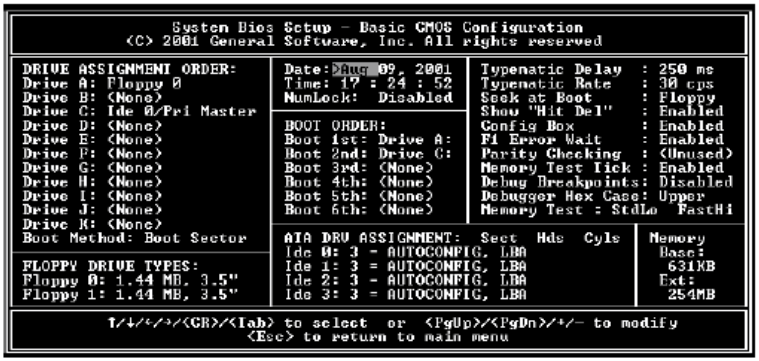


Figure 2-1: The Embedded BIOS Basic Setup Screen is used to configure drives, boot actions, and POST.

Configuring Drive Assignments

Embedded BIOS allows the user to map a different file system to each drive letter. The BIOS allows file systems for each floppy (Floppy0 and Floppy1), and each IDE drive (Ide0, Ide1, Ide2, and Ide3). Figure 2-1 shows how the first floppy drive (Floppy0) is assigned to drive A: in the system, and then shows how the first IDE drive (Ide0) is assigned to drive C: in the system.

To switch two floppy disks around or two hard disks around, just map Floppy0 to B: and Floppy1 to A:, and for hard disks map Ide0 to D: and Ide1 to C:.

Caution: Take care to not skip drive A: when making floppy disk assignments, as well as drive C: when making hard disk assignments. The first floppy should be A:, and the first hard drive should be C:. Also, do not assign the same file system to more than one drive letter. Thus, Floppy0 should not be used for both A: and B:. The BIOS permits this to allow embedded devices to alias drives, but desktop operating systems may not be able to maintain cache coherency with such a mapping in place.

Date/Time

Select the Date/Time option to change the date or time. The current date and time are displayed. Enter new values through the displayed window.

NumLock

Set this option to Disabled to turn the Num Lock key off when the computer is booted so you can use the arrow keys on both the numeric keypad and the keyboard.

Seek at Boot

Set this option to the device that will perform a Seek operation at system boot. The settings are Floppy (*default*), IDE, Both, and None.

Typematic Rate

The settings are 30 cps (*default*), 24, 20, 15, 12, 10, 8, and 6.

Typematic Delay

The settings are 250 ms (*default*), 500 ms, 750 ms, 1000 ms, and disabled.

Config Box

Set this option to show the configuration box during boot. The settings are Enabled (*default*) and Disabled.

Memory Test Tick

The settings are Enabled (*default*) and Disabled.

Memory Test

This option configures the test that will be performed on the Low memory (below 1 MB) and the High Memory (above 1MB). The settings are Full (exhaustive testing), Standard, and Fast. The default is StdLo and FullHi.

Loader
Parity Checking
Debug Breakpoints
Debugger Hex Case

These options are not available.

Show "Hit Del"

Set this option to Disabled to prevent the message

```
Hit <DEL> if you want to run Setup
```

from appearing on the first BIOS screen when the computer boots. The setting is either Disabled or Enabled. The default setting is Enabled.

F1 Error Wait

If this option is set to Enabled, the BIOS waits for the user to press <F1> before continuing. If this option is set to Disabled, the BIOS continues the boot process without waiting for <F1> to be pressed.

Configuring Floppy Drive Types

Choose either Floppy Drive 0 or 1 to specify the floppy drive type. The settings are *360 KB 5¼"*, *1.2 MB 5¼"*, *720 KB 3½"*, *1.44 MB 3½"* and *2.88 MB 3½"*.

Floppy0 refers to the first floppy disk drive on the drive ribbon cable (normally drive A:), and Floppy1 refers to the second drive (drive B:).

Configuring IDE Drive Types

The following table shows the drive assignments for Ide0-Ide3:

File System	Controller	Master/Slave
Ide0	Primary (1f0h)	Master
Ide1	Primary (1f0h)	Slave
Ide2	Secondary (170h)	Master
Ide3	Secondary (170h)	Slave

To use the primary master IDE drive in your system (the typical case), just configure Ide0 in this section, and map Ide0 to drive C: in the Configuring Drive Assignments section.

The IDE Drive Types section lets you select the type for each of the four IDE drives: None, User, Physical, LBA, or CHS.

The **User** type allows the user to select the maximum cylinders, heads, and sectors per track associated with the IDE drive. This method is now rarely used since LBA is now in common use.

The **Physical** type instructs the BIOS to query the drive's geometry from the controller on each POST. No translation on the drive's geometry is performed, so this type is limited to drives of 512MB or less. Commonly, this is used with embedded ATA PC Cards.

The **LBA** type instructs the BIOS to query the drive's geometry from the controller on each POST, but then translate the geometry according to the industry-standard LBA convention. This supports up to 128GB drives. ***Use this method for all new drives.***

The **CHS** type instructs the BIOS to query the drive's geometry from the controller on each POST, but then translate the geometry according to the Phoenix CHS convention. Using this type on a drive previously formatted with LBA or Physical geometry might show data as being missing or corrupted.

EMBEDDED BIOS supports user-defined steps in the boot sequence. When the entire system has been initialized, POST executes these steps in order until an operating system successfully loads. In addition, other pre-boot features can be run before, after, or between operating system load attempts.

The following actions are supported:

Drive A: - D: Boot operating system from specified drive. The standard boot record will be invoked, causing DOS, Windows95, Windows 98, Windows ME, Windows 2000, Windows NT, Windows XP, Linux, or other industry-standard operating systems to load.

CDROM: Boot from the first IDE CDROM found that contains an El Torito bootable CDROM.

None: No action; POST proceeds to the next activity in the sequence.

Reboot: Reboot the board.

Debugger; MFGMODE; DOS in ROM; Alarm; Maintenance; RAS; Power Off; CLI: Options not available.

Features Configuration Setup Screen

Advanced Power Management

Set this option to Enabled the power management and APM (Advanced Power Management) features. The settings for this option are: Disabled (*default*) and Enabled. Note that the CICH has limited APM support.

Graphical/Audio POST

Set this option to Enabled (*default*) the Splash Screen during boot. The settings for this option are: Disabled and Enabled (*default*).

POST Memory Manager

The settings are Enabled and Disabled (*default*).

System Management BIOS

The settings are Enabled (*default*) and Disabled. This option assembles the SMBIOS (formerly DMI) information.

Custom Configuration Setup Screen

The hardware-specific features are configured with the Custom Setup Screen.

L2 Cache

This option enables or disables the L2 Cache.

(Redir Debugger)

This option is not available.

Parallel Port

This option enables (*default*) or disables the Parallel Port.

Parallel Port IRQ

This option specifies the IRQ always used by the parallel port. The settings are (IRQ) 5 and (IRQ) 7 (*default*).

Parallel Port Address

This option specifies the base I/O port address of the parallel port on the motherboard. The settings are 378h (*default*), 278h and 3BCh.

Parallel Port Mode

This option specifies the parallel port mode. The settings are: Printer (*default*), ECP/EPP 1.7, SPP, SPP/EPP 1.9, ECP, ECP/EPP 1.9, and SPP/EPP 1.7.

SER A

This option enables (*default*) or disables the Serial Port A.

SER A Address

This option specifies the base I/O port address of the Serial port A on the motherboard. The settings are 3F8h (*default*), 2F8h, 3E8h, 2E8h, 338h, 220h, 228h, and 238.

SER A IRQ

This option specifies the IRQ of the Serial port A on the motherboard. The settings are 4 (*default*), 3, 5, 7, 12, 14, and 15.

SER B

This option enables (*default*) or disables the Serial Port B.

SER B Address

This option specifies the base I/O port address of the Serial port B on the motherboard. The settings are 3F8h, 2F8h (*default*), 3E8h, 2E8h, 338h, 220h, 228h, and 238.

SER B IRQ

This option specifies the IRQ of the Serial port A on the motherboard. The settings are 4, 3 (*default*), 5, 7, 12, 14, and 15.

SER C

This option enables (*default*) or disables the Serial Port C.

SER C Address

This option specifies the base I/O port address of the Serial port C on the motherboard. The settings are 3F8h, 2F8h, 3E8h (*default*), 2E8h, 338h, 220h, 228h, and 238.

SER C IRQ

This option specifies the IRQ of the Serial port C on the motherboard. The settings are 4, 3, 5 (*default*), 7, 12, 14, and 15.

SER D

This option enables (*default*) or disables the Serial Port D.

SER D Address

This option specifies the base I/O port address of the Serial port D on the motherboard. The settings are 3F8h, 2F8h, 3E8h, 2E8h (*default*), 338h, 220h, 228h, and 238.

SER D IRQ

This option specifies the IRQ of the Serial port D on the motherboard. The settings are 4, 3, 5, 7 (*default*), 12, 14, and 15.

Shadow Configuration Setup Screen

The Shadow Configuration Setup Screen (Figure 2-2) allows the selective enabling and disabling of shadowing in 16KB sections, except for the top 64KB of the BIOS ROM, which is shadowed as a unit. Normally, shadowing should be enabled at C000/C400 (to enhance VGA ROM BIOS performance) and then E000-F000 should be shadowed to maximize system ROM BIOS performance.

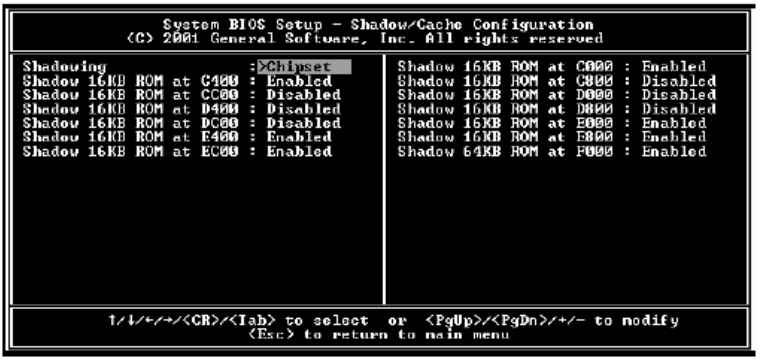


Figure 2-2: The Embedded BIOS Shadow Setup Screen is used to configure ROM shadowing.

Reset CMOS to Last Known Values

Loads the CMOS to the last known values.

Reset CMOS to Factory Defaults

The Fail-Safe CMOS factory Setup option settings can be loaded by selecting the Reset CMOS to Factory Defaults. Use this option as a diagnostic aid if the system is behaving erratically.

Write to CMOS and Exit

Exit BIOS saving the changes.

Exit without Changing CMOS

This option allows exiting the BIOS setup without saving any change to the CMOS.

Chapter 3 Upgrading

Upgrading the System Memory

The Raptor MicroATX allows an upgrade of the system memory with up to 512MB unbuffered SDRAM DIMM modules in two memory slots. ECC and non-ECC modules are supported (Although ECC modules may be used, the 815E chipset does not have support for ECC). It is very important that the quality of the DIMMs is good. Unreliable operation of the system may result if poor quality DIMMs are used. Always purchase your memory from a reliable source. We strongly recommend using PC133 memory module for higher performance when using 133MHz PSB processors, but PC100 memory modules may be used. PC66 memory modules cannot be used even if a Celeron 66MHz PSB processor is being used.

Upgrading the Microprocessor

The latest revision of the Raptor MicroATX currently supports full series of Intel Celeron (FC-PGA 66MHz PSB, FC-PGA 100MHz PSB and FC-PGA2 (0.13u) 100MHz PSB) and Pentium III (FC-PGA 100MHz PSB, FC-PGA 133 PSB and FC-PGA2 (0.13u) 133MHz PSB) PGA370 processors. Please, check the manufacturer's web site for details and revisions regarding CPU speed.

Since the Raptor MicroATX features CPU auto-sensing device there is no jumper to be set when changing the CPU.

User's Notes:

Appendix A Technical Specifications

Chipsets

Core Logic

Intel 815E (North Bridge)/C-ICH (South Bridge) Chipset.

Peripheral I/O

Standard Microsystems (SMSC) LPC47S422.

Micro Processor Support

Intel Celeron (FC-PGA 66MHz PSB, FC-PGA 100MHz PSB and FC-PGA2 (0.13u) 100MHz PSB) and Pentium III (FC-PGA 100MHz PSB, FC-PGA 133 PSB and FC-PGA2 (0.13u) 133MHz PSB) PGA370 processors.

System Memory

Memory Capacity

Up to 512MB unbuffered SDRAM DIMM Modules.

Memory Type

Two sockets for JEDEC standard (168 pins) DIMMs. The memory configuration is set automatically through BIOS via SPD. Supports SDRAM 3.3V SDRAM PC100 and PC133 memory modules. ECC and non-ECC, unbuffered modules are supported.

Bios

System BIOS

General Software Embedded BIOS 2000 with Flash BIOS option.

Flash BIOS

Optional feature for System BIOS. Flash programming built into the BIOS. BIOS to be flashed is read from a floppy when system booted from MS-DOS.

Embedded I/O

Floppy

2 Floppies up to 2.88 MB.

IDE

Dual channel PCI 32-bit EIDE controller – UDMA 66/100 supported. One extra connector (mini-Header 44 pin) in parallel to IDE1 for Solid State IDE disk or any 44 pin IDE device support.

Serial Ports

Four high speed RS-232 (or two RS-232 and two RS-422/485 optional) serial ports 16 Bytes FIFO (16550/16550D). Factory optional feature RS-422/485 Full duplex or Half-duplex (RTS flow control), termination resistors on/off, transient suppression on transmitter lines.

Parallel Port

One Centronics™ compatible bi-directional parallel port. EPP/ECP mode compatible.

Mouse Port

One PS/2 mouse and one PS/2 keyboard connectors.

Auxiliary Keyboard/Mouse header for front panel access.

USB Interfaces

Two Universal Serial Bus connectors.

On-board Ethernet

Two RJ45 Ethernet connectors.

Industrial Devices

Temperature and Voltage Device

Automatic CPU voltage & temperature monitoring device (optional).

Power Management

Power button function: advanced power management support.

I2C/SMBUS

SMBus/I2C header.

General Purpose I/O lines

Four general purpose I/O lines in a header.

Miscellaneous

CMOS/Battery

RTC with lithium battery. No external battery is required.

Control Panel Connections

Reset, Keylock, Speaker, Soft Power. LEDs for power and IDE.

CPU Socket

Standard ZIF (Zero Insertion Force), PGA 370.

Form Factor

MicroATX form factor (8" x 9.6").

PCB Construction

Six Layers, dry film mask.

Manufacturing Process

Automated surface mount.

Table A-1 Environmental

Environmental	Operating	Non-operating
Temperature	0° to +55° C	-40° to +65° C
Humidity	5 to 95% @ 40° C non-condensing	5 to 95% @ 40° C non-condensing
Shock	2.5G @ 10ms	10G @ 10ms
Vibration	0.25 @ 5-100Hz	5 @ 5-100Hz

Memory Map

Address Range Decimal	Address Range Hexadecimal	Size	Description
960K-1M	0F0000-0FFFFF	64 KB	Upper BIOS
896K-960K	0E0000-0EFFFF	64 KB	Lower BIOS
768K-896K	0C0000-0DFFFF	128 KB	Expansion Card BIOS and Buffer
640K-768K	0A0000-0BFFFF	128 KB	Standard PCI/ISA Video Memory
633K-640K	09E400-09FFFF	7KB	BIOS Reserved
512K-633K	080000-09E3FF	121 KB	Ext. Conventional memory
0K- 512K	000000-07FFFF	512 KB	Conventional memory

DMA Channels

DMA #	Data Width	System Resource
0	8- or 16-bits	
1	8- or 16-bits	Parallel port (for ECP) (if selected)
2	8- or 16-bits	Floppy Drive
3	8- or 16-bits	Parallel port (for ECP) (if selected)
4	Reserved-	cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

I/O Map

Address (hex)	Description
0000-000F	DMA 1
0020-0021	Interrupt Controller 1
0040	Timer/Counter 0
0041	Timer/Counter 1
0042	Timer/Counter 2
0043	Timer Control Word
0060	Keyboard Controller Byte _ Reset IRQ
0061	NMI Status and Control
0070, bit 7	NMI enable
0070, bits 6:0	RTC Index
0071	RTC Data
0072	RTC Extended Index
0073	RTC Extended Data
0080-008F	DMA page registers / POST code display also located at 0080h
0092	Port 92
00A0-00A1	Interrupt Controller 2
00B2-00B3	APM control
00C0-00DE	DMA 2
00F0	Coprocessor Error
0170 _ 0177	Secondary IDE channel
01F0 _ 01F7	Primary IDE channel
0278-027F	LPT2 (if selected)
02E8-02EF	COM4 (default)
02F8-02FF	COM2 (default)
0310	Watch-Dog Timer (if selected)
0376	Secondary IDE channel command port
0377	Floppy channel 2 command
0377, bit 7	Floppy disk change, channel 2
0377, bits 6:0	Secondary IDE channel status port
0378-037F	LPT1 (default)
03B4-03B5	Video (VGA)
03BA	Video (VGA)
03BC-03CD	LPT3 (if selected)
03C0-03CA	Video (VGA)
03CC	Video (VGA)
03CE-03CF	Video (VGA)
03D4-03D5	Video (VGA)
03DA	Video (VGA)

Address (hex)	Description
03E8-03EF	COM3 (default)
03F0-03F5	Floppy Channel 1
03F6	Primary IDE channel command port
03F7	Floppy Channel 1 command
03F7, bit 7	Floppy disk change channel 1
03F7, bits 6:0	Primary IDE channel status report
03F8-03FF	COM1 (default)
0CF8-0CFB - 4 bytes	PCI configuration address register
0CF9	Reset control register
0CFC-0CFF - 4 bytes	PCI configuration data register

PCI Configuration Space Map

Bus #	Device #	Function #	Description
00	00	00	815E (Host Bridge)
00	02	00	815E VGA Controller
00	1E	00	Hub Interface to PCI Bridge
00	1F	00	C-ICH LPC Bridge
00	1F	01	C-ICH Master IDE Controller
00	1F	02	C-ICH USB
00	1F	03	C-ICH SMBus Controller
01	08	00	LAN0 Controller (Ethernet 2459h)
01	09	00	LAN1 Controller (Ethernet 245Dh)
01	0F	00	PCI expansion slot 1
01	0E	00	PCI expansion slot 2
01	0D	00	PCI expansion slot 3
01	0C	00	PCI expansion slot 3

Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer

1	Reserved (keyboard)
2	Reserved (cascade)
3	COM2*
4	COM1*
5	COM3*
6	Floppy Drive
7	LPT1* / COM4*
8	Real time clock
9	User Available for PCI
10	User Available for PCI
11	User Available for PCI
12	PS/2 mouse port
13	Reserved (math coprocessor)
14	Primary IDE
15	Secondary IDE

**Default, but can be changed to another IRQ*

PCI Interrupt Routing Map

C-ICH Signal	ID SEL	PIRQ A	PIRQ B	PIRQ C	PIRQ D	PIRQ E	PIRQ F
PCI Slot 1	AD31	INTB	INTC	INTD	INTA		
PCI Slot 2	AD30	INTC	INTD	INTA	INTB		
PCI Slot 3	AD29	INTD	INTA	INTB	INTC		
PCI Slot 4	AD28	INTA	INTB	INTC	INTD		
Ethernet 2459h						INTE	
Ethernet 245Dh							INTF
USB					INTD		
SMBus			INTB				
VGA		INTA					

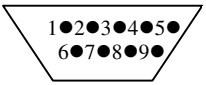
SMBUS

Device	Slave Address
MAX1617	0011000b
LM81	0101101b
DIMM0	1010000b
DIMM1	1010001b
Clock Chip Write	1010010b
Clock Chip Read	1010011b

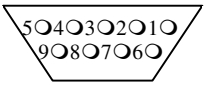
Connectors Pin-out

How to identify pin number 1: Looking to the solder side (The board side without components) of the PCB (Printed Circuit Board), pin number 1 will have a squared pad ■. Other pins will have a circular pad ●.

How to identify other pins: Connectors type DB, PS/2, RJ45, Power ATX and USB are industry standards. DB connectors, for instance, are numbered sequentially. The first row is numbered in sequence (be aware that male and female connectors are mirrored – male connectors are numbered from left to right when viewed from front and female connectors are numbered from right to left when viewed from front). The following rows resume the counting on the same side of pin number 1. The counting is NOT circular like Integrated Circuits (legacy from electronic tubes).

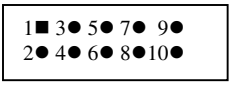


DB9 Male
Front view



DB9 Female
Front view

Header connectors are numbered alternately, i.e. pin number 2 is in the other row, but in the same column of pin number 1. Pin number 3 is in the same row of pin 1, but in the next column and so forth.



Header 10 pin connector
View from solder side of the PCB

Table A-9 Serial Port SER A DB9 Connector

Pin#	Serial Port DB9M – J33
1	DCD
2	RX
3	TX
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

Table A-10 Serial Port SER B Header Connector

Pin#	Serial Port Header J34
1	DCD
2	DSR
3	RX
4	RTS
5	TX
6	CTS
7	DTR
8	RI
9	GND
10	Key

Table A-11 J5 Power LED/Keylock Header Connector Pin-out

Pin#	PWR LED/KBD Lock Header – J5
1	Power LED Anode
2	NC
3	Cathode
4	KEYLOCK#
5	Cathode

Table A-12 Serial Port SER C Header Connector

Pin#	Serial Port Header J37
1	DCD - RS-422/485RXA(opt.)
2	DSR
3	RX - RS-422/485TXB(opt.)
4	RTS
5	TX - RS-422/485TXA(opt.)
6	CTS
7	DTR
8	RI – RS-422/485RXB(opt.)
9	GND
10	Key

Table A-13 Serial Port SER D Header Connector

Pin#	Serial Port Header J38
1	DCD - RS-422/485RXA(opt.)
2	DSR
3	RX - RS-422/485TXB(opt.)
4	RTS
5	TX - RS-422/485TXA(opt.)
6	CTS
7	DTR
8	RI – RS-422/485RXB(opt.)
9	GND
10	Key

Table A-14 J29 Ethernet 1 (Device 2459h) RJ45

Pin#	Ethernet RJ45 – J29
1	TX+
2	TX-
3	RX+
4	Shorted to 5
5	Shorted to 4
6	RX-
7	Shorted to 8
8	Shorted to 7

Table A-15 J17 USB/Ethernet 2 (optional) (Device 245D) Connector

Pin#	USB Connector – J17A
1	+5V – USB1
2	-D – USB1
3	+D – USB1
4	GROUND – USB1
5	+5V – USB2
6	-D – USB2
7	+D – USB2
8	GROUND – USB2
Pin#	**Ethernet 2 (optional) Connector – J17B**
1	TX+
2	TX-
3	RX+
4	Shorted to 5
5	Shorted to 4
6	RX-
7	Shorted to 8
8	Shorted to 7

Table A-16 J32 Parallel DB25 Connector

Pin#	Parallel DB25F – J32
1	-STROBE
2	+DATA BIT 0
3	+DATA BIT 1
4	+DATA BIT 2
5	+DATA BIT 3
6	+DATA BIT 4
7	+DATA BIT 5
8	+DATA BIT 6
9	+DATA BIT 7
10	ACK1
11	BUSY
12	PAPER EMPTY
13	SLCT
14	AUTOFEED
15	ERROR
16	INIT
17	SLCT IN
18-25	GND

Table A-17 J30 Ethernet 1 (Device 2459h) Header Connector

Pin#	Ethernet Header – J30
1	Connected to pin 4 & 5 of RJ45
2	Connected to pin 7 & 8 of RJ45
3	RX+
4	RX-
5	Speed LED Cathode
6	Speed LED Anode
7	ACT LED Cathode
8	ACT LED Anode
9	TX+
10	TX-

Table A-18 Infra Red, HDD LED, CPU Fan, SYS Fan, GPIO, SMBus, and Speaker.

Connector	Description					
J15	**Infra Red (optional)**					
	1)Rx	2)Tx	3)GND	4)NC	5)Key	6)Vcc
J6	**HDD LED**					
	1)Anode			2)Cathode		
J3	**CPU FAN**					
	1)Sense		2)+12V		3)GND	
J2	**SYS FAN**					
	1)Sense		2)+12V		3)GND	
J9	**Speaker**					
	1)+5V	2)NC		3)NC	4)Signal	
J14	**GPIO**					
	1)GP21	2)GP23	3)GND		4)GP34	5)GP35
J10	**SMBus/I2C**					
	1)SMCLOCK	2)KEY	3)GND		4)SMDATA	5)+5V

Table A-19 J11 Keyboard/Mouse Header Connector

Pin#	Keyboard/Mouse Header - J11
1	Mouse CLK
2	Keyboard CLK
3	HDD LED
4	Keyboard Data
5	VCC
6	VCC
7	GND
8	Mouse Data
9	GND
10	Key

Table A-20 J40 LCD Connector (Optional)

Pin#	Description	Pin#	Description
1	+5VSAFE	35	BE4
2	+12VSAFE	36	BE5
3	DCLK	37	BE6
4	LIGHT ON	38	BE7
5	DE	39	GND
6	HSYNC	40	RO0
7	GND	41	RO1
8	VSYNC	42	RO2
9	GND	43	RO3
10	RE0	44	GND
11	RE1	45	RO4
12	RE2	46	RO5
13	RE3	47	RO6
14	GND	48	RO7
15	RE4	49	GND
16	RE5	50	GO0
17	RE6	51	GO1
18	RE7	52	GO2
19	GND	53	GO3
20	GE0	54	GND
21	GE1	55	GO4
22	GE2	56	GO5
23	GE3	57	GO6
24	GND	58	GO7
25	GE4	59	GND
26	GE5	60	BO0
27	GE6	61	BO1
28	GE7	62	BO2
29	GND	63	BO3
30	BE0	64	GND
31	BE1	65	BO4
32	BE2	66	BO5
33	BE3	67	BO6
34	GND	68	BO7

User's Notes:

Appendix B Flash BIOS programming and codes

The Raptor MicroATX offers the optional FLASH BIOS. When installed, you will be able to update your BIOS without having to replace the EPROM. The General Software embedded BIOS 2000 will read the new BIOS file from a floppy disk when running MS-DOS, replace the old BIOS and ask you to reboot your computer.

When updating your BIOS, make sure you have a disk with the correct BIOS file (its size should be 4Mb (512kB)).

How to reflash the BIOS:

About the General Software Reflash utility:

Reflash is a simple utility that loads a valid Embedded BIOS image, and uses the media driver from the BIOS within that image to reflash the BIOS. Be aware that this operation MUST NOT BE INTERUPTED! A power outage may be fatal. No recovery method is provided, since Embedded BIOS does not support a boot block recovery structure at this time.

Running Reflash from the command line:

- Boot from MS-DOS without loading EMM386.exe and HIMEM.SYS.
- Have a directory containing the following files:
    - Reflash.exe
    - Reflash.cmd
    - BIOS.bin
    - BIOS.abs

  Where "BIOS" is the BIOS revision file that you want to load in the flash part.
- Type reflash and hit <enter>.
- Answer yes to the confirmation question.
- Reboot the machine when the procedure is over.

Troubleshooting POST

Embedded BIOS writes progress codes, also known as POST codes, to I/O port 80h during POST, in order to provide information to OEM developers about system faults. These POST codes may be monitored by a port 80h card in a PCI slot; they are not displayed on the screen.

Table B-1 Embedded BIOS 2000 POST Codes

Mnemonic Code	Code	System Progress Report
POST_STATUS_START	00h	Start POST (BIOS is executing).
POST_STATUS_CPUTEST	01h	Start CPU register test.
POST_STATUS_DELAY	02h	Start power-on delay.
POST_STATUS_ DELAYDONE	03h	Power-on delay finished.
POST_STATUS_ KBDBATRDY	04h	Keyboard BAT finished.
POST_STATUS_ DISABSHADOW	05h	Disable shadowing & cache.
POST_STATUS_ CALCCKSUM	06h	Compute ROM CRC, wait for KBC.
POST_STATUS_ CKSUMGOOD	07h	CRC okay, KBC ready.
POST_STATUS_BATVRFY	08h	Verifying BAT command to KB.
POST_STATUS_KBDCMD	09h	Start KBC command.
POST_STATUS_KBDDATA	0ah	Start KBC data.
POST_STATUS_ BLKUNBLK	0bh	Start pin 23,24 blocking & unblocking.
POST_STATUS_KBDNOP	0ch	Start KBC NOP command.
POST_STATUS_SHUTTEST	0dh	Test CMOS RAM shutdown register.
POST_STATUS_ CMOSDIAG	0eh	Check CMOS checksum.
POST_STATUS_CMOSINIT	0fh	Initialize CMOS contents.
POST_STATUS_ CMOSSTATUS	10h	Initialize CMOS status for date/time.
POST_STATUS_ DISABDMAINT	11h	Disable DMA, PICs.
POST_STATUS_ DISABPORTB	12h	Disable Port B, video display.

Mnemonic Code	Code	System Progress Report
POST_STATUS_BOARD	13h	Initialize board, start memory detection.
POST_STATUS_ TESTTIMER	14h	Start timer tests.
POST_STATUS_ TESTTIMER2	15h	Test 8254 T2, for speaker, port B.
POST_STATUS_ TESTTIMER1	16h	Test 8254 T1, for refresh.
POST_STATUS_ TESTTIMER0	17h	Test 8254 T0, for 18.2Hz.
POST_STATUS_ MEMREFRESH	18h	Start memory refresh.
POST_STATUS_ TESTREFRESH	19h	Test memory refresh.
POST_STATUS_TEST15US	1ah	Test 15usec refresh ON/OFF time.
POST_STATUS_TEST64KB	1bh	Test base 64KB memory.
POST_STATUS_TESTDATA	1ch	Test data lines.
POST_STATUS_TESTADDR	20h	Test address lines.
POST_STATUS_ TESTPARITY	21h	Test parity (toggling).
POST_STATUS_ TESTMEMRDWR	22h	Test Base 64KB memory.
POST_STATUS_SYSINIT	23h	Prepare system for IVT initialization.
POST_STATUS_ INITVECTORS	24h	Initialize vector table.
POST_STATUS_ 8042TURBO	25h	Read 8042 for turbo switch setting.
POST_STATUS_ POSTTURBO	26h	Initialize turbo data.
POST_STATUS_ POSTVECTORS	27h	Modification of IVT.
POST_STATUS_ MONOMODE	28h	Video in monochrome mode verified.
POST_STATUS_ COLORMODE	29h	Video in color mode verified.
POST_STATUS_ TOGGLEPARITY	2ah	Toggle parity before video ROM test.
POST_STATUS_ INITBEFOREVIDEO	2bh	Initialize before video ROM check.

Mnemonic Code	Code	System Progress Report
POST_STATUS_ VIDEOROM	2ch	Passing control to video ROM.
POST_STATUS_ POSTVIDEO	2dh	Control returned from video ROM.
POST_STATUS_ CHECKEGAVGA	2eh	Check for EGA/VGA adapter.
POST_STATUS_ TESTVIDEOMEMORY	2fh	No EGA/VGA found, test video memory.
POST_STATUS_RETRACE	30h	Scan for video retrace signal.
POST_STATUS_ ALTDISPLAY	31h	Primary retrace failed.
POST_STATUS_ ALTRETRACE	32h	Alternate found.
POST_STATUS_ VRFYSWADAPTER	33h	Verify video switches.
POST_STATUS_ SETDISPMODE	34h	Establish display mode.
POST_STATUS_ CHECKSEG40A	35h	Initialize ROM BIOS data area.
POST_STATUS_ SETCURSOR	36h	Set cursor for power-on msg.
POST_STATUS_ PWRONDISPLAY	37h	Display power-on message.
POST_STATUS_ SAVECURSOR	38h	Save cursor position.
POST_STATUS_BIOSIDENT	39h	Display BIOS identification string.
POST_STATUS_HITDEL	3ah	Display “Hit <DEL> to ...” message.
POST_STATUS_VIRTUAL	40h	Prepare protected mode test.
POST_STATUS_DESCR	41h	Prepare descriptor tables.
POST_STATUS_ENTERVM	42h	Enter virtual mode for memory test.
POST_STATUS_ENABINT	43h	Enable interrupts for diagnostics mode.
POST_STATUS_ CHECKWRAP1	44h	Initialize data for memory wrap test.
POST_STATUS_ CHECKWRAP2	45h	Test for wrap, find total memory size.
POST_STATUS_ HIGHPATTERNS	46h	Write extended memory test patterns.

Mnemonic Code	Code	System Progress Report
POST_STATUS_ LOWPATTERNS	47h	Write conventional memory test patterns.
POST_STATUS_ FINDLOWMEM	48h	Find low memory size from patterns.
POST_STATUS_ FINDHIMEM	49h	Find high memory size from patterns.
POST_STATUS_ CHECKSEG40B	4ah	Verify ROM BIOS data area again.
POST_STATUS_ CHECKDEL	4bh	Check for <DEL> pressed.
POST_STATUS_ CLREXTMEM	4ch	Clear extended memory for soft reset.
POST_STATUS_ SAVEMEMSIZE	4dh	Save memory size.
POST_STATUS_ COLD64TEST	4eh	Cold boot: Display 1st 64KB memtest.
POST_STATUS_ COLDLOWTEST	4fh	Cold boot: Test all of low memory.
POST_STATUS_ ADJUSTLOW	50h	Adjust memory size for EBDA usage.
POST_STATUS_ COLDHITEST	51h	Cold boot: Test high memory.
POST_STATUS_ REALMODETEST	52h	Prepare for shutdown to real mode.
POST_STATUS_ ENTERREAL	53h	Return to real mode.
POST_STATUS_ SHUTDOWN	54h	Shutdown successful.
POST_STATUS_DISABA20	55h	Disable A20 line.
POST_STATUS_ CHECKSEG40C	56h	Check ROM BIOS data area again.
POST_STATUS_ CHECKSEG40D	57h	Check ROM BIOS data area again.
POST_STATUS_ CLRHITDEL	58h	Clear “Hit <DEL>“ message.
POST_STATUS_ TESTDMAPAGE	59h	Test DMA page register file.
POST_STATUS_ VRFYDISPMEM	60h	Verify from display memory.
POST_STATUS_ TESTDMA0BASE	61h	Test DMA0 base register.

Mnemonic Code	Code	System Progress Report
POST_STATUS_ TESTDMA1BASE	62h	Test DMA1 base register.
POST_STATUS_ CHECKSEG40E	63h	Checking ROM BIOS data area again.
POST_STATUS_ CHECKSEG40F	64h	Checking ROM BIOS data area again.
POST_STATUS_PROGDMA	65h	Program DMA controllers.
POST_STATUS_ INITINTCTRL	66h	Initialize PICs.
POST_STATUS_ STARTKBDTEST	67h	Start keyboard test.
POST_STATUS_KBDRESET	80h	Issue KB reset command.
POST_STATUS_ CHECKSTUCKKEYS	81h	Check for stuck keys.
POST_STATUS_ INITCIRCBUFFER	82h	Initialize circular buffer.
POST_STATUS_ CHECKLOCKEDKEYS	83h	Check for locked keys.
POST_STATUS_ MEMSIZEMISMATCH	84h	Check for memory size mismatch.
POST_STATUS_ PASSWORD	85h	Check for password or bypass setup.
POST_STATUS_ BEFORESETUP	86h	Password accepted.
POST_STATUS_ CALLSETUP	87h	Entering setup system.
POST_STATUS_ POSTSETUP	88h	Setup system exited.
POST_STATUS_ DISPPWRON	89h	Display power-on screen message.
POST_STATUS_DISPWAIT	8ah	Display “Wait...” message.
POST_STATUS_ ENABSHADOW	8bh	Shadow system & video BIOS.
POST_STATUS_ STDCMOSSETUP	8ch	Load standard setup values from CMOS.
POST_STATUS_MOUSE	8dh	Test and initialize mouse.
POST_STATUS_FLOPPY	8eh	Test floppy disks.
POST_STATUS_ CONFIGFLOPPY	8fh	Configure floppy drives.
POST_STATUS_IDE	90h	Test hard disks.
POST_STATUS_ CONFIGIDE	91h	Configure IDE drives.

Mnemonic Code	Code	System Progress Report
POST_STATUS_ CHECKSEG40G	92h	Checking ROM BIOS data area.
POST_STATUS_ CHECKSEG40H	93h	Checking ROM BIOS data area.
POST_STATUS_ SETMEMSIZE	94h	Set base & extended memory sizes.
POST_STATUS_ SIZEADJUST	95h	Adjust low memory size for EBDA.
POST_STATUS_INITC8000	96h	Initialize before calling C800h ROM.
POST_STATUS_CALLC8000	97h	Call ROM BIOS extension at C800h.
POST_STATUS_POSTC8000	98h	ROM C800h extension returned.
POST_STATUS_ TIMERPRNBASE	99h	Configure timer/printer data.
POST_STATUS_ SERIALBASE	9ah	Configure serial port base addresses.
POST_STATUS_ INITBEFORENPX	9bh	Prepare to initialize coprocessor.
POST_STATUS_INITNPX	9ch	Initialize numeric coprocessor.
POST_STATUS_POSTNPX	9dh	Numeric coprocessor initialized.
POST_STATUS_ CHECKLOCKS	9eh	Check KB settings.
POST_STATUS_ ISSUEKBDID	9fh	Issue keyboard ID command.
POST_STATUS_RESETID	0a0h	KB ID flag reset.
POST_STATUS_ TESTCACHE	0a1h	Test cache memory.
POST_STATUS_ DISPSOFTERR	0a2h	Display soft errors.
POST_STATUS_ TYPEMATIC	0a3h	Set keyboard typematic rate.
POST_STATUS_MEMWAIT	0a4h	Program memory wait states.
POST_STATUS_CLRSCR	0a5h	Clear screen.
POST_STATUS_ ENABPTYNMI	0a6h	Enable parity and NMIs.
POST_STATUS_INITE000	0a7h	Initialize before calling ROM at E000h.

Mnemonic Code	Code	System Progress Report
POST_STATUS_CALLE000	0a8h	Call ROM BIOS extension at E000h.
POST_STATUS_POSTE000	0a9h	ROM extension returned.
POST_STATUS_ DISPCONFIG	0b0h	Display system configuration box.
POST_STATUS_ INT19BOOT	00h	Call INT 19h bootstrap loader.
POST_STATUS_ LOWMEMEXH	0b1h	Test low memory exhaustively.
POST_STATUS_ EXTMEMEXH	0b2h	Test extended memory exhaustively.
POST_STATUS_PCIENUM	0b3h	Enumerate PCI busses.

Critical Error BEEP Codes

Embedded BIOS tests much of the hardware early in POST before messages can be displayed on the screen. When system failures are encountered at these early stages, POST uses beep codes (a sequence of tones on the speaker) to identify the source of the error.

The following is a comprehensive list of POST beep codes for the system BIOS. BIOS extensions, such as VGA ROMs and SCSI adapter ROMs, may use their own beep codes, including short/long sequences, or possibly beep codes that sound like the ones below. When diagnosing a system failure, remove these adapters if possible before making a final determination of the actual POST test that failed.

Table B-2 Flash BIOS Beep Errors

Mnemonic Code	Beep Count	Description of Problem
POST_BEEP_REFRESH	1	Memory refresh is not working.
POST_BEEP_PARITY	2	Parity error found in 1st 64KB of memory.
POST_BEEP_BASE64KB	3	Memory test of 1st 64KB failed.
POST_BEEP_TIMER	4	T1 timer test failed.
POST_BEEP_CPU	5	CPU test failed.

Mnemonic Code	Beep Count	Description of Problem
POST_BEEP_GATEA20	6	Gate A20 test failed.
POST_BEEP_DMA	7	DMA page/base register test failed.
POST_BEEP_VIDEO	8	Video controller test failed.
POST_BEEP_KEYBOARD	9	Keyboard test failed.
POST_BEEP_SHUTDOWN	10	CMOS shutdown register test failed.
POST_BEEP_CACHE	11	External cache test failed.
POST_BEEP_BOARD	12	General board initialization failed.
POST_BEEP_LOWMEM	13	Exhaustive low memory test failed.
POST_BEEP_EXTMEM	14	Exhaustive extended memory test failed.
POST_BEEP_CMOS	15	CMOS restart byte test failed.
POST_BEEP_ADDRESS_LINE	16	Address line test failed.
POST_BEEP_DATA_LINE	17	Data line test failed.
POST_BEEP_INTERRUPT	18	Interrupt controller test failed.
POST_BEEP_PASSWORD	1	Incorrect password used to access SETUP.

User's Notes:

Appendix C Communication Devices

The Raptor MicroATX offers On-board two (optional second one) 10/100 Ethernet controllers and four serial ports (Two RS232 + Two RS-232 or RS-422/485(optional)).

On-board Ethernet

Each of the 82801E C-ICH's integrated LAN Controllers includes a 32-bit PCI controller that provides enhanced scatter-gather bus mastering capabilities and enables the LAN Controller to perform high speed data transfers over the PCI bus. Its bus master capabilities enable the component to process high-level commands and perform multiple operations; this lowers processor utilization by off-loading communication tasks from the processor. Two large transmit and receive FIFOs of 3 Kbytes each help prevent data underruns and overruns while waiting for bus accesses. This enables the integrated LAN Controller to transmit data with minimum interframe spacing (IFS).

The LAN Controller can operate in full duplex or half duplex mode. In full duplex mode the LAN Controller adheres to the IEEE 802.3x Flow Control specification. Half duplex performance is enhanced by a proprietary collision reduction mechanism.

The RJ45 Ethernet Connector pin-out of Ethernet 1 (Device 2459h) can be seen on *Table A-14*, the Ethernet 1 (Device 2459h) Header connector pin-out can be seen on *Table A-17* and the RJ45 Ethernet Connector (USB/RJ45 combo) pin-out of Ethernet 2 (Device 245Dh) (optional) can be seen on *Table A-15.*

Serial Ports

The Raptor MicroATX has two fixed RS-232 serial ports SER A and SER B, and two configurable RS-232 or RS-422/485 (optional) serial ports SER C and SER D.

Ports SER C and SER D may have termination resistors and can be configured as Full-duplex (RS-422) or Half-duplex (RS-485). The receiver may be set to always on (RS-422) or enabled by the RTS

signal (RS-485). The transmitter is always controlled by the RTS signal. Therefore, when using RS-422 and RS485 the software application must enable the RTS signal.

For information about jumper settings and connector pin-outs look up for the following tables:

- *Table 1-3* jumper settings for SER C and SER D RS-232/RS-422/485 selection.
- *Table 1-4* jumper settings for SER C RS-422/485 receiver mode.
- *Table 1-5* jumper settings for SER D RS-422/485 receiver mode.
- *Table 1-6* jumper settings for SER C Tx termination resistor option.
- *Table 1-7* jumper settings for SER C Rx termination resistor option.
- *Table 1-8* jumper settings for SER D Tx termination resistor option.
- *Table 1-9* jumper settings for SER D Rx termination resistor option.
- *Table A-9* SER A DB9 Connector pin-out.
- *Table A-10* SER B Header Connector pin-out.
- *Table A-12* SER C Header Connector pin-out.
- *Table A-13* SER D Header Connector pin-out.

TIA/EIA-232

RS is the abbreviation for recommended standard. Usually, it is based on or is identical to other standards, e.g., EIA/TIA-232-F. TIA/EIA-232, previously known as RS-232 was developed in the 1960's to interconnect layers of the interface (ITU–T V.11), but also the pignut of the appropriate connectors (25-pin D-type or 9-pin DB9S) (ISO 2210) and the protocol (ISSUED-T V.24). The interface standard specifies also handshake and control lines in addition to the 2 unidirectional receive data line (RD) and transmit data line (TD). The control lines data carrier detect (DCD), data set ready (DSR), request to send (RTS), clear to send (CTS), data terminal ready (DTR), and the ring indicator (RI) might be used, but do not necessarily have to be (for example, the PC-serial-mouse utilizes only RI, TD, RD and GND). Although the standard supports only low speed data rates and line length of

approximately 20 m maximum, it is still widely used. This is due to its simplicity and low cost.

Electrical

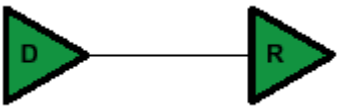
TIA/EIA-232 has high signal amplitudes of ±(5 V to 15 V) at the driver output. The triggering of the receiver depends on the sign of the input voltage: that is, it senses whether the input is above 3 V or less than –3 V. The line length is limited by the allowable capacitive load of less than 2500 pF. This results in a line length of approximately 20 m. The maximum slope of the signal is limited to 30 V/ms. The intention here is to limit any reflections that can occur to the rise-and fall-times of the signal. Therefore, transmission line theory does not need to be applied, so no impedance matching and termination measures are necessary.

Do not connect termination resistor when operating in RS-232 mode.

Protocol

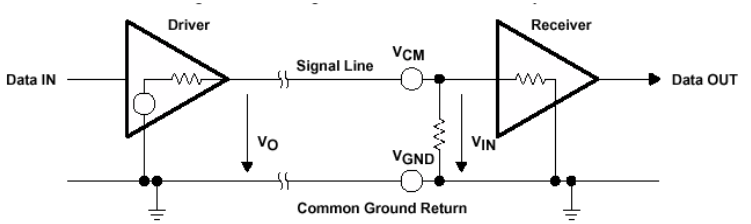
Different from other purely electrical-layer-standards, TIA/EIA-232 defines not only the physical layer of the interface (ITU-T V.11), but also the pinout of the appropriate connectors (25-pin D-type or 9-pin DB9S) (ISO 2210) and the protocol (ITU-T V.24). The interface standard specifies also handshake and control lines in addition to the 2 unidirectional receive data line (RD) and transmit data line (TD). The control lines might be used, but do not necessarily have to be.

RS-232 is Single-Ended Point-to-point Transmission



Single-Ended, Point-to-Point

Single-ended transmission is performed on one signal line, and the logical state is interpreted with respect to ground. For simple, low-speed interfaces, a common ground return path is sufficient; for more advanced interfaces featuring higher speeds and heavier loads, a single return path for each signaling line (twisted pair cable) is recommended. The figure below shows the electrical schematic diagram of a single-ended transmission system.



Advantages of Single-Ended Transmission

The advantages of single-ended transmission are simplicity and low cost of implementation. A single-ended system requires only one line per signal. It is therefore ideal for cabling, and connector costs are more important than the data transfer rate, e.g. PC, parallel printer port or serial communication with many handshaking lines, e.g. EIA-232. Cabling costs can be kept to a minimum with short distance communication, depending on data throughput, requiring no more than a low cost ribbon cable. For longer distances and/or noisy environments, shielding and additional ground lines are essential. Twisted pair cables are recommended for line lengths of more than 1 meter.

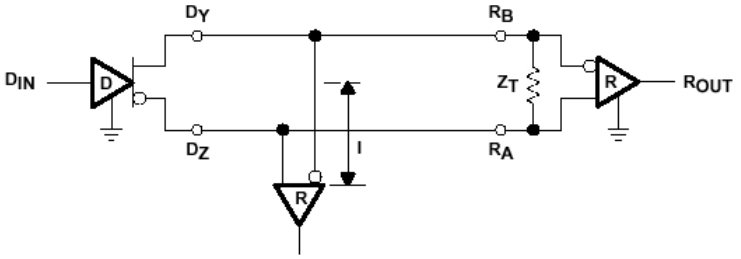
TIA/EIA-422

TIA/EIA-422 (RS-422) allows a multi-drop interconnection of one driver, transmitting unidirectionally to up to 10 receivers. Although it is not capable of bidirectional transfer, it is still applicable and used for talker-audience scenarios.

Electrical

TIA/EIA-422 (ITU-T V.11) is comparable to TIA/EIA-485. It is limited to unidirectional data traffic and is **terminated only at the line-end opposite to the driver**. The maximum line length is 1200m, the maximum data rate is determined by the signal rise- and fall-times at the receiver's side (requirement: <10% of bit duration). TIA/EIA-422 allows up to ten receivers (input impedance of 4 kΩ attached to one driver. The maximum load is limited to 80 Ω. Although any TIA/EIA-485 transceiver can be used in a TIA/EIA-422 system, dedicated TIA/EIA-422 circuits are not feasible for TIA/EIA-485, due to short circuit current limitations. The TIA/EIA-422 standard requires only

short circuit limitation to 150 mA to ground, while TIA/EIA-485 additionally has to limit short circuit currents to 250 mA from the bus pins to –7 V and 12 V to address malfunctions in combination with ground shifts.

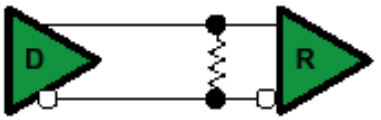


RS-422 is terminated only at the line-end opposite to the driver even if there is only one receiver.

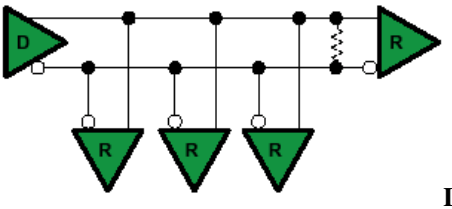
Protocol

Not applicable/none specified. The Raptor MicroATX requires transmitter enabled by the RTS signal.

RS-422 is Differential and may be either Point-to-Point or Multi-Drop Connected



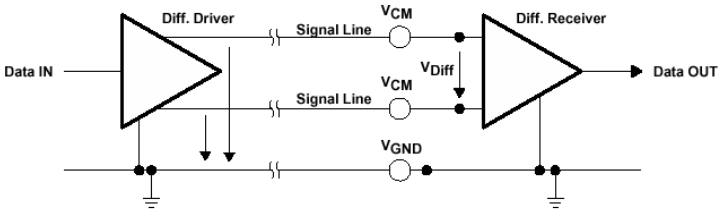
Differential, Point-to-Point



Differential, Multi-Drop

Differential Transmission

For balanced or differential transmission, a pair of signal lines is necessary for each channel. On one line, a true signal is transmitted, while on the second one, the inverted signal is transmitted. The receiver detects voltage difference between the inputs and switches the output depending on which input line is more positive. As shown below, there is additionally a ground return path.



Balanced interface circuits consist of a generator with differential outputs and a receiver with differential inputs. Better noise performance stems from the fact that noise is coupled into both wires of the signal pair in much the same way and is common to both signals. Due to the common mode rejection capability of a differential amplifier, this noise will be rejected. Additionally, since the signal line emits the opposite signal like the adjacent signal return line, the emissions cancel each other. This is true in any case for crosstalk from and to neighboring signal lines. It is also true for noise from other sources as long as the common mode voltage does not go beyond the common mode range of the receiver. Since ground noise is also common to both signals, the receiver rejects this noise as well. The twisted pair cable used in these interfaces in combination with a correct line termination—to avoid line reflections—allows very high data rates and a cable length of up to 1200 m.

Advantages of Differential Transmission

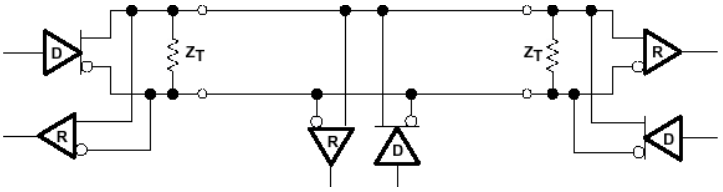
Differential data transmission schemes are less susceptible to common-mode noise than single-ended schemes. Because this kind of transmission uses two wires with opposite current and voltage swings compared to only one wire for single-ended, any external noise is coupled onto the two wires as a common mode voltage and is rejected by the receivers. This two-wire approach with opposite current and voltage swings also radiates less electro-magnetic interference (EMI) noise than single-ended signals due to the canceling of magnetic fields.

TIA/EIA-485

Historically, TIA/EIA-422 was on the market before TIA/EIA-485. Due to the lack of bi-directional capabilities, a new standard adding this feature was created: TIA/EIA-485 . The standard (TIA/EIA-485-A or ISO/IEC 8284) defines the electrical characteristics of the interconnection, including driver, line, and receiver. It allows data rates in the range of 35 Mbps and above and line lengths of up to 1200 m. Of course both limits can not be reached at the same time. Furthermore, recommendations are given regarding wiring and termination. The specification does not give any advice on the connector or any protocol requirements.

Electrical

TIA/EIA-485 describes a half-duplex, differential transmission on cable lengths of up to 1200 m and at data rates of typically up to 35 Mbps (requirement similar to TIA/EIA-422, but tr<30% of the bit duration, there are also faster devices available, suited for higher rates under certain load-conditions). The standard allows a maximum of 32 unit loads of 12 kΩ, equal to 32 standard nodes or even higher count with increased input impedance. The maximum total load should not drop below 52 Ω. The common-mode voltage levels on the bus have to maintain between –7 V and 12 V. The receivers have to be capable to detect a differential input signal as low as 200 mV.

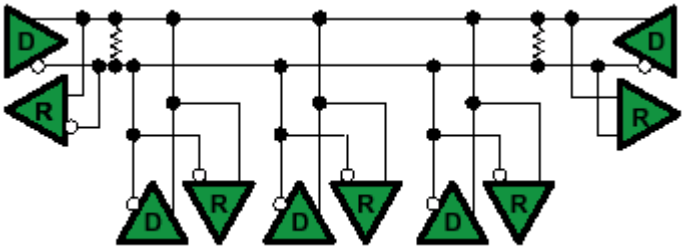


RS-485 is terminated at both sides of the common bus, even if only two stations are connected to the backbone.

Protocol

Not applicable/none specified; exceptions: SCSI systems and the DIN-Bus DIN66348. The Raptor MicroATX requires transmitter enabled by the RTS signal.

RS-485 is Differential and Multi-Point Connected



Differential Transmission

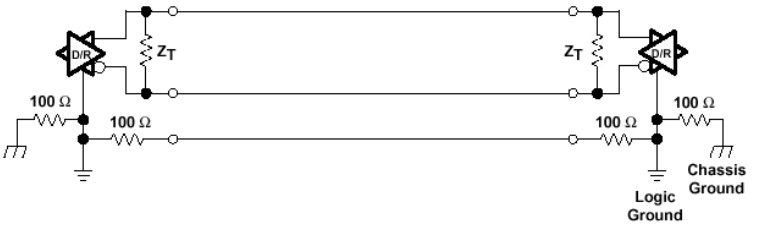
Please, read the Differential Transmission explanation in the previous RS-422 section.

Termination Resistors

Follow instructions in the previous RS-422 and RS-485 sections. The termination resistors available through SW1 are rated to 120Ω.

Ground Connections

All 422- and 485-compliant system configurations shown up to this point do not have incorporated signal-return paths to ground. Obviously, having a solid ground connection so that both receivers and drivers can talk error free is imperative. The figure below shows how to make this connection and recommends adding some resistance between logic and chassis ground to avoid excess ground-loop currents. Logic ground does not have any resistance in its path from the driver or receiver. A potential problem might exist, especially during transients, when a high-voltage potential between the remote grounds could develop. Therefore, some resistance between them is recommended.



Appendix D On-Board Video Controller

The Raptor MicroATX has an On-board video controller/LCD (optional). The On-board video controller is based on the Intel 82815 GMCH.

82815 GMCH Integrated Graphics Support

The GMCH includes a highly integrated graphics accelerator. Its architecture consists of dedicated multi-media engines executing in parallel to deliver high performance 3D, 2D, and motion compensation video capabilities. The 3D and 2D engines are managed by a 3D/2D pipeline preprocessor allowing a sustained flow of graphics data to be rendered and displayed. The deeply pipelined 3D accelerator engine provides 3D graphics quality and performance via per-pixel 3D rendering and parallel data paths which allow each pipeline stage to simultaneously operate on different primitives or portions of the same primitive. The GMCH graphics accelerator engine supports perspective-correct texture mapping, trilinear and anisotropic Mip-Map filtering, Gouraud shading, alpha-blending, fogging and Z-buffering. A rich set of 3D instructions permit these features to be independently enabled or disabled. For the GMCH, a Display Cache (DC) can be used for the Z-buffer (textures and display buffer(s) are located only in system memory). If the display cache is not used, the Z-buffer is located in system memory.
The GMCH integrated graphics accelerator's 2D capabilities include BLT and arithmetic STRBLT engines, a hardware cursor and an extensive set of 2D registers and instructions. The high performance 64-bit BitBLT engine provides hardware acceleration for many common Windows operations. In addition to its 2D/3D capabilities, the GMCH integrated graphics accelerator also supports full MPEG-2 motion compensation for software-assisted DVD video playback, a VESA DDC2B compliant display interface and a digital video out port which may support (via an external TMDS transmitter) digital Flat Panel or Digital CRT displays.

DVO

The GMCH provides interfaces to a standard progressive scan monitor, and TMDS transmitter. These interfaces are only active when running in internal graphics mode.

•The GMCH directly drives a standard progressive scan monitor up to a resolution of 1600x1200 pixels.

•The GMCH provides a Digital Video Out interface to connect an external device to drive a 1280x1024 resolution non-scalar DDP digital Flat Panel with appropriate EDID 1.2 data or digital CRTs. The interface has 1.8V signaling to allow it to operate at higher frequencies.

Display (CRT)

The display function contains a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics and video subsystems to analog data for the monitor. The GMCH's integrated 230 MHz RAMDAC provides resolution support up to 1600x1200. Circuitry is incorporated to limit the switching noise generated by the DACs. Three 8-bit DACs provide the R, G, and B signals to the monitor. Sync signals are properly delayed to match any delays from the D-to-A conversion. Associated with each DAC is a 256 pallet of colors. The RAMDAC can be operated in either direct or indexed color mode. In Direct color mode, pixel depths of 15, 16, or 24 bits can be realized. Non-interlaced mode is supported. Gamma correction can be applied to the display output.
The GMCH supports a wide range of resolutions, color depths, and refresh rates via a programmable dot clock that has a maximum frequency of 230 MHz.

Table D-1 in the next page shows a partial list of display modes supported.

For information about jumper settings and connector pin-outs look up for the following tables:

- *Table 1-11* jumper settings for LCD Panel (optional) Voltage Selection.
- *Table 1-12* jumper settings for Enable/Disable the I2C Channel of the DVO Connector.
- *Table A-20* Pin out of the LCD Header Connector (optional).

Connector J39 (DVO) and J19 (VGA) have standard industry pin outs.

Table D-1 List of Display Modes Supported

Resolution	Bits Per Pixel (frequency in Hz)		
	8-bit Indexed	16-bit	24-bit
320x200	70	70	70
320x240	70	70	70
352x480	70	70	70
352x576	70	70	70
400x300	70	70	70
512x384	70	70	70
640x400	70	70	70
640x480	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
720x480	75,85	75,85	75,85
720x576	60,75,85	60,75,85	60,75,85
800x600	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
1024x768	60, 70,72,75,85	60, 70,72,75,85	60, 70,72,75,85
1152x864	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
1280x720	60,75,85	60,75,85	60,75,85
1280x960	60,75,85	60,75,85	60,75,85
1280x1024	60,70,72,75,85	60,70,72,75,85	60,70,75,85
1600x900	60,75,85	60,75,85	
1600x1200	60,70,72,75		

DVO

The GMCH has a dedicated port for Flat Panel support. This port is a 16 bit digital port (4 control bits and 12 data bits) with a 1.8V interface for high speed signaling. The port is designed to connect to transmission devices.
The GMCH supports a variety of Flat Panel display modes and refresh rates that require up to a 65 MHz dot clock over this interface.
Table D-2 shows some of the display modes supported by the GMCH.
The GMCH supports scaling for all of the resolutions listed in *Table D-2*. Actual scaling results are dependant on the third party flat panel transmitter. If the flat panel transmitter does not support scaling, the resolutions are supported by the GMCH via centering.

Table D-2 List of Flat Panel Modes Supported

Resolution	Bits Per Pixel (frequency in Hz)		
	8-bit Indexed	16-bit	24-bit
320x200	60	60	60
320x240	60	60	60
352x480	60	60	60
352x480	60	60	60
352x576	60	60	60
400x300	60	60	60
512x384	60	60	60
640x350	60	60	60
640x400	60	60	60
640x480	60	60	60
720x480	60	60	60
720x576	60	60	60
800x600	60	60	60
1024x768	60	60	60

On-Board DVO to LCD TTL signals Converter (Optional)

The Raptor MicroATX has an on-board (optional) DVO to TTL LCD converter that enables the connection of LCD panels without the need for interfaces in the DVO connector. The converter is based on the SmartASIC 1015 chip.

The 1015 has several features that allow the image scaling.

Multiple TFT LCD Panel Support

- Programmable output timing parameters to match specifications of various TFT LCD panels.
- Single or dual pixel output (24/48 bit RGB).

Image Scaling

The SP1015 support several input modes, and the input image may have different sizes. It is essential to support automatic image scaling so that the input image is always displayed at full screen regardless of the input mode. This chip scales the images in both horizontal and vertical directions. It calculates the correct scaling ratio for both directions based upon the LCD panel resolution and the input mode and

timing information. The scaling ratio is re-adjusted whenever a different input mode is detected. The ratio is then fed to the buffer memory read control logic to fetch the image data with the right sequence and timing. Some of the image data may be read more than once to achieve the scaling effect. The SP1015 can only perform up-scaling, i.e., resolutions smaller or equal to the panel can be fit into the panel.

Image Interpolation

A basic image scaling algorithm replicates the input images to achieve the scaling effect, however, this replication scheme usually results in poor image quality. To achieve better and improved image quality, the SP1015 support image interpolation through a proprietary interpolation algorithm.

Dithering

These controllers support 16.7 million true colors for a 6-bit panel. Two dithering algorithms are implemented and users can choose between them. The first one is area-based dithering, and the second one is frame-based frame modulation, which is also called frame rate control.

Text Enhancement

In order to generate a good picture, the SP1015 incorporate a proprietary scheme to detect text and non-text picture. Then the appropriate process is applied to improve the text image based on the detection of the incoming source. By using this text enhancement function correctly, the text image will look more pleasant and nearly perfect after scaling up or down.

Sharpness Enhancement

No matter how many times the original image got enlarged or reduced by the internal interpolator, the SP1015 can always enhance the overall image sharpness (edge) to different degrees for various requirements through its embedded powerful DSP arrays. The sharpness can be adjusted bi-directionally, which means it can either be sharper or softer to a certain point.

Supported Input Modes

The SP1015 can handle up to 3 different input modes (custom solutions may differ from these four modes). An input mode is defined by the relationship of its horizontal resolution with its vertical resolution. Therefore, input modes with the same horizontal and vertical resolution but with different frame rates are still considered as a single input mode.

- 640x480 (VGA)
- 800x600 (SVGA)
- 1024x768 (XGA)

Special Notes about the On-board Video Controller

LVDS and DVI devices may be connected to the DVO port. The video BIOS in the Raptor MicroATX are ready to deal with some modules. EDID and EDID-less operation are available. The use of the DVO port and the on-board SP 1015 depends on many parameters set in the video BIOS and in on-board EEPROMs. Therefore, the use of these devices will depend on custom solutions provided by the manufacturer of the Raptor MicroATX.

The 82815 is a single video engine/pipeline device. Therefore, the resolution and frequencies available when using only CRT, DVI/LVDS, on-board SP 1015, and any possible combination of these options will depend on the crossing of possibilities offered by each single device and the 82815 itself.

Please, make sure that you have the proper support from the manufacturer prior to using the DVO and/or on-board LCD devices.

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