Personal System/2
Model 95 XP 486
Technical Reference

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Notes:

Preface

The Technical Reference library is intended for those who develop hardware and software products for IBM Personal Computers and IBM Personal System/2 products. Users should understand computer architecture and programming concepts.

This manual consists of the following sections:

Section 1, "System Overview," describes the system, features, and specifications.

Section 2, "Programmable Option Select," describes the registers used for configuration.

Section 3, "System Board," describes the system-specific hardware implementations of the Micro Channel architecture.

Section 4, "Processor Complex" describes the components and features of the processor complex.

This technical reference should be used with the following publications. These publications contain additional information on many of the subjects discussed in this technical reference.

IBM Personal System/2 Hardware Interface Technical Reference — Architectures

IBM Personal System/2 Hardware Interface Technical Reference — Common Interfaces

IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference

Information about diskette drives, fixed disk drives, adapters, and external options are in separate option technical references.

Warning: The term "Reserved" describes certain signals, bits, and registers that should not be changed. Use of reserved areas can cause compatibility problems, loss of data, or permanent damage to the hardware. When the contents of a register are changed, the state of the reserved bits must be preserved. When possible, read the register first and change only the bits that must be changed.

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Section 1. System Overview

Description

The IBM* Personal System/2* Model 95 is floor-standing computer system with a keyboard. The system can support up to four removable-media DASD devices (diskette, tape, optical) and three nonremovable-media DASD devices.

All Model 95 systems use the same system board. This system board has:

- Eight Micro Channel* connectors
- Eight connectors for memory
- Parallel port, serial port, and diskette drive controllers
- Processor complex connector
- Real-time clock.

The processor complex determines system performance and the model/submodel byte information. The major components on the processor complex are:

- System microprocessor
- DMA controller
- Memory controller.

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System Board Devices and Features

The following table lists the system board devices and features. The *Hardware Interface Technical Reference – Common Interfaces* describes devices common to PS/2 products by type number.

Device	Type	Features
Microprocessor	---	Connector for processor complex
System Timers	1	Channel 0 – System timer Channel 2 – Tone generation for speaker Channel 3 – Watchdog timer
RAM Subsystem	---	Eight connectors on system board Refer to the processor complex for more information
CMOS RAM Subsystem	---	64-byte CMOS RAM with real-time clock/calendar 8KB CMOS RAM extension (KB = 1,024 bytes) Battery backup
Audio Subsystem	1	Driven by: – System-timer channel 2 – The 'audio sum node' signal.
Interrupt Controller	1	16 levels of system interrupts Interrupts are level-sensitive
Keyboard/Auxiliary Device Controller	2	Keyboard connector Auxiliary device connector Password security
Diskette Drive Controller	2	Supports: – 3.5-in. diskette drive (1.44MB) – 5.25-in. diskette drive (360KB and 1.2MB)
Serial Controller	3	RS-232C interface Programmable as serial port 1 – 8 DMA, FIFO, and character modes Supports DMA operation
Parallel Controller	3	Programmable as parallel port 1 – 4 Supports bidirectional input and output Supports DMA operation
Micro Channel	---	Eight connectors for Type 3 adapters: – One 32-bit connector with auxiliary video extension – One 32-bit connector with base video extension – Six 32-bit connectors with matched memory extension One connector contains a fixed disk adapter One connector contains a video adapter

Figure 1-1. System Board Devices and Features

System Board I/O Address Map

Hex Addresses	Device
0020, 0021	Interrupt Controller (Master)
0040, 0042 – 0044, 0047	System Timers
0060	Keyboard, Auxiliary Device
0061	System Control Port B
0064	Keyboard, Auxiliary Device
0070, 0071	RT/CMOS and NMI Mask
0091	Card Selected Feedback Register
0092	System Control Port A
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
00A0 – 00A1	Interrupt Controller (Slave)
0100 – 0107	Programmable Option Select
0108 – 010F	Information Panel
0278 – 027D	Parallel Port 3
02F8 – 02FF	Serial Port 2
0378 – 037D	Parallel Port 2
03BC – 03BF	Parallel Port 1
03F0 – 03F7	Diskette Drive Controller
03F8 – 03FF	Serial Port 1
1278 – 127D	Parallel Port 1 (DMA mode)
1378 – 137D	Parallel Port 4
3220 – 3227	Serial Port 3
3228 – 322F	Serial Port 4
4220 – 4227	Serial Port 5
4228 – 422F	Serial Port 6
5220 – 5227	Serial Port 7
5228 – 522F	Serial Port 8
83F8 – 83FF	Serial Port 1 (DMA mode)
82F8 – 82FF	Serial Port 2 (DMA mode)
B220 – B227	Serial Port 3 (DMA mode)
B228 – B22F	Serial Port 4 (DMA mode)
C220 – C227	Serial Port 5 (DMA mode)
C228 – C22F	Serial Port 6 (DMA mode)
D220 – D227	Serial Port 7 (DMA mode)
D228 – D22F	Serial Port 8 (DMA mode)

Figure 1-2. System Board I/O Address Map

Micro Channel Compatibility

Following is a description of restrictions in the support of certain Micro Channel Procedures.

Streaming Data

The system board supports 10 MHz-streaming data procedures involving transfers between adapters.

Devices on the system board and the processor complex work with streaming-data adapters; however, they do not

use the streaming data procedure. Transfers default to the basic transfer procedure.

Data Parity

The system board supports data-parity procedures involving transfers between adapters.

Devices on the system board and the processor complex work with adapters that support data parity; however, they do not use the data parity option. Transfers default to the basic transfer procedure.

Address Parity

The system board supports address-parity procedures involving transfers between adapters.

Devices on the system board and the processor complex work with adapters that support address parity; however, they do not use the address parity option. Transfers default to the basic transfer procedure.

Select Feedback Return Signal

The system board and the processor complex support the 'selected feedback return' signal except for I/O devices at addresses below hex 0110. These devices are controlled by the system master only and should not be accessed by bus masters.

Synchronous Channel Check

Synchronous channel checks for errors other than Micro Channel data-parity errors or Micro Channel address-parity errors are not supported in this system.

Synchronous channel checks for data-parity or address-parity errors, typically issued by slaves, are the responsibility of the master that owned the channel and issued the access to the slave. However, in this system, these channel checks can also be detected by logic on the system board, resulting in an NMI.

DMA

In this system, the DMA controller supports DMA slaves with 8-bit or 16-bit data widths. Transfers are limited to the memory address space below 16MB.

Specifications

Size:	
Width	203 mm (8.0 in)
Depth	508 mm (20.0 in)
Height	501 mm (19.75 in)
Weight:	
Minimum Configuration	22 kg (50 lb)
Maximum Configuration	30 kg (67 lb)
Cables:	
Power Cable	1.8 m (6 ft)
Keyboard Cable	3.05 m (10 ft)
Air Temperature:	
System On	
0 - 3000 ft	10.0 to 35.0°C (50 to 95°F)
3000 - 7000 ft	10.0 to 32.2°C (50 to 90°F)
System Off	10.0 to 43.0°C (50 to 110°F)
Humidity:	8% to 80%
Maximum Altitude	2134 m (7000 ft)
Heat Output	515 W (1757 BTU per hour)
Acoustical Readings	
See Figure 1-4 on page 1-7	
Electrical:	
Input Voltage:	Range is switch selected. Sinewave input required
Low Range	90 (min) – 137 (max) Vac
High Range	180 (min) – 265 (max) Vac
Input Frequency:	50 ± 3Hz or 60 ± 3Hz
Maximum Current Draw:	
Low Range	9.2 A
High Range	4.6 A
Input in Kilovolt-Ampere (kVA):	
Minimum Configuration (as shipped)	0.18 kVa
Maximum Configuration	0.78 kVa
Electromagnetic Compatibility	FCC Class B

Figure 1-3. Physical Specifications

Description	L_{WAd} in bels		L_{pAm} in dB		$<L_{pA}>_m$ in dB	
	Operate	Idle	Operate	Idle	Operate	Idle
Model 95	5.3	5.3	33	33	36	36

Notes:

L_{WAd} is the declared sound power level for the random sample of machines.

L_{pAm} is the mean value of the A-weighted sound pressure levels at the operator position (if any) for the random sample of machines.

$<L_{pA}>_m$ is the mean value of the A-weighted sound pressure levels at the one-meter positions for the random sample of machines.

All measurements made in accordance with ANSI S12.10, and reported in conformance with ISO DIS 9296.

The measurements are preliminary data and subject to change.

Figure 1-4. Acoustical Readings

Power Supply

The power supply requires a sinewave input and converts the ac input voltage to three dc output voltages. The switch near the power cord is used to select the input-voltage range. The power supply provides power for the following:

- System board
- Processor complex
- Micro Channel adapters
- Internal diskette drives
- Internal fixed disk drives
- Auxiliary device
- Keyboard.

The power switch and one light-emitting diode (LED) are on the front of the system unit. The power supply is operating properly when the LED is lit.

Outputs

The power supply provides separate voltage sources for the system board and the drives. The system-board voltages are +5 Vdc, +12 Vdc, and −12 Vdc. The voltages for the internal drives are +5 Vdc and +12 Vdc. The following is a list of the power provided for system components.

System Component	Maixmum Current	
	+12	+5
Internal Fixed Disk Drives *	2.5 A	1.5 A
Total of Fixed Disk Drives	7.5 A	4.6 A
Auxiliary Device		300 mA
Keyboard		275 mA
* Per power supply connector		

Figure 1-5. System-Provided Power

The following are the load currents allowed for the connectors for the Type 3 adapters. The formulas used to determine the power requirements and the definition of adapter types can be found in the section of the *Hardware Interface Technical Reference — Architectures* that describes the Micro Channel architecture.

Supply Voltage	Maximum Current
+ 5.0 Vdc	2.0 A
+12.0 Vdc	0.175 A
−12.0 Vdc	0.040 A

Figure 1-6. Load Current for Micro Channel Adapter Connector

Output Protection

A short circuit placed on any dc output (between outputs or between an output and dc return) latches all dc outputs into a shutdown state with no damage to the power supply.

If an overvoltage fault occurs (internal to the power supply), the power supply latches all dc outputs into a shutdown state before any output exceeds 130% of its nominal value.

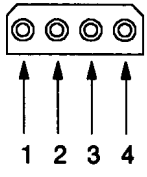
If either of these shutdown states is actuated, the power supply returns to normal operation only after the fault has been removed and the power switch has been turned off for at least one second.

Voltage Sequencing

At power-on time, the output voltages track within 50 milliseconds of each other when measured at the 50% points.

Power Supply Connectors

The power supply provides three 4-pin connectors for internal devices. The connectors can be extended to provide power to more than one internal drive as long as the total power for all connectors does not exceed the connector specifications shown in Figure 1-5 on page 1-8.



Pin	Signal	Pin	Signal
1	+12 Vdc	3	DC Return
2	DC Return	4	+5 Vdc

Figure 1-7. Voltage Assignments for the Internal Drive Power-Supply Connectors

Section 2. Programmable Option Select

Description

Programmable Option Select (POS) eliminates the need for switches by replacing their function with programmable registers. This section describes the POS information used on the Model 95 system board. For additional POS information, refer to the *Hardware Interface Technical Reference.*

Warning:

- IBM recommends that programmable options be set only through the System Configuration utilities. Directly setting the POS registers or CMOS RAM POS parameters can result in multiple assignment of the same system resource, improper operation of the feature, loss of data, or possible damage to the hardware.
- Application programs should not use the adapter identification (ID) unless absolutely necessary. Compatibility problems can result.
- If an adapter and the system board are in setup mode at the same time, bus contention will occur, no useful programming can take place, and damage to the hardware can occur.
- After setup operations are complete, the Adapter Enable/Setup register (hex 0096) should be set to hex 00, and the System Board Enable/Setup register (hex 0094) should be set to hex FF.
- Bit 7 (channel reset) in the Adapter Enable/Setup register must be 0 to program the adapters.
- Only 8-bit instructions are supported for setup operations. Using 32- or 16-bit I/O instructions on 8-bit POS registers will cause erroneous data to be written or read.

Setup functions respond to I/O addresses hex 0100 through 0107 only when their unique setup signal is active. The following precautions must be taken before setting individual bits in the POS registers.

Adapter Setup:

- Bit 3 in the Adapter Enable/Setup register must be set to 1 to allow adapter setup.
- Bits 7 – 0 in the System Board Enable/Setup register must be set to 1 to avoid driving a 'setup' signal to a system board function.

System Board Setup:

- Bits 7 and 6 in the System Board Enable/Setup register must be set to 0 individually while other bits are set to 1 to setup corresponding system board functions.
- Bit 3 in the Adapter Enable/Setup register must be set to 0 to avoid driving a 'setup' signal to an adapter.

POS Address Map

The following table shows the organization of the I/O address space used by POS. Bit 0 of POS Register 2 and bits 6 and 7 of POS Register 5 are fixed. All other bits in POS Registers 2 through 5 are free-form.

Address (Hex)	Function
0094	System Board Enable/Setup Register
0096	Adapter Enable/Setup Register
0100	POS Register 0—Adapter Identification Byte (Low Byte)
0101	POS Register 1—Adapter Identification Byte (High Byte)
0102	POS Register 2—Option Select Data Byte 1 Bit 0 is Card Enable.
0103	POS Register 3—Option Select Data Byte 2
0104	POS Register 4—Option Select Data Byte 3
0105	POS Register 5—Option Select Data Byte 4
0106	Reserved
0107	Reserved

Figure 2-1. POS I/O Address Map

Card Selected Feedback

When an adapter is addressed, it responds by setting the '-card selected feedback' signal (-CD SFDBK) to active. -CD SFDBK is derived from the address decode and driven by a totem pole driver. It is latched by the system board and can be read through the Card Selected Feedback register at address hex 0091.

The Card Selected Feedback register is a read-only register at address hex 0091. It allows programs to monitor -CD SFDBK and thereby determine if the system board I/O or an adapter is addressed and functioning.

Bit	Function
7 – 1	Reserved
0	-Card Selected Feedback

Figure 2-2. Card Selected Feedback Register (Hex 0091)

Bits 7 – 1 These bits are reserved.

Bit 0 This bit is set to 1 whenever -CD SFDBK was active on a previous cycle or whenever the system board I/O functions (diskette drive, serial, or parallel interfaces) are accessed by an I/O or DMA cycle. Reading this register resets the bit to 0.

System Board Setup

The integrated I/O functions on the system board use POS information during setup. The diskette drive controller, serial port, and parallel port are treated as a single device. The System Board Enable/Setup register is used to place the system board into the setup mode.

System Board Enable/Setup Register (Hex 0094)

This is a read/write register; all bits in this register default to 1 (enabled). Setup functions should only be accessed one at a time.

Bit	Function
7	Enable/-Setup System Board Functions
6	Enable/-Setup Diskette Drive Functions
5–0	Reserved

Figure 2-3. System Board Enable/Setup Register (Hex 0094)

Bit 7 When this bit is set to 0, various system board I/O functions are placed in the setup mode. The diskette drive controller, serial port, and parallel port are controlled through System Board POS Register 2 (hex 0102).

When this bit is set to 1, the system board function is enabled.

Bit 6 Additional setup for diskette drive. When this bit is set to 0, these setup functions are available through the Diskette Drive POS Register 4.

Bits 5–0 These bits are reserved.

System Board POS Register 2 (Hex 0102)

When the system board is in the setup mode, the diskette drive controller, serial port, and parallel port are controlled by this read/write register. Reading this register returns the current state of these system board functions.

Bit	Function
7	Disable Parallel Port Extended Mode
6, 5	Parallel Port Select
4	Enable Parallel Port
3	Serial Port IRQ Select
2	Enable Serial Port
1	Enable Diskette Drive Interface
0	Enable System Board

Figure 2-4. System Board POS Register 2 (Hex 0102)

Bit 7 When set to 0, this bit allows the parallel port to be configured as an 8-bit, parallel, bidirectional interface. When set to 1, this bit disables the bidirectional mode. This bit is set to 0 after power-on.

Bits 6, 5 These bits select the configuration of the system board parallel port.

Bits 6 5	Assignment	Hex Address	Interrupt Level
0 0	Parallel 1	03BC – 03BF*	7
0 1	Parallel 2	0378 – 037D	7
1 0	Parallel 3	0278 – 027D	7
1 1	Parallel 4	1378 – 137D	7

* The addresses are hex 1278 – 127D for DMA operations

Figure 2-5. Parallel Port Select Bits

Bit 4 When this bit and bit 0 are set to 1, the system-board parallel port is enabled.

Bit 3 When this bit is set to 1, the serial port uses interrupt request level 4. When set to 0, the serial port uses interrupt request level 3.

Bit 2 When this bit and bit 0 are set to 1, the system board serial port is enabled.

Bit 1 When this bit and bit 0 are set to 1, the diskette drive interface is enabled.

Bit 0 When set to 1, this bit allows bits 4, 2, and 1 to enable and disable their respective devices. When set to 0, this bit disables the diskette drive interface, system board serial port, and system board parallel port, regardless of the state of bits 4, 2, and 1.

System Board POS Register 3 (Hex 0103)

The system board has connectors that provide installation of eight memory cards (for more information about these memory connectors, see "System Board Memory Connectors" on page 3-3). Information about each memory card is contained in four read-only data registers; each data register is selected by writing its index to the write-only index register.

POS Register 3 provides access to the read-only data registers and a write-only index register. To determine the memory information for a particular connector, write the appropriate index to POS Register 3, then read POS Register 3. The following shows the relationship of the index value, the memory connector, and the data register information available.

Index Value (Hex)	Description
01	Presence Detect Information for A1 and B1
05	Presence Detect Information for A2 and B2
09	Presence Detect Information for A3 and B3
0D	Presence Detect Information for A4 and B4
All values not show are reserved.	

Figure 2-6. System Board POS Register 3 (Hex 0103) — Write

The following information is returned by reading POS Register 3 when the appropriate value is written to POS Register 3. For coding of the presence detect signals, see Figure 4-12 on page 4-11.

Bit	Description
7	Presence Detect 3, Connector B
6	Presence Detect 2, Connector B
5	Presence Detect 1, Connector B
4	Presence Detect 0, Connector B
3	Presence Detect 3, Connector A
2	Presence Detect 2, Connector A
1	Presence Detect 1, Connector A
0	Presence Detect 0, Connector A

Figure 2-7. System Board POS Register 3 (Hex 0103) — Read

System Board POS Registers 4 (Hex 0104)

This register is accessed when bit 7 of the System Board Enable/Setup register is set to 0. The register is used to specify the arbitration levels used by the serial port during transmit and receive operations in the DMA mode.

Bit	Description
7–4	Receive Arbitration Level
3–0	Transmit Arbitration Level

Figure 2-8. System Board POS Register 4 (Hex 0104)

Bits 7–4 These bits select the arbitration level used for the transfer of data being received through the serial port.

Bits 3–0 These bits select the arbitration level used for the transfer of data being transmitted through the serial port.

System Board POS Register 5 (Hex 0105)

This register is used to specify the arbitration level used by the parallel port and the I/O addresses used by the serial port.

Bit	Description
7	Reserved
6–4	Serial Address Select
3–0	Parallel Port Arbitration Level

Figure 2-9. System Board POS Register 5 (Hex 0105)

Bit 7 This bit is reserved.

Note: This bit may read as 0 but does not indicate any occurrence of channel check.

Bits 6–4 These bits are used to select the I/O addresses used by the serial port on the system board. The I/O addresses can be the compatible addresses or the extended address (see the technical reference for the serial port controller for more information on addressing).

Bits 6 5 4	Assignment	Hex Address	
		Compatible	Extended
0 0 0	Serial 1	03F8–03FF	83F8–83FF
0 0 1	Serial 2	02F8–02FF	82F8–82FF
0 1 0	Serial 3	3220–3227	B220–B227
0 1 1	Serial 4	3228–322F	B228–B22F
1 0 0	Serial 5	4220–4227	C220–C227
1 0 1	Serial 6	4228–422F	C228–C22F
1 1 0	Serial 7	5220–5227	D220–D227
1 1 1	Serial 8	5228–522F	D228–D22F

Figure 2-10. Serial Port Address Select Bits

Bits 3–0 These bits select the arbitration level used by the parallel port controller.

Diskette Drive POS Registers 4 (Hex 0104)

This register is accessed when the bit 6 of the System Board Enable/Setup register is set to 0. The register is used to specify the arbitration level used by the diskette drive controller.

Bit	Description
7–4	Reserved
3–0	Diskette Drive Arbitration Level

Figure 2-11. Diskette Drive POS Register 4 (Hex 0104)

Bits 7–4 These bits are reserved.

Bits 3–0 These bits select the arbitration level used by the diskette drive controller.

Adapter Enable/Setup Register (Hex 0096)

This read/write register selects the connector to be configured.

Bit	Symbol
7	Channel Reset
6–4	Reserved = 0
3	Card Setup Enable
2–0	Channel Select 2–0

Figure 2-12. Adapter Enable/Setup Register (Hex 0096)

Bit 7 When set to 1, this bit activates the 'channel reset' signal to all connectors.

Bits 6–4 These bits are reserved and must be set to 0.

Bit 3 When set to 1, this bit enables the '-card setup' signal selected by bits 2 through 0.

Bits 2–0 These bits are the address bits for the '-card setup' signal. Connectors 1 through 8 are addressed as 0 through 7. When bit 3 is set to 1, these bits select the connector for setup cycles.

Each channel connector has a unique '-card setup' signal (-CD SETUP) associated with it. This signal is used to select the adapters for setup cycles, which allows access to the POS registers. The individual connectors are selected through the Adapter Enable/Setup register. Setup information is then read from or written to the selected adapter through I/O addresses hex 0100 through 0107.

Note: -CD SETUP only goes active when an operation is performed in the I/O address range hex 0100 through 0107.

Selectable Boot Sequence

Selectable boot allows the user to specify the order in which the drives are searched when looking for the boot record of an operating system. Only the diskette and fixed disk drives can be part of the search sequence. Changing the sequence for selectable boot affects the drive letter ordering the next time the system is booted.

The user selects the boot sequence with the Select Startup option in the Set Feature utility. The user is presented with a list of possible drives from which to select. After the sequence is selected, it is stored in nonvolatile RAM (NVRAM). When the system boots, it searches for a drive that contains a bootable record using the specified sequence.

After the operating system boots, the drive lettering is determined by the sequence and which drive contained the bootable source. If the operating system boots from a diskette drive, that drive is drive A. If the operating system boots from a fixed disk drive, that fixed disk drive is drive C. Other drives specified in the sequence can change also.

Section 3. System Board

Description

This section describes miscellaneous system ports and connectors for the Model 95. For additional information about these and other topics, refer to other descriptions in the *Hardware Interface Technical Reference*.

Diskette Drive Connector

The system provides three 2-by-17-pin connectors for attaching internal diskette drives. Each connector passes control and data signals between the diskette drive controller on the system board and the drives and provides the power to each drive.

The following figure shows the signal assignments and pin numbers for the diskette drive connectors.

Pin	Signal	Pin	Signal
1	Ground	2	Data Rate Select 1
3	+5VDC	4	Drive Type ID 1
5	Ground	6	+12DC
7	Ground	8	-Index
9	Drive Type ID 0	10	Reserved
11	Ground	12	-Drive Select
13	Ground	14	Reserved
15	Ground	16	-Motor Enable
17	Media Type ID 1	18	-Direction In
19	Ground	20	-Step
21	Ground	22	-Write Data
23	Ground	24	-Write Enable
25	Ground	26	-Track 0
27	Media Type ID 0	28	-Write Protect
29	Ground	30	-Read Data
31	Ground	32	-Head 1 Select
33	Data Rate Select 0	34	-Diskette Change

Figure 3-1. Diskette Drive Connector

System Board Memory Connectors

The Model 95 system board has eight 72-pin memory connectors that support a variety of memory cards. The connectors are numbered as viewed from the top of the system.

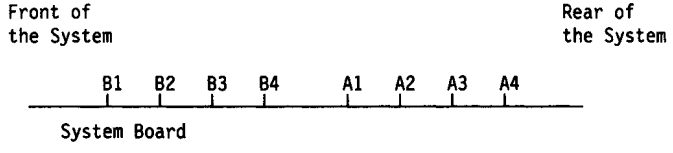


Figure 3-2. Memory Connector Numbering

The following figure shows the pin assignments for the 1- by 72-pin memory connectors. Refer to "Memory Presence Detect" on page 4-11 for decoding of the presence detect signals.

Pin	Signal	Pin	Signal
1	Ground	37	Parity Data 1
2	Data 0	38	Parity Data 3
3	Data 16	39	Ground
4	Data 1	40	Column Address Strobe 0
5	Data 17	41	Column Address Strobe 2
6	Data 2	42	Column Address Strobe 3
7	Data 18	43	Column Address Strobe 1
8	Data 3	44	Row Address Strobe 0
9	Data 19	45	Row Address Strobe 1
10	+5 Vdc	46	Block Select 1
11	-Column Address Strobe P	47	Write Enable
12	Address 0	48	Reserved
13	Address 1	49	Data 8
14	Address 2	50	Data 24
15	Address 3	51	Data 9
16	Address 4	52	Data 25
17	Address 5	53	Data 10
18	Address 6	54	Data 26
19	Reserved	55	Data 11
20	Data 4	56	Data 27
21	Data 20	57	Data 12
22	Data 5	58	Data 28
23	Data 21	59	+5 Vdc
24	Data 6	60	Data 29
25	Data 22	61	Data 13
26	Data 7	62	Data 30
27	Data 23	63	Data 14
28	Address 7	64	Data 31
29	Block Select 0	65	Data 15
30	+5 Vdc	66	Block Select 2
31	Address 8	67	Presence Detect 0
32	Address 9	68	Presence Detect 1
33	Row Address Strobe 3	69	Presence Detect 2
34	Row Address Strobe 2	70	Presence Detect 3
35	Parity Data 2	71	Block Select 3
36	Parity Data 0	72	Ground

Figure 3-3. System Board Memory Connector

Real-Time Clock/Complementary Metal-Oxide Semiconductor RAM

The real-time clock/complementary metal-oxide semiconductor RAM (RT/CMOS) chip contains the real-time clock and 64 bytes of CMOS RAM. The internal clock circuitry uses 14 bytes of this memory, and the rest is allocated for configuration and system-status information.

In addition to the 64 bytes of CMOS RAM, an 8KB CMOS RAM extension is provided for configuration and other system information.

A battery maintains voltage to the RT/CMOS RAM and 8KB CMOS RAM extension when the power supply is not in operation.

The system cover can be locked to prevent battery removal and, consequently, prevents the loss of password and configuration information.

The following table shows the RT/CMOS RAM bytes and their addresses.

Address (Hex)	RT/CMOS RAM Bytes
000–00D	Real-Time Clock Bytes
00E	Diagnostic Status Byte
00F	Shutdown Status Byte
010	Diskette Drive Type Byte
011	First Fixed Disk Drive Type Byte
012	Second Fixed Disk Drive Type Byte
013	Reserved
014	Equipment Byte
015, 016	Low and High Base Memory Bytes
017, 018	Low and High Expansion Memory Bytes
019–031	Reserved
032, 033	Configuration CRC Bytes
034	Reserved
035, 036	Low and High Usable Memory Above 1MB
037	Date Century Byte
038–3F	Reserved

Figure 3-4. RT/CMOS RAM Address Map

RT/CMOS Address Register and NMI Mask (Hex 0070)

This read/write register is used in conjunction with the port at hex 0071 to read and write the RT/CMOS RAM bytes.

Bit	Function
7	NMI Mask
6	Reserved
5–0	RT/CMOS RAM Address

Figure 3-5. RT/CMOS Address Register and NMI Mask (Hex 0070)

Warning: The operation following a write to hex 0070 must access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Bit 7 When this bit is set to 1, the NMI is masked off (the NMI is disabled). This bit is set to 1 by a power-on reset. This is a write-only bit.

Bit 6 This bit is reserved.

Bits 5–0 These bits are used to select RT/CMOS RAM addresses.

RT/CMOS Data Register (Hex 0071)

This port is used in conjunction with the address register at hex 0070 to read and write the RT/CMOS RAM bytes.

Bit	Function
7–0	RT/CMOS Data

Figure 3-6. RT/CMOS Data Register (Hex 0071)

RT/CMOS RAM I/O Operations

During I/O operations to the RT/CMOS RAM addresses, interrupts must be masked to prevent other interrupt routines from changing the CMOS Address register before data is read or written.

Warning: The operation following a write to hex 0070 must access hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

Writing RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Write the data to address hex 0071.
3. Write the address, hex 0D, to the RT/CMOS and NMI Mask register; this leaves hex 0070 pointing to Status Register D.
4. Read address hex 0071 to restore the RT/CMOS (see the warning above).

Reading RT/CMOS RAM requires the following steps:

1. Write the RT/CMOS RAM address to the RT/CMOS and NMI Mask register (hex 0070).
2. Read the data from address hex 0071.
3. Write the address, hex 0D, to the RT/CMOS and NMI Mask register; this leaves hex 0070 pointing to Status Register D.
4. Read address hex 0071 to restore the RT/CMOS.

Real-Time Clock Bytes (Hex 000 – 00D)

Bit definitions and addresses for the real-time clock bytes are shown in the following table.

Address (Hex)	Function	Byte Number
000	Seconds	0
001	Second Alarm	1
002	Minutes	2
003	Minute Alarm	3
004	Hours	4
005	Hour Alarm	5
006	Day of Week	6
007	Date of Month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 3-7. Real-Time Clock Bytes

Note: The Setup program initializes status registers A, B, C, and D when the time and date are set. Interrupt hex 1A is the BIOS interface to read and set the time and date. It initializes the register the same way as the Setup program.

Status Register A (Hex 00A)

Bit	Function
7	Update in Progress
6–4	22-Stage Divider
3–0	Rate Selection Bits

Figure 3-8. Status Register A

Bit 7 When set to 1, this bit indicates the time-update cycle is in progress. When set to 0, it indicates the current date and time can be read.

Bits 6–4 These three divider-selection bits identify which time-base frequency is being used. The system initializes these bits to binary 010, which selects a 32.768 kHz time base. This is the only value supported by the system for proper time-keeping.

Bits 3–0 These bits allow the selection of a divider output frequency. The system initializes the rate selection bits to a binary 0110, which selects a 1.024 kHz square-wave output frequency and a 976.562-microsecond periodic interrupt rate.

Status Register B (Hex 00B)

Bit	Function
7	Set
6	Periodic Interrupt Enable
5	Alarm Interrupt Enable
4	Update-Ended Interrupt Enable
3	Square Wave Enable
2	Date Mode
1	24-Hour Mode
0	Daylight Savings Enable

Figure 3-9. Status Register B

Bit 7 When set to 0, this bit updates the cycle, normally by advancing the counts at a rate of one per second. When set to 1, this bit immediately ends any update cycle in progress, and the program can initialize the 14 time bytes without any further updates occurring until this bit is set to 0.

Bit 6 This bit is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in Status Register A. When set to 1, this bit enables the interrupt. The system initializes this bit to 0.

Bit 5 When set to 1, this bit enables the alarm interrupt. The system initializes this bit to 0.

Bit 4 When set to 1, this bit enables the update-ended interrupt. The system initializes this bit to 0.

Bit 3 When set to 1, this bit enables the square-wave frequency as set by the rate-selection bits in Status Register A. The system initializes this bit to 0.

Bit 2 This bit indicates if the time-and-date calendar updates use binary or binary-coded-decimal (BCD) formats. When set to 1, this bit indicates a binary format. The system initializes this bit to 0.

Bit 1 This bit establishes if the hours byte is in the 24-hour or 12-hour mode. When set to 1, this bit indicates the 24-hour mode. The system initializes this bit to 1.

Bit 0 When set to 1, this bit enables the daylight savings time mode. When set to 0, it disables the mode, and the clock reverts to standard time. The system initializes this bit to 0.

Status Register C (Hex 00C)

Bit	Function
7	Interrupt Request Flag
6	Periodic Interrupt Flag
5	Alarm Interrupt Flag
4	Update-Ended Interrupt Flag
3–0	Reserved

Figure 3-10. Status Register C

Note: Interrupts are enabled by bits 6, 5, and 4 in Status Register B.

Bit 7 This bit is used in conjunction with bits 6, 5, and 4. When set to 1, this bit indicates that an interrupt has occurred; bits 6, 5, and 4 indicate the type of interrupt.

Bit 6 When set to 1, this bit indicates that a periodic interrupt occurred.

Bit 5 When set to 1, this bit indicates that an alarm interrupt occurred.

Bit 4 When set to 1, this bit indicates that an update-ended interrupt occurred.

Bits 3–0 These bits are reserved.

Status Register D (Hex 00D)

Bit	Function
7	Valid RAM
6–0	Reserved

Figure 3-11. Status Register D

Bit 7 This read-only bit monitors the power-sense pin. A low state of this pin indicates a loss of power to the real-time clock (dead battery). When set to 1, this bit indicates that the real-time clock has power. When set to 0, it indicates that the real-time clock has lost power.

Bits 6–0 These bits are reserved.

CMOS RAM Configuration

The following figure shows the bit definitions for the CMOS RAM configuration bytes.

Diagnostic Status Byte (Hex 00E)

Bit	Function
7	Real-Time Clock Chip Power
6	Configuration Record and Checksum Status
5	Incorrect Configuration
4	Memory Size Miscompare
3	Fixed Disk Controller/Drive C Initialization Status
2	Time Status Indicator
1	Adapter Configuration Miscompare
0	Adapter ID Time-Out

Figure 3-12. Diagnostic Status Byte

Bit 7 When set to 1, this bit indicates the real-time clock chip lost power.

Bit 6 When this bit is set to 1, the checksum is incorrect.

Bit 5 This is a check, at power-on time, of the Equipment byte. When set to 1, the configuration information is incorrect. Power-on checks require that at least one diskette drive be installed (bit 0 of the Equipment byte, hex 014, is set to 1).

Bit 4 When set to 1, this bit indicates the power-on check determined that the memory size is not the same as in the configuration record.

Bit 3 When set to 1, this bit indicates that the controller or drive C failed initialization, which prevents the system from attempting a power-on reset.

Bit 2 When set to 0, this bit indicates the time is valid. When set to 1, this bit indicates the time is invalid.

Bit 1 This bit indicates if the installed adapters match the configuration information. When this bit is set to 1, the adapters do not match the configuration information.

Bit 0 When set to 1, this bit indicates a time-out occurred while an adapter ID was being read.

Shutdown Status Byte (Hex 00F): This byte is defined by the power-on diagnostic programs.

Diskette Drive Type Byte (Hex 010): This byte indicates the type of diskette drive installed.

Bit	Function
7–4	First Diskette Drive Type
3–0	Second Diskette Drive Type

Figure 3-13. Diskette Drive Type Byte

Bits 7–4 These bits indicate the first diskette drive type, as shown in the following table.

Bits 7 6 5 4	Function
0 0 0 0	No Drive Present
0 0 0 1	Double-sided Diskette Drive (48 tracks per inch, 360KB)
0 0 1 0	Double-sided Diskette Drive (80 tracks per inch, 1.2MB)
0 0 1 1	High-capacity Diskette Drive (720KB)
0 1 0 0	High-density Diskette Drive (1.44MB)
All combinations that are not shown are reserved.	

Figure 3-14. Diskette Drive Type Byte (Bits 7–4)

Bits 3–0 These bits indicate the second diskette drive type, as shown in the following table.

Bits 3 2 1 0	Function
0 0 0 0	No Drive Present
0 0 0 1	Double-sided Diskette Drive (48 tracks per inch, 360KB)
0 0 1 0	Double-sided Diskette Drive (80 tracks per inch, 1.2MB)
0 0 1 1	High-capacity Diskette Drive (720KB)
0 1 0 0	High-density Diskette Drive (1.44MB)
All combinations that are not shown are reserved.	

Figure 3-15. Diskette Drive Type Byte (Bits 3–0)

First Fixed Disk Drive Type Byte (Hex 011): This byte defines the type of the first fixed disk drive (drive C). Hex 00 indicates that a fixed disk drive is *not* installed.

Second Fixed Disk Drive Type Byte (Hex 012): This byte defines the type of the second fixed disk drive (drive D). Hex 00 indicates that a fixed disk drive is *not* installed.

Note: For more information about fixed disk drive types, refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference.*

Reserved Byte (Hex 013): This byte is reserved.

Equipment Byte (Hex 014): The equipment byte, for the power-on diagnostic tests, defines the basic equipment in the system.

Bit	Function
7, 6	Number of Diskette Drives
5, 4	Display Operating Mode
3, 2	Reserved
1	Math Coprocessor Presence
0	Diskette Drive Presence

Figure 3-16. Equipment Byte

Bits 7, 6 These bits indicate the number of diskette drives installed, as shown in the following table.

Bits 7 6	Number of Diskette Drives
0 0	One Drive
0 1	Two Drives
1 0	Three Drives
1 1	Reserved

Figure 3-17. Equipment Byte (Bits 7, 6)

Bits 5, 4 These bits indicate the operating mode of the display attached to the video port, as shown in the following table.

Bits 5 4	Display Operating Mode
0 0	Reserved
0 1	40-Column Mode
1 0	80-Column Mode
1 1	Monochrome Mode

Figure 3-18. Equipment Byte (Bits 5, 4)

Bits 3, 2 These bits are reserved.

Bit 1 When set to 1, this bit indicates that a math coprocessor is installed.

Bit 0 When set to 1, this bit indicates that a diskette drive is installed.

Low and High Base Memory Bytes (Hex 015 and 016): These bytes define the amount of memory below the 640KB address space.

The value from these bytes represents the number of 1KB blocks of base memory. For example, hex 0280 is equal to 640KB. The low byte is hex 15; the high byte is hex 16.

Low and High Expansion Memory Bytes (Hex 017 and 018): These bytes define the amount of memory above the 1MB address space.

The value from these bytes represents the number of 1KB blocks of expansion memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 17; the high byte is hex 18.

Reserved Bytes (Hex 019 through 031): These bytes are reserved.

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check (CRC) data for bytes hex 010 through hex 031 of the 64-byte CMOS RAM. The low byte is hex 33; the high byte is hex 32.

Reserved Byte (Hex 034): This byte is reserved.

Low and High Useable Memory Bytes (Hex 035 and 036): These bytes define the total amount of continguous useable memory from 1MB to 16MB.

The hexadecimal values in these bytes represent the number of 1KB blocks of useable memory. For example, hex 0800 is equal to 2048KB. The low byte is hex 35; the high byte is hex 36.

Date Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century. Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for information about reading and setting this byte.

Reserved Bytes (Hex 038 through 03F): These bytes are reserved.

Miscellaneous System Functions

Nonmaskable Interrupt

The nonmaskable interrupt (NMI) signals the system microprocessor that a parity error, a channel check, a system channel time-out, or a system Watchdog time-out has occurred. The NMI stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices. The NMI masks all other interrupts and the IRET instruction restores the interrupt flag to the state it was in prior to the interrupt. A system reset causes a reset of the NMI.

The NMI requests that are caused by channel check and system-board memory-parity errors are subject to mask control with the NMI mask bit in the RT/CMOS Address register. The Watchdog Timer and system channel time-out are not masked by this bit. (See "RT/CMOS Address Register and NMI Mask (Hex 0070)" on page 3-6). The power-on default of the NMI mask is 1 (NMI disabled). Prior to enabling the NMI after a power-on reset, the parity check and channel check state are initialized by the POST.

Warning: The operation following a write to hex 0070 should access port hex 0071; otherwise intermittent malfunctions and unreliable operation of the RT/CMOS RAM can occur.

System Control Port B (Hex 0061)

Bit definitions for the read and write functions of this port are shown in the following tables.

Bit	Function
7	Reset Timer 0 Output Latch (IRQ0)
6–4	Reserved
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-19. System Control Port B (Hex 0061) – Write

Bit	Function
7	Memory Parity Check
6	Channel Check
5	Timer 2 Output
4	Toggles with Each Refresh Request
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 3-20. System Control Port B (Hex 0061) – Read

Bit 7 Setting this bit to 1 resets IRQ0. Reading this bit as a 1 indicates a memory parity check has occurred.

Bit 6 Reading this bit as a 1 indicates a channel check has occurred.

Bit 5 This bit indicates the condition of the timer/counter 2 'output' signal.

Bit 4 This bit toggles for each refresh request.

Bit 3 Setting this bit to 0 enables channel check. Setting this bit to 1 disables channel check and clears the channel check latch.

Bit 2 Setting this bit to 0 enables system board memory parity check. This bit is set to 1 during a power-on reset. To clear a parity error, set this bit to 1 and then to 0.

Bit 1 Setting this bit to 1 enables speaker data.

Bit 0 Setting this bit to 1 enables the timer 2 gate.

System Control Port A (Hex 0092)

Bit	Function
7, 6	Fixed-Disk Activity Light
5	Reserved
4	Watchdog Timer Status
3	Security Lock Latch
2	Reserved = 0
1	Alternate Gate A20
0	Alternate Hot Reset

Figure 3-21. System Control Port A (Hex 0092)

Bits 7, 6 These bits control the fixed-disk activity light. Setting either bit to 1 turns the fixed-disk activity light on. Setting both bits to 0 turns the light off. The power-on reset condition of each bit is 0.

Bit 5 This bit is reserved.

Bit 4 This read-only bit indicates the watchdog-timer status. When this bit is set to 1, a watchdog time-out has occurred. For more information about the Watchdog Timer, refer to System Timers in *Hardware Interface Technical Reference – Common Interfaces.*

Bit 3 This bit provides the security lock for the secured area of RT/CMOS. Setting this bit to 1 electrically locks the 8-byte, power-on password. Once this bit is set by POST, it can only be cleared by turning the system off.

Bit 2 This bit is reserved.

Bit 1 This bit is ORed with bit 1 in the keyboard output port to enable the 'address 20' signal (A20). When both bits are set to 0, A20 is disabled and set to 0. This bit is set to 0 during POST. (See the "Keyboard Controller" section in the *Hardware Interface Technical Reference.*)

Bit 0 This bit provides an alternate method of resetting the system microprocessor. This alternate method supports operating systems requiring faster operation than was provided on the IBM Personal Computer AT*. Resetting the system microprocessor is used to switch the microprocessor from the protected mode to the real address mode. The alternate reset takes 13.4 microseconds.

This bit is set to 0 either by a system reset or a Write operation. When a Write operation changes this bit from 0 to 1, the alternate reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. While the reset is occurring, the latch remains set so that POST can read this bit. If the bit is 0, POST assumes the system was just powered on. If the bit is 1, POST assumes a switch from the protected mode to the real mode has taken place.

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* Personal Computer AT is a trademark of the International Business Machines Corporation.

Power-On Password

RT/CMOS RAM has eight bytes reserved for the power-on password and its check character. The eight bytes are initialized to hex 00. The microprocessor can only access these bytes during power-on self-test (POST). After POST is completed, if a power-on password is installed, the password bytes are locked and cannot be accessed by a program. A power-on password can be from 1 to 7 characters.

During power-on password installation, the password (1 to 7 keyboard scan codes), is stored in the security space.

Power-on password installation is a function of a program contained on the Reference Diskette. Once the power-on password utility has been installed, the password can be changed only during the POST. When the new power-on password is installed, changed, or removed, the password is not visible on the display.

The system unit cover can be physically locked to prevent unauthorized access to the battery. This helps prevent unauthorized battery removal and loss of power-on password and configuration information.

For information about the keyboard password, see the "Keyboard and Auxiliary Device Controller" section in the *Hardware Interface Technical Reference*.

Hardware Compatibility

The Model 95 maintains many of the interfaces used by the IBM Personal Computer AT. In most cases command and status organization of these interfaces is maintained.

The functional interfaces for the Model 95 are compatible with the following interfaces:

- The Intel** 8259 interrupt controllers (without edge triggering).
- The Intel 8253 timers driven from 1.193 MHz (timer 0 and 2 only).
- The Intel 8237 DMA controller address/transfer counters, page registers and status fields only. The Command and Request registers are not supported. The rotate and mask functions are not supported. The Mode register is partially supported.
- The NS16450 serial port.
- The Intel 8088, 8086, 80286, and 80386 microprocessors.
- The Intel 8272 diskette drive controller.
- The Motorola** MC146818 Time of Day Clock command and status (CMOS reorganized).
- The keyboard interface at address hex 0060.
- Display modes supported by the IBM Monochrome Display and Printer Adapter, the IBM Color/Graphics Monitor Adapter, and the IBM Enhanced Graphics Adapter.
- The parallel printer ports (Parallel 1, Parallel 2, and Parallel 3) in compatibility mode.
- Generally compatible with the Intel 8087, 80287, and 80387 math coprocessors.

Error Codes

POST returns a message in the form of a multiple-character code to indicate the type of test that failed. Two formats are used for these error messages:

- An eight-character error code for all errors *not* related to SCSI devices
- An 11 character code for all errors related to SCSI devices
  - The first three characters identify the device type
  - The next eight characters identify specifics of the error.

An information panel is used to display the first eight characters of an error message in case the system is operating without a video display. Only the code for the first error found during POST is displayed on the information panel; subsequent errors are indicated only on the video display (the information panel will continue to display the first error).

The error code consists of two 4-character elements, the major error code and the minor error code. The following figure gives the failure indicated with the associated error code.

Note: For information on unlisted error codes, contact Developer Assistance at 1-800-IBM-7763 (this number is for developers who are registered with IBM).

Major Code	Minor Code	Description
0001		System Bus Error - system board or processor complex
	0100	Unexpected interrupt
	0200	Timer failure
	0300	Timer interrupt failure
	0400	Protected mode failure
	0500	Last keyboard command not accepted
	0600	Converting logic test
	0700	NMI test failed
	0800	Timer bus-test failed
	10xx	System board memory parity error
	11xx	I/O channel check error
	1200	Watchdog timeout
	1300	DMA arbitration timeout
	1400	Channel feature card ROM checksum error
	1500	ROM checksum error or DMA error
	1600	System board port read/write failure
	1800	System board parity or L2-cache error during previous power-on
	2000	Microprocessor test error
	6100	Dead battery
	6300	Clock not updating
	6400	Memory configuration error
	6500	Adapter ID mismatch
	6600	Adapter busy error
	6700	Clock not updating
	6900	Processor complex configuration error
	7000	ASCII setup conflict error
	7100	Rolling bit test failure on CMOS shutdown address byte
	7200	Rolling bit test failure on NVRAM diagnostic byte
	7300	Bad CMOS/NVRAM checksum
	7400	Bad configuration

Figure 3-22 (Part 1 of 2). POST Error Message Table

Major Code	Minor Code	Description
0002		Memory errors
	0xxx	Memory error
	1xxx	Unrecoverable error in first 1MB
	2100	ROM to RAM remap error
	25xx	Unsupported memory-type installed or memory pair mismatch
0003		Keyboard
	0100	Keyboard error
	0200	Keyboard locked
	0300	Keyboard to system board interface error
	0400	Keyboard clock high
	0500	No keyboard +5V
0004	0100	Display error
0005	0100	Display error
0006		Diskette
	0100	Diskette drive or controller error
	0200	Diskette IPL boot record not valid
	0604	Non-media sense
0011	0100	Async chip error
0017		Fixed disk error
	8000	Fixed disk 0 failed
	8100	Fixed disk 1 failed
	8200	Disk controller error
	9000	Hard file 0 error
	9100	Hard file 1 error
0024	0100	System board video error
0086		Mouse
	0100	System bus error - keyboard/pointing device interface
	0200	Pointing device error
	0300	Pointing device or system bus error
0129		Cache
	0x00	Cache error
I999		Special instruction codes
	00xx	Initial microcode load (IML) error
	03xx	No bootable device
	04xx	IML to system mismatch

Figure 3-22 (Part 2 of 2). POST Error Message Table

Notes:

Section 4. Processor Complex

The processor complex provides certain devices and features that work in conjunction with those devices and features provided by the system board. In addition, the processor complex determines system performance and certain channel timings. This section describes these aspects of the processor complex.

A system can have either a Type 1 or Type 2 processor complex. The major difference between the two types is speed. Programs can identify the type by reading the model and submodel bytes and the BIOS revision level (Interrupt hex 15, function code AH = hex C0). The following table shows these bytes and the processor complex types.

Model Byte	Submodel Byte	Revision Level	Speed	Processor Complex
F8	14	00	25 MHz	Type 1
F8	16	00	33 MHz	Type 2

Figure 4-1. Model and Submodel Bytes

Refer to the *IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference* for a listing of other systems, and check the supplements section for updates to that listing.

Type 1

The following are the devices and features for the Type 1 processor complex.

Device	Type	Features
Microprocessor		80486 – 25 MHz 32-bit address and 32-bit data interface
Cache	---	8KB, 4-way, write-through, internal cache Optional L2 cache card interface
ROM Subsystem	---	128KB physical ROM
RAM Subsystem	---	Eight connectors support 4 to 32MB, interleaved Expandable on the system board only
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Math Coprocessor	---	Math coprocessor functions included in 80486

Figure 4-2. Type 1 Processor Complex Feature and Devices

The following shows the performance and other timing information for the Type 1 processor complex. These timings affect the channel performance for operations involving the processor complex or system board memory.

Device	Cycle Time (ns)
Microprocessor (25 MHz – 40 ns Clock):	
Access to Channel:	
Default Transfer Cycle	240
Extended Transfer Cycle	320
Refresh Rate (Typically performed every 15.1 μs)	500 (min)
DMA Controller (10 MHz – 100 ns Clock):	
Single Transfer: 300 + I/O Access + Memory Access	
Burst Transfers: 300 + (I/O Access + Memory Access)N *	
System Board Memory Access	300
Default Transfer Cycle	200
Synchronous Extended Transfer Cycle	300
* N is the number of transfers in the burst transfer.	

Figure 4-3. System Performance Specifications, Type 1 Processor Complex

Device	Cycle Time (ns) per Memory Type		
	70 ns	80 ns	85 ns
Microprocessor (25 MHz – 40 ns Clock):			
Memory Read (Cache Hit)	40	40	40
Memory Read (Cache Miss, Page Hit, Burst)	320	320	400
Memory Read (Cache Miss, Page Miss, Burst)	440	480	560
Memory Write (Page Hit)	160	160	200
Memory Write (Page Miss)	280	320	360
Microprocessor – with Optional L2 Cache			
Memory Read (Cache Hit, Optional Cache Hit)	40	40	40
Memory Read (Cache Miss, Optional Cache Hit, Burst)	200	200	200
Memory Read (Cache Miss, Optional Cache Miss, Page Hit, Burst)	320	320	400
Memory Read (Cache Miss, Optional Cache Card Miss, Page Miss, Burst)	440	480	560
Memory (Page Hit)	160	160	200
Memory Write (Page Miss)	280	320	360
Bus Master Access to System Board RAM			
Page Hit (minimum)	300	300	300
Page Miss (minimum)	300	300	300

Figure 4-4. Memory Performance Specifications, Type 1 Processor Complex

Type 2

The following are the devices and features for the Type 2 processor complex.

Device	Type	Features
Microprocessor		80486—33 MHz 32-bit address and 32-bit data interface
Cache	---	8KB, 4-way, write-through, internal cache Optional cache card interface
ROM Subsystem	---	128KB physical ROM
RAM Subsystem	---	Eight connector support 4 to 32MB interleaved Expandable on the system board only
DMA Controller	1	Eight independent DMA channels Single or burst transfers and read verification
Math Coprocessor	---	Math coprocessor functions included in 80486

Figure 4-5. Type 2 Processor Complex Feature and Devices

The following shows the performance and other timing information for the Type 2 processor complex. These timings affect the channel performance for operations involving the processor complex or system board memory.

Device		Cycle Time (ns)
Microprocessor (33 MHz – 30 ns Clock):		
Access to Channel:		
Default Transfer Cycle		240
Extended Transfer Cycle		320
Refresh Rate (Typically performed every 15.1 μs)		500 (min)
DMA Controller (10 MHz – 100 ns Clock):		
Single Transfer:	300 + I/O Access + Memory Access	
Burst Transfers:	300 + (I/O Access + Memory Access)N *	
System Board Memory Access	300	
Default Transfer Cycle	200	
Synchronous Extended Transfer Cycle	300	
* N is the number of transfers in the burst transfer.		

Figure 4-6. System Performance Specifications, Type 2 Processor Complex

Device	Cycle Time (ns) per Memory Type		
	70 ns	80 ns	85 ns
Microprocessor (33 MHz – 30 ns Clock):			
Memory Read (Cache Hit)	30	30	30
Memory Read (Cache Miss, Page Hit, Burst)	240	300	300
Memory Read (Cache Miss, Page Miss, Burst)	360	420	420
Memory Write (Page Hit)	120	150	150
Memory Write (Page Miss)	240	270	270
Microprocessor – with Optional L2 Cache			
Memory Read (Cache Hit, Optional Cache Hit)	30	30	30
Memory Read (Cache Miss, Optional Cache Hit, Burst)	150	150	150
Memory Read (Cache Miss, Optional Cache Miss, Page Hit, Burst)	240	300	300
Memory Read (Cache Miss, Optional Cache Card Miss, Page Miss, Burst)	360	420	420
Memory Write (Page Hit)	120	150	150
Memory Write (Page Miss)	240	270	270
Bus Master Access to System Board RAM			
Page Hit (minimum)	300	300	300
Page Miss (minimum)	300	300	300

Figure 4-7. Memory Performance Specifications, Type 2 Processor Complex

I/O Address Map

The following shows the I/O address for devices located on the processor complex.

Hex Addresses	Device
0000 – 001F	DMA Controller (0 – 3)
0081 – 0083, 0087	DMA Page Registers (0 – 3)
0089 – 008B, 008F	DMA Page Registers (4 – 7)
0090	Central Arbitration Control Point
00C0 – 00DF	DMA Controller (4 – 7)
00E0	Memory Control Register Select
00E1	Parity Trap Register
00E2	Cache Control Register
00E3	Cache Status Register
00E4	Memory Control Data Read/Write

Figure 4-8. Processor Complex I/O Address Map

Optional Cache

The Type 1 and Type 2 processor complexes have a 160-pin connector for an optional cache card (L2 cache). The optional cache card provides secondary cache and cache controller for the system microprocessor.

The optional cache card provides the system microprocessor with an additional 256KB cache. It operates as 2-way set-associative, write-through cache with parity. The primary cache in the 80486 must be enabled to operate the secondary cache. The L2 cache is controlled through the Cache Control Register (Hex 00E2), and its status is indicated in the Cache Status Register (Hex 00E3).

Micro Channel

This section describes the implementation of the Micro Channel architecture on Model 95 systems. For general Micro Channel information, refer to *Hardware Interface Technical Reference – Architectures.*

Note: The system does not support adapters that use the matched memory extension.

Central Arbiter

The central arbitration control point gives intelligent subsystems on the channel the ability to share and control the system. It allows burst data transfers and prioritization of control between devices. This arbiter supports up to 16 arbitrating devices.

Arbitration Bus Priority Assignments

The following table shows the assignment of arbitration levels. The functions with the lowest arbitration level have the highest priority.

ARB Level	Primary Assignment
-2	Memory Refresh
-1	NMI
0	DMA Channel 0 (Programmable to any arbitration level)
1	DMA Channel 1
2	DMA Channel 2
3	DMA Channel 3
4	DMA Channel 4 (Programmable to any arbitration level)
5	DMA Channel 5
6	DMA Channel 6
7	DMA Channel 7
8–B	Available
C	SCSI Adapter
D, E	Available
F	System Microprocessor

Figure 4-9. Arbitration Bus Priority Assignments

Note: Devices designed for arbitration level 0 or 1 should have limited bandwidth or short bursts so diskette overruns can be prevented or recovered by retry operations. The diskette drive controller, on arbitration level 2, can be held inactive by devices on levels 0 and 1, by a refresh operation, and by the previous controlling master. The diskette drive controller should not be held inactive for more than 12 microseconds to prevent overrun.

Nonmaskable interrupt (NMI) service is executed at a priority level higher than 0, called -1. Memory refresh is prioritized at -2, two levels higher than 0. Levels -1 and -2 are reached on the system board only, while the 'arbitrate/-grant' signal is in the arbitrate state.

When the central arbitration control point receives a level -1 request (NMI, a system-board internal signal), it activates -PREEMPT, waits for the end of transfer, and then places ARB/-GNT in the arbitrate state, which denies channel activity to arbitrating devices. The central arbitration control point gives the grant to the level -1 request, and holds ARB/-GNT in the arbitrate state until the operation is complete and the NMI is reset.

Central Arbiter Programming

The central arbitration control point provides access to programmable options through the Arbitration register, which is accessed at I/O address hex 0090. The bits are defined differently for read and write operations, as shown in the following tables.

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Mask
5	Enable Extended Arbitration
4–0	Reserved

Figure 4-10. Arbitration Register (Hex 0090) – Write

Bit	Definition
7	Enable System Microprocessor Cycle
6	Arbitration Masked by NMI
5	Bus Time-out
4	Reserved
3–0	Value of Arbitration Bus During Previous Grant State

Figure 4-11. Arbitration Register (Hex 0090) – Read

Bit 7 Setting this bit to 1 enables system microprocessor cycles during arbitration cycles. This bit can be set to 0 if an arbitrating device requires total control of the channel bandwidth. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates system microprocessor cycles are enabled during arbitration.

Bit 6 Setting this bit to 1 causes the central arbitration control point to enter the arbitration state. The system microprocessor controls the channel until this bit is reset to 0. This bit is set to 0 by a system reset.

Reading this bit as a 1 indicates that an NMI has occurred and has masked arbitration.

Warning: This bit should be set to 1 only by diagnostic routines and system error-recovery routines.

Bit 5 Setting this bit to 1 enables extended arbitration. The minimum arbitration cycle is 300 nanoseconds; this bit extends that minimum cycle to 600 nanoseconds. This bit is set to 0 during a system reset.

Reading this bit as a 1 indicates that a bus time-out has occurred, and resets bit 6 in this register to 0.

Bit 4 This bit is reserved and should be 0.

Bits 3 – 0 These bits are undefined for a write operation and should be set to 0.

Reading these bits returns the arbitration level of the arbiter controlling the channel during the most recent grant state. This information allows the system microprocessor to determine the arbitration level of the device that caused a bus time-out.

Memory Subsystem

Memory on the system board is parity-checked, interleaved random-access memory and must be installed in matched pairs: one in an A connector and one in the matching B connector (for memory connector information, see "System Board Memory Connectors" on page 3-3). The memory in each pair must be the same speed and size. Memory on adapters in the channel are not mapped into the cacheable address space of the system microprocessor.

System board memory is designed so that the system microprocessor can access memory while a bus master has control of the channel. The memory controller manages this dual access by interleaving the microprocessor and bus master accesses. In addition, system board memory is organized into pairs of banks so that the microprocessor can perform burst cycles with two-way interleaved accesses. Because of this organization, the microprocessor can perform zero-wait-state transfers for every other 32-bit transfer in the burst cycle.

Memory Presence Detect

The presence-detect signals are used by the system to determine size and speed of memory on the memory card. The pins are either not connected (1), or connected to ground (0).

A set of four bits shows the state of all presence-detect signals for a specific memory connector; the bit is 0 when the signal is connected to ground. The following figure shows the information indicated by these bits as well as the bank size of the memory card. All combinations not shown are reserved.

Presence Detect 3 2 1 0	Memory Card Definition	Bank Size
0 1 0 0	4MB 70-ns Memory	4MB
0 0 0 0	4MB 80-ns Memory	4MB
1 1 0 0	2MB 70-ns Memory	1MB
1 0 0 1	2MB 80-ns Memory	1MB
0 1 0 1	2MB 85-ns Memory	1MB
0 1 1 0	1MB 85-ns Memory	1MB
1 1 1 1	Connector is Empty	

Figure 4-12. Presence-Detect Bits

Memory Controller Registers

The memory controller, located on the processor complex, has several internal registers that are used to control the memory in the memory connectors on the system board. The memory controller manages this memory in banks of 1MB or 4MB. The size of the bank determines its granularity.

Connectors A1 through A4 contain banks 0 through 7; connectors B1 through B4 contain banks 8 through hex F.

Each internal register is accessed by writing its internal address (index) to the Memory Controller Address register at hex 00E0 and then accessing the data through the Memory Controller Data register at hex 00E4. These registers can be accessed only from the system microprocessor.

I/O port 00E2 controls the internal 80486 cache and the optional cache functions. I/O port 00E3 is used for cache status and memory bank parity error determination. I/O port 00E1 is also used for memory bank parity error determination.

All registers in the memory controller are 8-bit read/write registers. The following shows the function and index for each internal register. These registers are programmed during POST to configure the memory controller according to the type and amount of memory and other system requirements.

Index	Register Function
90	Memory Bank 0 Base Address
91	Memory Bank 1 Base Address
92	Memory Bank 2 Base Address
93	Memory Bank 3 Base Address
94	Memory Bank 4 Base Address
95	Memory Bank 5 Base Address
96	Memory Bank 6 Base Address
97	Memory Bank 7 Base Address
98	Memory Bank 8 Base Address
99	Memory Bank 9 Base Address
9A	Memory Bank A Base Address
9B	Memory Bank B Base Address
9C	Memory Bank C Base Address
9D	Memory Bank D Base Address
9E	Memory Bank E Base Address
9F	Memory Bank F Base Address
A0	Split Address
A1	Memory Encoding
A2	Cache/Timer Control
A3	Boundary 0 Cache Control
A4	Boundary 1 Cache Control (Low Address)
A5	Boundary 1 Cache Control (High Address)
A6	Memory Bank Enable 1
A7	Memory Bank Enable 2
A8	System Bus Request Timer
A9	System Bus Hold Timer
AA	System Bus Idle Timer

Figure 4-13. Memory Controller Register Assignments

The 16 Memory Bank Base Address registers and individual bits in the two Bank Enable registers control the enabling and mapping of all memory on the system board. Individual bits in the Parity Trap register (hex 00E1) indicate whether the respective bank has detected a parity error.

The following figure shows the relationship of each of the control or status registers to the bank of memory that it represents. The error-indicator bit is in the Parity Trap register (hex 00E1).

Bank Number	Index of Memory Bank Address Register	Memory Bank Enable Register and Bit	Error Indicator Bit
0	90	Register 1, Bit 0	0
1	91	Register 1, Bit 1	1
2	92	Register 1, Bit 2	2
3	93	Register 1, Bit 3	3
4	94	Register 1, Bit 4	4
5	95	Register 1, Bit 5	5
6	96	Register 1, Bit 6	6
7	97	Register 1, Bit 7	7
8	98	Register 2, Bit 0	0
9	99	Register 2, Bit 1	1
A	9A	Register 2, Bit 2	2
B	9B	Register 2, Bit 3	3
C	9C	Register 2, Bit 4	4
D	9D	Register 2, Bit 5	5
E	9E	Register 2, Bit 6	6
F	9F	Register 2, Bit 7	7

Figure 4-14. Memory Control

Memory Bank Base Address Register (Index Hex 90 – 9F)

Each bank of memory has an 8-bit, read/write register that determines the base address for that bank. The banks can be set to respond to any starting 1MB address from 0 to 255MB. 4MB memory cards must be on 4MB address boundaries.

The 16 Base Address registers are at indexes hex 90 to 9F.

Bit	Function
7	Address Bit A27
6	Address Bit A26
5	Address Bit A25
4	Address Bit A24
3	Address Bit A23
2	Address Bit A22
1	Address Bit A21
0	Address Bit A20

Figure 4-15. Memory Bank Base Address Register (Index Hex 90 – 9F)

Split Address Register (Index Hex A0)

This 8-bit, read/write register at index hex A0 determines the starting address for the split memory block. The split-memory block can be positioned at any 1MB boundary from 1MB to 255MB; it must not be positioned below 1MB.

The bit definitions and functions are described below:

Bit	Function
7	Split Address Bit A27
6	Split Address Bit A26
5	Split Address Bit A25
4	Split Address Bit A24
3	Split Address Bit A23
2	Split Address Bit A22
1	Split Address Bit A21
0	Split Address Bit A20

Figure 4-16. Split Address Register (Index Hex A0)

Bits 7 – 0 These bits define the starting address of the split-memory block. When split memory is enabled, these bits determine its starting address. The starting location can be at any 1MB boundary from 1MB to 255MB. This register must not be set to 00.

Memory Encoding Register (Index Hex A1)

This 8-bit, read/write register at index hex A1 controls miscellaneous functions within the memory controller.

Bit	Function
7	-System Bus Enable
6	-Reserved
5	-Disable ROM Space Decode
4	-Lock
3	-Enable Split
2	-640
1	ROM enable
0	-Enable Planar Parity Check

Figure 4-17. Memory Encoding Register (Index Hex A1)

Bit 7 This bit is used to isolate system-board memory from the channel during initialization of the memory controller. When the bit is set to 1, channel accesses to system board memory are disabled and the memory controller ignores all channel requests. When the bit is set to 0, the channel is enabled.

Bit 6 This bit is reserved.

Bit 5 This bit controls the memory-controller decode of the first 4096 locations in system ROM space from 000E0000 to 000E0FFF. When the bit is set to 0, the decode of these addresses is disabled; when set to 1, the memory controller selects ROM or system RAM for all addresses from hex 000E0000 to 000FFFFF and from hex FFFE0000 to FFFFFFFF.

While this bit is 0, accesses to addresses hex 000E0000 to 000E0FFF are not directed to the space allocated for system ROM code and can be decoded on the channel.

Bit 4 This bit determines whether locked-access operations from the system microprocessor are enabled. When this bit is set to 0, lock is enabled and microprocessor cycles are performed as follows:

- When the system microprocessor owns the channel and is accessing memory with the 'lock' signal active, the microprocessor must complete the entire operation before another master can be granted control of the channel. This includes the DMA controller.

- When a bus-master owns the channel and the microprocessor tries to run a locked cycle operation, the microprocessor waits until the bus master releases the channel.

Bit 3 This bit determines if the split-memory block is assigned addresses or is disabled. The top 128KB of the first 1MB is always mapped into the ROM address space and the code in ROM is copied into this space.

When this bit is set to 0, the split-memory block is enabled. The split-memory block size is dependent on the value of the 640 bit. Its address is determined in Memory Encoding Register 2. When this bit is set to 1, the split-memory block is disabled.

Bit 2 This bit determines where the first active 1MB of memory is split. When this bit is set to 0, the system maps 640KB of the first 1MB to addresses hex 00000000 to 0009FFFF. The split-memory block, 256KB, is mapped to the address specified in the Split Address register.

When this bit is set to 1, the system maps 512KB of the first 1MB to addresses hex 00000000 to 0007FFFF. The split-memory block, 384KB, is mapped to the address specified in Split Address register. The addresses hex 00080000 to 0009FFFF are unassigned.

Note: The memory address space from the memory split to 896KB is not cached.

Bit 1 This bit determines how addresses hex 000E0000 to 000FFFFF are assigned.

When this bit is set to 1, ROM is enabled and the read-access addresses are assigned to ROM; the write-access addresses are assigned to RAM. When this bit is set to 0, ROM is disabled and read accesses are assigned to RAM; write accesses are disabled while ROM is disabled.

Note: This bit should be set to 0 because system performance can be degraded when ROM is enabled.

Bit 0 When set to 0, this bit enables parity checking of system board memory. Setting this bit to 1 clears the pending parity error. For compatibility with other systems, enabling and disabling of parity checking should also be done through System Control Port B at address hex 0061

(see the register definition on "System Control Port B (Hex 0061)" on page 3-17).

Note: When a parity error occurs, clear the error using this bit then clear the error using the bit in System Control Port B.

Cache/Timer Control Register (Index Hex A2)

This 8-bit, read/write register at index hex A2 controls the cache and timer functions.

Bit	Function
7	-Enable Processor Preempt Timers
6–3	Reserved
2	-Enable Boundary 1 Check
1	-Enable Boundary 0 Check
0	-Enable Cache

Figure 4-18. Cache/Timer Control Register (Index Hex A2)

Bit 7 This bit controls the timers used to allocate bus cycles to the microprocessor. In system environments with several bus-master-type adapters, the system microprocessor can be prevented from gaining control of the channel for long periods of time. When this bit is set to 0, the system-bus timer registers (index hex A8 through AA) are enabled, and the system microprocessor can be ensured a percentage of the channel bandwidth.

Bits 6–3 Reserved

Bit 2 This bit controls the boundary check for a noncacheable address from 16MB to 256MB. When the bit is set to 0, boundary checks are enabled. For detail, see "Boundary 1 Cache Control Registers (Index Hex A4 and A5)" on page 4-20.

Bit 1 This bit controls the boundary check for a noncacheable address below 16MB. When the bit is set to 0, boundary checks are enabled. For detail, see "Boundary 0 Cache Control Register (Index Hex A3)" on page 4-19.

Bit 0 This bit enables or disables the internal cache in the system microprocessor and the external cache, if it is installed. When this bit is set to 0, both caches are enabled. When this bit is set to 1, both caches are disabled.

After disabling the caches and before enabling them, they should be flushed (see "Cache Control Register (Hex 00E2)" on page 4-26).

Boundary 0 Cache Control Register (Index Hex A3)

This 8-bit, read/write register at index hex A3 contains the upper-range and lower-range control bits. This register determines the memory range, from 1MB up to 16MB, that will not be cached.

When the cache is enabled, memory below 1MB is cached except for the following:

- The addresses from hex 000A0000 to 000DFFFF are never cached.
- The addresses from hex 000E0000 to 000FFFFF are not cached when ROM is enabled, and are cached when ROM is disabled.
- The addresses from hex 00080000 to 000DFFFF are not cached when the memory split is at 512KB.

The range check for noncacheable addresses is enabled by bit 1 in the Cache/Timer Control register. When the boundary 0 range check is disabled, all addresses from 1MB to 16MB are cacheable and the addresses are not checked. When the range check is enabled, the memory controller checks the range of the memory address to determine if it is cacheable. If the address is equal to or greater than the lower boundary limit *and* equal to or less than the upper boundary limit, it is considered to be noncacheable.

Bit	Function
7–4	Upper Limit for Boundary 0
3–0	Lower Limit for Boundary 0

Figure 4-19. Boundary 0 Cache Control Register (Index Hex A3)

Bits 7–4 These bits contain the upper boundary limit and are compared to address bits A23 through A20 (address bits A24 thru A31 must be 0).

Bits 3–0 These bits contain the lower boundary limit and are compared to address bits A23–A20 (address bits A24 thru A31 must be 0).

Boundary 1 Cache Control Registers (Index Hex A4 and A5)

These two registers are 8-bit, read/write registers at index hex A4 and A5. The lower-boundary register (index hex A4) contains the lower-range control bits and the upper-boundary register (index hex A5) contains the upper-range control bits. The upper-range and lower-range control bits determine the noncacheable addresses in the memory space from 16MB to 256MB.

When the cache is enabled, memory below 1MB is cached except for the following:

- The addresses from hex 000A0000 to 000DFFFF are never cached.
- The addresses from hex 000E0000 to 000FFFFF are not cached when ROM is enabled, and are cached when ROM is disabled.
- The addresses from hex 00080000 to 000DFFFF are not cached when the memory split is at 512KB.

The range check for noncacheable addresses is enabled by bit 2 in the Cache/Timer Control register. When the boundary 1 range check is disabled, all addresses from 16MB to 256MB are cacheable and the addresses are not checked. When the range check is enabled, the memory controller checks the range of the memory address to determine if it is cacheable. If the address is equal to or greater than the lower boundary limit *and* equal to or less than the upper boundary limit, it is considered to be noncacheable.

The Lower Boundary 1 Cache Control register contains the lower boundary limit and is compared to address bits A27 through A20 (address bits A28 through A31 must be 0).

The Upper Boundary 1 Cache Control register contains the upper boundary and is compared to address bits A27 through A20 (address bits A28 through A31 must be 0). When the boundary includes the first 1MB of memory, any area that normally would be cacheable (for example hex 0E0000 to 0FFFFF) will be noncacheable.

Bit	Function
7	Lower Limit Boundary A27
6	Lower Limit Boundary A26
5	Lower Limit Boundary A25
4	Lower Limit Boundary A24
3	Lower Limit Boundary A23
2	Lower Limit Boundary A22
1	Lower Limit Boundary A21
0	Lower Limit Boundary A20

Figure 4-20. Lower Boundary 1 Cache Control Register (Index Hex A4)

Bit	Function
7	Upper Limit Boundary A27
6	Upper Limit Boundary A26
5	Upper Limit Boundary A25
4	Upper Limit Boundary A24
3	Upper Limit Boundary A23
2	Upper Limit Boundary A22
1	Upper Limit Boundary A21
0	Upper Limit Boundary A20

Figure 4-21. Upper Boundary 1 Cache Control Register (Index Hex A5)

Memory Bank Enable Register 1 (Index Hex A6)

This 8-bit, read/write register at index A6 controls the enabling of the first eight banks of memory in the system-board memory connectors A1 through A4.

Bit	Function
7	Disable Bank 7 (Port 97)
6	Disable Bank 6 (Port 96)
5	Disable Bank 5 (Port 95)
4	Disable Bank 4 (Port 94)
3	Disable Bank 3 (Port 93)
2	Disable Bank 2 (Port 92)
1	Disable Bank 1 (Port 91)
0	Disable Bank 0 (Port 90)

Figure 4-22. Memory Bank Enable Register 1 (Index Hex A6)

Bits 7–0 Each bit controls the enabling of memory for the specified bank. When the bit is set to 1, the bank is disabled. When the bit is 0, the bank is enabled and responds to the address specified in its Base Address register.

Note: Because memory must be enabled in pairs, corresponding banks should be enabled in Memory Bank Enable Register 2. These two registers should be set to the same value.

Memory Bank Enable Register 2 (Index Hex A7)

This 8-bit, read/write register at index hex A7 controls the enabling of the second 8 banks of memory in the system-board memory connectors B1 through B4.

Bit	Function
7	Disable Bank F (Port 9F)
6	Disable Bank E (Port 9E)
5	Disable Bank D (Port 9D)
4	Disable Bank C (Port 9C)
3	Disable Bank B (Port 9B)
2	Disable Bank A (Port 9A)
1	Disable Bank 9 (Port 99)
0	Disable Bank 8 (Port 98)

Figure 4-23. Memory Bank Enable Register 2 (Index Hex A7)

Bits 7 – 0 Each bit controls the enabling of memory for the specified bank. When the bit is set to 1, the bank is disabled. When the bit is 0, the bank is enabled and responds to the address specified in its Base Address register.

Note: Because memory must be enabled in pairs, corresponding banks should be enabled in Memory Bank Enable Register 1. These two register should be set to the same value.

System Bus Request Timer Register (Index Hex A8)

The System Bus Request Timer Register, the System Bus Hold Timer Register, and the System Bus Idle Timer Register work together to determine the percentage of time that the system microprocessor owns the channel. Each register is an 8-bit read/write register and they are active only when bit 7 of the Cache/Timer Control register is set to 1.

The values in these three registers are moved to counters, which are decremented for every other clock cycle of the system microprocessor.

For the Type 1 Processor Complex, each count represents 80 nanoseconds. For the Type 2 Processor Complex, each count represents 60 nanoseconds.

The System Bus Request Timer register at index hex A8 determines how long the system microprocessor will wait before preempting for use of the channel.

The value in this register is moved to a counter when the system microprocessor loses ownership of the channel. Decrementing the counter begins when the system microprocessor wants to use the channel and another master owns it.

If the count reaches 0 and the system microprocessor has not yet gained control of the channel, -PREEMPT is driven active.

System Bus Hold Timer Register (Index Hex A9)

This register determines the maximum amount of time that the system microprocessor maintains ownership of the channel.

The value in this register is moved to a counter when the system microprocessor loses ownership of the channel. Decrementing the counter begins as soon as the system microprocessor is granted ownership of the channel.

If -PREEMPT was driven active because of the System Bus Request Timer register the system microprocessor still owns the channel when the count reaches 0, the system microprocessor gives up ownership of the channel.

Note: If the system microprocessor gained control of the channel without driving -PREEMPT active, the channel is given up when another device requests the channel.)

System Bus Idle Timer Register (Index Hex AA)

This register determines the maximum amount of time that system microprocessor will retain control of the channel without using it.

The value in this register is moved to a counter each time the system microprocessor accesses the channel. Decrementing begins when the system microprocessor starts the channel access.

If the system microprocessor still owns the channel when the count reaches 0, the system microprocessor gives up ownership of the channel

Parity Trap Register (Hex 00E1)

This 8-bit, read-only register at address hex 00E1 is used to determine if system-board memory caused a parity error. When a parity error occurs, the state of 'row address select' signals is latched into this register.

If a bit is a 1, it indicates that the memory in that pair of matching connectors (A and B) was the cause of the error. To determine which memory card caused the error, test bits 0 and 1 in the Cache Status register (Hex 00E3).

If all bits in this register are 0, the error was not caused by the memory on the system board.

After each parity check, this register must be cleared using the parity-check bit (bit 0 of the Memory Controller register, index A1) to reset the latch.

Bit	Function
7	Error Indicator Connector A4 or B4
6	Error Indicator Connector A4 or B4
5	Error Indicator Connector A3 or B3
4	Error Indicator Connector A3 or B3
3	Error Indicator Connector A2 or B2
2	Error Indicator Connector A2 or B2
1	Error Indicator Connector A1 or B1
0	Error Indicator Connector A1 or B1

Figure 4-24. Parity Trap Register (Hex 00E1)

The bank that generated the parity error can by determined by bits 0 and 1 in the Cache Status Register (Hex 00E3).

Cache Control Register (Hex 00E2)

This 8-bit, read/write register at address hex 00E2

Bit	Function
7	-Flush Level 1 Cache
6	-Flush Level 2 Cache
5	-Enable Level 2 Cache
4–0	Reserved

Figure 4-25. Cache Control Register (Hex 00E2)

Bit 7 This bit controls the flushing of the level 1 cache. When the bit is toggled from 1 to 0, the cache is placed in the flushed state for one processor cycle. When this bit is set to 1, the cache is in the enabled state.

Note: To ensure that the cache is flushed, the cache must be in the enabled state before setting this bit to 0.

Bit 6 This bit controls the flushing of the level 2 cache. When the bit is set to 0, the cache is placed and held in the flushed state. When this bit is set to 1, the state of the level 2 cache is controlled by bit 5.

Bit 5 This bit and bit 6 work together to control the state of the level 2 cache. When this bit is 0, the level 2 cache is enabled.

To disable both caches at the same time, use the Cache/Timer Control register (index hex A2), then use the Cache Control register to flush both caches.

Bits 4–0 These bits are reserved.

Notes:

1. Refer to the 80486 microprocessor specification for information on CR0, which must also be set to enable the internal 8KB cache.
2. The cache must be disabled and flushed before enabling ROM or changing the cacheable boundaries.

Cache Status Register (Hex 00E3)

This 8-bit, read-only register contains diagnostic information related to the cache operation.

Bit	Function
7	Reserved
6	Processor Type
5, 4	-L2 Cache Installed
3	-L2 Cache Parity Error
2	Reserved
1	-Parity Error Bank A
0	-Parity Error Bank B

Figure 4-26. Cache Status Register (Hex 00E3)

Bit 7 This bit is reserved.

Bit 6 This bit indicates the type of processor complex that is present. When the bit is a 0, the Type 1 processor complex is installed; when the bit is 1, the Type 2 is installed.

Bits 5, 4 These bits identify the presence of the level 2 cache. When both bits are 0, the 256KB level-2 cache is present; when both bits are 1, the level 2 cache is not present. Other combinations of these bits are reserved.

Bit 3 When this bit is a 0, a parity error was detected in the level 2 cache.

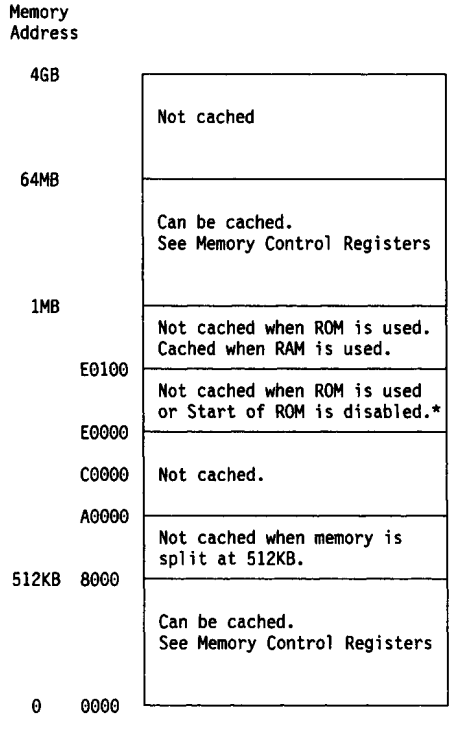
Bit 2 This bit is reserved.

Bit 1 When this bit is a 0, a parity error was detected in system-board memory in an A connector.

Bit 0 When this bit is a 0, a parity error was detected in system-board memory in a B connector.

Processor Cache Address Map

The following map is a summary of the Memory Control register options. Only system-board memory is mapped into the microprocessor and level-2 caches. The level 2 (L2) cache is optional.



* Refer to Bit 5 on page 4-16 for details.

Figure 4-27. Cache Address Map Summary

Read-Only Memory Subsystem

The ROM subsystem is located on the processor complex and consists of 128KB in a 128K by 8-bit arrangement. The ROM is active at power-on at address space hex 000E0000 to 000FFFFF. The ROM contains the code that initializes the system to load and execute POST and BIOS code from a DASD device. After POST ensures the proper operation of system memory, POST and BIOS code from a DASD device can be copied to RAM, and ROM disabled. ROM is also assigned at the top of the 4GB address space from hex FFFE0000 to FFFFFFFF.

Two bits in the Memory Control register (index A1) control ROM addressing. The ROM-enable bit determines whether ROM or RAM is accessed at address space hex 000E0000 to 000FFFFF, and the disable-ROM-space-decode bit selects the system decode and cacheability of the first 4KB of ROM address space.

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Numerics