POINTER
386

The material in this manual is for information only and is subject to change without notice.

VERSION: 2.0

RADIO FREQUENCY INTERFERENCE STATEMENT

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference with radio and television reception.

If this equipment does cause interference to radio or TV reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

* *Reorient the receiving antenna.*
* *Relocate the computer away from the receiver.*
* *Move the computer away from the receiver.*
* *Plug the power cord of computer into a different outlet so that computer and receiver are on different branch circuits.*
* *Ensure that card slot covers are in place when no card is installed.*
* *Ensure that card mounting screws, attachment connector screws, and ground wires are tightly secured.*
* *If peripherals are used with this system, it is suggested to use shielded, grounded cables, with in-line filters if necessary.*

If necessary, the user should consult the dealer service representative for additional suggestions.

The manufacturer is not responsible for any radio or TV interferences caused by unauthorized modifications to this equipment. It is the responsibility of the user to correct such interferences.

Note

1. Electronic components are sensitive to dust and dirt. Do inspect and clean the computer system regularly.

2. Turn off the power whenever you install or remove any connector, memory module and add-on card. Before turning on the power, make sure that all the connectors, memory modules and add-on cards are secured.

3. After power is on, please wait for a minute. The system BIOS are going through a self-test during this period and nothing is shown on the screen. After the self-test, the system BIOS will initialize the display adaptor and show messages.

4. The SIMM sockets are fragile device. Do not force the SIMM modules into the sockets. It may break the locking latches.

Preface

The manual provides information about the installation and maintenance of OCTEK Pointer-386 motherboard. In-depth explanations of the functions of this motherboard are provided. In the appendix, the system BIOS setup is explained.

The content in this manual is only for reference and is intended to provide basic information for the general users. There are also technical information for hardware and software engineers.

In this manual, there are 4 chapters. Chapter 1 contains a brief introduction and specification of OCTEK Pointer-386 motherboard. In the chapter 2, the functions of Pointer-386 are explained. It also outlines many advanced features of the CPU and the system architecture. Chapter 3 explains the installation of coprocessor, DRAM modules and jumpers. Technical information is provided in the chapter 4.

System BIOS and the system setup are described in the appendix A. All setup procedures are explained. Appendix B contains the information about the memory expansion board.

Additional information are given in appendix C, D, E and F for the maintenance purpose.

CONTENT

Chapter 1	*INTRODUCTION*	*1-1*
Chapter 2	*GENERAL FEATURES*	*2-1*
	Specification	*2-1*
	Processor	*2-3*
	Math Coprocessor	*2-6*
	Cache Memory	*2-7*
	Memory System	*2-8*
	Dual Bus Design	*2-10*
	System Functions	*2-11*
Chapter 3	*INSTALLING COMPONENTS*	*3-1*
	Installing Math Coprocessor	*3-1*
	Installing RAM Modules	*3-3*
	Installing External Battery	*3-5*
	Configuration of Memory	*3-6*
	DRAM Configuration	*3-8*
	Configuration of Cache Memory	*3-9*
	Control of System Speed	*3-13*
	Reset CMOS Setup Information	*3-13*
	System Board Jumper Setting	*3-14*
	System Board Connectors	*3-15*

Chapter 4 *TECHNICAL INFORMATION* *4-1*
Memory Mapping *4-1*
I/O Address Map *4-2*
System Timers *4-4*
System Interrupts *4-6*
Direct Memory Access (DMA) *4-7*
Real Time Clock and CMOS RAM *4-8*
CMOS RAM Address Map *4-9*
Real Time Clock Information *4-10*
System Expansion Bus *4-11*

APPENDIX A *SYSTEM BIOS* *A-1*
Self-test *A-1*
System Setup *A-4*
CMOS Setup *A-6*
Extended Setup Program *A-11*
Easy Setup OPTi Chipset *A-12*
Advanced Setup OPTi Chipset *A-19*

APPENDIX B *MEMORY EXPANSION CARD* *B-1*

APPENDIX C *OPERATION & MAINTENANCE* *C-1*

APPENDIX D *TROUBLESHOOTING* *D-1*

APPENDIX E *SYSTEM BOARD LAYOUT* *E-1*

APPENDIX F *MEMORY EXPANSION CARD LAYOUT* *F-1*

Chapter 1
Introduction

OCTEK Pointer-386 consists of 32-bit 80386 microprocessor, a large cache memory and highly integrated chipsets to provide high performance, reliability and compatibility. OCTEK Pointer-386 is a perfect choice for CAD/CAM workstation and file server and supports sophisticated 32-bit computing applications and multi-user operating systems.

To speed up the performance of the system, a cache memory with maximum size up to 64KB is incorporated. Frequently used program codes can be fetched by CPU from the high speed cache memory without wait state. Furthermore, access to the main memory is accelerated because the cache controller and the memory controller are integrated together, and operate concurrently. Thus the overhead of accessing the main memory is minimized.

Aimed at supporting advanced CAD/CAM applications, OCTEK Pointer-386 supports 80387 or WEITEK 3167. The total memory is 16MB. 8MB memory is installed on board and additional 8MB is on memory expansion board which is installed on a fast speed 32-bits memory expansion slot.

Fast A20 gate and fast reset generation are incorporated to improve the performance of advanced operation system and expanded memory managers.

Compatibility and reliability are important issues. I/O channel is compatible to standard AT bus. Therefore any peripherals may be used on OCTEK Pointer-386. On board POWERGOOD generator is essential to ensure the reliability of the system and is well-designed to work with all power supplies.

Chapter 2
General Features

SPECIFICATION

Processor:

Intel 80386DX CPU
with optional 80387DX Math Co-processor
or WEITEK 3167 Coprocessor

Speed:

Turbo/normal speed
Software/hardware selectable

I/O Slot:

Compatible to standard AT bus
Two 8-bit and six 16-bit slots

Cache Memory:

32KB or 64KB cache memory
Direct mapped/Write through

Memory:

Shadow RAM for system BIOS and video BIOS
Page/Interleaved mode
SIMM sockets for 256K or 1M modules
8M bytes on board
Up to 16M bytes with optional memory expansion board

System support functions:

- *8-Channel DMA (Direct Memory Access)*
- *16-level interrupt*
- *3 programmable timers*
- *CMOS RAM for system configuration*
- *Real time clock with battery backup*
- *Fast A20 gate and fast reset*

Other Features:

- *On board POWERGOOD generation*
- *External battery connector*
- *Hardware turbo switch*

PROCESSOR

80386DX is a 32-bit microprocessor with 32-bit external data bus and 32-bit external address bus. Therefore it processes more data at the same time than 80286 and can access a large memory size which is necessary for 32-bit applications. To combine the wider bus structure and all the advanced functions on chip, total 275,000 transistors are integrated together.

A complicated pipeline architecture is implemented. Next four bytes of instructions are prefetched into the CPU whenever the bus is idle. The size of the prefetch queue is increased to hold 12 bytes. This architecture reduces the overhead of retrieving and decoding of the instructions.

80386DX is not only an enhanced version of 80286, but designed to overcome the deficiencies of 80286.

80286 PC/AT has been used for many years and its limitations become obvious when more powerful applications are being developed. This microprocessor is limited by its 16-bit architecture. So, it takes longer time to transfer data. The 64KB segment size also becomes an obstacle to complicated software. Software developers have to partition their software into multiple code and data segments, which means larger program size and less efficiency. 80286 lacks a complete facility to switch between real and protected mode. So operating systems need to handle the mode switching and the performance is greatly downgraded.

80386DX is aimed to provide advanced facilities to sophisticated software, but still remains compatible with existing software. It operates at real mode and protected mode. At real mode, all existing software for XT/AT can be used without any problem. Furthermore, new mechanism allows switching between real mode and protected mode at fast speed. Hence applications using

EMS memory can run efficiently although they only use software driver to emulate EMS memory.

The protected mode of 80386 is fully compatible with 80286. All privilege - level and I/O protection system are supported. New system control instructions, memory paging, I/O premission bit map are provided to make 80386 ideal for multi-tasking operation systems.

In addition, a virtual 8086 mode is provided. In this mode, the CPU can be considered by the programs as being divided into several 8086 CPUs and each program has their own CPU and memory space. Several programs for XT/AT as well as operating systems for 80286 and 80386DX can be executed simultaneously. Programs are isolated and protected from each other by 80386DX. Each program can consider that it is running at a XT/AT.

Internal memory management unit is much more complicated than 80286, but provides a more flexible addressing scheme for the next generation operation system. Multitasking, concurrent operation and manipulating huge data base can be accomplished with excellent performance. Paging mechanism is employed by 80386DX to allow powerful operating system to implement virtual memory. Each segment is divided into several pages which are 4K bytes per page. Page mechanism is transparent to software and allows software to address 64 terabytes.

Furthermore, the 64KB segment boundary which is an barrier of 8088 and 80286 is removed and the segment length can be increased up to 4GB. It eliminates the need for the software to manage multiple code and data segments.

80386DX includes many new instructions for system control, high level language support and processor control. These instructions are used in protected mode. New operation systems and software can make use of these instructions for their advanced features, such as concurrent operation and virtual memory.

MATH COPROCESSOR

The demand for sophisticated, number-crunching scientific and business applications has rapidly increased in recent years. 80386DX features an integer Arithmetic Logic Unit which only handles simple integer operations such as addition and multiplication. Floating-point operations which are actually utilized by applications must be accomplished through software routines.

To overcome this obstacle, external Math coprocessor is necessary. The Math coprocessor contains complex hardware and large data registers for floating-point numeric operations. In OCTEK Pointer-386, the Math coprocessor is optional and both Intel 80387 and WEITEK 3167 are supported.

80387 is upward object-code compatible from 80287 and 8087, but runs 6 to 11 times faster than 80287 used in AT. It fully implements the IEEE 754 Binary Floating-point Arithmetic standard with a high precision 80-bits internal architecture.

WEITEK 3167 can deliver more power than 80387 and is supported by various operation systems and high level programming language compilers. It has a direct interface with the CPU. So the data are transferred between them at full speed.

CACHE MEMORY

The system performance can not simply be improved by increasing the clock rate of the system. The performance depends on many factors, such as system architecture and memory configuration.

A cache memory system with low cost DRAM as main memory and high speed SRAM as cache memory becomes the only choice for high performance system in terms of price and performance. The frequently used data code instructions are kept in the high speed cache memory. Therefore, most of the memory operations are carried out in the cache memory instead of the slow speed main memory.

OCTEK Pointer-386 incorporates a cache controller with maximum 64K byte cache memory. The cache controller is integrated into the chipset, which will simplify the system design and reduce the chip count. The cache controller works jointly with the memory controller. This arrangement can speed up memory access when a cache read miss occurs and hence the overall performance is improved. For a cache read hit, the CPU operation is completed with zero wait state.

The cache memory size is 32KB or 64KB and the line size is 4, 8 or 16 bytes. The design of the cache controller is intended to provide optimum performance with simple construction. With 64KB cache memory, hit rate exceeds 95% and the wait state is almost eliminated.

MEMORY SYSTEM

Four banks of DRAMs can be installed. Two banks are available on motherboard and others are on optional memory expansion board. One bank of DRAM refers to four pieces of SIMM modules. The maximum memory size is 16MB when using 1MB DRAM for all banks.

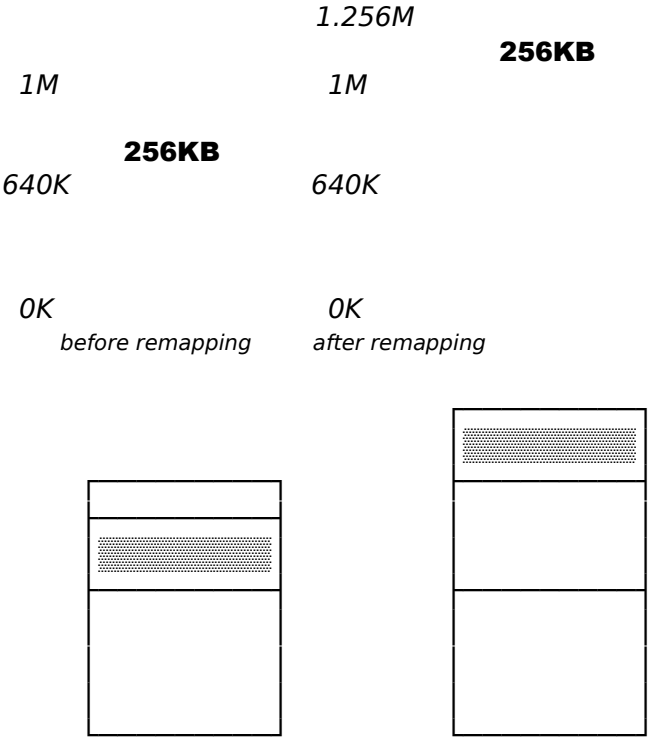
The memory system provides a flexible memory configuration. 256KB and 1MB DRAM can be used together. Several combinations of DRAM types are allowed. So, a basic system is equipped with 1MB using 256KB DRAM and then memory size is increased to 5MB by putting another bank of 1MB DRAM. In general, the 8MB on-board memory will be sufficient for most applications. The use of memory expansion board may not be necessary.

The memory system supports page-interleaved mode. The memory is divided into pages. Successive memory accesses within the same page need not require wait state and thus CPU can run at full speed. When more than one bank of memory are installed, the page size is effectively increased because several banks of memory can be kept active. If four banks are filled, the page size is increased by a factor of four.

To enhance the system performance, shadow RAM mode is supported. In shadow RAM mode, system BIOS and video BIOS contained in low speed memory such as EPROM and ROM are copied into DRAM. Improvement is significant because access to DRAM is much faster than ROM.

Another useful feature is memory remapping. 640K bytes is allocated as base memory. On the other hand, system BIOS and video BIOS occupy some locations between 640K and 1M. When 1M bytes or more are installed, there are some portions of DRAM overlapping with the BIOS which cannot be accessed. Memory remapping allows these portion of memory to be

accessed at other locations and thus can be utilized by the software. Memory remapping is supported by hardware and can be enabled in system setup.

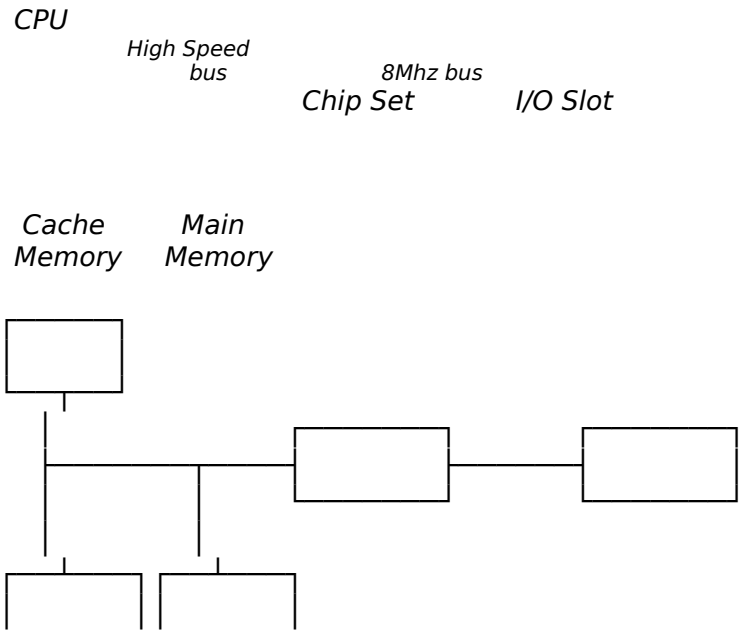


Memory remapping

DUAL BUS DESIGN

It is very important that a high speed system should be compatible with existing peripherals without lowering the performance. To be compatible, the I/O slot should run at 8MHz or slower. On the other hand, the rest of the system are running at full speed.

A dual bus design is employed. A high speed bus links the CPU, coprocessor, cache memory and main memory. This bus is synchronous with clock of the CPU and the data transfer is 32 bits. Whenever there is a request for transferring to or from I/O slot, the chipset is responsible for handling the conversion between the buses. The clock rate of the high speed bus will not be reduced, which eliminates many compatibility problem.



SYSTEM FUNCTIONS

System functions include:

- Interrupt
- DMA
- Timer
- Real time clock
- Clock and ready generation
- I/O channel control

All system functions are 100% compatible to AT standard. I/O channel of OCTEK Pointer-386 is designed to be compatible with standard AT bus. All the expansion cards conformed to the standard AT bus can be used in OCTEK Pointer-386 without problem.

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Chapter 3
Installing Components

Important Note : Turn off the power before installing or replacing any component.

INSTALLING MATH COPROCESSOR

Math coprocessor 80387 and WEITEK 3167 are PGA devices. Beside the CPU, there is a 121-pin PGA socket. To install Math coprocessor, be sure to line up pin 1 of the Math coprocessor with pin 1 of the socket as shown below. Make sure that the coprocessor is firmly inserted into the socket.

The WEITEK 3167 is a 121-pin chip which matches the pin count of the socket. Align the pins and gently insert the chip into the socket. However, 80387 has 69 pins and its package is smaller and different from WEITEK 3167. So, it only occupies the inner pins of the socket.

Before installing the Math coprocessor, make sure all the pins are straight. The pins are very fragile. Once these pins are bent, the coprocessor may be damaged.

Check whether the system BIOS can find the coprocessor after reset. The system BIOS will display a list of devices on the motherboard after self-test. If the coprocessor is installed, it should show the type of coprocessor.

INSTALLING RAM MODULES

OCTEK Pointer-386 has eight sockets for SIMM modules. Whenever adding memory modules to the motherboard, install four modules at the same time. Also make sure that the chips on the modules face toward the memory expansion slot as shown in next page.

To install a module, the module edge is angled into the socket's contact and then the module is pivoted into position, where the locking latches will secure it. If the module edge is not completely inserted into the socket, it cannot be pivoted to be in vertical position and should be dragged out and inserted again. Do not force the module into the SIMM socket. It will damage the locking latches.

The modules should be locked by the locking latches of the sockets firmly. Please check carefully before turning on the power. Otherwise, the system will not work properly.

If the BIOS reports an memory error or parity error, drag out the modules and insert them again. If the locking latches are damaged, contact your dealer to replace the socket.

INSTALLING EXTERNAL BATTERY

To back up the information stored in CMOS RAM, an external battery is needed to provide power after the system is turned off. The connector (P8) for the battery is located beside the keyboard connector on the rear of the board. Use a 3.6V battery. Turn off the power before install the battery. The location of the connector P8 is shown below.

CONFIGURATION OF MEMORY

The configuration of the memory is very flexible. Either 256KB or 1MB SIMM modules are acceptable. There are several combinations of DRAM types you may consider. So, a basic system can be equipped with fewer memory and later more memory can be installed when upgrading the system. The different configurations of memory is illustrated on next page.

There are totally four banks of DRAM. Two banks (bank 0 and 1) are on the motherboard and the others (bank 2 and 3) are on the memory expansion board. If bank 0 and 1 are filled, you have to use bank 2 and 3.

Page mode is always active. Interleaved mode is only enabled for those banks with similar pairs or quartet of DRAMs. The performance is automatically improved whenever the interleaved mode is active.

The memory size is detected automatically by system BIOS and indicated during memory test after reset. No jumper is needed to be set for the memory size and DRAM type.

To determine what DRAM speed rating should be used depends on the system speed and wait state. The highest performance is accomplished by using zero wait state, but high speed DRAM has to be used. If zero wait state is selected, fast page mode DRAM is needed.

The wait state setting is applied to four banks of memory. Therefore make sure to install DRAM modules with the same speed rating, or accommodate the wait state setting to the new DRAM type.

Because of the shadow RAM and memory remapping feature, the memory size may not equal to the actual memory size. Suppose that there is 1MB on board. If memory remapping is disabled, the BIOS will show the memory size is 640KB. After enabled, the memory size is increased to 896KB. The rest of the memory (128KB) is assigned for shadow RAM and can not be used by software.

The number of wait state is assigned in the BIOS setup. Improper setting may make the system malfunction. In this case, reset the CMOS setup using JP11. Then reset the system and go through the system setup again.

DRAM CONFIGURATION

	Bank 0	Bank 1	Bank 2	Bank 3	Total Memory	Inter-leaved
1	0	0	0	0	0	
2	256K	0	0	0	1M	2W
3	256K	256K	0	0	2M	2W
4	256K	256K	256K	0	3M	
5	256K	256K	256K	256K	4M	4W
6	1M	0	0	0	4M	
7	256K	1M	0	0	5M	
8	1M	256K	0	0	5M	
9	256K	256K	1M	0	6M	2W
10	256K	1M	256K	0	6M	
11	1M	256K	256K	0	6M	
12	256K	256K	1M	256K	7M	2W
13	256K	1M	256K	256K	7M	2W
14	1M	256K	256K	256K	7M	2W
15	1M	1M	0	0	8M	2W
16	256K	1M	1M	0	9M	
17	1M	1M	256K	0	9M	2W
18	1M	256K	1M	0	9M	
19	256K	256K	1M	1M	10M	2W
20	256K	1M	1M	256K	10M	
21	1M	1M	256K	256K	10M	2W
22	1M	256K	1M	256K	10M	
23	1M	1M	1M	0	12M	2W

24	256K	1M	1M	1M	13M	2W
25	1M	1M	1M	256K	13M	2W
26	1M	256K	1M	1M	13M	2W
27	1M	1M	1M	1M	16M	4W

CONFIGURATION OF CACHE MEMORY

Note : If you have any question about the configuration of cache memory, consult your local dealer. Improper configuration will cause the system malfunction.

The cache memory is either 32K or 64K bytes. 32K bytes is sufficient for general applications and the performance is improved when the size is increased to 64K bytes.

32K bytes cache memory requires four SRAMs (U3, U5, U7, U9) and another tag RAM (16Kx1) should be installed on U16 and JP3 is set to 1-2. The speed rating of U16 must be equal to the tag RAM on U14 and U15. 32K byte cache memory can only buffer 8M byte main memory. 64K bytes cache memory requires all eight SRAMs (U3 to U10). When the cacheable memory size is 8MB, U16 is not needed and JP3 has no jumper. When the main memory on board exceeds 8M bytes, U16 is needed. Up to 16M bytes can be buffered with this configuration.

Make sure that the number of SRAMs is correct and they are installed properly. Otherwise the system will not work.

There are several jumpers to setup the cache memory. JP1, 2 and 3 are used to define the cache memory size. JP3 is only used when U16 is installed.

JP 4 and 5 are used to setup the line size. Line size is the number of bytes which will be fetched from the main memory to the cache memory at one time when a cache read miss occurs. A burst mode read mechanism is implemented in the memory controller so as to minimize the overhead of reading multiple bytes. The line size is set to 16 bytes by the system BIOS. So the default setting of JP 4 and 5 are set to 16 bytes.

Note that the 256K bytes remapped area may not be included in the cacheable range when the memory is 8M or 16M bytes. When there is 8MB on board and the remapping function is enabled, the actual memory size is 8.256MB, which is over 8MB boundary. In this case, it is recommended to exclude the 256KB remapped area from the cacheable memory, because U16 is not needed. If the 256KB remapped area is set to be cacheable, U16 has to be installed.

When the memory size is 16M bytes, the actual memory size is 16.256M when the remapping function is enabled. The remapped area should not be included in the cacheable range. The setting of the 256KB remapped area is explained in appendix A.

16Kx1 (U16) Speed Rating

System Speed	*SRAM*	*Tag RAM*
25MHz	*35*	*25*
33MHz	*25*	*15*

The location of U16 is shown below.

The jumper settings for the configuration of cache memory.

Cache Memory Size

	32KB	64KB
JP1	1-2	2-3
JP2	2-3	1-2
JP3	1-2	2-3

Line Size

	4 bytes	8 bytes	16 bytes
JP4	1-2	1-2	2-3
JP5	1-2	2-3	2-3

CONTROL OF SYSTEM SPEED

System Speed can be controlled by hardware switch and keyboard. Connector P3 is connected to the turbo switch of the case. When the system speed is fast, the turbo LED of the case should be turned on.

To change the speed by keyboard, use '-' and '+' of the numeric keypad. Press 'Ctrl', 'Alt' and '-' for slow speed and Press 'Ctrl', 'Alt' and '+' for fast speed.

Whenever the system speed is set to slow by turbo switch, it cannot be changed by keyboard, and vice versa.

RESET CMOS SETUP INFORMATION

Sometimes, the improper setting of system setup may make the system malfunction. In this case, turn off the power and disconnect the external battery. Then place a jumper on JP11 for a while. The internal CMOS status register will be cleared. Then remove the jumper and turn on the power. The BIOS finds the CMOS status register is reset and regards the setup information as invalid. So it will prompt you to correct the information.

SYSTEM BOARD JUMPER SETTING

There are several options which allow user to select by hardware switches.

ROM Size

JP6	
1-2	27512
2-3	27256 *

Display Selection

JP10	
1-2	CGA, EGA, VGA
2-3	Monochrome display *

Note : * factory setting

JP7, JP8 and JP9 are reserved Jumpers.

JP7	JP8	JP9
1-2	1-2	2-3

SYSTEM BOARD CONNECTORS

Under typical conditions, these connectors should be connected to the indicators and switches of the

system unit.

Connector	*Function*
P1	*Hardware reset connector*
P2	*Speaker connector*
P3	*Turbo switch connector*
P4	*Turbo LED connector*
P5	*Power LED & Ext-Lock connector*
P6, P7	*Power supply connector*
P8	*External battery connector*
KB1	*Keyboard connector*

Pin assignments of the connectors are illustrated as follows:

P 1 - Hardware Reset Connector

Pin	*Assignment*
1	*Selection Pin*
2	*Ground*

P 2 - Speaker Connector

Pin	Assignment
1	Data out
2	+5 Vdc
3	Ground
4	+5 Vdc

P 3 - Turbo Switch Connector

Pin	Assignment
1	Selection Pin
2	Ground

P 4 - Turbo LED Connector

Pin	Assignment
1	+5 Vdc
2	LED signal

P 5 - Power LED & Ext-Lock Connector

Pin	*Assignment*
1	*+5 Vdc*
2	*Key*
3	*Ground*
4	*Keyboard inhibit*
5	*Ground*

P6,P7 - Power Supply Connector

Pin	*Assignment*
1	*POWERGOOD*
2	*+5 Vdc*
3	*+12 Vdc*
4	*-12 Vdc*
5	*Ground*
6	*Ground*

Pin	*Assignment*
1	*Ground*
2	*Ground*
3	*-5 Vdc*
4	*+5 Vdc*
5	*+5 Vdc*
6	*+5 Vdc*

P 8 - External Battery Connector

Pin	Assignment
1	+ Vdc
2	not used
3	Ground
4	Ground

KB 1 - Keyboard Connector

Pin	Assignment
1	Keyboard clock
2	Keyboard data
3	Spare
4	Ground
5	+5 Vdc

Chapter 4
Technical Information

This section provides technical information about OCTEK Pointer-386 and is intended for advanced users interested in the basic design and operation of OCTEK Pointer-386.

MEMORY MAPPING

Address	*Range*	*Function*
000000-7FFFFF	*000K-512K*	*System Board Memory (512K)*
080000-09FFFF	*512K-640K*	*System Board Memory (128K)*
0A0000-0BFFFF	*640K-768K*	*Display Buffer (128K)*
0C0000-0DFFFF	*768K-896K*	*Adaptor ROM / Shadow RAM (128K)*
0E0000-0EFFFF	*896K-960K*	*System ROM / Shadow RAM (64K)*
0F0000-0FFFFF	*960K-1024K*	*System BIOS ROM / Shadow RAM (64K)*
100000-7FFFFF	*1024K-8192K*	*System Memory*
800000-FFFFFF	*8192K-16318K*	*System Memory*

I/O ADDRESS MAP

I/O Address Map on System Board

I/O address hex 000 to 0FF are reserved for the system board I/O.

ADDRESS (HEX)	DEVICE
000-01F	DMA Controller 1, 8237
020-03F	Interrupt Controller 1, 8259, Master
040-05F	Timer, 8254
060-06F	Keyboard Controller
070-07F	Real Time Clock, NMI (non-maskable interrupt) mask
080-09F	DMA Page Register, 74LS612
0A0-0BF	Interrupt Controller 2, 8259
0C0-0DF	DMA Controller 2, 8237
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor Port

I/O address hex 100 to 3FF are available on the I/O channel.

ADDRESS (HEX)	DEVICE
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2
2F8-2FF	Serial Port 2
300-31F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	SDLC, bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome Display and Printer Adapter
3C0-3CF	Reserved
3D0-3DF	Color Graphics Monitor Adapter
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1

SYSTEM TIMERS

OCTEK Pointer-386 has three programmable timer/counters controlled by 82C206 and they are defined as channels 0 through 2:

Channel 0	*System Timer*
Gate 0	*Tied on*
Clk in 0	*1.190 Mhz OSC*
Clk out 0	*8259 IRQ 0*

Channel 1	*Refresh Request Generator*
Gate 1	*Tied on*
Clk in 1	*1.190 Mhz OSC*
Clk out 1	*Request Refresh Cycle*

Channel 2	*Tone Generation of Speaker*
Gate 2	*Controlled by bit 0 of port hex 61 PPI bit*
Clk in 2	*1.190 Mhz OSC*
Clk out 2	*Used to drive the speaker*

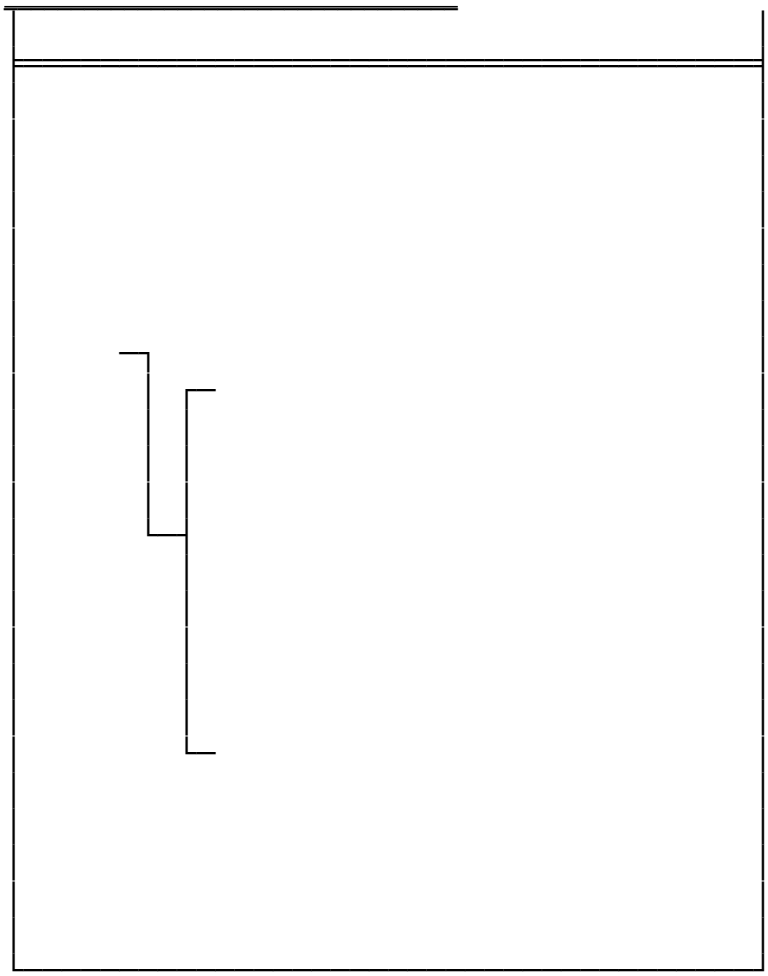
Note : Channel 1 is programmed to generate a 15-micro-second period signal.

The 8254 Timer/Counters are treated by system programs as an arrangement of four programmable external I/O ports. Three are treated as counters and the fourth is a control register for mode programming.

SYSTEM INTERRUPTS

Sixteen levels of system interrupts are provided on OCTEK Pointer-386. The following shows the interrupt-level assignments in decreasing priority.

Level		Function
Microprocessor NMI		*Parity or I/O Channel Check*
Interrupt Controllers		
CTLR 1	*CTLR 2*	
IRQ0		*Timer Output 0*
IRQ1		*Keyboard (Output Buffer Full)*
IRQ2		*Interrupt from CTLR 2*
	IRQ8	*Real-time Clock Interrupt*
	IRQ9	*Software Redirected to INT 0AH (IRQ2)*
	IRQ10	*Reserved*
	IRQ11	*Reserved*
	IRQ12	*Reserved*
	IRQ13	*Coprocessor*
	IRQ14	*Fixed Disk Controller*
	IRQ15	*Reserved*
IRQ3		*Serial Port 2*
IRQ4		*Serial Port 1*
IRQ5		*Parallel Port 2*
IRQ6		*Diskette Controller*
IRQ7		*Parallel Port 1*



DIRECT MEMORY ACCESS (DMA)

OCTEK Pointer-386 supports seven DMA channels.

Channel	*Function*
0	*Spare (8 bit transfer)*
1	*SDLC (8 bit transfer)*
2	*Floppy Disk (8 bit transfer)*
3	*Spare (8 bit transfer)*
4	*Cascade for DMA Controller 1*
5	*Spare (16 bit transfer)*
6	*Spare (16 bit transfer)*
7	*Spare (16 bit transfer)*

The following shows the addresses for the page register.

Page Register	*I/O Address (HEX)*
DMA Channel 0	*0087*
DMA Channel 1	*0083*
DMA Channel 2	*0081*
DMA Channel 3	*0082*
DMA Channel 5	*008B*
DMA Channel 6	*0089*
DMA Channel 7	*008A*
Refresh	*008F*

REAL TIME CLOCK AND CMOS RAM

Real time clock and CMOS RAM are contained on board. Real time clock provides the system date and time. CMOS RAM stores system information. Both are backed up by battery and will not lose information after power off. The following page shows the CMOS RAM Address Map.

CMOS RAM ADDRESS MAP

Addresses	Description
00-0D	* Real-time clock information
0E	* Diagnostic status byte
0F	* Shutdown status byte
10	Diskette drive type byte - drives A and B
11	Reserved
12	Fixed disk type byte - drives C and D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	* Low expansion memory byte
31	* High expansion memory byte
32	* Date century byte
33	* Information flags (set during power on)
34-3F	Reserved

REAL TIME CLOCK INFORMATION

The following table describes real-time clock bytes and specifies their addresses.

Byte	*Function*	*Address*
0	*Seconds*	*00*
1	*Second alarm*	*01*
2	*Minutes*	*02*
3	*Minute alarm*	*03*
4	*Hours*	*04*
5	*Hour alarm*	*05*
6	*Day of week*	*06*
7	*Date of month*	*07*
8	*Month*	*08*
9	*Year*	*09*
10	*Status Register A*	*0A*
11	*Status Register B*	*0B*
12	*Status Register C*	*0C*
13	*Status Register D*	*0D*

SYSTEM EXPANSION BUS

OCTEK Pointer-386 provides eight 16-bit slots.

The I/O channel supports:

* *I/O address space from hex 100 to hex 3FF*
* *Selection of data access (either 8 or 16 bit)*
* *24 bit memory addresses (16MB)*
* *Interrupts*
* *DMA channels*
* *Memory refresh signal*

The following figure shows the pin numbering for I/O channel connectors J3 to J10.

The following figure shows the pin numbering for I/O channel connectors J13-J20.

The following tables summarize pin assignments for the I/O channel connectors.

I/O Channel (A-Side)

I/O Pin	*Signal Name*	*I/O*
A1	*-I/O CH CK*	*I*
A2	*SD7*	*I/O*
A3	*SD6*	*I/O*
A4	*SD5*	*I/O*
A5	*SD4*	*I/O*
A6	*SD3*	*I/O*
A7	*SD2*	*I/O*
A8	*SD1*	*I/O*
A9	*SD0*	*I/O*
A10	*-I/O CH RDY*	*I*
A11	*AEN*	*O*
A12	*SA19*	*I/O*
A13	*SA18*	*I/O*
A14	*SA17*	*I/O*
A15	*SA16*	*I/O*
A16	*SA15*	*I/O*
A17	*SA14*	*I/O*
A18	*SA13*	*I/O*
A19	*SA12*	*I/O*
A20	*SA11*	*I/O*
A21	*SA10*	*I/O*
A22	*SA9*	*I/O*
A23	*SA8*	*I/O*

A24	SA7	I/O
A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

I/O Channel (B-Side)

I/O Pin	Signal Name	I/O
B1	GND	Ground
B2	RESET DRV	I
B3	+5 Vdc	Power
B4	IRQ9	I
B5	-5 Vdc	Power
B6	DRQ2	I
B7	-12 Vdc	Power
B8	0WS	I
B9	+12 Vdc	Power
B10	GND	Ground
B11	-SMEMW	O
B12	-SMEMR	O
B13	-IOW	I/O
B14	-IOR	I/O
B15	-DACK3	I
B16	DRQ3	O
B17	-DACK1	I
B18	DRQ1	O
B19	-Refresh	I/O
B20	CLK	O
B21	IRQ7	I
B22	IRQ6	I
B23	IRQ5	I
B24	IRQ4	I
B25	IRQ3	I

B26	-DACK2	O
B27	T/C	O
B28	BALE	O
B29	+5 Vdc	Power
B30	OSC	O
B31	GND	GROUND

I/O Channel (C-Side)

I/O Pin	*Signal Name*	*I/O*
C1	*SBHE*	*I/O*
C2	*LA23*	*I/O*
C3	*LA22*	*I/O*
C4	*LA21*	*I/O*
C5	*LA20*	*I/O*
C6	*LA19*	*I/O*
C7	*LA18*	*I/O*
C8	*LA17*	*I/O*
C9	*-MEMR*	*I/O*
C10	*-MEMW*	*I/O*
C11	*SD8*	*I/O*
C12	*SD9*	*I/O*
C13	*SD10*	*I/O*
C14	*SD11*	*I/O*
C15	*SD12*	*I/O*
C16	*SD13*	*I/O*
C17	*SD14*	*I/O*
C18	*SD15*	*I/O*

I/O Channel (D-Side)

I/O Pin	Signal Name	I/O
D1	-MEM CS16	I
D2	-I/O CS16	I
D3	IRQ10	I
D4	IRQ11	I
D5	IRQ12	I
D6	IRQ15	I
D7	IRQ14	I
D8	-DACK0	O
D9	DRQ0	I
D10	-DACK5	O
D11	DRQ5	I
D12	-DACK6	O
D13	DRQ6	I
D14	-DACK7	O
D15	DRQ7	I
D16	+5 Vdc	Power
D17	-MASTER	I
D18	GND	Ground

THIS IS INTENTIONALLY LEFT BLANK

Appendix A
System BIOS

The system BIOS provides an interface for operating systems and applications to access hardware. It is fully compatible with standard AT BIOS and works in the network system. It also performs self-test after reset and includes a setup program to setup the system.

SELF-TEST

To ensure the computer hardware is functional, the system BIOS will carry out a self-test upon reset. The test is very intensive and covers all parts of hardware. It takes a while before some messages are shown on the screen. It does not mean that the system is not working when the screen is blank. So wait for a while after turning on the power and listen carefully to the speaker. Some errors are reported by a number of beep sounds. After completing the self-test, the BIOS will display some messages on the screen.

Unlike most of the tests which take a short time, the memory test may be very slow, especially when the memory size is large. Therefore the system BIOS allows you to bypass the memory test by pressing 'ESC'. The following message will be shown during memory test:

Press <ESC> Key to bypass MEMORY test

It is recommended to complete the memory test. The total memory size is displayed after the memory test.

In case of serious errors, the BIOS will suspend the test. If the display is not initialized, the BIOS will report the error through a sequence of beep sounds. Otherwise, error message will be shown on the screen.

There are two types of errors reported by beep sounds. One is conveyed as one long beep followed by a number of short beeps. The meanings of the errors are as below :-

Short Beep Count	*Meaning*
3	*Memory Failure*
8	*Display Adapter Failure*

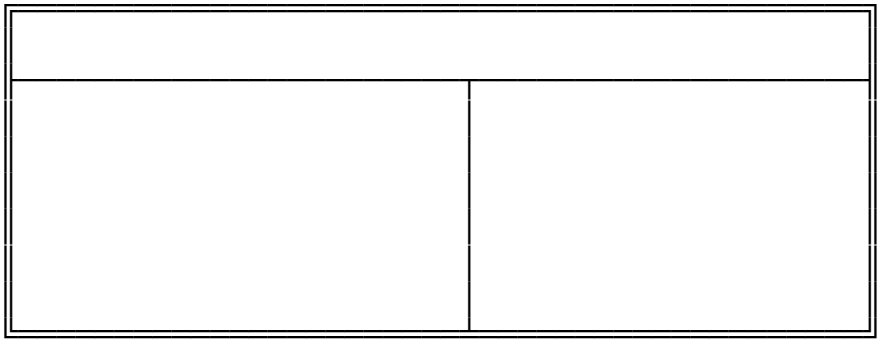
The other type of errors are serious failure and are conveyed as a number of beep and repeated infinitely.

Beep Count	*Meaning*
1	*DRAM Refresh Failure*
3	*Base 64K Byte Memory Failure*
4	*System Timer Failure*
5	*Processor Failure*
6	*Keyboard Controller - Gate A20 Failure*
7	*Virtual Mode Exception Error*
9	*ROM-BIOS Checksum Failure*

If no error is found during self-test, the system BIOS will proceed to boot from floppy disk or hard disk. The system BIOS will list the system configuration on the screen as below.

System Configuration (C) Copyright 1985-1990, American Megatrends Inc.,

Main Processor	:	80386	Base Memory Size	:	640 KB
Numeric Processor	:	None	Ext. Memory Size	:	7424 KB
Floppy Drive A:	:	1.2 MB, 5¼"	Hard Disk C: Type	:	2
Floppy Drive B:	:	1.44MB, 3½"	Hard Disk D: Type	:	None
Display Type	:	VGA or EGA	Serial Port(s)	:	None
ROM-BIOS Date	:	04/30/90	Parallel Port(s)	:	3BC



Do check the list to make sure that the configuration is correct. Sometimes, problems arise because of the incorrect information of the configuration. For example, if you forget to modify the setup after changing the floppy disk drive from one type to another, it can not boot from floppy disk or may not work properly. If you check the list, you can find the cause of the problem.

SYSTEM SETUP

The BIOS incorporates two setup sections:

(1) CMOS SETUP
(2) EXTENDED SETUP PROGRAM

It is important that all the setup procedures should be completed before operating the system. Otherwise, the system will not run properly with the incorrect setup information. Run the setup again if the configuration is changed.

To enter the setup section, press 'Del' when the following message is shown:

Press <Del> if you want to run SETUP/EXTD-SET

Whenever the system BIOS finds that the configuration of the system is altered, error message will be shown and you may press 'F1' to run setup. Then the following messages are shown on the screen.

EXIT FOR BOOT
RUN CMOS SETUP
RUN XCMOS SETUP

In CMOS SETUP section, you can enter system configuration information which will be stored in CMOS RAM on the motherboard. The information includes the devices of the system as well as memory size.

XCMOS SETUP (EXTENDED SETUP PROGRAM) allows you to modify the registers of the chipsets. These registers are programmed with default settings by the BIOS. You may change the settings to improve the system performance or to suit the system configuration. Improper settings of the registers may cause the system malfunction. Consult your dealer if you have any doubt.

(1) CMOS SETUP

The memory size and the numeric processor are detected by the BIOS. So you are only required to set those options on the left side of the screen. The system configuration information are shown as follows:

CMOS SETUP (C) Copyright 1985-1990, American Megatrends Inc.,

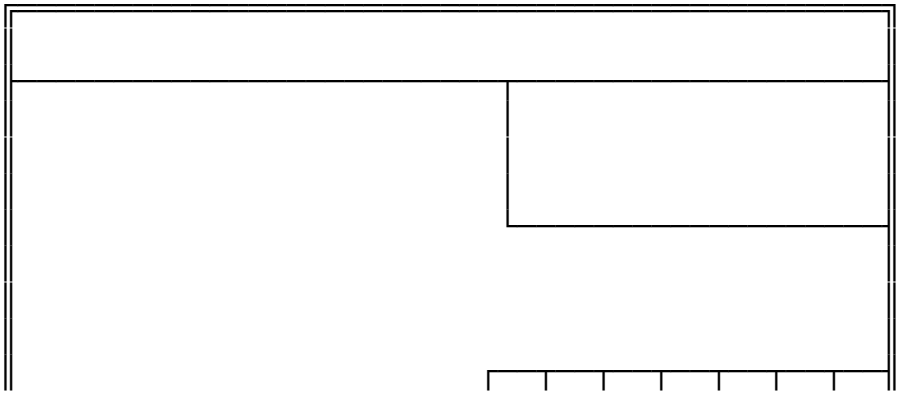
Date (mn/date/year)	*:*	*Sun, Jul 01, 1990*	*Base memory size*	*: 640 KB*
Time (hour/min/sec)	*:*	*12 : 05 : 30*	*Ext. memory size*	*: 7424 KB*
Floppy Drive A:	*:*	*1.2 MB, 5¼"*	*Numeric Processor:*	*None*
Floppy Drive B:	*:*	*1.44 MB, 3½"*		

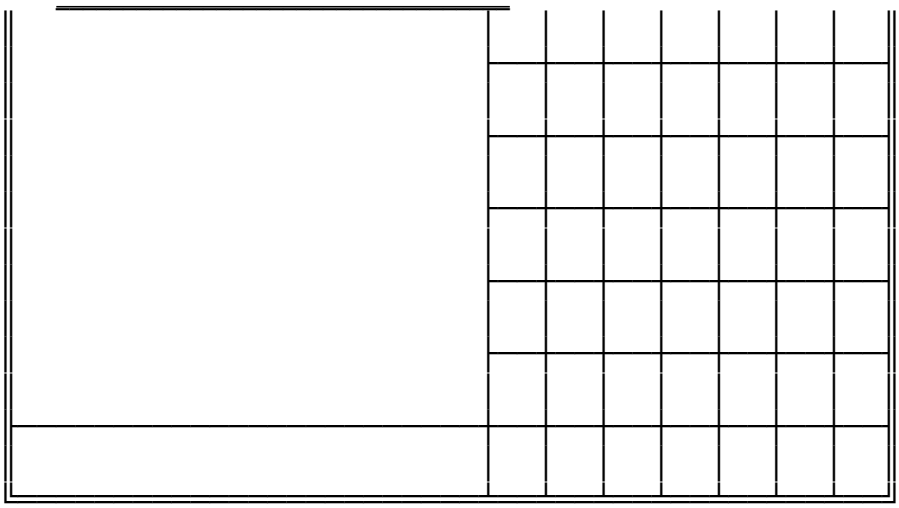
			Cyln	*Head*	*WPcom*	*LZone*	*Sect*	*Size*
Hard Disk C: type	*:*	*Not Installed*						
Hard Disk D: type	*:*	*Not Installed*						
Primary Display	*:*	*VGA or EGA*						
Keyboard	*:*	*Installed*						
Video BIOS Shadow	*:*	*Disabled*						
Scratch RAM Option	*:*	*1*						
Main BIOS Shadow	*:*	*Enabled*						
Memory Relocation	*:*	*Enabled*						
Cache Memory	*:*	*Enabled*						

Sun	*Mon*	*Tue*	*Wed*	*Thu*	*Fri*	*Sat*
1	*2*	*3*	*4*	*5*	*6*	*7*
8	*9*	*10*	*11*	*12*	*13*	*14*
15	*16*	*17*	*18*	*19*	*20*	*21*
22	*23*	*24*	*25*	*26*	*27*	*28*
31						
2099	*29*	*30*	*31*	*1*	*2*	*3*
4	*5*	*6*	*7*	*8*	*9*	*10*
11						

Month	*:*	*Jan, Feb, ... Dec*
Date	*:*	*01, 02, 03, ...*
Year	*:*	*1901, 1902, ...*

ESC=Exit,↓→↑←=Select,PgUp/PgDn=Modify





OPTION 1 TIME AND DATE

Use PgUp and PgDn keys to change the value. The date and time cannot be entered directly. An calender is displayed on the lower right corner of the screen for your reference.

OPTION 2 FLOPPY DISK DRIVE

Four types of floppy disk drives are supported:

1. *5-¼ inch standard drive (360K)*
2. *5-¼ inch high-density drive (1.2M)*
3. *3-½ inch standard drive (720K)*
4. *3-½ inch high-density drive (1.44M)*

The system BIOS supports two floppy disk drives and they are recognized as drive A and B. Select the correct types. Otherwise the drives cannot work properly. If one of them is not installed, select 'Not Installed' for that drive.

The BIOS is able to detect the type of the drives automatically. But remember to check the settings before exit.

OPTION 3 FIXED DISK DRIVE

There are 47 types of fixed disks supported by the BIOS. Consult your fixed disk manual to determine its correct type. The parameters such as cylinder number, head number, sector number and pre-compensation must match your fixed disk's parameters.

Use PgUp and PgDn keys to change the fixed disk type. If the type of your fixed disk is not included in the hard disk list, define a new type as type 47. Use left and right arrow keys to move between the parameter fields and enter the parameters. The parameters will be stored in the CMOS RAM and your fixed disk can be used afterwards. Each hard disk can be assigned a different type 47 hard disk. So two hard disks which are not included in the list can be used together in your system.

If the type of fixed disk is wrong, it takes a while before the BIOS can identify the error. After setting the fixed disk type, if the system halts after reboot, please wait for a while. It is most likely that the setting of fixed disk type is incorrect.

When you install a new hard disk, make sure whether it is already formatted. If not, the BIOS has to check for a while before reporting the hard disk error. In fact, the error arises only because the hard disk is not formatted. If the hard disk is formatted, you can run DOS FDISK and DOS FORMAT.

Some fixed disks are specially handled and must be set to 'Not Installed'. Consult the fixed disk manual for details.

OPTION 4 DISPLAY

Four types of display are supported:

1. *CGA 80 column mode*
2. *CGA 40 column mode*
3. *EGA and VGA*
4. *Monochrome*

If the type of display is incorrect, the BIOS will prompt you and ask you to set up again. But the BIOS is still able to display messages on the display attached to the system. Thus you can enter the setup program.

The jumper JP10 must be set according to this setting. Otherwise, the BIOS will report error after self-test.

OPTION 5 KEYBOARD

If a keyboard is attached to the system, select 'Installed'. The BIOS will test the keyboard during self-test.

OPTION 6 VIDEO BIOS SHADOW

If enabled, the content of the video BIOS is copied to the on board memory and thus the operation of the video BIOS is speeded up. This feature is useful for VGA BIOS because it does not occupy the main memory space.

OPTION 7 SCRATCH RAM OPTION

The BIOS may require memory storage for certain functions and the storage can be allocated in two ways. One way is to use the BIOS stack and another is to allocate a 1K bytes memory in the base memory. Generally, the former option is appropriate. If the hard disk type 47 is defined or if you run program like OS/2 which will use 80386DX instruction, select the option 2.

OPTION 8 MAIN BIOS SHADOW

If enabled, the content of the system BIOS is copied to the on board memory and thus the operation of the system BIOS is speeded up.

OPTION 9 MEMORY RELOCATION

Of the on board memory, 640K bytes are allocated for main memory and 128K bytes are assigned for shadow RAM function. So, there will be 256K bytes left below 1M bytes. If this option is enabled, this part of memory can be used by applications but will be accessed at other location. If disabled, this memory area cannot be used.

OPTION 10 CACHE MEMORY

The cache controller is incorporated in the chipset and can be enabled or disabled. If disabled, the performance will be very low.

(2) EXTENDED SETUP PROGRAM

All the registers of the chipsets are set to default values by the system BIOS. Usually, there is no need to modify these registers unless the configuration is changed. Since improper settings of these registers may cause the system malfunction, check your settings carefully before exit.

In EXTENDED SETUP PROGRAM, the main menu is shown as below:

EASY SETUP OPTI CHIPSET
ADVANCED SETUP OPTI CHIPSET
WRITE CMOS REGISTERS AND EXIT
DO NOT WRITE CMOS REGISTERS AND EXIT

Select 'Write CMOS register and exit' to save the new settings in the CMOS RAM. The BIOS will then reboot the system and the new settings are in effect afterwards.

After changing the registers' settings, test your system first to make sure that the settings are correct. It is possible that your system becomes unstable and you need to setup the registers again.

There are two ways to program the registers: advanced setup and easy setup. Advanced setup is more complicated and you have to program the registers bit by bit. In easy setup, the system BIOS allows you to modify some registers which are likely to be changed if system configuration is modified.

EASY SETUP OPTI CHIPSET

In most cases, the easy setup is adequate and also is simple to use. There are four groups of selections:

(1) OPTi Clock Selection
(2) OPTi Wait State Setting
(3) OPTi Fast Gate A20 Control
(4) OPTi Cache Configuration Setting

In this section, you simply use the up and down arrow keys to move between options and press 'Enter' to select. The BIOS will set the registers accordingly.

(1) OPTi Clock Selection

CPU Clock Selection

When set to CLKIN, the CPU will run at 33MHz for 66MHz oscillator or 25MHz for 50MHz oscillator. If ICLK is selected, the CPU will run at low speed equal to ICLK.

ICLK Clock Selection

ICLK is used by peripherals on the motherboard and slots, such as display and DMA. If normal speed mode is enabled, the CPU will also use ICLK clock. ICLK is generated from CLKIN and the speed of ICLK is shown below.

	CPU Speed	
ICLK	33 Mhz	25 Mhz
CLKIN/4	8.25	6.25
CLKIN/3	11.00	8.33
CLKIN/2	16.50	12.50

The system performance can be improved by selecting a higher ICLK speed. To be compatible with general add-on cards, the ICLK must be 8.33 Mhz or less. There are many old version add-on cards that can only run at the slow speed. So, be careful when you want to set to higher speed.

ATCLK Stretch Enable/Disable

It is a special feature to improve the system performance by speeding up I/O slot operation. When ATCLK Stretcg enables, the performance is further improved. However, test your configuration before permanently enabling this feature. Some add-on cards may not take advantages of this feature and you need to disable this feature.

(2) OPTi Wait State Setting

The number of wait state for memory read and write operations depends on the clock speed of CPU and the speed rating of the DRAM. The following table shows the recommended speed ratings. To ensure the stability of the system, select DRAM equivalent to or better than these ratings.

	Number of	*wait state*
CPU speed	*1*	*0*
25 Mhz	*100ns*	*70ns*

	Number of	*wait state*
CPU speed	*2*	*1*
33 Mhz	*100ns*	*70ns*

Check carefully whether your DRAM is suitable for the number of wait states you want to select. Improper setting can make the system unstable. The DRAM timing is tight at 33Mhz or at zero wait state. Since the specification of DRAM from different manufacturers may vary, you would better consult your local dealer for the detail information.

(3) OPTi Fast Gate A20 Control

The control signal GATE A20 is a special signal for protected mode operation and is usually generated by external logic. Fast gate A20 control is a feature to toggle this signal without delay.

In this section, the status of fast gate A20 control can be set to a default statue after power up. Some applications using protected mode will need the fast gate A20 control to be enabled. One of the application is Windows 3.0. If you find that some other applications are working intermittently, try enable it and check whether the problem is solved.

Please note that this feature is not a standard feature in PC AT design. So make sure that your applications work fine with this feature enabled before permanently setting to 'enable'.

(4) OPTi Cache Controller Setting

There are two selections:

256KB Remaped Area Cached Enabled/Disabled
Cacheable Address Range

256K Remaped Area Cached Enable/Disable

The 256KB remaped area is treated differently by the chipset's cache controller. If the 256KB remaped feature is enabled, the remaped area is located at a new address. Select 'enable' to inform the cache controller to include this area in the cacheable area. Refer to chapter 3 for the detail information.

Cacheable Address Range

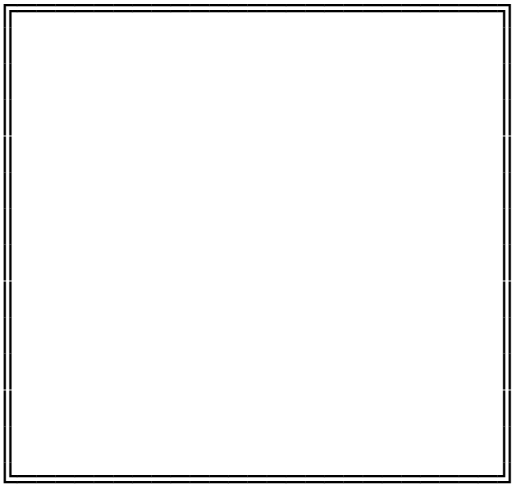
Cacheable address range should be equal to the total memory size on board. Remember to modify this setting whenever the memory size is altered. If some portions of memory are not included in the cacheable address range, you may not notice the difference of performance, but the system is indeed running slower.

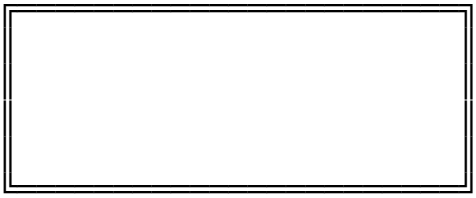
ADVANCED SETUP OPTi CHIPSET

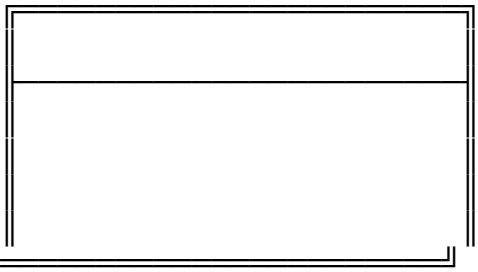
In this setup section, a setup menu is shown as following.

OPTI 386 CACHE EXTD SETUP PROGRAM Ver - 2.0B, (C) 1990, American Megatrends Inc.

BITS 7 - 0
82C381 00H -> 11 R00 00 R Go to Prev/Next Register - ↑ ↓
Go to Prev/Next Entry -
Scroll Bit Value - PgUp/PgDn
82C382D 11H -> R R R R R 0 R R Return to MAIN MENU - <ESC>
14H -> 01 1R R R R R
16H -> R R R R 0 R R R
17H -> 11 1R R R R R CLOCK Select
18H -> 11 1R R R R R
19H -> 11 11 11 11 ATCLK Stretch ENABLE / DISABLE
1AH -> 11 1R R R R R
1BH -> 11 11 11 11
0 -> ATCLK stretch DISABLE
1 -> ATCLK stretch ENABLE







Under normal circumstances, advanced setup is not necessary. In advanced setup, you can directly modify each bits of the registers in the chipset. A comprehensive explanations are provided for your reference.

In advanced setup, use arrow keys to move the cursor between each field. The corresponding explanation is displayed on the right side of the screen. Use PgUp and PgDn keys to change the bit value. Related bits are grouped together.

'0' represents the bit is 0 and '1' represents the bit is 1. 'R' means reserved bit which is not allowed to be changed.

Some of the internal registers of the chipset cannot be accessed in EASY SETUP and can only be modified in ADVANCED SETUP. They will be explained in the following section.

Non-cacheable memory block

The chipset supports two non-cacheable memory blocks. The cache controller will not cache these partitions of memory. You need to define the starting address of the memory block as well as the block size.

The registers 18 and 19 define the first block and the registers 1A and 1B define the second block. The settings of registers 18 and 19 are explained below and these settings are also applied to the register 1A and 1B.

Register 18 defines the size of the non-cacheable memory block 1. The definition of bit 5 to bit 7 is illustrated below. Other bits are reserved.

Bit 7	Bit 6	Bit 5	Size
0	0	0	64K
0	0	1	128K
0	1	0	256K
0	1	1	512K
1	0	0	1M
1	0	1	4M
1	1	0	8M
1	1	1	Disable

When `1 1 1' is selected, the non-cacheable memory block 1 will be disabled.

Register 19 defines the starting address of the non-cacheable memory block. Depending on the setting of register 18, some of the bits may be `Don't care'. The definition of this register is illustrated below. Note that bit 7 stands for A23 and Bit 0 stands for A16.

Block Size	*bit 7 A23*	*bit 6 A22*	*bit 5 A21*	*bit 4 A20*	*bit 3 A19*	*bit 2 A18*	*bit 1 A17*	*bit 0 A16*
64K	*V*	*V*	*V*	*V*	*V*	*V*	*V*	*V*
128K	*V*	*V*	*V*	*V*	*V*	*V*	*V*	*X*
256K	*V*	*V*	*V*	*V*	*V*	*V*	*X*	*X*
512K	*V*	*V*	*V*	*V*	*V*	*X*	*X*	*X*
1M	*V*	*V*	*V*	*V*	*X*	*X*	*X*	*X*
4M	*V*	*V*	*X*	*X*	*X*	*X*	*X*	*X*
8M	*V*	*X*	*X*	*X*	*X*	*X*	*X*	*X*

`X' is `Don't care' bit and `V' is valid bit. For example, if 64K block size is selected in register 18, all bits are considered. But when the block size is 512K, only bit 3 to bit 7 are valid, which means A19 to A23 are considered.

If you want to set the segment 0 A 0 0 0 H to be the block 1, you enter 0 0 0 0 1 0 1 0 to register 19 with 64K block size. When the block size is increased to 256K, the lower two bits are ignored.

Appendix B
Memory Expansion Card

Memory expansion card contains bank 2 and bank 3 of memory. There are 8 SIMM modules on the card and total memory on this card is 8MB. Please refer to Chapter 3 for the configuration of the memory.

After installing the memory card, the system BIOS will determine the type of DRAM and the amount of total memory. There is no need to set any jumper. The system BIOS will prompt you to setup the memory size after re-boot.

However, you should make sure that the memory on the memory expansion board can be used reliably with the current setting of wait state. If there is any problem, increase the number of wait state.

There is a mounting plate on rear of the card. This mounting plate is used to keep the card on the slot firmly. Use a screw to fasten the card to the case.

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Appendix C
Operation and Maintenance

STATIC ELECTRICITY

When installing or removing any add-on card, DRAM module or coprocessor, you should discharge the static electricity on your body. Static electricity is dangerous to electronic device and can build-up on your body. When you touch the add-on card or motherboard, it is likely to damage the device. To discharge the static electricity, touch the metal of your computer. When handling the add-on card, don't contact the components on the cards or their "golden finger". Hold the cards by their edges.

KEEPING THE SYSTEM COOL

The motherboard contains many high-speed components and they will generate heat during operation. Other add-on cards and hard disk drive can also produce a lot of heat. The temperature inside the computer system may be very high. In order to keep the system running stably, the temperature must be kept at a low level. A easy way to do this is to keep the cool air circulating inside the case. The power supply contains a fan to blow air out of the case. If you find that the temperature is still very high, it would be better to install another fan inside the case. Using a larger case is recommended if there are a number of add-on cards and disk drives in the system.

CLEANING THE "GOLDEN FINGER"

Whenever inserting an add-on card to the motherboard, make sure that there is no dirt on the "golden finger" of the add-on card. If not, the contact between the "golden finger" and the slot may be poor and thus the add-on card may not work properly. Use a pencil eraser to clean the "golden finger" if dirt is found.

CLEANIGN THE MOTHERBOARD

The computer system should be kept clean. Dust and dirt is harmful to electronic devices. To prevent dust from accumulating on the mother-board, installing all mounting plates on the rear of the case. Regularly examine your system, and if necessary, vaccum the interior of the system with a miniature vacuum.

Appendix D
Troubleshooting

POOR PERFORMANCE

If the performance of the system becomes very poor after enabling cache memory, it is likely that the jumper setting for the cache memory is incorrect. Refer to CONFIGURATION OF CACHE MEMORY in the Chapter 3 for the description of the related jumper. Note that if U16 is not installed, there should be no jumper on JP3.

MAIN MEMORY ERROR

After power up, the monitor remains blank, and there are beep sounds indicating a main memory failure. In this case, turn off the power and remove all SIMM modules. Carefully place the modules back to the sockets and make sure that all the modules are locked by the locking latches firmly.

In some other cases, the total memory found by the BIOS is different from the actual amount of memory on board. (Note that 128K bytes memory is reserved for the shadow RAM function and will not be counted by the BIOS). It is also a memory failure and you can follow the instruction above.

CACHE MEMORY FAILURE

If the system hangs after memory test, it is likely that the cache memory has some problems. May be some of the SRAMs are damaged or the contact of the IC pins is poor. Try to press the SRAM to make sure that the SRAMs are inserted in the sockets, or examine the SRAM to see whether any pins are bent under or out. If the bent pins are found, remove the SRAM, straighten the pin and place the SRAM again. You may also check the BIOS setup of the cache configuration. If the cache controller is enabled, you should select chipset's cache controller. Otherwise, the system will fail.

IMPROPER SETTING OF WAIT STATE

If the system hangs after memory test, another possible cause is the improper setting of the wait state for memory operation. The number of wait state must match the speed of the DRAM. Reset the CMOS RAM and set up the wait state. Try to increase the number of wait state.

Appendix E
System Board Layout

Appendix F
Memory Expansion Card Layout