EC Declaration of Conformity

We

Iwill Corp.

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Taiwan, R.O.C.

Declare under sole responsibility that the

PIILD motherboard

Meets the intent of Directive 89/336/ECC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the official Journal of the European Communities:

EN 50081-1 Emissions:

EN 55022   Radiated, Class B

EN 55022   Conducted, Class B

EN 60555-2 Power Harmonics

EN 50082-1 Immunity:

IEC   801-2 Electrostatic Discharge

IEC   801-3 RF Radiate

IEC   801-4 Fast Transient

About This Manual

This manual will introduce to the user how this product is consisted. All useful information will be described in later chapters. Keep this manual for your future upgrade or system re-configuration.

Chapter 0 Overview

The features and specifications of this motherboard

Chapter 1 Quick Installation

The quick reference for experienced users

Chapter 2 Hardware Installation

The detailed information on jumper setting, connection, and hardware installation

Chapter 3 System BIOS Setup

The detail information of the system BIOS setup options

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Warning

Most of the features of this product have passed strict verification and are subject to change at any time without notice. If any malfunction occurs due to the future technical changes made by the respective component manufacturers, Iwill assumes no responsibility or liability for it.

Content

Chapter 0

Overview

Thank you for purchasing Iwill PIILD motherboard This operation manual will instruct you how to configure and install the system properly. It contains an overview about the engineering design and features of this product. Also, this manual provides useful information for later on upgrade or configuration change. Keep this for your future need.

YEAR 2000 issue

The IBM compatible PC utilizes a Motorola MC146818 compatible Real-Time Clock (RTC) chip to maintain the date and time. Unfortunately, the "century" is not manipulated by the RTC. It uses 8-bit of information to report the year and can only hold the last two digits of a year in packed BCD format. So 1997 is reported solely as 97. Since the RTC also contains non-volatile memory, IBM specified a location in the memory to hold "century" information. By combining the century data with the year data, software can obtain a full 4-digit year. When the Year 2000 occurs, the RTC reports the year as '00' and the "century" in RTC memory will contain '19.' Combining the full 4-digit year yields 1900, not 2000. Any applications which compares dates, or uses relative dates to perform functions will see an incorrect dates.

Motherboards contain BIOS, which is one of the key ingredients to check for systems designed to handle the year 2000. **All motherboards currently shipped from Iwill contain BIOS capable of handling the year 2000 date correctly**. The BIOS contains a feature that checks the least two significant digits of the year stored in the RTC during each BIOS request (INT 1Ah) to read the date and, if less than `80', updates the century byte to `20'. This feature enables operating systems and applications using the BIOS date/time services to reliably manipulate the year as a four-digit value.

Be aware that the BIOS capability alone does not ensure that the system will handle the transition correctly. Other system components such as the operating system and application software also need to be able to handle the year 2000 date and recognize the date format from other pieces.

0.1 Features

0.1.1 Processor

Single Pentium®II processor support

Supports 66 MHz bus speed

Supports all published Pentium®II processor voltages

S.E.C. (Single Edge Contact) cartridge Slot 1 connector

Easy-jumper to set the processor speed from 233 MHz to 333 MHz

0.1.2 Core Logic

Intel 82443LX PCI/A.G.P. controller (PAC)

    Integrated DRAM controller

    Integrated PCI bus mastering controller

    Integrated Accelerated Graphics Port (A.G.P.) bus controller

Intel 82371AB PCI/ISA/IDE Xcelerator (PIIX4)

    Multifunction PCI-to-ISA bridge (PCI Rev 2.1 compliant)

    Integrated IDE controller with Ultra DMA/33 support

    USB host interface with support for two USB ports

    Enhanced DMA controller and standard Interrupt controller and Timer function

    Support system Management Bus (SMB)

0.1.3 Main Memory

Four 168-pin DIMM (Dual In Line Memory Module) sockets

Supports up to 512 MB of 3.3 V Unbuffered Synchronous DRAM (SDRAM)

Supports up to 1 GB of 3.3 V Extended Data Out (EDO) memory

64-bit data interface with ECC support

0.1.4 Multi I/O

ALI M5135 super I/O controller

    Supports two floppy disk drives (include 3 Mode drive) and/or QIC-80 tape drive

    Supports one multi-mode parallel port

    Supports two high speed 16550 FIFO serial ports

    Integrated keyboard controller

    Integrated PS/2 mouse controller

0.1.5 Expansion slots

Three ISA slot
Three PCI slot
One shared ISA/PCI slot
One A.G.P. slot

0.1.6 Form Factor

Compliance with ATX Version 2.01 specification
Supports ATX power supply connector
Supports the remote on/off switch
Physical dimensions: length: 220 mm / width: 305 mm

0.1.7 Manageability

Optional NS LM78 System Hardware Monitor

0.1.8 Other features

Award BIOS
Using Flash ROM to provide on-board-upgrade ability without changing components
Plug and Play compatible
Supports Advanced Power Management (APM)

0.2 Environment Requirements

Temperature 0-55 degrees C (operating or storage)
5% to 95% non-condensing relative humidity
At least a 250 W power supply
The power supply must comply with the following recommendations found in the spec.:
    The potential relation between 3.3 VDC and +5 VDC power rails
    The current capability of the +5VSB line
    All timing parameters

0.3 Motherboard Components Placement

The following figure shows the location of the motherboard components.

1 JP23
VCC
NC
IRRX
GND
IRTX
IRMODE
NC
7

J9   J1
J2   J3
            J4
            J5

J6/7/8   1
J11-14   J10

            SLOT1
            AGP
            FAN

DIMM0~3
FLOPPY

1
1
            1
PWR ON   SEC. IDE
PRI. IDE

Reset   Cathode-
GND   Anode+
RESET   IDE

JP1   1 JP19
233   1--2:Normal
266   2--3:Clear CMOS
300   3
350
RS0
RS1

10   1
20   11
VCC SPEAKER   KEYLOCK Anode+
GND   NC
NC   Cathode-
Buzz   Keylock
                         GND

3
SENSE
+12V
GND
1

8
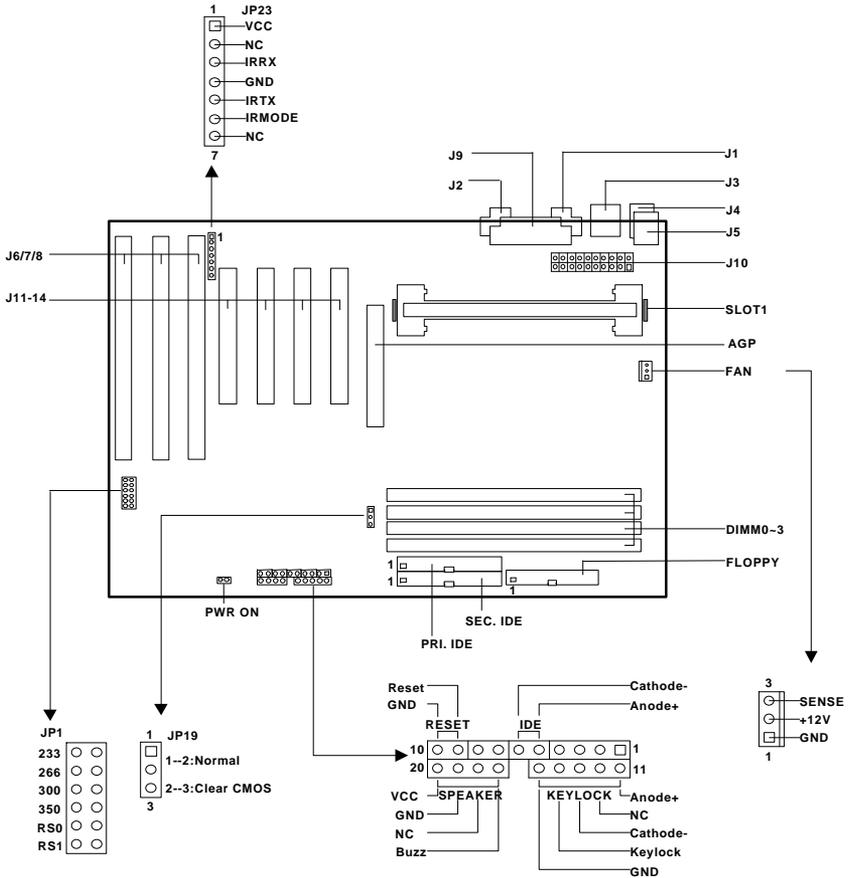
Location	ScreenPrinting	Description
J1	J1	Serial 1 connector
J2	J2	Serial 2 connector
J3	J3	Two USB connectors
J4	J4	PS/2 keyboard connector
J5	J5	PS/2 mouse connector
J6--J8	J6,J7,J8	ISA expansion slots
J9	J9	Parallel connector
J10	J10	Standard ATX power connector
J11--J14	PCI1--4	PCI expansion slots
J15	AGP	A.G.P. connector
J16	Slot1	Processor Slot 1 socket
J17	FAN	Processor fan header
J19,J22--J24	DIMM0--3	168-pin DIMM Sockets
J25	PRI.IDE	Primary IDE connector
J26	SEC.IDE	Secondary IDE connector
J27	FLOPPY	Floppy drive connector
J28	RESET	Reset Switch header
J30	SPEAKER	Speaker header
J31	IDE	IDE LED header
J32	KEYLOCK	Power LED and Keylock switch header
JP1	JP1	Jumper for processor frequency selection
JP10	PWR ON	Remote power on/off header
JP19	JP19	Jumper for clearing CMOS
JP23	JP23	IR (infrared) connector

0.4 Back Panel Connectors

The following figure shows the location of the back panel I/O connectors, which include:

PS/2-style keyboard and mouse connectors

Two USB connectors

Two serial port connectors

One parallel port connector
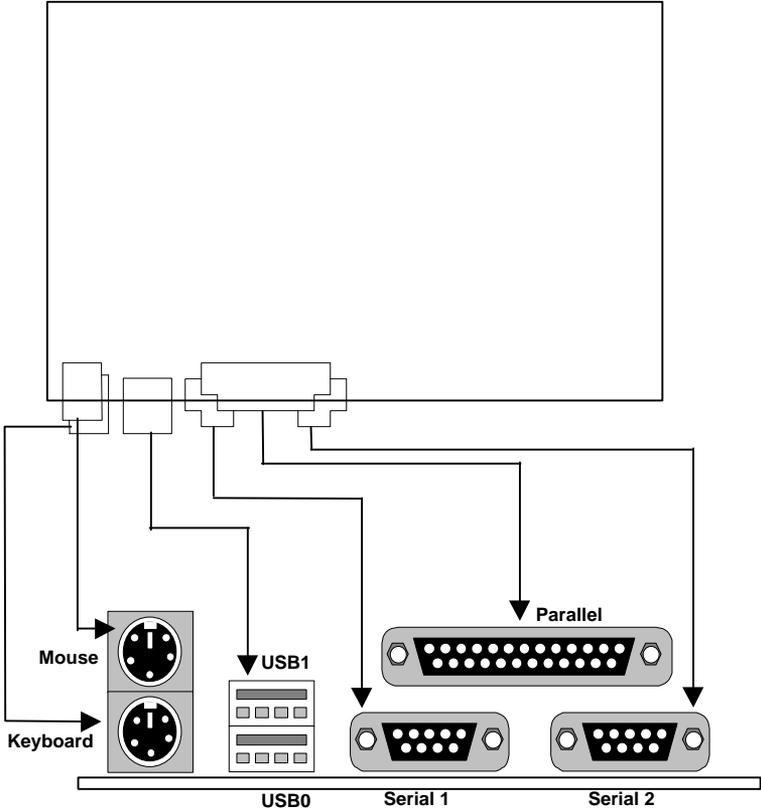
0.5 Form Factor

The motherboard is designed to fit into an ATX form-factor chassis. The I/O connector locations and the mounting hole locations are in compliance with the ATX specification. Please see detail in the following figure.

A: 0.400 inch   H: 0.150 inch

B: 1.000 inch   I: 0.650 inch
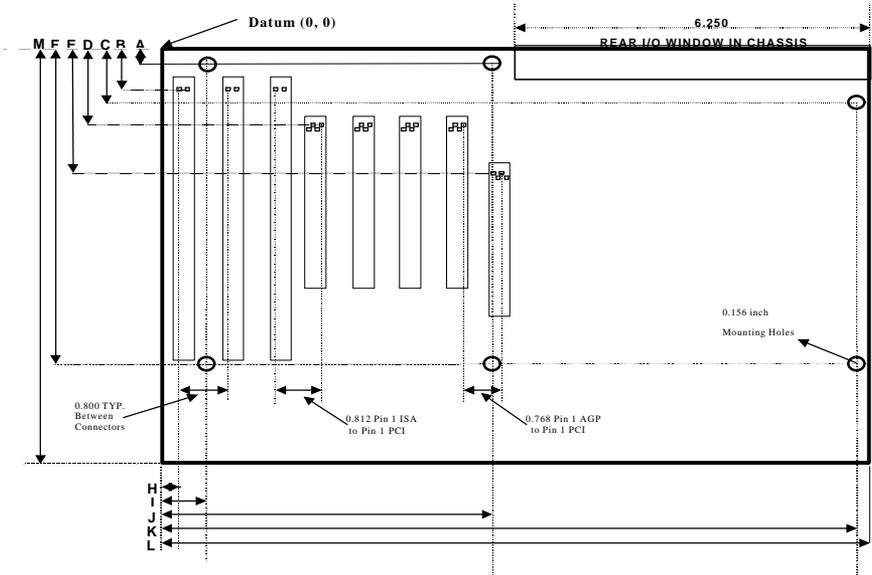
C: 1.300 inch   J: 5.550 inch

D: 1.625 inch   K: 11.750 inch

E: 2.630 inch   L: 12.000 inch

F: 6.500 inch

M: 8.661 inch

Chapter 1

Quick Installation

Several easy installation steps will be described in this chapter to help the experienced users with quick installation. If you are a beginner or need to know more about this product, refer to the Chapter 2.

Step 1. Install retention mechanism and Pentium II processor

There is one set of the thread studs that need to be screwed to the Slot 1's retention mechanism with a criss-cross screwdriver. Insert the Pentium II processor along the retention mechanism in vertical direction down to Slot 1 connector. Make sure that they are connected thoroughly.

Step 2. Install processor fan

Attach the processor cooler's power cable to the header marked "FAN".

Step 3. Select the processor frequency

JP1 is used to select the processor frequency. Simply place one jumper cap onto the speed number according to the internal frequency you see on your processor. For example: select 333 for a Pentium II processor 333 MHz.

Step 4. Install the memory module

At least one piece of 168-pin 3.3V unbuffered SDRAM or EDO DIMM is needed to be located into the DIMM sockets.

Step 5. Connect the internal peripherals

The internal peripherals means devices that are in the computer chassis like the floppy disk drive, hard disk drive, CD-ROM drive .etc. There are one 34-pin flat cable for floppy disk drive and one 40-pin flat cable for IDE devices included in your retail package. The protected key on cables' connector will guide you the correct direction when you insert the cables.

Step 6. Connect the Reset button

The J28 is a 2-pin reset header. Connect the momentary type switch on the chassis to this header for reset function. (See section 0.3 for detail pin definition.)

Step 7. Connect the Speaker

The J30 is a 4-pin speaker header. Connect the speaker to this header. (See section 0.3 for detail pin definition.)

Step 8. Connect the power LED and keylock switch

The J32 is a 5-pin keylock header. It contains two functions: Power LED and Keylock switch. Connect chassis's power LED and keylock switch (if supported) to this header. (See section 0.3 for detail pin definition.)

Step 9. Connect the IDE LED

The J31 is a 2-pin IDE LED header. Connect the chassis's LED to this header. (See section 0.3 for detail pin definition.)

Step 10. Connect the Power ON button

All the ATX computer chassis provide a power on button. Connect the button to the header marked as "PWR ON".

Step 11. Install the Power Supply cord

This motherboard provides the 20-pin ATX power connector. This works conjunction with the *Power On button* to provide remote On/Off function.

Step 12. Install the Keyboard

Connect the keyboard to the PS/2 keyboard connector at the back panel.

Step 13. Install the Display Card

Insert the display card into the ISA, PCI or AGP expansion slot.

Step 14. Connect the External Peripherals

The external device means devices outside the computer chassis like the serial mouse, printer, PS/2 mouse, external modem ..etc.

Step 15. Power on the system

Once the system is powered on, make sure you enter the BIOS setup program and loads the manufacturer's default settings. After the system reboot, you are ready to install your operating system and we wish you to enjoy it.

Chapter 2

Hardware Installation

2.1 Preparation and Inspection

This motherboard, like all other electronic equipment, is static sensitive. Please take the proper precautions when handling it. If possible, ground yourself by touching a metal table or your computer frame. Keep the board in its conductive wrapping until it is configured and ready to be installed in your system.

2.2 Unpack the PIILD

You should find the following components when opening the box:

> One PIILD motherboard
>
> This operation manual
>
> One 40-pin IDE cable
>
> One 34-pin floppy cable
>
> One Bus Master Driver diskette
>
> One set of Pentium® II Retention kit

For installation, you may need some or all of the following tools:

> Medium size flat blade screwdriver
>
> Medium sized Phillips head screwdriver
>
> A 3/16 inch nut driver or wrench

2.3 Installation procedures

2.3.1 Processor (J16 and FAN)

The motherboard supports single Pentium® II processor. The processor's VID pins automatically program the voltage regulator on the motherboard to the required processor voltage. The motherboard currently supports processors that run internally from 233 MHz to 333 MHz.

The Pentium® II processor is packaged in a Single Edged Contact (S.E.C.) cartridge. The cartridge includes the processor core, second-level cache, thermal plate and back cover. The processor connects to the motherboard through the Slot 1 connector, a 242-pin edge connector. When mounted in a Slot 1 connector, the processor is secured by a retention mechanism attached to the motherboard.

First, screw the main body of Slot 1 retention mechanism to the motherboard then insert the processor cartridge along the retention mechanism in vertical direction. A "click" sound will be heard while the processor is located right in position. Finally, attach the cooler's power cable to the processor fan header on the motherboard.

Signal of FAN header (processor fan header)

Pin 1   Ground

Pin 2   +12 V

Pin 3   SENSE

Note 1. Processor cooler is always required to prevent over-heat.

Note 2. The second-level cache is located on the substrate of the S.E.C. cartridge. The cache size and cacheable memory size are dependent on the processor used.

2.3.2 Processor frequency Selection (JP1)

JP1 is a 2x6-pin jumper block with Easy-jumper cap on it for you to select the processor's working speed easily.

233	266	300	333	RS0	RS1	Processor
ON	OFF	OFF	OFF	OFF	OFF	For Pentium®II 233 MHz
OFF	ON	OFF	OFF	OFF	OFF	For Pentium®II 266 MHz
OFF	OFF	ON	OFF	OFF	OFF	For Pentium®II 300 MHz
OFF	OFF	OFF	ON	OFF	OFF	For Pentium®II 333 MHz

Note: This jumper is able to provide more powerful functions, which are reserved for technician's special testing purpose only. **DO NOT use these functions unless you are an experienced user and you are willing to take your risk**.

233	266	300	333	Multiplier		RS0	RS1	External Clock
OFF	OFF	OFF	OFF	x 2		OFF	OFF	68 MHz
ON	OFF	ON	OFF	x 2.5		ON	OFF	66 MHz
ON	ON	OFF	OFF	x 3		OFF	ON	75 MHz
ON	OFF	OFF	OFF	x 3.5		ON	ON	83 MHz
OFF	ON	OFF	OFF	x 4				
OFF	OFF	ON	OFF	x 4.5				
OFF	OFF	OFF	ON	x 5				
OFF	OFF	ON	ON	x 5.5				
OFF	ON	OFF	ON	x 6				
ON	OFF	OFF	ON	x 6.5				

2.3.3 Main memory (DIMM0--3)

The motherboard has four dual inline memory module (DIMM) sockets, which supports memory size from 8 MB to 512 MB with SDRAM and 1 GB with EDO DRAM. The Synchronous DRAM (SDRAM) improves memory performance through memory access that is synchronous with the memory clock. The Error Checking and Correcting (ECC) memory improves system security by detecting and correcting error bit when accessing memory.

The motherboard supports the following memory features:

JEDEC MO-161 compliant 168-pin DIMMs with gold-plated contacts

3.3 V memory module only

ECC logic detects multiple-bit errors and corrects single-bit errors (SDRAM)

Unbuffered SDRAM or 60-ns 3.3 V EDO DIMMs

4 / 16 / 64 Mbit DRAM technology

Symmetrical and asymmetrical DRAM addressing

Single-sided or double-sided DIMMs

3.3 V EDO and SDRAM DIMMs can be installed on the same motherboard

Memory can be installed in DIMM sockets without any order restriction. The memory type, size, speed can vary between sockets. The BIOS automatically detects memory type, size and speed.

Note 1. In order to reduce the loading, the total memory chip count installed on the system should not exceed 72.

2.3.4 Accelerated Graphics Port (AGP)

The Accelerated Graphics Port (A.G.P.) is a high-performance interconnect, especially for graphic-intensive 3D applications. A.G.P. is independent of the PCI bus and is intended for exclusive use with graphical display devices. The A.G.P. supports AC timing for 133 MHz data transfer rates, allowing data throughput of 533 MB/sec.

The most important feature of A.G.P. is DIME (Direct Memory Execute). DIME needs to allocate some system memory via the O.S. to access large textures outside the local graphic memory of the card. In order to take advantage of DIME feature, some software components should be installed or upgraded in the system.

For Windows NT 4.0:   Upgrade to "Windows NT 4.0 Service Pack 3".

For Windows 95:   Upgrade to Windows 95 OSR 2.1.

Install DirectX 5 from Microsoft.

2.3.5 Primary/Secondary IDE connectors (PRI.IDE and SEC.IDE)

The motherboard has two bus-mastering IDE interfaces, which support PIO Mode 3 / 4 and Ultra DMA 33 mode transfer. These interfaces support IDE disks, ATAPI devices (ex: CD-ROM), ZIP and LS-120 devices. If two devices are connected to one channel, one should be set to "Master" and the other one to "Slave" (Refer to device operation guide).

Simply connect the 40-pin IDE cable between the IDE/ATAPI devices and these connectors on the motherboard. For a performance reason, we suggest that connect the disk drive to the primary channel and other devices like CD-ROM to the secondary channel.

2.3.6 Floppy drive connector (FLOPPY)

The motherboard has one floppy interface, which supports 360K, 720K, 1.2M, 1.44M, 2.88M, 3 Mode floppy drives and QIC-80 Floppy tape drive. It supports up to two devices in any capacity with the same connector. Simply connect 34-pin floppy cable between this connector and floppy drives.

2.3.7 Serial port connector (J1 and J2)

The two 9-pin D-Sub serial port connectors on the back panel are compatible with 16550 UART. These ports are used for serial mouse, serial printer, fax modem ..etc. Simply connect the serial devices to these connectors.

2.3.8 Parallel port connector (J9)

The connector for the multi-mode parallel port is a 25-pin D-Sub connector located on the back panel. It is used for the printer or other parallel devices. Simply connect the parallel cable between devices and the parallel port connector.

2.3.9 Universal Serial Bus (J3)

The USB is suitable for mid-to-low speed devices like mouse, keyboard, joystick...etc. In the past, all these devices were using different connectors, and it is difficult for end users to install the system. With USB technology, users only need to plug all their USB peripherals on the connector in chain and ready to go.

The motherboard supports following USB features:

      Self-identifying, hot pluggable peripherals

      Support of isochronous and asynchronous transfer type

      Supports for a maximum of 127 physical devices

      Supports data transfer rate up to 12 Mbit/sec

The motherboard has two USB ports; any USB peripheral can be connected to either port. For more than two USB devices, an external hub can be connected to either port.

2.3.10 PS/2 keyboard and mouse connectors (J4 and J5)

The keyboard connector is a 6-pin mini-DIN connector located on the back panel (the bottom one). Simply connect the standard PS/2 keyboard into this connector. The PS/2 mouse connector is a 6-pin mini-DIN connector on the back panel. Simply connect the PS/2 mouse into this connector.

Note that power to the computer should be turned off before a keyboard and/or mouse is connected or disconnected.

2.3.11 ATX power connector (J10)

This motherboard supports an ATX power connector. Simply connect the power cord of power supply to this connector.

Signal of ATX power supply connector

Pin 1	+3.3 V	Pin 11	+3.3 V
Pin 2	+3.3 V	Pin 12	-12 V
Pin 3	Ground	Pin 13	Ground
Pin 4	+5 V	Pin 14	PWR_ON#
Pin 5	Ground	Pin 15	Ground
Pin 6	+5 V	Pin 16	Ground
Pin 7	Ground	Pin 17	Ground
Pin 8	PWRGOOD	Pin 18	-5 V
Pin 9	+5VSB	Pin 19	+5 V
Pin 10	+12 V	Pin 20	+5 V

2.3.12 Power On header (PWR ON)

This header can be connected to chassis's power switch. Because of debounce circuitry on the motherboard, the switch must be pressed for at least 50 ms to signal the power supply to switch on or off. At least two seconds must pass before the power supply will recognize another on/off signal.

Note: Hold the power on switch in for four seconds will force the system switch off.

2.3.13 IDE LED header (IDE)

The J31 is a 2-pin IDE LED header. It can be connected to an LED on the chassis, which will light up when IDE devices is working. (See section 0.3 for detail pin definition.)

2.3.14 RESET header (RESET)

The J28 is a 2-pin reset header. It can be connected to a momentary type switch that is normally open. When the switch is close, the system will reset. (See section 0.3 for detail pin definition.)

2.3.15 Power LED and keylock switch header (KEYLOCK)

The J32 is a 5-pin keylock switch header. It has two functions: Power LED and Keylock switch. The power LED can be connected to a chassis's LED. When the computer is powered on, the LED will be lighted up. The keylock header can be connected to a switch on the chassis. When the switch is close, keyboard function will be disabled temporarily until the switch is open. (See section 0.3 for detail pin definition.)

2.3.16 SPEAKER header (SPEAKER)

The J30 is a 4-pin speaker header. The speaker provides error beep code information during the POST in the event that the computer can not use the video interface. (See section 0.3 for detail pin definition.)

2.3.17 Infrared connector (JP23)

Serial Port 2 can be configured to support an IrDA module connected to this connector. After the IrDA interface is configured, data can be transferred between devices by using application software.

Signal of JP23 connector

Pin 1	VCC	Pin 5	IRTX
Pin 2	NC	Pin 6	IRMODE
Pin 3	IRRX	Pin 7	NC
Pin 4	Ground		

2.3.18 Clear CMOS jumper block (JP19)

To reset the RTC (Real Time Clock) CMOS data, you need to change the jumper cap of JP19 from *1-2 close* to *2-3 close*, then set to *1-2 close* again. After that, you should get into BIOS setup program and choose LOAD SETUP DEFAULTS, then you will now get original manufacturer default setting in your CMOS.

2.3.19 System Hardware Monitor

The system hardware monitor supports following features:

Temperature sensor to monitor system temperature

Voltage sense monitoring to detect voltage level (+12 V, -12 V, +5 V, -5 V, +3.3 V)

Fan speed sensors for up to three fans

With a proprietary application, the system hardware monitor logic will check the voltage, temperature and fan speed all the time. If any failure occurs, the application will prompt warning message in a real time.

Chapter 3

System BIOS Setup

3.1 Introduction

The motherboard uses an AWARD BIOS, which is stored in flash memory and can be upgraded with a disk-based program. The setup program is for viewing and changing the BIOS setting for a computer. These settings are stored in battery-backed RAM so that it retains all the settings when the power is turned off.

3.1.1 Upgrade BIOS

The BIOS can be upgraded from a diskette with the Award Flash utility -- AWDFLASH.EXE. The BIOS image file and the update utility are available from Iwill's WEB site: www.iwill.com.tw.

3.1.2 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS being updated in flash memory. The BIOS can be recovered from a diskette. To create a BIOS recovery diskette, a bootable diskette must be created and the recovery files copied to it. The recovery files are available from Iwill.

Note: No video is displayed during the recovery process.

3.1.3 Enter BIOS setup program

The BIOS setup program is accessed by pressing the <Del> key after Power-On Self Test (POST) memory test begins and before the scanning of IDE devices. During that time, a message "Press DEL to enter SETUP" will be displayed at the bottom of the screen. If the message disappears before you respond, you can restart the system by

Turning off the system power then turn it on again, or

Pressing the "RESET" button on the system case, or

Pressing <Ctrl>, <Alt> and <Del> keys simultaneously.

3.1.4 Using BIOS setup program

The following table shows the function keys available for menu screens.

<Up>	Move to the previous field
<Down>	Move to the next field
<Left>	Move to the field in the left hand
<Right>	Move to the field in the right hand
<Esc>	Quit from setup program without saving changes, or Exit from current menu page and return to main menu page
<PgUp> or <+>	Select the previous value for a field
<PgDn> or <->	Select the next value for a field
<F1>	Bring up a help screen for the current field
(Shift)<F2>	Change screen color. F2 to select color forward, (Shift) F2 to select color backward
F10 key	Save the current value and exit setup program

NOTE

Generally, the BIOS default settings have been carefully chosen by the system manufacturer to provide the absolute maximum performance and reliability. It is very dangerous to change any setting without full understanding. We strongly recommend that

DO NOT update your BIOS if the system works perfect.

DO NOT change any setting unless you fully understand what it means.

If the system does not work smoothly after changing the BIOS setting, follow the procedures described before to enter setup program then load the default to the original manufacturer default setting.

If the system is no longer able to boot after changing the setting, the only way to recover it is to clear the data stored in RTC CMOS. To reset the RTC CMOS data, you need to change the jumper cap of JP19 from *1-2 close* to *2-3 close*, then set to default *1-2 close* again. After that, you should get into BIOS setup program and choose LOAD SETUP DEFAULTS to get original manufacturer default setting in your CMOS.

3.2 Main Menu

The main menu allows you to select from several setup pages. Use the arrow keys to select among these pages and press <Enter> key to enter the sub-menu. Note that a brief description of each highlighted selection appears at the bottom of the screen.

The main menu includes the following setup pages.

STANDARD CMOS SETUP

Allocates resources for hardware components

BIOS FEATURES SETUP

Specifies advanced features available through the BIOS

CHIPSET FEATURES SETUP

Specifies advanced features available through the chipset

POWER MANAGEMENT SETUP

Specifies power management features

PNP /PCI CONFIGURATION

Specifies Plug and Play and PCI features

INTEGRATED PERIPHERALS

Specifies on-board controller features

LOAD SETUP DEFAULTS

Load the manufacturer default setting into CMOS

SUPERVISOR / USER PASSWORD

Specifies passwords

IDE HDD AUTO DETECTION

Auto-detect the parameters of IDE disks

SAVE & EXIT SETUP

Save current value to CMOS and exit setup

EXIT WITHOUT SAVING

Abandon all changes and exit setup

3.3 STANDARD CMOS SETUP

This setup page is used for allocating resources for hardware components.

3.3.1 Date

This field specifies the current date. The date format is <day>, <month>, <date>, and <year>.

3.3.2 Time

This field specifies the current time. The time format is <hour>, <minute>, and <second>. The time is calculated based on the 24-hour military-time clock.

3.3.3 Primary Master / Primary Slave / Secondary Master / Secondary Slave

This field specifies the geometric parameters and translation mode of IDE disk drives.

3.3.3.1 TYPE

This field specifies the drive type that corresponds to the drive installed in the system. If set to *User*, the number of *Cylinders*, *Heads*, and *Sectors* can be modified.

Options	Description
1 – **45**	Specifies pre-defined disk drive type
User	Specifies disk drive type by user
Auto	BIOS automatically fills in the values for the cylinders, heads and sectors fields
None	No disk drive attached

3.3.3.2 Cylinders

If device *TYPE* is set to *Auto*, this field reports the number of cylinders for your hard disk and can not be modified. If the *TYPE* is set to *User*, you must type the correct number of cylinders for your hard disk.

3.3.3.3 Heads

If device *TYPE* is set to *Auto*, this field reports the number of heads for your hard disk and can not be modified. If the *TYPE* is set to *User*, you must type the correct number of heads for your hard disk.

3.3.3.4 Sectors

If device *TYPE* is set to *Auto*, this field reports the number of sectors for your hard disk and can not be modified. If the *TYPE* is set to *User*, you must type the correct number of sectors for your hard disk.

3.3.3.5 MODE

This field specifies the IDE translation mode.

Options	Description
NORMAL	Specifies traditional CHS addressing mode
LARGE	Specifies extended CHS translation mode
LBA	Specifies LBA translation mode
AUTO	BIOS specifies translation method automatically

3.3.4 Drive A / Drive B

This field specifies the traditional type of the floppy drives.

Options	Description
None	No floppy drive is connected
360K, 5.25 in.	A 360K floppy drive is connected
1.2M, 5.25 in.	A 1.2M floppy drive is connected
720K, 3.5 in.	A 720K floppy drive is connected
1.44M, 3.5 in.	A 1.44M floppy drive is connected
2.88M, 3.5 in.	A 2.88M floppy drive is connected

3.3.5 Floppy 3 Mode Support

3 Mode floppy drive is a kind of 3.5 inches drive, which is used at NEC PC98 computer. It supports 1.2M and 1.44M format with the same drive. This field specifies which drive 3 Mode is supported. When a floppy drive is specified to support 3 Mode, the respective drive setting in "Drive A / Drive B" field will be invalid.

Options	Description
Disabled	No 3 Mode drive is connected
Drive A	A 3 Mode drive is connected as drive A
Drive B	A 3 Mode drive is connected as drive B
Both	Both drive A and drive B are 3 Mode drives

3.3.6 Video

This field specifies the type of the graphics adapters used for the primary system monitor.

Options	Description
EGA/VGA	Specifies EGA or VGA adapter
CGA 40	Specifies CGA adapter with 40 column mode
CGA 80	Specifies CGA adapter with 80 column
MONO	Specifies Monochrome adapter

3.3.7 Halt On

This field specifies the failure event, which should halt the system if occurred.

Options	Description
All Errors	When the BIOS detects a non-fatal error, the system will stop and you will be prompted
No Errors	The system will not stop for any error that may be detected
All, But Keyboard	The system will stop for any errors except keyboard error
All, But Diskette	The system will stop for any errors except diskette error
All, But Disk/Key	The system will stop for any errors except diskette and keyboard errors

3.3.8 Base Memory

The POST will determine the amount of base (conventional) memory installed in the system. The value of the base memory is typically 640K. This field has no options.

3.3.9 Extended Memory

The BIOS determines how much extended memory is present during the POST. This is the amount of memory located above 1MB in the processor's memory address map. This field has no options.

3.3.10 Other Memory

This refers to the memory located in the 640K to 1024K address space. This is memory that can be used for different applications. DOS uses this area to load device drivers in an effort to keep as much base memory free for application programs. The BIOS is the most frequent user of this RAM area since this is where it shadows RAM. This field has no options.

3.4 BIOS FEATURES SETUP

This setup page specifies advanced features available through the BIOS.

3.4.1 Virus Warning

When this function is enabled, the BIOS will monitor the boot sector and partition table of the hard disk drive for any attempt at modification. If an attempt is made, the BIOS will halt the system and then prompts an error message. Afterwards, if necessary, you can run an anti-virus program to locate and remove the problem before any damage is done.

Note that many disk diagnostic programs will attempt to access the boot sector table, which can cause the above warning message. If you will be running such a program, we recommend that you first disable Virus Warning beforehand.

Options   **Enabled**

                 Disabled (*)

3.4.2 CPU Internal Cache

This field configures the CPU internal cache (L1 cache).

Options   **Enabled (*)**

                 Disabled

3.4.3 External Cache

This field configures the system external cache (L2 cache).

Options   **Enabled (*)**

                 Disabled

3.4.4 Quick Power On Self Test

When enabled, BIOS will shorten or skip some items during POST.

Options   **Enabled (*)**

                 Disabled

3.4.5 Boot Sequence

This field configures the boot sequence of boot devices.

Options	Description
A,C,SCSI (*)	System will first try to boot from floppy drive then master IDE disk drive on primary channel and then SCSI disk drive
C,A,SCSI	Master IDE disk drive on primary channel, floppy drive, SCSI disk driver
C,CDROM,A	Master IDE disk drive on primary channel, ATAPI CDROM drive, floppy drive
CDROM,C,A	ATAPI CDROM drive, master IDE disk drive on primary channel, floppy drive
D,A,SCSI	Slave IDE disk drive on primary channel, floppy drive, SCSI disk drive
E,A,SCSI	Master IDE disk drive on secondary channel, floppy drive, SCSI disk drive
F,A,SCSI	Slave IDE disk drive on secondary channel, floppy drive, SCSI disk drive
SCSI,A,C	SCSI disk drive, floppy drive, ATAPI CD-ROM drive
SCSI,C,A	SCSI disk drive, master IDE disk drive on primary channel, floppy drive
C only	Master IDE disk drive on primary channel only
LS/ZIP,C	LS-120 or ZIP drive, master IDE disk drive on primary channel

3.4.6 Swap Floppy Drive

When enabled, the logical drive letter of floppy drive A and B will be exchanged without changing the physical cable.

Options	**Enabled**
	Disabled (*)

3.4.7 Boot Up Floppy Seek

When enabled, BIOS will check floppy drive status during POST. If an error occurred, system will be paused and an error message will be prompted.

Options	**Enabled (*)**
	Disabled

3.4.8 Boot Up NumLock Status

This field configures the numeric keypad after system booting up.

Options	Description
On (*)	Keypad works as number keys
Off	Keypad works as arrow keys

3.4.9 Gate A20 Option

This field configures how the gate A20 is handled. The gate A20 is a device used to address memory above 1 Mbytes. Initially, the gate A20 was handled via a pin on the keyboard. Today, while keyboards still provide this support, it is more common, and much faster, for the system chipset to provide support for gate A20.

Options	Description
Fast (*)	GateA20 signal supported by core logic
Normal	GateA20 signal supported by keyboard controller

3.4.10 Typematic Rate Setting

This field configures how the keyboard is handled. When enabled, the *Typematic Rate (Chars/Sec)* and *Typematic Delay (Msec)* fields will be available.

Options	**Enabled**
	Disabled (*)

3.4.11 Typematic Rate (Chars/Sec)

This field specifies how many characters will be prompted in one second when a key is pressed continuously.

Options   **6 (*), 8, 10, 12, 15, 20, 24, 30**

3.4.12 Typematic Delay (Msec)

This field specifies the delay between when a key was first pressed and when the acceleration begins.

Options   **250 msec (*), 500 msec, 750 msec, 1000 msec**

3.4.13 Security Option

This field configures how the system security is handled. It works conjunction with *SETTING SUPERVISOR / USER PASSWORD* page to control the security level of the system.

Options	Description
Setup (*)	System need password to enter BIOS setup program
System	System need password to boot

3.4.14 PCI / VGA Palette Snoop

This field controls the ability of a primary PCI graphics controller to share a common palette with an ISA/VESA video or MPEG card

Options	Description
Enabled	PCI VGA co-works with ISA MPEG card
Disabled (*)	All cases except above

3.4.15 OS Select for DRAM >64MB

When enabled, this field allows you to access the memory that over 64MB under OS/2.

Options	**OS/2**
	Non-OS/2 (*)

3.4.16 Report No FDD For WIN 95

For a floppy diskless system that running Windows 95, this field should be set to *Yes*.

Options	**Yes**
	No (*)

3.4.17 Video BIOS Shadow

When enabled, the video BIOS will be copied to system memory and increase the video speed.

Options	**Enabled** (*)
	Disabled

3.4.18   C8000-CBFFF / CC000-CFFFF / D0000-D3FFF Shadow
D4000-D7FFF / D8000-DBFFF / DC000-DFFFF Shadow

When enabled, the extended ROM data located at the respective address range will be copied to system memory.

Options	**Enabled**
	Disabled (*)

3.5 CHIPSET FEATURES SETUP

This setup page is used to specify advanced features available through the chipset. The default settings have been chosen carefully for the most operating conditions. **DO NOT change the value of any field in this setup page without full understanding.**

3.5.1 Auto Configuration

When enabled, BIOS will divide all the EDO/FPM memory into two categories: 50ns DRAM and 60ns DRAM. A set of pre-defined values about DRAM timing will be used for each category. Then the user can assign the correct timing easily. When disabled, user can specify the DRAM timing value and some engineering knowledge is needed while handling it.

    Options   **Enabled** (*)

                    Disabled

3.5.2 DRAM Speed Selection

This field selects pre-defined EDO/FPM DRAM timing for different speed categories. It is available only when the *Auto Configuration* field set to *Enabled*.

Options	Description
50ns (*)	Pre-defined timing for 50ns EDO DRAM
60ns	Pre-defined timing for 60ns EDO DRAM

3.5.3 MA Wait State

This field configures the wait state of EDO/FPM DRAM address line. This is for experienced users only.

Options	Description
Slow (*)	Inserts one system clock as wait state
Fast	No wait state

3.5.4 EDO RAS# To CAS# Delay

This field specifies the EDO/FPM DRAM timing from RAS# to CAS#. This is for experienced users only.

Options	Description
2	2 system clocks
3 (*)	3 system clocks

3.5.5 EDO RAS# Precharge Time

This field specifies the EDO/FPM DRAM timing for RAS# pre-charge. This is for experienced users only.

Options	Description
3 (*)	3 system clocks
4	4 system clocks

3.5.6 EDO DRAM Read Burst

This field specifies the timing of EDO/FPM DRAM burst read. This is for experienced users only.

Options	Description
x222 (*)	2 system clocks for each burst read cycle
x333	3 system clocks for each burst read cycle

3.5.7 EDO DRAM Write Burst

This field specifies the timing of EDO/FPM DRAM burst write. This is for experienced users only.

Options	Description
x222 (*)	2 system clocks for each burst write cycle
x333	3 system clocks for each burst write cycle

3.5.8 DRAM Data Integrity Mode

When enabled, the BIOS will use ECC (Error Checking and Correcting) protocol to increase integrity of system data. When ECC is selected, all memory modules the system used must support ECC.

Options	**ECC**
	Non-ECC (*)

3.5.9 CPU-TO-PCI IDE Posting

When enabled, the data from processor to PCI IDE can be posted to increase performance. Otherwise, the cycles are treated as normal I/O write transaction. This field is for the experienced users only.

Options	**Enabled**
	Disabled (*)

3.5.10 System BIOS Cacheable

When enabled, accesses to the system BIOS will be cached.

    Options   **Enabled (*)**

                      Disabled

3.5.11 Video BIOS Cacheable

When enabled, access to the video BIOS will be cached.

    Options   **Enabled**

                      Disabled (*)

3.5.12 Video RAM Cacheable

When enabled, access to the video memory located at A0000H to BFFFFH will be cached.

    Options   **Enabled**

                      Disabled (*)

3.5.13 8 Bit I/O Recovery Time

This field specifies the number of clocks, which the system will delay after the completion of an 8 bit input/output request.

    Options   **1 (*) / 2 / 3 / 4 / 5 / 6 / 7 / NA / 8**

3.5.14 16 Bit I/O Recovery Time

This field specifies the number of clocks, which the system will delay after the completion of an 16 bit input/output request.

    Options   **1 (*) / 2 / 3 / NA / 4**

3.5.15 Memory Hole At 15M-16M

Some add-in cards need to re-map its resource to a block of main memory address range. Any host cycles that match this memory hole are passed on to the add-in cards.

    Options   **Enabled**

                      Disabled (*)

3.5.16 AGP Aperture Size (MB)

This field specifies the size of system memory that can be used for A.G.P. graphics aperture.

    Options   **4 / 8 / 16 / 32 / 64 (*) / 128 / 256**

3.5.17 SDRAM RAS-to-CAS Delay

This field specifies the delay in assertion of CAS# from the assertion of RAS# of SDRAM memory. This is for the experienced users only.

Options	Description
Slow (*)	3 system clocks delay
Fast	2 system clocks delay

3.5.18 SDRAM RAS Precharge Time

This field specifies the SDRAM RAS# pre-charge requirements. This is for experienced users only.

Options	Description
Fast (*)	2 system clocks for RAS# precharge
Slow	3 system clocks for RAS# precharge

3.5.19 SDRAM CAS Latency Time

This field specifies the SDRAM CAS latency timing parameter (the time from CAS# assertion to data valid). This is for experienced users only.

Options	Description
2	2 system clocks
3 (*)	3 system clocks

3.5.20 Passive Release

When enabled, the south bridge PIIX4 will support the Passive Release mechanism when it is a PCI master. The PCI revision 2.1 compliant requires this field to be enabled. This field is for experienced users only.

Options	**Enabled** (*)
	Disabled

3.5.21 Delayed Transaction

When enabled, the south bridge PIIX4 will supports the Delayed Transaction mechanism when it is the target of a PCI transaction. The PCI revision 2.1 compliant requires this field to be enabled. This field is for experienced users only.

Options	**Enabled** (*)
	Disabled

3.6 POWER MANEGEMENT SETUP

This setup page specifies power management features.

There are several modes used to save computer's energy:

Doze Mode	The CPU clock will run at slower speed, and all other devices still operate at full speed
Standby Mode	The CPU clock will run at slower speed, and the fixed disk drive will be power off, and the video will be power off, and all other devices still operate at full speed
Suspend Mode	All devices except the CPU will be shut off

Each power saving mode has a respective timer. The value of the timer can be assigned or reloaded and it will count down to zero. When the timer equals to zero, the system will be forced into the related power saving mode. If any predefined signal or event is detected during the timer counting period, the timer will be reloaded automatically.

3.6.1 Power Management

Options	Description
Disable	The computer always runs at full speed. No power is saved
Min Saving	When idled for one hour, the system will enter suspend mode
Max Saving	When idled for fifteen minutes, the system will enter suspend mode
User Define (*)	User can specify the timer value of each power saving mode

3.6.2 PM Control by APM

When enabled, an Advanced Power Management (APM) protocol will be activated to handle the power saving mode.

Options   **Yes (*)**

No

3.6.3 Video off Method

This field specifies the method that video subsystem used for power saving.

Options	Description
V/H SYNC+Blank (*)	Turn off the vertical and horizontal synchronization ports and write blanks to the video buffer
Blank Screen	Writes blanks to the video buffer only
DPMS	Initial display power management signaling with DPMS

3.6.4 Video Off After

This field specifies the power saving mode, which will shut off the video.

Options   **Doze / Standby (*) / Suspend / NA**

3.6.5 MODEM Use IRQ

This field specifies the IRQ channel for MODEM used.

Options   **3 (*) / 4 / 5 / 7 / 9 / 10 / 11 / NA**

3.6.6 Doze Mode

This field specifies the timer value of Doze Mode. It is available only when the *Power Management* field set to *User Define*.

Options   **1 Min / 2 Min / 4 Min / 8 Min / 12 Min / 20 Min**
                       30 Min / 40 Min / 1 Hour / Disable

3.6.7 Standby Mode

This field specifies the timer value of Standby Mode. It is available only when the *Power Management* field set to *User Define*.

Options   **1 Min / 2 Min / 4 Min / 8 Min / 12 Min / 20 Min**
                       30 Min / 40 Min / 1 Hour / Disable

3.6.8 Suspend Mode

This field specifies the timer value of Suspend Mode. It is available only when the *Power Management* field set to *User Define*.

     Options   **1 Min / 2 Min / 4 Min / 8 Min / 12 Min / 20 Min**
                    30 Min / 40 Min / 1 Hour / Disable

3.6.9 HDD Power Down

This field specifies the timer value for HDD power down. It is available only when the *Power Management* field set to *User Define*.

     Options   **1 Min / 2 Min / 3 Min / 4 Min / 5 Min / 6 Min**
                    7 Min / 8 Min / 9 Min / 10 Min / 11 Min / 12 Min
                    13 Min / 14 Min / 15 Min / Disable

3.6.10 VGA Active Monitor

When enabled, the system will not enter any power saving mode as long as video is active.

     Options   **Enabled**
                    Disabled (*)

3.6.11 Soft-Off by PWR-BTTN

This field specified the function of power button.

Options	Description
Instant-Off	When power button pressed, turn off the system immediately.
Delay 4 Sec.	Turn off the system after the power button has been pressed for four seconds.

3.6.12 Resume by Ring

When enabled, the system can be resumed from power saving mode by MODEM ring signal.

     Options   **Enabled**
                    Disabled (*)

3.6.13 IRQ 8 Break Suspend

When enabled, the system can be resumed from power saving mode by a predefined timer alarm.

     Options   **Enabled**
                    Disabled (*)

3.6.14 Reload Global Timer Events

This field configures the events to reload the power saving mode timer.

IRQ [3-7,9-15], NMI

If enabled, timer will be reloaded when any of these interrupts occurs.

Primary IDE 0

If enabled, timer will be reloaded when master disk of primary IDE channel is active.

Primary IDE 1

If enabled, timer will be reloaded when slave disk of primary IDE channel is active.

Secondary IDE 0

If enabled, timer will be reloaded when master disk of secondary IDE channel is active.

Secondary IDE 1

If enabled, timer will be reloaded when slave disk of secondary IDE channel is active.

Floppy Disk

If enabled, timer will be reloaded when floppy disk is active.

Serial Port

If enabled, timer will be reloaded when serial port is active.

Parallel Port

If enabled, timer will be reloaded when parallel port is active.

3.7 PNP/ PCI CONFIGURATION

This setup page specifies Plug and Play and PCI features

3.7.1 PNP OS Installed

The field specifies whether a Plug and Play operating system is installed.

Options   **Yes**

            No (*)

3.7.2 Resources Controlled By

The BIOS has the capability to assign the system resource to all of the boot and Plug and Play devices. However, this capability means absolutely nothing unless you are using a Plug and Play operating system such as Windows® 95.

Options   Description

Auto   Resource controlled by BIOS automatically

Manual (*) Resource controlled by the user

3.7.3 Reset Configuration Data

When enabled, the extended configuration data (ESCD) will be cleared during each boot time.

| Options | **Enabled** |
| | **Disabled** (*) |

3.7.4 IRQ 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15 assigned to
DMA 0 / 1 / 3 / 5 / 6 / 7 assigned to

If the *Resources Controlled By* field is set as *Manual*, these resource fields can be assigned by the user.

Options	Description
Legacy ISA	Resource will not be assigned to any PnP device
PCI/ISA PnP	Resource is available to PnP devices

3.7.5 PCI IDE IRQ Map To

This field configures the IRQ channel for the add-in PCI IDE controller.

INT A: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INT A.

INT B: Generally, the secondary interrupt on add-in cards that require two or more interrupts is classified as INT B.

INT C and INT D: A third interrupt on add-in cards is classified as INT C and a fourth interrupt is classified as INT D.

The PCI-to-ISA bridge supports four programmable PIRQ signals and can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 7, 9, 10, 11, 12, 14, and 15). Any PCI interrupt source (either onboard or from a PCI add-in card) connects to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are mechanically tied together on the motherboard and share the same interrupt.

The following table describes the PCI interrupt routine of this motherboard:

	PCI#1	PCI#2	PCI#3	PCI#4
PIRQA	INTA	INTB	INTC	INTD
PIRQB	INTB	INTC	INTD	INTA
PIRQC	INTC	INTD	INTA	INTB
PIRQD	INTD	INTA	INTB	INTC

Options	Description
PCI-AUTO (*)	The BIOS detects PCI IDE card's location automatically
PCI-Slot1	The PCI IDE card located on PCI slot 1
PCI-Slot2	The PCI IDE card located on PCI slot 2
PCI-Slot3	The PCI IDE card located on PCI slot 3
PCI-Slot4	The PCI IDE card located on PCI slot 4
ISA	The PCI IDE card connects its IRQ to ISA bus through a paddle card

3.7.6 Used MEM base addr

Some add-in cards ask for a special range of the system address space. This field specifies the base address of the memory address space.

> Options **N/A (*) / C800 / CC00 / D000 / D400 / D800 / DC00**

3.7.6.1 Used MEM Length

This field is available only when the *Used MEM base addr* field has been assigned to a base address. It specifies the memory size for the add-in card used.

> Options **8K (*) / 16K / 32K / 64K**

3.7.7 Assign IRQ For USB

When disabled, the BIOS will not assign IRQ channel to USB controller.

> Options **Enabled (*)**
>
> **Disabled**

3.8 INTEGRATED PERIPHERALS

3.8.1 IDE HDD Block Mode

When enabled, the IDE controller will use the faster block mode to access devices.

> Options **Enabled (*)**
>
> **Disabled**

3.8.2 IDE Primary Master / Slave PIO
IDE Secondary Master / Slave PIO

These fields configure the PIO (Programmable Input Output) transfer mode for IDE controller.
The maximum transfer rate of each PIO mode are listing as follow:

	Maximum transfer rate
PIO Mode 0	3.3 MB/sec
PIO Mode 1	5.2 MB/sec
PIO Mode 2	8.3 MB/sec
PIO Mode 3	11 MB/sec
PIO Mode 4	16.6 MB/sec

Options	Description
Auto (*)	The BIOS negotiates with device automatically
Mode 0	Use Mode 0 timing to access device
Mode 1	Use Mode 1 timing to access device
Mode 2	Use Mode 2 timing to access device
Mode 3	Use Mode 3 timing to access device
Mode 4	Use Mode 4 timing to access device

3.8.3 IDE Primary Master / Slave Ultra DMA
IDE Secondary Master / Slave Ultra DMA

When selected *Auto*, the IDE controller will use Ultra DMA 33 Mode to access device if the device supports it. The maximum transfer rate of Ultra DMA 33 Mode is 33.3 MB/sec.

Options	**Auto** (*)
	Disabled

3.8.4 On-Chip Primary / Secondary PCI IDE

These fields enable or disable the onboard IDE controller.

Options	**Enabled** (*)
	Disabled

3.8.5 USB Keyboard Support

This field enables or disables the USB keyboard supported.

Options	**Enabled**
	Disabled (*)

3.8.6 Onboard FDC Controller

This field enables or disables the onboard floppy controller.

    Options   **Enabled (*)**

                  Disabled

3.8.7 Onboard Serial Port 1 / 2

These fields configure the onboard serial ports. There are several port address and IRQ channels that can be selected.

Options	Description
3F8 / IRQ 4	Port address 3F8h, IRQ 4
2F8 / IRQ 3	Port address 2F8h, IRQ 3
3E8 / IRQ 4	Port address 3E8h, IRQ 4
2E8 / IRQ 3	Port address 2E8h, IRQ 3
Auto	BIOS assigns port address and IRQ channel automatically
Disabled	Disables serial port

3.8.8 Onboard Parallel Port

This field configures the onboard parallel port. There are several port addresses and IRQ channel that can be selected.

Options	Description
378 / IRQ 7	Port address 378h, IRQ 7
278 / IRQ 5	Port address 278h, IRQ 5
3BC / IRQ 7	Port address 3BCh, IRQ 7
Disabled	Disable parallel port

3.8.9 Parallel Port Mode

This field configures the operating mode of onboard parallel port.

    Options   **SPP (*)** / **EPP1.7** / **ECPEPP1.7 /PS2 / EPP1.9** / **ECP / ECPEPP1.9**

3.8.9.1 ECP Mode Use DMA

When the *Parallel Port Mode* field is configured as *ECP*, *ECPEPP* mode, it need a DMA channel for data transfer. This field specifies the DMA channel for ECP parallel port use.

Options	Description
1	Use DMA channel 1
3 (*)	Use DMA channel 3

3.9 LOAD SETUP DEFAULTS

This setup page is used for loading the manufacturer default values.

3.10 SUPERVISOR / USER PASSWORD SETTING

These setup pages are used for password setting. Note that the User Password can enter BIOS setup program, but has no rights to change the value of any fields.

When a password has been enabled and the *Security Option* field is set as *Setup*, you will be prompted to enter the password every time you try to enter BIOS Setup program. This prevents an unauthorized person from changing any part of your system configuration. Additionally, if the *Security Option* field is set as *Boot*, the BIOS will request a password every time your system boot. This would prevent unauthorized use of your computer.

To disable a password, just press <Enter> when you are prompted to enter the new password. A message will confirm that the password is disabled. Once the password is disabled, the system will boot and you can enter setup program freely.

3.11 IDE HDD AUTODETECTION

This setup page detects and configures hard disk parameters automatically.

3.12 SAVE & EXIT SETUP

Save current CMOS value and exit BIOS setup program.

3.13 EXIT WITHOUT SAVING

Abandon all CMOS value changes and exit BIOS setup program.