PCI48AF

Version 3.0B

User's Manual

94-LON-AQ-249

PCI48AF
User's Manual

NOTES

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NOTES

Chapter 1 Specifications

Architecture

Two bus : PCI bus and ISA bus

Main Processor

- Supports Intel 486, DX4, P24D, P24T, SL-Enhanced, Cyrix M7, Cx5x86, UMC U5 and AMD 486 CPUs in 25, 33, 40, 50MHz, 3V/5V CPU Interface.
- Supports CPU L1 Writeback
- Supports Cyrix linear wrap and (1+4) Mode.

L2 Cache Controller

- Write Back Cache with standard SRAM
- 8 Tag Bit, always force dirty
- Supports Cache Size of 128K to 512K with 32Kx8, 64Kx8, 128Kx8
- Write hit 0 wait support

DRAM Controller

- Supports 5V EDO DRAM
- Up to 128MB of on board main memory
- Four 72-pin SIMM (Single In-line Memory Module) Sockets for 512Kx36, 1Mx36, 2Mx36, 4Mx36, 8Mx36 , 16Mx36 or 32Mx36 module.

PCI Local Bus

- Synchronous 20, 25, 33MHz PCI clock
- Supports PCI Rev 2.0 with 4 PCI device, 3 slot PCI masters, 1 slot PCI Slave.

Built in IDE Controller

- Supports through ATA PIO mode 3, 4 harddisk
- 4x32 bits Read-Ahead buffer and write-post buffer support

- Dedieated IDE pins, concurrent with PCI bus

BIOS

Licensed BIOS

I/O

Two serial ports (16550)
One parall port (ECP, EPP)
One floppy port
Two Enhance PCI-IDE port

Clock/Calendar

Battery Backed Real Time Clock(146818 compatible) and 128 bytes of CMOS RAM

DMA Channels

Seven DMA channels(8237 compatible)

Interrupts

Sixteen levels of hardware interrupts(dual 8259 compatible)

System Timer

Three channels of programmable system timer (8254 compatible)

Expansion Slots

Four PCI
Four ISA

Connectors

Connectors for: power supply, keyboard, reset switch, Power LED, keylock, speaker, turbo switch, turbo LED and hard disk access LED

Physical Dimensions

3/4 Baby AT form factor

Power Requirement

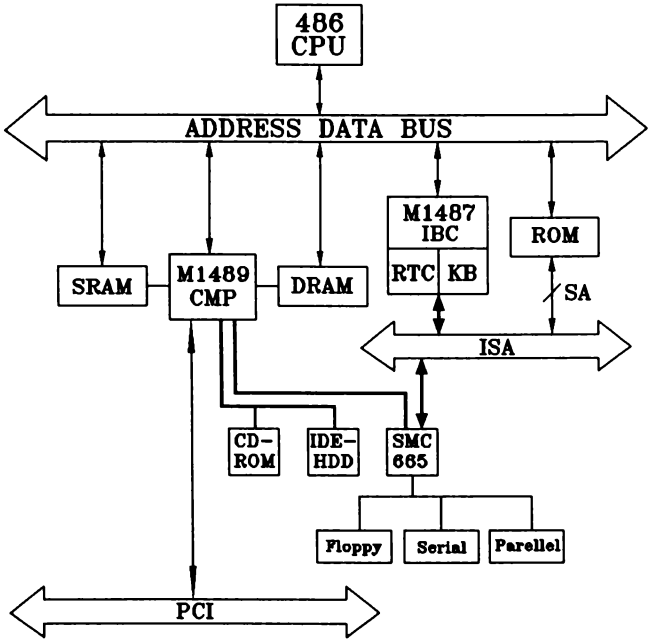
+ 5V @ 2 AMPs (Normal Operation)
+ 5V @ 1 AMP (Power Saving Mode)

NOTES

Chapter 2 Hardware Description

This chapter briefly describes each of the major features of the PCI48AF system board. The function block of the board is shown in *Figure 1.* The layout of the board is shown in *Figure 2* to show the locations of key components. The topics covered in this chapter are as follows:

- ☐ **2.1 PCI48AF Motherboard**
- ☐ **2.2 486 Microprocessor**
- ☐ **2.3 Cache Controller and Cache Memory**
- ☐ **2.4 I/O Port Address Map**
- ☐ **2.5 Memory Map**
- ☐ **2.6 BIOS**
- ☐ **2.7 System Timer**
- ☐ **2.8 DMA Channels**
- ☐ **2.9 Interrupt Controllers**
- ☐ **2.10 Real Time Clock and CMOS RAM**
- ☐ **2.11 On board I/O**



CMP: Cache Memory PCI Controller

IBC: ISA Bus Controller

Figure 1: Function block of the PCI48AF

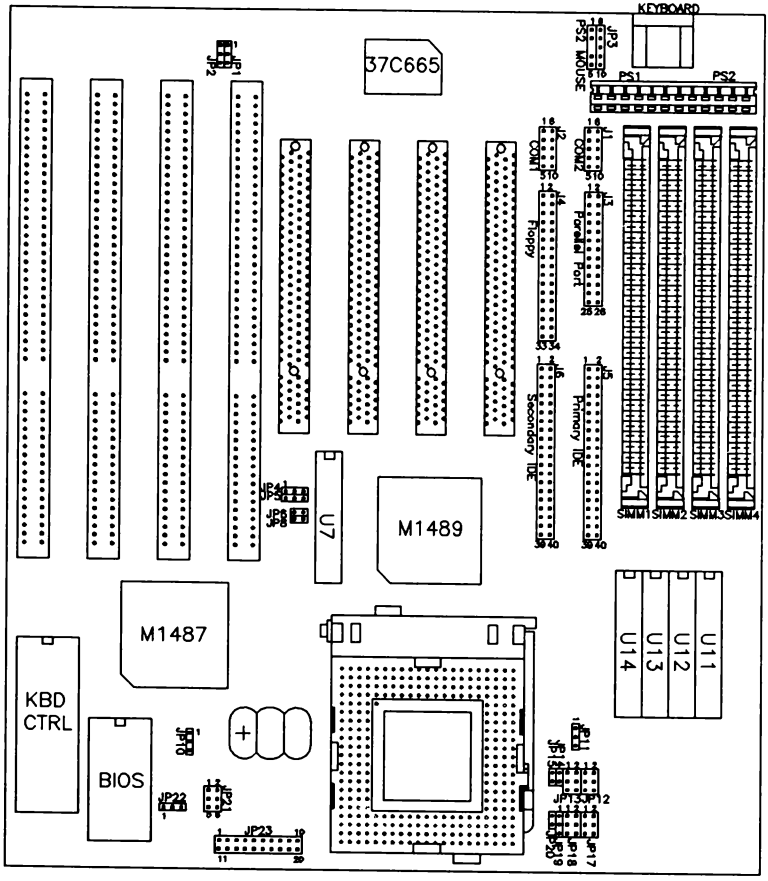


Figure 2: Layout and connector locations of the PCI48AF

2.1 PCI48AF Motherboard

The PCI48AF is designed by implementing a highly integrated chipset, the **M1487 and M1489.** The M1487 integrated all the functions of a AT compatible Motherboard. The M1489 converts CPU to PCI bus.

Also included on the PCI48AF are M1489 and 37C665. The M1487 provides PCI-IDE interface. The 37C665, is a supper I/O chip which provides two 16550 compatible serial ports, one ECP/EPP parallel port and a 2.88MB floppy interface.

2.2 486 Microprocessor

The Central Processing Unit (CPU) of the PCI48AF motherboard is a 486 microprocessor. There are various models in the 486 family: 486SX, 486DX, 486DX2, 486DX4, P24C, P24CT, P24D. 5x86 **(AMD), CX5x86 (Cyrix).**

The 486DX2 is the basic model in the 486 family. The 486DX4, in additions to the features of the 486DX2, provides on-chip 80387 compatible math coprocessor. The 486DX2 has a core frequency two times the bus frequency and provides twice the performance.

The socket on board also supports the OverDrive processor. The OverDrive is an upgrade processor for 486 family. It has Pentium equivalent core with 486 compatible pin-outs. It provides capability of a user to upgrade from a 486 to Pentium performance with a simple processor change.

2.3 Cache Controller and Cache Memory

This cache is organized as direct map with a line size of 16 bytes. The on-chip cache memory is logically organized as 128 sets, each containing four lines.

For the Pentium OverDrive processor, the cache line size is 32 bytes.

For the secondary cache, the system controller, M1489, supports 486 burst cycles. The PCI48AF can be configured with *128KB* to *512KB* of *write-back secondary cache memory*, greatly enhancing system performance in the event of on-chip cache miss cycles.

The system controller also provides *page mode* operations for main memory. The main memory also supports burst mode operations of the 486, further enhancing system performance.

2.4 I/O Port Address Map

The CPU of the PCI48AF communicates via I/O ports. There are a total of 1K port address space defined. The following tables list the I/O port addresses used in the PCI48AF and those assigned to other devices that can be used by I/O expansion cards.

Table 2: I/O port addresses of the devices on the PCI48AF

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0Ah0 - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
3F0h - 3F7h	Floppy Disk Controller
278h - 27Fh	Parallel Port #2(LPT2)
2F8h - 2FFh	Serial Port #2(COM2)
378h - 37Fh	Parallel Port #1(LPT1)
1F0h - 1F7h	Hard Disk Controller
3F8h - 3FFh	Serial Port #1(COM1)

Table 3: I/O port addresses of devices on the I/O slots

Address	Description
1F0h - 1F8h	Floppy Disk Controller
200h - 207h	Game Port
278h - 27Fh	Parallel Port #2(LPT2)
2F8h - 2FFh	Serial Port #2(COM1)
300h - 31Fh	Prototype Card
360h - 36Fh	Reserved
378h - 3FFh	Parallel Port #1(LPT1)
380h - 38Fh	SDLC #2
3A0h - 3AFh	SDLC #1
3B0h - 3BFh	MDA Video Card (including LPT0)
3C0h - 3CFh	Reserved
3D0h - 3DFh	CGA Video Card
3F0h - 3F7h	Hard Disk Controller
3F8h - 3FFh	Serial Port #1(COM1)

2.5 Memory Map

The PCI48AF has a maximum memory capacity of 128MB. The first megabyte is divided into four blocks with each block dedicated to a fixed function. The following table illustrates the memory map for the PCI48AF.

Table 4: Memory map of the PCI48AF

Memory	Address	Description
0KB	000000h - 09FFFFh	Conventional RAM
640KB	0A0000h - 0BFFFFh	128KB of Video RAM
768KB	0C0000h - 0EFFFFh	192KB of I/O Expansion ROM
896KB	0E0000h - 0FFFFFF	64KB of System BIOS ROM
1MB	100000h - 7FEFFFFh	127MB of User RAM
128MB	7FF0000h - 7FFFFFFh	Duplicated 64KB of System BIOS ROM at 0F0000h

2.6 BIOS

The PCI48AF contains a 1M Boot Block FLASH ROM that contains the system BIOS. The BIOS resides at the upper 64KB of address space in the first megabyte.

In protected mode, the BIOS is also mapped to the upper 64KB of the 128MB space and can be accessed at either location.

2.7 System Timer

The PCI48AF has three channels of timer/counter in the M1487 chip, which is Intel 8254 compatible. The function of each channel is listed as follows:

Table 5: System timer of the PCI48AF

Channel	Function
0	**System Timer** - This timer generates the time base for the system timer. Its output is tied to IRQ0.
1	**Memory Refresh Request** - This timer is used to generate memory refresh requests. It triggers the memory refresh cycle.
2	**Tone Generator for Speaker** - This timer provides the speaker tone. Various sounds can be generated by programming the timer.

2.8 DMA Channels

The PCI48AF contains the equivalent of two 8237A DMA controllers in the M1487.

The M1487 provides the user with two DMA controllers, four channels of DMA*(DMA #1)* for 8-bit transfers, and three channels of DMA*(DMA #2)* for 16 bit transfers.(The first 16-bit DMA channel is used for cascading.)

Channel		Function
Controller #1	**Controller #2**	
0		DRQ0, Reserved
1		DRQ1, SDLC
2		DRQ2, Floppy Disk Controller
3		DRQ3, Reserved
	4	DRQ4, Cascade for DMA
	5	DRQ5, Reserved
	6	DRQ6, Reserved
	7	DRQ7, Reserved

2.9 Interrupt Controllers

The PCI48AF contains two Intel M1487 compatible interrupt controllers in the M1487. Sixteen channels are partitioned into the cascaded controllers (INTC1, INTC2) with 8 inputs each. Of these 16 channels, there are connected internally to various devices, allowing 13 user definable channels of interrupt. Any or all of these interrupts can be masked.

Level	Function
NMI	RAM Parity Check
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ8	Real Time Clock
IRQ9	Software Redirected to Int 0Ah
IRQ10	Reserved
IRQ11	Reserved
IRQ12	Reserved
IRQ13	80287
IRQ14	Fixed Disk Controller
IRQ15	Reserved
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Parallel Port #2
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1

2.10 Real Time Clock and CMOS RAM

The PCI48AF contains an MC146818 compatible Real Time Clock (RTC) and 128 bytes of CMOS RAM in the M1487.

The CMOS RAM stores the system's configuration information entered via the Setup program. The RTC and the CMOS RAM are kept active by a battery when the system power is turned off.

2.11 On board I/O

The PCI48AF provides the following I/O functions on board : serial, parallel, Floppy and IDE.

There are two 16550 compatible serial ports. The parallel port is bidirectional and support ECP/EPP high speed parallel port spec. The floppy port support high density 2.88M floppy drives. The IDE is PCI local bus IDE.

Chapter 3 Configuring the PCI48AF

This chapter provides illustrated instruction on configuring the PCI48AF motherboard.

This chapter is divided into five major areas.

- **3.1 CPU Related Jumpers/Switches**
  - **3.1.1 Installing the CPU**
  - **3.1.2 Setting CPU Related Jumpers**
- **3.2 Main Memory Configurations/Installation**
- **3.3 Cache Memory Configuration/Installing**
- **3.4 L2 Cache Setting**
- **3.5 On Board ECP Function Jumpers**
- **3.6 Miscellenous Jumpers**

3.1 CPU Related Jumpers and Switches

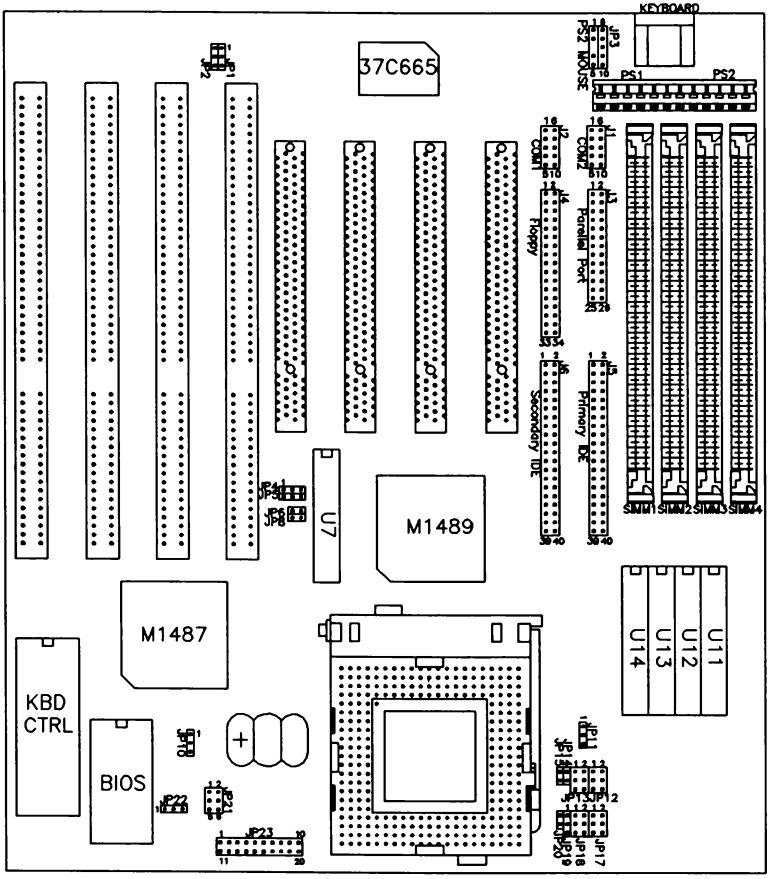


Figure 3: CPU related jumpers

3.1.1 Installing and/or Upgrading the CPU

To install a CPU, refer to the following figures. If there is a ZIF socket, lift the lever to its vertical position to install the CPU.

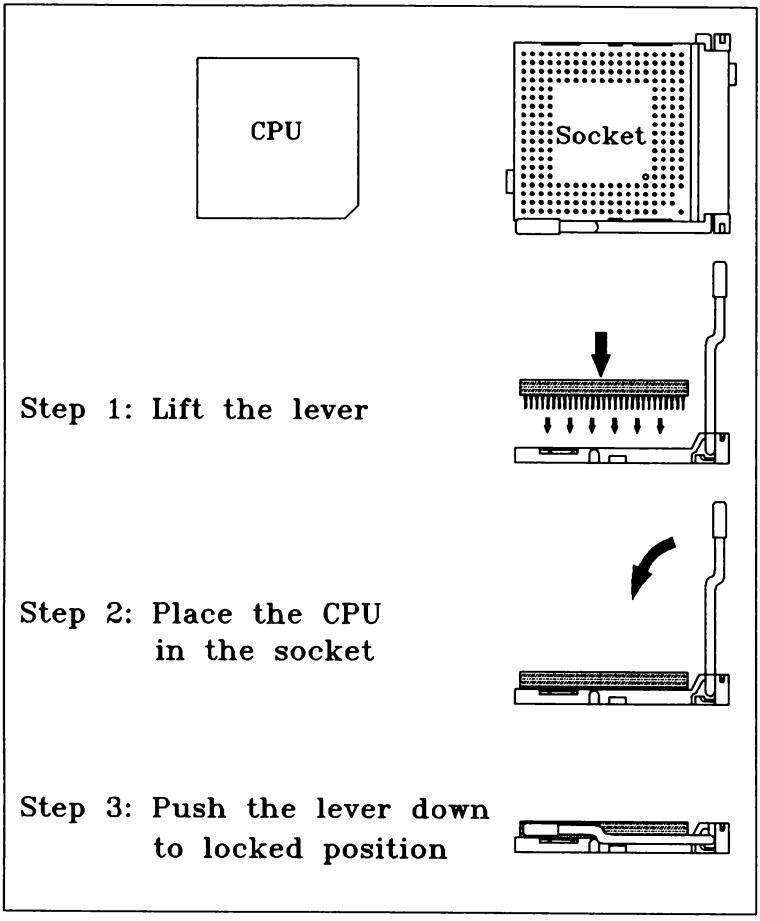


Figure 4: Installing the CPU

3.1.2 Setting CPU Related Jumpers

3.1.2a Setting CPU type: JP14, JP15, JP13, JP12, JP18, JP17, JP11, JP10, JP19, JP20

	JP14	JP15	JP13	JP12	JP18
486SX	OFF	OFF	1 - 2	OFF	OFF
486DX/DX2	OFF	OFF	1 - 2	OFF	OFF
486SX/486SX2-S	ON	OFF	3 - 4	3 - 4	3 - 4
486DX/DX2/DX4-S Cyrix DX4-100 GP4	ON	OFF	3 - 4	3 - 4	3 - 4
AMD486/66/80	OFF	ON	1 - 2	OFF	OFF
AMD486/100		OFF			
AMD486+/66/80 AMD 5x86	ON	OFF	3 - 4	3 - 4	3 - 4
AMD486+/100/120					
M7/Ti486 66/80/100 Cyrix DX4-100 GP	ON	OFF	5 - 6	5 - 6	5 - 6
P24D	ON	OFF	3 - 4	3 - 4	3 - 4
Cx5x86 (M1SC)	ON	OFF	3 - 4	3 - 4	3 - 4
P24T	ON	OFF	3 - 4	3 - 4	3 - 4
U5 (UMC)	OFF	OFF	1 - 2	1 - 2	1 - 2

	JP17	JP11	JP10	JP19	JP20
486SX	OFF	1 - 2	1 - 2	OFF	ON
486DX/DX2	OFF	1 - 2	2 - 3	2 - 3	ON
486SX/486SX2-S	OFF	1 - 2	1 - 2	OFF	ON
486DX/DX2/DX4-S Cyrix DX4-100 GP4	OFF	1 - 2	2 - 3	2 - 3	ON
AMD486/66/80	OFF	1 - 2	2 - 3	2 - 3	ON
AMD486/100					
AMD486+/66/80 AMD 5x86	1 - 3, 5 - 6	2 - 3	2 - 3	2 - 3	ON
AMD486+/100/120	5 - 6				
M7/Ti486 66/80/100 Cyrix DX4-100 GP	1 - 2	1 - 2	2 - 3	2 - 3	OFF
P24D	5 - 6	2 - 3	2 - 3	2 - 3	ON
Cx5x86 (M1SC)	5 - 6	1 - 2	2 - 3	2 - 3	ON
P24T	OFF	2 - 3	2 - 3	1 - 2	ON
U5 (UMC)	OFF	1 - 2	1 - 2	OFF	ON

3.1.2b Setting CPU Frequency Related Jumpers

CPU Speed	JP6	JP8
25MHz	OFF	OFF
33MHz	ON	ON
40MHz	ON	OFF
50MHz	OFF	ON

3.1.2c: CPU Voltage Select: JP21

JP21	Function
1 - 2	3.45V
3 - 4	4.0V
5 - 6	5.0V

3.2 Main Memory Installing

Installing DRAM Memory

SIMM1	SIMM2	SIMM3	SIMM4	Total Memory
256K x 36(S)	256K x 36(S)	X	X	2MB
512K x 36(D)	X	X	X	2MB
1M x 36(S)	X	X	X	4MB
256K x 36(S)	256K x 36(S)	256K x 36(S)	256K x 36(S)	4MB
512K x 36(D)	X	256K x 36(S)	256K x 36(S)	4MB
512K x 36(D)	X	512K x 36(D)	X	4MB
256K x 36(S)	1M x 36(S)	X	X	5MB
256K x 36(S)	256K x 36(S)	1M x 36(S)	X	6MB
512K x 36(D)	X	1M x 36(S)	X	6MB
1M x 36(S)	1M x 36(S)	X	X	8MB
2M x 36(D)	X	X	X	8MB
256K x 36(S)	256K x 36(S)	1M x 36(S)	1M x 36(S)	10MB
512K x 36(D)	X	1M x 36(S)	1M x 36(S)	10MB
512K x 36(D)	X	2M x 36(D)	X	10MB
1M x 36(S)	X	2M x 36(D)	X	12MB
4M x 36(S)	X	X	X	16MB
1M x 36(S)	1M x 36(S)	1M x 36(S)	1M x 36(S)	16MB
2M x 36(D)	X	1M x 36(S)	1M x 36(S)	16MB
2M x 36(D)	X	2M x 36(D)	X	16MB
256Kx36(S)	4M x 36(S)	X	X	17MB
1M x 36(S)	4M x 36(S)	X	X	20MB
4M x 36(S)	4M x 36(S)	X	X	32MB
8M x 36(D)	X	X	X	32MB
16M x 36(S)	X	X	X	64MB
4M x 36(S)	4M x 36(S)	4M x 36(S)	4M x 36(S)	64MB
8M x 36(D)	X	4M x 36(S)	4M x 36(S)	64MB
8M x 36(D)	X	8M x 36(D)	X	64MB
16M x 36(S)	16M x 36(S)	X	X	128MB
32M x 36(D)	X	X	X	128MB

3.3 Cache Memory Installing

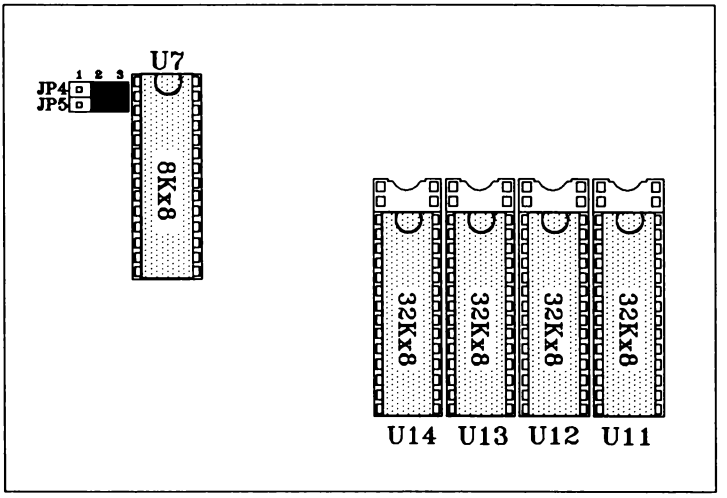


Figure 5: 128KB cache

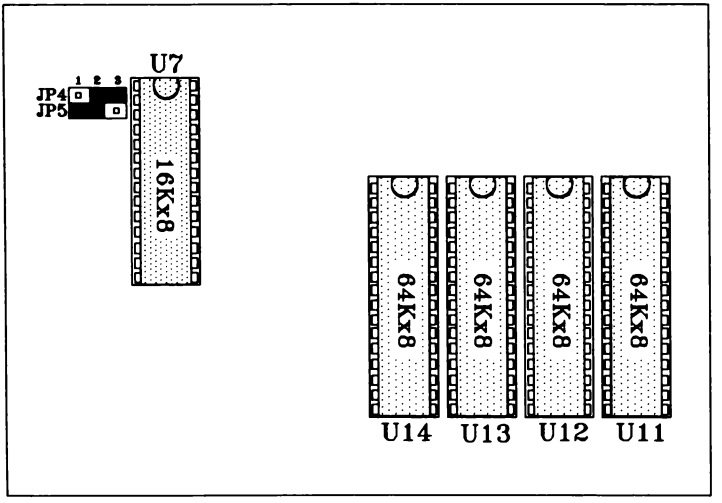


Figure 6: 256KB cache

3.4 L2 Cache Setting: JP4, JP5, JP7

	JP4	JP5	U7	U11 - U14
128K	2 - 3	2 - 3	8Kx8	32Kx8
256K	2 - 3	1 - 2	16Kx8	64Kx8
512K	1 - 2	1 - 2	32Kx8	128Kx8

3.5 On board ECP Function Jumpers

Parellel Port ECP Mode DMA Selection: JP1, JP2

JP1	JP2	DMA Channel
2 - 3	2 - 3	DMA1
1 - 2	1 - 2	DMA3

3.6 Miscellaneous Jumpers

Clear CMOS RAM Jumper: JP22

JP22	Function
1 - 2	Normal
2 - 3	Clear CMOS RAM

3.7 PCI Slots

PCI0, PCI1, PCI2: Master.

PCI3: Slave only.

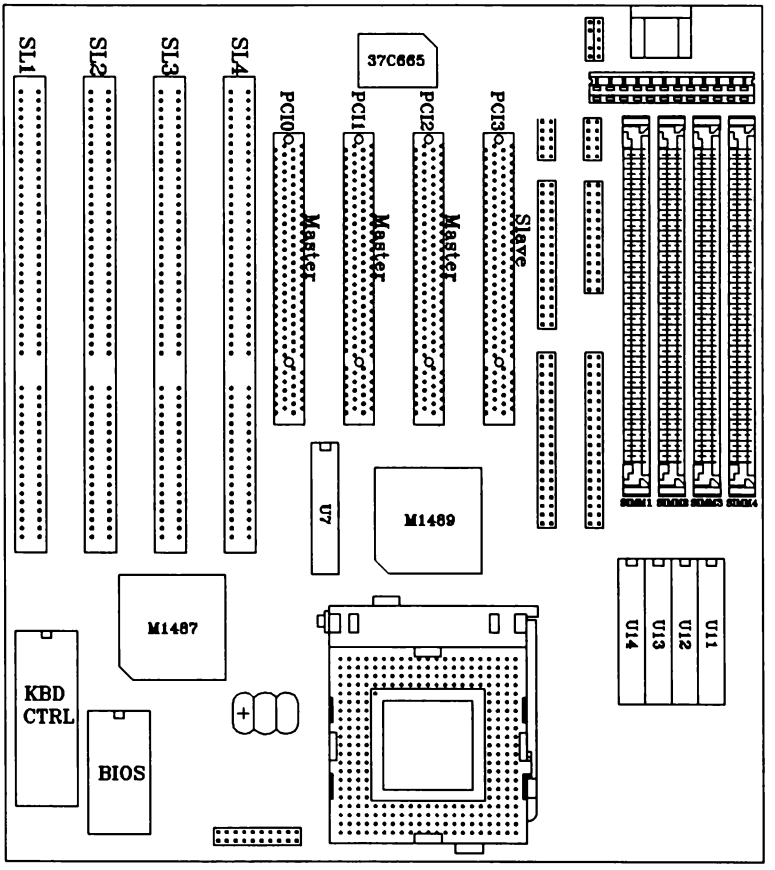


Figure 7: PCI slots location of the PCI48AF

Chapter 4 Installation

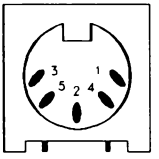
This chapter describesthe interface that the PCI48AF provides for creating a working system. Refer to Figure 2 for the location of the connectors.

The following items are covered in this chapter.

- ☐ **4.1 Keyboard Connector: KB1**
- ☐ **4.2 Power Supply Connector: PS1, PS2**
- ☐ **4.3 Speaker Connector: JP23 (Pins 1-4)**
- ☐ **4.4 Power LED and Keylock Connector: JP23 (Pins 11 - 15)**
- ☐ **4.5 Turbo Switch Connector: JP23 (Pins 7 &17)**
- ☐ **4.6 Turbo LED Connector: JP23 (Pins 8 & 18)**
- ☐ **4.7 Reset Switch Connector: JP23 (Pins 9 &19)**
- ☐ **4.8 Hard Disk Access LED Connector: JP23 (Pins 10 & 20)**
- ☐ **4.9 Multi I/O Connector: J1, J2, J3, J4, J5, J6**

4.1 Keyboard Connector: KB1

The keyboard connector, **KB1**, is a *5-pin DIN* connector for attaching an IBM AT or an IBM Enhanced 101-key compatible keyboard.



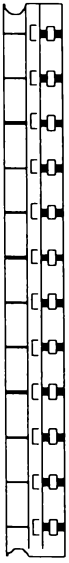
KB1 Pin #	Description
1	Keyboard Clock
2	Keyboard Data
3	N.C.
4	Ground
5	Vcc

4.2 Power Supply Connector: PS1, PS2

When using an AT compatible power supply, plug both of the power supply connectors into **PS1, PS2**.

Make ure the power supply connectors are connected in the right orientation. The power supply conncetors are connected in the right orientation if the black wires of each power cable are ADJACENT to each other. That is, black wires of each connector should be aligned in the center of the power supply connector, **PS1, PS2 of the PCI48AF**.

The following table indicates the pin-out assignments of the power supply connector.

PS1, PS2 Pin #		Description	Wire Color
1		Power Good	Orange
2		+5V	Red
3		+12V	Yellow
4		-12V	Blus
5		Ground	Black
6		Ground	Black
7		Ground	Black
8		Ground	Black
9		-5V	White
10		+5V	Red
11		+5V	Red
12		+5V	Red

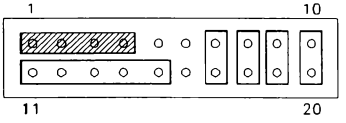
4.3 Speaker Connector: JP23 (Pins 1 - 4)

Pins 1 - 4 of the 20-pin connector, **JP23**, provide an interface to a speaker for audio tone generation. A speaker with 8-Ohm or higher impedence is recommended.

Note

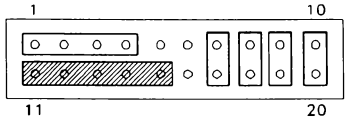
*Orientation is not required when connecting a speaker to pins 1 - 4 of **JP23**.*

JP23 Pin #	Description
1	Speaker Out
2	N.C.
3	Ground
4	+5V



4.4 Power LED and Keylock Connector:JP23(Pins 11 - 15)

Pins 11 - 15 of the 20-pin connector, **JP23**, allow the user to connect the power LED and keylock switch of the system's front panel. The power LED indicates the *ON/OFF* status of the system. The keylock switch, when *CLOSED*, will disable the keyboard function.



JP23 Pin #	Description
11	Power LED
12	N.C.
13	Ground
14	Keylock
15	Ground

4.5 Turbo Switch Connector: JP23(Pins 7 & 17)

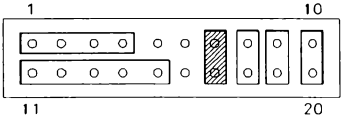
Pins 7 & 17 of the 20-pin connector, **JP23**, allow the user to connect a turbo switch on the front panel of the system chassis.

A turbo switch is usually a push-on switch. When the switch is on, pins 7 & 17 are SHORTED and the system will be running at **FULL*(TURBO)*** speed.

To switch to **LOW*(NON-TURBO)*** speed, simply PRESS the switch. To return to turbo speed, press the switch again.

Note

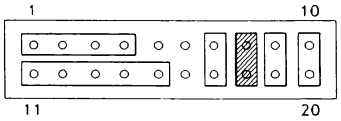
Orientation is not required when connecting a turbo switch to pins 7 & 17 of JP23.



4.6 Turbo LED Connector: JP23(Pins 8 & 18)

Pins 8 & 18 of the 20-pin connector, **JP23**, provide the user with an interface for connecting a turbo **LED** indicator in the system's front panel.

This LED, when on, indicates the **TURBO**(*FULL*) speed mode of the PCI48AF system.



JP23 Pin #	Description
8	Anode
18	Cathode

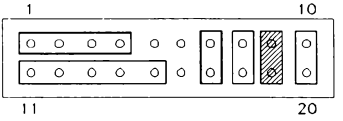
4.7 Reset Switch Connector: JP23(Pins 9 & 19)

Pins 9 & 19 of the 20-pin connector, **JP23,** provide an interface for a reset switch. The reset switch allows the user to reset the system without turning the power switch off and on.

To reset the PCI48AF based system, *SHORT* pins 9 and 19 of **JP23** by pressing the reset switch of the system chassis.

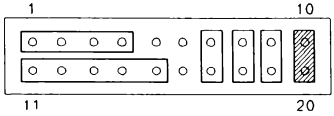
Note

Orientation is not required when connecting a reset switch pins 9 and 19 of JP23.



4.8 Hard Disk LED Connector: JP23(Pins 10 & 20)

These connectors allow the user to connect the hard disk access LED on the system's front panel. The LED will be on whenever the system is accessing the hard drive.



JP23 Pin#	Description
10	Anode
20	Cathode

4.9 Multi I/O Connector: J1, J2, J3, J4, J5 and J6

Follow the pin 1 indication on the M.B. to properly install the cables.

Connector	Function
J2	Serial port #1
J1	Serial port #2
J3	Parallel port
J5	Primary HDD
J6	Secondary HDD
J4	Floppy