

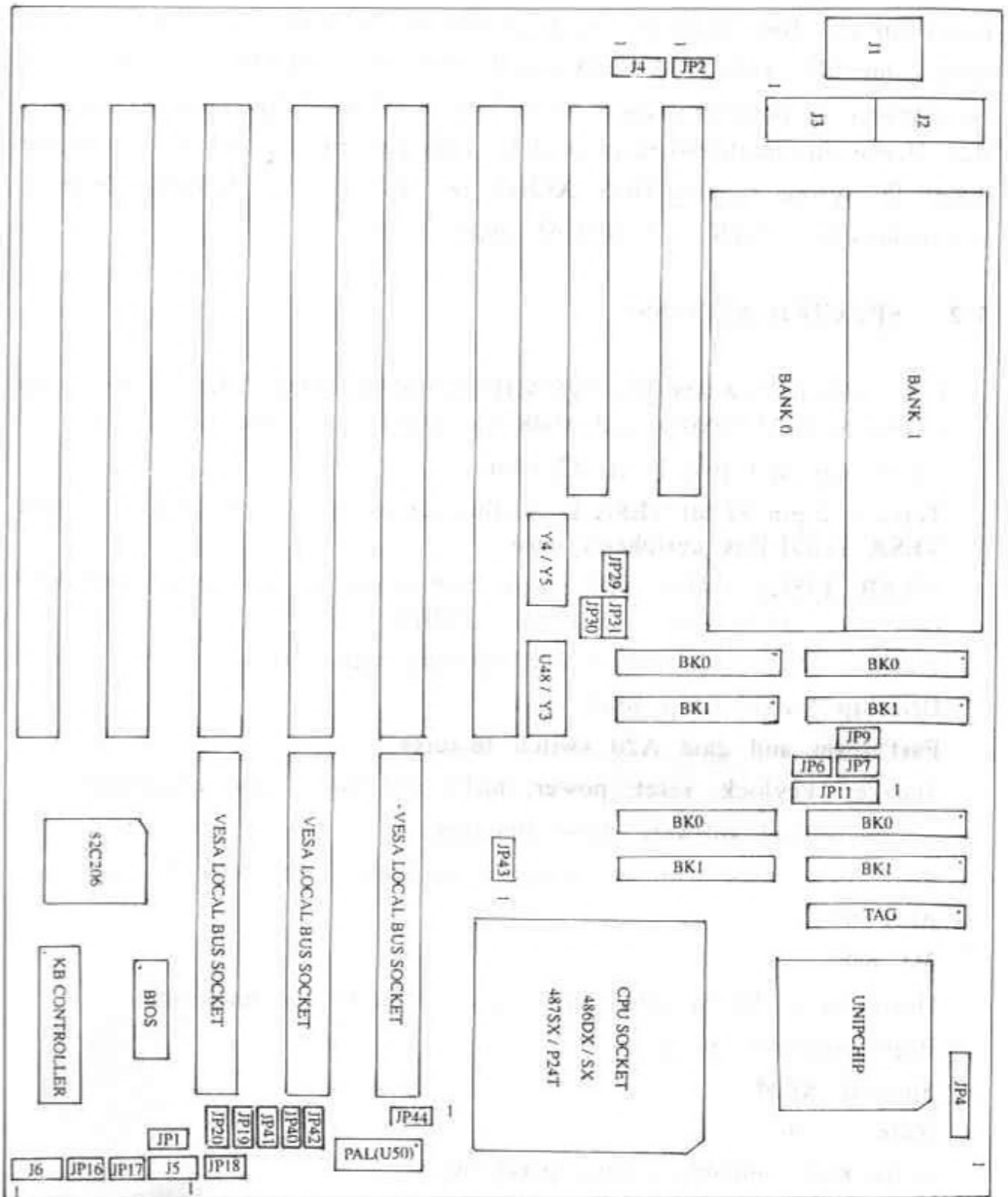
CHAPTER 1 OVERVIEW

1-1 INTRODUCTION:

This 486 motherboard is a VESA (Video Electronics Standard Association) Local-Bus (VL-Bus) motherboard. There are six 16-bit and two 8-bit ISA slots fully compatible with IBM PC/AT, and three 32-bit VL-Bus connectors. The performance of peripheral cards at VL-Bus is substantially faster than at ISA Bus. Hence this motherboard is ideal for high performance and high integrated 80486 PC system running DOS, XENIX 386, UNIX, OS/2, NOVELL Netware environments, as well as CAD/CAE applications.

1-2 SPECIFICATIONS:

- . CPU SUPPORTS: 80486DX2-66/50MHz, 80486DX-50/33/25MHz. Intel Overdrive 80486SX-33/25/20MHz and 80487SX, P24T microprocessor options.
- . Six 16-bit and two 8-bit AT slots.
- . Three 112-pin 32-bit VESA Local-Bus connectors are provided to support VESA Local-Bus peripheral cards.
- . 256KB, 128KB, 64KB, 32KB write-back cache or direct map cache with fast burst mode and posted write buffer.
- . 1/2/4/5/8/16/20/32/64/80/128 MB memory size options.
- . UNIchip Single Chip solution.
- . Fast reset and gate A20 switch features.
- . Speaker, keylock, reset, power, turbo and turbo light connectors.
- . Hardware and software turbo function.
- . Real time clock with an rechargeable battery on-board.
- . AMI BIOS.
- . 3/4 baby AT size 26 X 22 cm .
- . Designed to be mounted in standard PC/AT type enclosure.
- . Page interleave mode.
- . Shadow RAM
- . Video cache.
- . Fully programmable timing parameters.
- . Cache RAM read/write 0 wait state.



2-2 JUMPERS SETTINGS

JP1: DISPLAY MODE SELECT

OPEN	Monochrome
CLOSE	Color

JP2 : CMOS OPERATION SELECT

1-2	Normal operation
2-3	Discharge CMOS

JP4 : CPU TYPE SELECT

80486DX/DX2	1-2,4-5,6-7
80486SX	5-6
80487SX	2-3,4-5,6-7

JP29, JP30, JP31 : CPU SPEED SELECT

	JP29	JP30	JP31
20MHz	OPEN	CLOSE	CLOSE
25MHz	CLOSE	OPEN	CLOSE
33MHz	CLOSE	CLOSE	OPEN
50MHz	OPEN	CLOSE	OPEN
486DX2-50	CLOSE	OPEN	CLOSE
486DX2-66	CLOSE	CLOSE	OPEN

Note: If there are two oscillators (Y3 and Y5) instead of AV9107 (U48) and crystal (Y4) on the motherboard, you should change the oscillator Y3 instead of changing jumper (JP29, JP30, JP31) for various CPU speed. The CPU speed must match the oscillator speed.

CPU	OSC
486SX-20/25/33	20/25/33MHz
486DX-25/33/50	25/33/50MHz
486DX2-50/66	25/33MHz

JP6, JP7, JP9, JP11: CACHE SIZE SELECT

	JP6	JP7	JP9	JP11
32K	OPEN	OPEN	OPEN	2-3
64K	OPEN	CLOSE	OPEN	1-2
128K	OPEN	CLOSE	CLOSE	1-2,3-4
256K	CLOSE	CLOSE	CLOSE	1-2,4-5

JP40, JP41, JP42, JP43, JP44: VESA LOCAL-BUS SELECT

VL-Bus	MASTER	JP40	JP41	JP42	PAL (U50)
VL-Bus	MASTER	OPEN	OPEN	OPEN	Insert the PAL
VL-Bus	SLAVE	CLOSE	CLOSE	CLOSE	Pull out the PAL

JP43

1-2

Adjusted VL-BUS clock

2-3

Normal VL-BUS clock

JP19

CLOSE

CPU clock > 33MHz

OPEN

CPU clock ≤ 33MHz

JP44

1-2

VL-BUS MASTER and CPU clock >33MHz

2-3

Others

JP20

OPEN

0WS write for VL-Bus

CLOSE

1WS write for VL-Bus

2-3 INSTALLATION OF RAM

- Note:
1. 70ns DRAM is required.
 2. No jumper setting is required for any RAM configuration.
 3. Each bank requires four SIMM modules.
 4. Possible RAM configurations are as follows:

RAM SIZE	RAM TYPE OF BANK0	RAM TYPE OF BANK1
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1MB	256KB X 9 SIMM	
2MB	256KB X 9 SIMM	256KB X 9 SIMM
4MB	1MB X 9 SIMM	
5MB	256KB X 9 SIMM	1MB X 9 SIMM
8MB	1MB X 9 SIMM	1MB X 9 SIMM
16MB	4MB X 9 SIMM	
20MB	4MB X 9 SIMM	1MB X 9 SIMM
32MB	4MB X 9 SIMM	4MB X 9 SIMM
64MB	16MB X 9 SIMM	
80MB	16MB X 9 SIMM	4MB X 9 SIMM
128MB	16MB X 9 SIMM	16MB X 9 SIMM

2-4 INSTALLATION OF SRAM (CACHE MEMORY)

Refer to section 2-2 for jumper setting

Possible SRAM and TAG RAM configurations are as follows:

	BANK0 (U38,U39,U41,U43)	BANK1 (U36,U37,U40,U42)	TAG RAM (U33)
32KB	8K X 8		8K X 8
64KB	8K X 8	8K X 8	8K X 8
128KB	32K X 8		8K X 8
256KB	32K X 8	32K X 8	32K X 8

CHAPTER 3 FAST SETUP

1. According to the CPU type and CPU clock, set the jumper JP4, JP29, JP30, JP31, JP44.
2. According to the CACHE MEMORY SIZE, Set the jumper JP6, JP7, JP9, JP11.
3. Press to enter the BIOS SETUP main menu after turning on the power supply.
4. Load the AUTO CONFIGURATION WITH BIOS SETUP DEFAULT on main menu.
5. Set the time, date, floppy disk drive and hard disk type in STANDARD CMOS SETUP.
6. Set the SRAM READ, SRAM WRITE, SRAM BURST, DRAM Read/Write and AT BUS CLK in ADVANCED CHIPSET SETUP as follows (20ns SRAM):

	SRAM READ	SRAM WRITE	SRAM BURST	DRAM R/W	ATBUS CLK
486SX-20	0	0	ENABLED	1	CLK/2.5
486SX/DX-25, 486DX2-50	0	0	ENABLED	1	CLK/3
486SX/DX-33, 486DX2-66	0	0	ENABLED	1	CLK/4
486DX-50	1	1	DISABLED	2	CLK/6

7. Write to CMOS and Exit.