ATARI Computer GmbH
Technologiezentrum

PC 5

AMI-386 BIOS PLUS

USER MANUAL

American Megatrends Inc.
4025 Pleasantdale Road, Ste 320
Atlanta, Ga - 30340

Ph. (404) 263 8181
Fax. (404) 263 9381

Table Of Contents

Section 1

Section 2

Section 1

1.0 BIOS Overview

This guide explains how to :

a) Install the AMI-386 BIOS .
b) Use the built-in Set-up Procedure.
c) Select the Clock Speed / Wait States through the Keyboard.
d) Interpret the errors reported by the AMI-BIOS.
e) Use the 3 1/2" floppy drive support effectively.

2.0 Installing the AMI-386 BIOS

Skip this paragraph if the BIOS is already plugged on the MotherBoard.

Before you begin the installation ensure the following:
i) The Board is powered down.
ii) ROM's are susceptible to static electricity. So observe the following precautions when you handle a ROM :
a) Unpack the ROM's on a ground connected anti-static mat.
b) Wear an anti-static wristband, grounded at the same point as the anti-static mat.
(A cheaper solution is to use a sheet of conductive aluminium foil grouded through a 1 Mega-ohm resistor instead of an anti-static mat. Similarly, a strip of conductive aluminium foil wrapped around the wrist and grounded through a 1 Megaohm resistor will serve the purpose of a wrist band.)

Ensure that the ODD & EVEN BIOS go into their respective sockets.

3.0 Starting Up The System

Power up the system and wait for the BIOS to show up the BIOS activity on the screen.

4.0 Memory Test Bypass

The BIOS performs diagnostics of the system and displays the size of the memory being tested.

Note that you can bypass the memory test by pressing the <ESC> key. This option would be quite useful when the memory on the system is quite large. You should hit the <ESC> key when the message Press <ESC> Key to bypass MEMORY test appears on the screen.

Also note the Ref. number at the bottom of the screen. Make a note of this number before you call Customer Support at AMI for assistance with the BIOS.

5.0 CMOS Setup

Immediately after the memory and cache test, you will get the following prompt on the screen :

Press <DEL> key to run SETUP Utility

Hit <DEL> key to get into the Setup Mode. Note that <DEL> key will get you into the set-up mode only when the message :
Press <DEL> key to run SETUP Utility, is displayed on the screen.

If you hit <DEL> key the following message appears on the screen:
WANT TO RUN SETUP UTILITY (Y/N)?

If you hit <Y> or <y> and the <ENTER> key you have the Setup screen.

5.0.1 Time/Date Setup

The Setup screen looks like below :

C M O S S E T U P
Curret date is : XX-XX-XXXX
Enter new date (MM-DD-YYYY)?

To this question you would have to enter the date in the format shown on the screen.

If you feel that the current date should remain unchanged, you would just have to hit the <ENTER> key. In such a case the new date is set to the same value as the current date.

The next question you have on the screen is:

Current time is :XX:XX:XX
Enter new time (HH:MM:SS)?

To this question you key in the time in the format defined. Press <ENTER> key alone if the current time is right.

As soon as you have done this the BIOS shows you the type of the display on your system.

After that, the setup takes two differet paths depending upon the CMOS being initialized or uninitialized.

5.0.2 CMOS Initialized

Under these conditions you would see the following messages :

Fixed disk drive C type : X (if installed else Not Installed.)
- Fixed disk drive D type : X (if installed else Not Installed.)

Diskette drive A is 3 1/2"
Diskette drive B is Double Sided (Other options as above)
Base Memory Size is : XXX KB
Expansion memory size is : XXXX KB

Are these options correct (Y/N)?

Note that the information about Drive A indicates 3 1/2", as CMOS had been set earlier to reflect this status. If on the contrary, CMOS had been set for a 1.2 MB drive, the message in place of 3-1/2" it would be High Capacity.

If you feel that the information displayed above is right, hit <Y> and the <ENTER> key to proceed to system boot with the new information.

5.0.3 CMOS Uninitialised

5.0.3.1 Disk Drive Type Definition

In this case you would have to enter the type of the fixed Drive C in response to the message :

**** WARNING ****
Entering the wrong disk drive TYPE
causes improper operation of the disk.
If disk not installed press <RETURN>
For disk TYPE details press <ESC>

Enter disk drive C type (1-47)?

Note that the disk type details are only a key stroke away. Hit <ESC> key to find for yourself. You could always come back by hitting <ESC> again. Refer to Appendix B for drive details.

Once you have convinced yourself about the drive type enter the appropriate number and hit <ENTER>.

Note that pressing <ENTER> key alone indicates the absence of the Drive C.

You would then be asked to enter the type of the disk Drive D. The procedure for doing this is the same as that for Drive C. Remember if you do

not have disk Drive D on your system, you just have to hit the <ENTER> key.

6.0 Floppy Drive Type Definition

Diskette drive A is 3 1/2" (Y/N)?

The above question is asked if the drive has been found to have 80 tracks. Since a drive with 80 tracks could either be a
- high capacity i.e 1.2 MB drive
- or 3 1/2" i.e 720 KB drive,

you would have to answer this question.
By entering <N> or <n> you can select the high capacity drive. Alternatively enter <Y> or <y> to select a 720 KB drive. This question could come up for the case of drive B as well provided it has been detected as a 80 track drive by the BIOS.

If you hit the <ENTER> key alone, the BIOS assumes the drive to be a 1.2 MB drive.

At this point you have entered all the information the BIOS requires for starting up the system.

BIOS detects a few details by itself, e.g. the diskette drive type in case of a 360 KB drive as shown below:

Diskette drive B is : Double Sided (Other options as above)
Base Memory Size is : XXX KB
Expansion memory size is : XXXX KB

Are these options correct (Y/N)?

If you are convinced at this stage that all the information you have entered upto this point is right, hit <Y> or <y> key followed by <ENTER> key. When you do this the BIOS goes all over again to boot up the system with the information specified.

However, if you would like to modify some information, then you should hit either <N> or <n> key followed by enter. You would now go through the setup all over again.

7.0 Summary of Set-up

The Set-up screen thus requires you to set
a) Date.
b) Time.
c) Hard Disk Type For Drive C (if present).
d) Hard Disk Type For Drive D (if present).
The Set-up procedure also automatically detects the following:
a) Type Of Display Card.
b) Size Of Real Memory.

c) Size of Memory beyond 1 MB.
d) Presence of 360 kb floppy drives.
e) Presence of a 80287.

Also, if a second Hard Disk drive is physically connected but the CMOS is not set for this Drive D, the BIOS informs you about the same and gives you a chance to configure the drive through SETUP.

Having setup the CMOS, the BIOS runs through the diagnostics again, tests the memory, sets up the devices configured and proceeds to boot.

Note that the Set-up option is available even after a soft reset.

8.0 When does the BIOS prompt you to run Set-up?

The BIOS prompts you to run Set-up under the following conditions
a) CMOS options not set.
b) Display Configuration Mismatch.
c) Memory Size mismatch.
d) Hard Disk Set-up error.
e) CMOS battery is low.
f) An additional hard disk presence is detected.

9.0 Selecting Clock Speed/Wait States

AMI-BIOS allows you to change Clock Speeds and Wait States through the keyboard at any time. Following are the key combinations and their meanings :-

Key Combinations	Meaning
1. <CNTRL><ALT><+>	Switch to high speed.
2. <CNTRL><ALT><->	Switch to low speed.
3. <CNTRL><L.SHIFT><ALT><+>	Switch to zero Wait state.
4. <CNTRL><L.SHIFT><ALT><->	Switch to one Wait state.

10.0 Errors Reported By AMI-BIOS

AMI-BIOS performs various diagnostic tests at the time the system is powered up. Whenever an error is encountered during these tests, either you hear a few short beeps or see an error display on your monitor. If the error occurs before the display device is initialised the system reports the error by giving a number of short beeps.

If the error is FATAL then system halts after reporting the FATAL error. If the error is NON-FATAL the process continues after reporting the NON--FATAL error.

10.0.1 Fatal Errors

Beep Count	Meaning
1	DRAM refresh failure .
2	Parity Circuit failure.
3	Base 64KB RAM failure.
4	System Timer failure.
5	Processor Failure.
6	Keyboard Controller - Gate A20 error.
7	Virtual Mode Exception Error.
8	Display Memory R/W Test Failure. (*)
9	ROM-BIOS CheckSum Failure.

(*) Non-Fatal Error.

10.0.2 Error Messages

Fatal Errors

1. Channel - 2 of Timer Not functional.
2. Stray Interrupt sensed in controller.
3. Interrupt controller #2 not functional.

Non-Fatal Errors

1. Keyboard Error.
2. Keyboard/Interface Error.
3. CMOS battery state low.
4. CMOS system options not set.
5. CMOS checksum failure.
6. CMOS memory size mismatch.
7. CMOS system time and date not set.
8. CMOS display configuration mismatch.
9. Display setting not proper.
10. Keyboard is locked ..... Unlock it.
11. Floppy disk controller failure.
12. Hard disk unit 0 error.
13. Hard disk unit 1 error.
14. Hard disk unit 0 failure.
15. Hard disk unit 1 failure.
16. Hard disk unit 1 is not defined in CMOS.
17. Cache Memory Bad - Do Not Enable Cache.

11.0 Use of 3 1/2" Support Effectively

DOS 3.20 provides support for 3 1/2" drives. For this purpose it needs support from the ROM BIOS. AMI-BIOS release date 12/03/86 onwards provides the necessary support.

The 3 1/2" drive can be freely configured as Drive A or Drive B with this

BIOS. Thus it is possible to boot off directly from a 3 1/2" drive.

Earlier versions of DOS would require the use of DRIVER.SYS to provide the necessary support.

- A few points would have to be kept in mind when you use the 3 1/2" drive and a 1.2 MB together. Ensure that when you perform the Setup you define the drives correctly. Incorrect definition could make the drive unusable.

The table below describes the valid combinations on a AT:

CMOS Status	Physical Drive Status	Functional
1.2 MB	1.2 MB	YES
3 1/2"	3 1/2"	YES
Undefined	1.2 MB	YES

The remaining combinations are invalid. Please make a note of these combinations before you call us for help.

Should you feel that you need assistance with the BIOS at any stage, call AMI Tech. Support at (404) 263-8181.

Section - 2

1.0 Overview

AMI-386 BIOS PLUS provides the following in a ROM :

a) Field proven extensively used AMI-386 BIOS.
b) Built-in CMOS setup utility with support for 47 Disk drive types, 3 1/2" Floppy Disk drives & Enhanced Keyboard.
c) A Diagnostics program - superior to the IBM Advanced Diagnostics - with special enhancements & a user-friendly interface.
d) A Built-in Calendar.

This portion of the manual explains how to use the Diagnostics program alone.

386 BIOS PLUS comes in 256K ROM chips. Hence make sure that when you plug these ROMs that the DIP Switch on the System Board is set to indicate 256K Chips.

2.0 Selecting The Diagnostics Option

Hit the <DEL> key on the numeric keypad when you see the following message at the time of system startup:

Press <DEL> Key to run SETUP or DIAG

The above message is seen on the 4th line of the screen.

Hitting <DEL> key brings the following message after a few seconds on the screen

Want to run SETUP or DIAG (Y/N)?

If you answer <Y> or <y> followed by <ENTER> then you would be asked to select either Setup or Diagnostics as shown below:

SETUP or DIAG (1/2)?

Hit <1> to use the built-in SETUP option.

Hit <2> to use the Advanced Diagnostics option.

3.0 Diagnostics Menu

Note the following in the Diagnostics Opening Menu :

a) The Guide Line in Reverse Video specifying the usage of the Cursor Keys, <ENTER> & <ESC> key.

b) The Configuration of the system in the "Devices Present" box.

c) The Real Time Clock ticking away at the right hand top corner of the screen.

d) Diagnostics Options Line - Hard Disk, Floppy, Keyboard, Video & Miscellaneous Diagnostics.

e) Hard Disk Diagnostics Options Window - detailing the various hard disk diagnostics that are available.

f) Note that the Block Cursor is on the Hard Disk & the first option under hard disk diagnostics - Hard Disk Format.

4.0 Key Conventions

Use the Left & Right arrow keys to move in the Diagnostics Options Line.

Use the Up & Down arrow keys to move within a Diagnostics Options Window.

Use the <ENTER> key to select the option in the Diagnostics Options Window.

Use <ESC> key to abort & return to previous menu.

5.0 Diagnostics Options Window

The individual diagnostics options are as below :

1. Hard Disk options.
2. Floppy Disk drive options.
3. Keyboard options.
4. Video options.
5. Miscellaneous options.

Hard Disk Diagnostics

1.0 Using Hard Disk Options

The Hard Disk options discussed below fall in two categories :

a) Destructive Operation - The data on the Hard Disk is lost.
b) Non-destructive Operation - The data on the Hard Disk is undisturbed.

The list below gives the various Hard Disk Options & the category they fall in :

a) Hard Disk Format	-	Destructive Operation.
b) Auto Interleave	-	Destructive Operation.
c) Media Analysis	-	Destructive Operation.
d) Performance Test	-	Non-destructive Operation.
e) Seek Test	-	Non-destructive Operation.
f) Read/Verify Test	-	Non-destructive Operation.
g) Check Test Cylinder	-	Data on the Test Cylinder alone is lost.

All the options under Hard Disk Diagnostics require more or less the following inputs:

a) Disk Drive
b) Drive Type
c) Interleave Factor
d) Bad Track List
e) Start Cylinder
f) End Cylinder
g) Start Head
h) End Head

All the above input fields have a default value. Thus a user need not necessarily key-in all the inputs.

We shall discuss the inputs required & their meaning for Hard Disk Format Option. This discussion can however be extended for the rest of the Hard Disk Options.

2.0 Hard Disk Format Option - (Destructive Operation)

Figs 6 & 7 reflect the various screens the user goes thru' when this option is selected.

Note that in case of a single drive System the disk drive for the operation is assumed to be drive C.

a) Drive Type Definition

The default value for the drive type is the SETUP value set during the CMOS setup.

However if the drive was not set during CMOS Setup, the user now has an option of setting the drive to be one among the 46 standard Disk drive types.

Note that all the information about the drive unfolds when the disk drive type is being chosen.

If the disk drive type does not fall within the 46 standard disk types, use the USER option to define your own parameters for the drive.

Note that this USER definition is valid only as long as the Diagnostics is in effect. This feature is provided for you to test a disk drive, the definition for which is not available in the ROM.

b) Interleave Factor

Choose an optimum interleave factor. Refer to the Appendix - A for details on how to decide on an Optimum interleave.

The default value for the interleave factor is 3.

c) Mark Bad Tracks

If the manufacturer has defined certain bad patches on the disk, enter <Y> to this question.

The user then goes into a menu which allows for complete editing of the bad track list.

Exit Bad track entry by hitting <ESC> or selecting the Save And Exit option. Note the usage of <ESC> key here.

The default answer for this question is <N>.

d) Cylinder Number

Enter the Start & End Cylinder Number if you want to override the defaults.

The same is true for Start & End Head number.

The default value for the start Cylinder & Head is 0 and that of the End cylinder & head is the value of the maximum cylinder & head respectively.

e) Proceed

If all the entries are correct, you could hit <Y>. Else you could say <N> & go over all the entries again.
The default answer is <N>.

f) Warning

If you had hit <Y> to the previous question, you get a WARNING message . You could proceed to format if you are absoulutely sure about the information you have entered upto this point.

g) Activity Screen

PLUS then proceeds to format the Hard Disk with the specified parameters. While it is formatting PLUS displays the Operation in progress, the Cylinder & Head No. that is being formatted.

You could always hit <ESC> key to abort the format operation.

2.0 Auto Interleave Option - (Destructive Operation)

This is the most powerful feature which enables you to get the peak performance out of your Hard Disk.

With this feature you need not speculate about the value of the Interleave Factor. PLUS is entrusted with the job of finding the optimum Interleave value by a trial & error method & formatting the Hard Disk with this value.

Discover the big advantage with this feature.

3.0 Media Analysis Option - (Destructive Operation)

Media analysis performs the following operations on the Hard Disk:

- Preformats the Hard Disk with specified parameters like Format Option.
- Analysis the surface of the Hard Disk for any errors & makes a note of them.
- Marks the Bad Patches.

This takes quite some time & for best results this test should run uninterrupted.

The parameters required for this are to be inputted in the same way like the Format Option.

a) Drive Type Definition

The default value for the drive type is the SETUP value set during the CMOS setup.

However if the drive was not set during CMOS Setup, the user now has an option of setting the drive to be one among the 46 standard Disk drive types.

Note that all the information about the drive unfolds when the disk drive type is being chosen.

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Choose an optimum interleave factor. Refer to the Appendix - A for details on how to decide on an Optimum interleave.

The default value for the interleave factor is 3.

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If the manufacturer has defined certain bad patches on the disk, enter <Y> to this question.

The user then goes into a menu which allows for complete editing of the bad track list.

Exit Bad track entry by hitting <ESC> or selecting the Save And Exit option. Note the usage of <ESC> key here.

The default answer for this question is <N>.

d) Cylinder Number

Enter the Start & End Cylinder Number if you want to override the defaults.

The same is true for Start & End Head number.

The default value for the start Cylinder & Head is 0 and that of the End cylinder & head is the value of the maximum cylinder & head respectively.

e) Proceed

If all the entries are correct, you could hit <Y>. Else you could say <N> & go over all the entries again.
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- Preformats the Hard Disk with specified parameters like Format Option.
- Analysis the surface of the Hard Disk for any errors & makes a note of them.
- Marks the Bad Patches.

This takes quite some time & for best results this test should run uninterrupted.

The parameters required for this are to be inputted in the same way like the Format Option.

4.0 Performance Test - (Non-Destructive Operation)

This test enables the user to check out his disk performance. The critical factor in deciding the disk performance is the Interleave Factor. Changing the Interleave factor can bring about drastic changes in Disk Performance.

This test determines the Data Transfer Rate & the Track to Track Seek time. Data Transfer Rate is measured in the units Kilobytes/Second & the Track to Track seek time in milliseconds.
Higher value for Data transfer rate implies a better disk performance & lower value of track to track seek time indicates a better disk.

Refer to Appendix A for more on Interleave Factor & how to choose the same for best Disk Performance.

5.0 Seek Test - (Non-Destructive Operation)

This test checks the seek capability of the HardDisk on the specified Cylinder & Head range. First a sequential seek is performed & then a random seek is performed.
Any errors during this test are reported.

6.0 Read/Verify Test - (Non-Destructive Operation)

This test performs sequential & random read & verify operation on the specified Cylinder,Head range.

7.0 Force Bad Tracks - (Destructive Operation)

This operation enables an User to define a set of tracks as bad. Certain specific applications require this option.

Floppy Diagnostics

All the options under floppy diagnostics require more or less the require the following inputs :

a) Drive No.
b) Start Track No.
c) End Track No.

As in the case of hard disk the list below gives the effect of each of the diskette tests :

a) Diskette Format - Destructive.
b) Speed Test - Non-destructive.
c) Random R/W Test - Destructive.
d) Sequential R/W Test - Destructive.
e) Disk Change Line Test - Non-destructive.

1.0 Diskette Format - (Destructive)

This test allows an user to check out the NEC 765 controller's abilities to format a diskette.

The user need not be bothered about the drive or the diskette in the drive. PLUS automatically determines the best way a diskette can be formatted for reliability. e.g. In case of a 1.2MB drive the user need not specify whether the diskette to be formatted is 1.2 MB or 360 KB capacity. PLUS finds the most reliable format automatically.

Note that this test does not write a DOS format on the diskette.

2.0 Drive Speed Test - (Non-destructive)

This test determines the speed of rotation of the drive. Please note that the following are the allowable speeds for the various drives :

a) 1.2 MB drive -360 rpm for a 1.2 Mb diskette in it.
-300 rpm for a 360 Kb diskette in it.

b) 360 KB drive -300 rpm.

c) 720 KB drive -300 rpm.

Allow for a tolerance of 1% on all the speeds.
Ensure that the diskette is formatted before performing this test.

3.0 Random Read/Write Test - (Destructive)

This test performs a random read/write operation on the diskette & thus checks out the random seek capability of the drive.

Again ensure that the diskette is formatted before performing this test.

4.0 Sequential Read/Write Test - (Destructive)

This test performs a Sequential read/write operation & checks out the sequential seek, read & write capability of the drive.

This test requires a formatted diskette.

5.0 Disk Change Line Test - (Non-destructive)

This test is valid only for drives with the disk change line feature namely

- 1.2 Mb drive
- 720 Kb or 3 1/2" drive.

This test checks whether the status of the disk change line changes when the diskette is removed/inserted in the drive.

This test requires a formatted diskette.

Keyboard Diagnostics

There are two types of diagnostics performed on the keyboard/keyboard controller.

They are :

a) Controller Test.
b) Scan/ASCII Code Test.

1.0 Controller Test

This test exercises the keyboard controller & the keyboard status flags & takes about 2 minutes. Any error resulting from this test is reported.

Observe the CAPS, NUM & SCROLL LED's going on & off during the course of this test.

2.0 Scan / ASCII Code Test

Upon invoking this test a keyboard layout is shown on the screen. This keyboard layout might not necessarily correspond with your keyboard.

The objective of this test is to determine whether the keys depressed match with their scan code.

Thus every time a key is depressed the scan code & the ASCII code of the key is shown.

Use <CNTRL><BREAK> key to abort this test.

Function keys 11 & 12 in an Enhanced keyboard cannot be checked out by this test.

Video Diagnostics

Video diagnostics includes the following :

a) Sync Test - Checks the Sync capability.
b) Adapter Test - Performs test on the Display Memory.
c) Attribute Test - Checks the attributes of the Display memory.
d) 80 x 25 Display Test - Checks the 80 x 25 character set of the display adapter.

The video diagnostics requires very little input & the results can be visually observed.

Miscellaneous Diagnostics

This includes the following tests :

a) Serial Communication Port Test.
b) Printer Port Test.

1.0 Serial Communication Port Test

This test requires a special RS-232C connector to be plugged on to the port.

The details of this connector are as below :

- RD & TD Shorted.
- DSR & DTR Shorted.
- CTS & RTS Shorted.

This test exercises the port for different :

- Baud Rates
- 7 Bit / 8 Bit &
- Odd / Even Parity

The results of the test are shown on the screen.

2.0 Printer Port Test

This test writes a pattern on the Printer & the results are observed on the Printer.

Appendix A

1.0 Interleave Factor - What is it ?

To understand the meaning of Interleave associated with Hard Disks, we shall take you thru' an analogy. We hope we have made the meaning clear when we finish the analogy.

Consider the game of a roulette where a round table is set in motion & people wait for the motion to stop on their lucky number.

We shall add a slight twist to this game.

Assume we have 17 sectors on the roulette round table & that we have 17 coins numbered & stacked up in the order 1 thru' 17 with coin 1 at the top.

We shall now set the round table in motion at a reasonable speed & give ourselves the task of placing the coin from the stack pile on every sector taking the minimum time and remaining static at one place during the course of the game.

Assume you have placed coin 1 in a certain sector. By the time you pick up the next coin & place it, the immediate sector following coin 1 would have passed you. So what you would then do, is to place it on the sector just passing by.

Thus after placing the coins in all the sectors, you should stop the roulette table & look at coins numbers in the contiguous sectors.

You are sure to find that they are not in an increasing order. You soon realise that this disorder is due to the fact that the game requires you to place all the coins in minimum time.

If you had wanted the coins in an order, you would have had to wait for at least 17 revolutions before placing all the coins.

The average number of contiguous sectors between a sector occupied by coin 'n' & by coin 'n+1' can be termed as Interleave factor.

In this analogy the Hard Disk is the roulette table in motion at a constant speed of 3600 rpm & the person can be visualised as the head & the related data transfer hardware.

Information is organised in sectors & the sectors are accesed by their numbers. Thus using a specific interleave to number the sectors helps in achieving a data tansfer rate change.

For a Hard disk with factory specified access times, the only factor in the control of the user is the Interleave factor.

We realise this & we have the Auto Interleave feature which does exactly this.
Thus it is important that the value chosen gives the best performance.

Appendix - B

Please turn over for Appendix - B.

Type	Cylinders	Heads	Write-precomp	Landing-zone	Capacity
1	306	4	128	305	10 MB
2	615	4	300	615	21 MB
3	615	6	300	615	31 MB
4	940	8	512	940	64 MB
5	940	6	512	940	48 MB
6	615	4	NONE	615	21 MB
7	462	8	256	511	31 MB
8	733	5	NONE	733	31 MB
9	900	15	NONE	901	115 MB
10	820	3	NONE	820	21 MB
11	855	5	NONE	855	36 MB
12	855	7	NONE	855	51 MB
13	306	8	128	319	21 MB
14	733	7	NONE	733	44 MB
15	000	0	000	000	00 MB
16	612	4	ALL CYLS.	663	21 MB
17	977	5	300	977	42 MB
18	977	7	NONE	977	58 MB
19	1024	7	512	1023	61 MB
20	733	5	300	732	31 MB
21	733	7	300	732	42 MB
22	733	5	300	733	31 MB
23	306	4	ALL CYLS.	336	10 MB
24	925	7	ALL CYLS.	925	56 MB
25	925	9	NONE	925	72 MB
26	754	7	754	754	46 MB
27	754	11	NONE	754	72 MB
28	699	7	256	699	42 MB
29	823	10	NONE	823	71 MB
30	918	7	918	918	55 MB
31	1024	11	NONE	1024	98 MB
32	1024	15	NONE	1024	133 MB
33	1024	5	1024	1024	44 MB
34	612	2	128	612	10 MB
35	1024	9	NONE	1024	80 MB
36	1024	8	512	1024	71 MB
37	615	8	128	615	42 MB
38	987	3	987	987	25 MB
39	987	7	987	987	60 MB
40	820	6	820	820	42 MB
41	977	5	977	977	42 MB
42	981	5	981	981	42 MB
43	830	7	512	830	50 MB
44	830	10	NONE	830	72 MB
45	917	15	NONE	918	115 MB
46	000	00	000	000	00 MB

AMI-386XT SERIES-4 MANUAL

American Megatrends, Inc.
Ph. (404) 263-8181
4025 Pleasantdale Road
Suite 350, Atlanta, GA 30340

CONTENTS

Important Notice

AMI is not responsible for any errors or omissions in writing this manual. AMI reserves the right to change, modify or append any part or section of this manual at any time.

Introduction to The Manual

Section - 1	It is essential to go through this section and follow the instructions for proper installation of the board.
Section - 2	It is essential to go through this section to familiarize yourself with the AMI-386 BIOS.
Section - 3	You are advised to go through this section to familiarize yourself with the motherboard.
Section - 4	You may skip this section unless you need detailed technical information. All port descriptions required for personalized software developement are given in this section.
Section - 5	You may skip this section if you are familiar with the IBM AT[1] I/O Channel and Connector Specifications.
Section - 6	Read this section to get the information about the built-in Advanced Diagnostics features.

[1] IBM AT is a registered trademark of International Business Machine Corporation.

SECTION - 1

Unpacking and Installation

1.1 Unpacking the AMI-386XT Motherboard

Your AMI-386XT motherboard contains sensitive electronic components, which can be easily damaged by static electricity.

In this section, we describe the precautions you should take while unpacking, as well as during installation. It is very important that the instructions be followed correctly, to avoid static damage, and to successfully install the board.

1) The motherboard should be left in its original packing until the time when it is to be installed.

2) Unpacking and installation should be done on a ground connected anti-static mat. The operator should be wearing an anti-static wristband, grounded at the same point as the anti-static mat.
(A cheaper solution is to use a sheet of conductive aluminum foil grounded through a 1 Mega-ohm resistor, instead of the anti-static mat. Similarly, a strip of conductive aluminum foil wrapped round the wrist and grounded through a 1 Mega-ohm resister will serve the purpose of a wrist-band.)

Inspect the cardboard carton for obvious damage. In case damage is detected, call us, we are ready to help you.

Inside the carton, the card is packed in an anti-static bag, and sandwiched between sheets of sponge. Remove the sponge and lift out the anti-static bag with the card. Extract the card and place it ONLY ON A GROUNDED ANTI-STATIC SURFACE component side up.

Save the original packing materials, in case the card has to be shipped again. Shipping it in any other type of packing may damage the card.

Again inspect the card for damage. Press down all the ICs mounted on sockets to make sure they are properly seated.
DO NOT APPLY POWER TO THE BOARD IF IT HAS BEEN DAMAGED.

You are now ready to install your AMI-386XT motherboard.

1.2 Installing the AMI-386XT motherboard.

Mounting the Motherboard in the chassis.

Before attempting to mount the board in the chassis, take a look at Fig.I to aquaint yourself with the locations of stand-offs and mounting screws. (Stand-offs and mounting screws are supplied with the chassis and NOT WITH THE MOTHERBOARD.)

Note: The mounting hole pattern on AMI-386XT motherboard is interchangable with that of the IBM AT/XT motherboard. It is assumed that the chassis is designed for standard IBM AT/XT motherboard mounting.[1]

CAUTION: During mounting and installation static protection is to be maintained as during unpacking.

Place the chassis on the anti-static mat and remove the cover. Take the plastic clips, nylon stand-offs and screws, for mounting the motherboard, and keep them separate. (Look into the chassis manufacturers booklet for instructions.)

The chassis has to be connected to ground to avoid static damage to the board, while mounting. To ground the chassis, connect an alligator clip with a wire lead to any unpainted part of the chassis. Ground the other end of the lead at the same point as the mat and the wristband. Rotate the chassis so that the front is to your right and the rear to your left. The side facing you is where the motherboard is to be mounted and the power supply will be mounted on the far side.

Take the four nylon stand-offs and push them into the holes provided for them in the motherboard see Fig. I) from the solder side. The stand-offs will lock in place.

On the chassis, locate the slots where the stand-offs go in. Now, hold the motherboard (component side up) with the edge with three stand-offs towards you, and the edge with no stand-offs, away from you. (The edge connectors on the motherboard, for the adaptor cards, should be on your left.) Carefully slide the board into the chassis, making sure that the stand-offs go into the slots provided for them (see Fig. II). If the stand-offs are properly locked, the board should not slide right or left (forwards

[1] IBM AT is a registered trademark of International Business Machine Corporation.

and backwards with respect to the chassis) and should be level with the chassis. The far edge of the board should fit into the slots in the plastic clips. In case the board is not sitting properly, SLIDE IT OUT COMPLETELY and try again.

Now, put the two motherboard mounting screws in the holes provided for them (Fig. I) and tighten them. (You may have to shift the board slightly to align the screw mounting holes on the motherboard with those on the chassis.)

Now that the motherboard is properly mounted, the connectors have to be put in and the option jumpers and DIP switches set to your requirement.

Figure III gives you the positions of the connectors, the option jumpers and the DIP switches on the card. The following table describes the options that can be selected.

NOTE: The options are factory set to the default selections and these options are indicated in the table by underscoring.

1.3 List of Jumper Options and Switch Settings for AMI-386XT

J1: TURBO LED

J2: 2 pin BERG strip
When shorted gives hard reset to the system

J4: 3 pin single in line .
Short 1-2 if using 32K X 8 EPROM's (eg. 27256)
Short 2-3 if using 16K X 8 or 8K X 8 EPROM's (eg 27128 or 2764)

J19: 4 pin single-in-line BERG
Speaker Connector

J20: 5 pin single-in-line BERG
Keyboard Lock Connector

J21: 4 pin single-in-line BERG
Battery Connector for RTC/CMOS

J22: 5 pin DIN socket
Keyboard Connector

J23-28: 62 pin I/O Connectors

J31-34: 36 pin I/O Connectors

J39: 80 pin I/O Connector for 32 bit memory

PS8-9: 6 pin Power Supply Connectors

SW: 5 bit slide switch

5	Video adapter card option
4	Power on system clock frequency
3	Numeric processor option
2	512k to 640k cache on/off option
	On board EGA BIOS option

ON-BOARD EGA BIOS OPTION

SW1	ON/OFF	EPROM MAP	DESCRIPTION
	ON	0C0000-0C7FFF 0F0000-0FFFFF	On Board EGA BIOS enabled(32 bit access)
	OFF	0E0000-0FFFFF	BIOS On EGA Card selected(8 bit access)

512K TO 640K CACHE ON/OFF OPTION

SW2	ON/OFF	DESCRIPTION
	ON	If 512KB below 1MB option is selected in 32bit memory card then 512KB to 640KB memory on the I/O expansion BUS will be cached if present
	OFF	If 512KB below 1MB option is selected in the 32bit memory card then 512KB to 640KB memory on the I/O expansion BUS will not be cached. All other memory will be cached.

80387 NUMERIC PROCESSOR PRESENT/NOT PRESENT OPTION

SW3	ON/OFF	DESCRIPTION
	ON	Numeric coprocessor physically not present on the board. This switch should always be on when the numeric processor is not present.
	OFF	80387 is physically present on the board.

POWER-ON SYSTEM CLOCK FREQUENCY SELECTION

SW4	ON/OFF	DESCRIPTION
	ON	POWER ON System clock frequency is 6MHz. However the clock can be changed to 16 MHz using keyboard clock switching option.
	OFF	POWER ON System clock frequency is 16MHz

VIDEO ADAPTER CARD OPTION

SW5	ON/OFF	VIDEO ADAPTER CARD
	ON	COLOR GRAPHICS CARD
	OFF	MONOCHROME DISPLAY ADAPTER

C35: Variable Capacitor

The system board has a variable capacitor. Its purpose is to adjust the 14.31818 MHz oscillator (OSC) signal that is used to obtain the color burst signal required for color televisions.

MEMORY BOARD SWITCH SETTING

SWITCH	OPTION	STATE	DESCRIPTION
SW1	BANK SELECT	ON	Two 32bit memory bank present
		OFF	One 32bit memory bank present
SW2	MEMORY SIZE BELOW 1MB	ON	640K below 1MB
		OFF	512K below 1MB
SW3	384KB MEMORY ABOVE 1MB OR 2MB	ON	Enable
		OFF	Disable

SECTION 2

BIOS Overview

This guide explains how to :

a) Install the AMI-386 BIOS on the AMI-386 Motherboard.
b) Use the built-in Set-up Procedure.
c) Select the Clock Speed / Wait States through the Keyboard.
d) Interpret the errors reported by the AMI-BIOS.
e) Use the 3 1/2" floppy drive support effectively.

2.A Installing the AMI-386 BIOS

Skip this paragraph if the BIOS is already plugged on the AMI-386XT Board.

Before you begin the installation ensure the following:
i) The Board is powered down.
ii) ROM's are susceptible to static electricity. So observe the following precautions when you handle a ROM :
a) Unpack the ROM's on a ground connected anti-static mat.
b) Wear an anti-static wristband, grounded at the same point as the anti-static mat.
(A cheaper solution is to use a sheet of conductive aluminium foil grouded through a 1 Mega-ohm resistor instead of an anti-static mat. Similarly, a strip of conductive aluminium foil wrapped around the wrist and grounded through a 1 Megaohm resistor will serve the purpose of a wrist band.)

Now follow the steps below:
- Unpack the ROM's and identify the Labels 386-0, 386-1, 386-2 and 386-3.
- Locate the IC Sockets U70, U71, U72 and U73 on the 386 Motherboard.
- Plug in the following order :
  - ROM with label 386-0 in U70 socket,
  - ROM with label 386-1 in U71 socket,
  - ROM with label 386-2 in U72 socket,
  - ROM with label 386-3 in U73 socket.

When you do these make sure that the notch on the ROM is facing away from the I/O connector.

2.A.1 Starting Up The System

Follow the procedure recommended in Section 1 of the Hardware manual.

Power up the system and wait for the BIOS to show up the BIOS activity on the screen.

2.A.2 Memory Test Bypass

The BIOS performs diagnostics of the system and displays the size of the memory being tested.

Note that you can bypass the memory test by pressing the <ESC> key. This option would be quite useful when the memory on the system is quite large. You should hit the <ESC> key when the message **Press <ESC> Key to bypass MEMORY test** appears on the screen.

Also note the **Ref.** number at the bottom of the screen. Make a note of this number before you call Customer Support at AMI for assistance with the BIOS.

Cache Test

The 386-BIOS as a part of its diagnostics tests the cache memory. The BIOS also displays the size and status of the cache memory on the screen. This display can be seen on the second line just past the memory size display.

The size of the cache memory is usually 64 KB. In case the cache memory is found bad then the BIOS alarms the user with the following message :

CACHE MEMORY BAD - DO NOT ENABLE CACHE

Refer to Section 2.C for more information about enabling/disabling cache. The discussion on the advantages of cache can be found in the Hardware section 3.1.

2.B CMOS Setup

Immediately after the memory and cache test, you will get the following prompt on the screen :

Press <DEL> key to run SETUP Utility

Hit <DEL> key to get into the Setup, Mode. Note that <DEL> key will get you into the set-up mode only when the message :
Press <DEL> key to run SETUP Utility, is displayed on the screen.

If you hit <DEL> key the following message appears on the screen:
WANT TO RUN SETUP UTILITY (Y/N)?

If you hit <Y> or <y> and the <ENTER> key you have the Setup screen.

2.B.1 Time/Date Setup

The Setup screen looks like below :

C M O S S E T U P
Curret date is : XX-XX-XXXX
Enter new date (MM-DD-YYYY)?

To this question you would have to enter the date in the format shown on the screen.

If you feel that the current date should remain unchanged, you would just have to hit the <ENTER> key. In such a case the new date is set to the same value as the current date.

The next question you have on the screen is:

Current time is :XX:XX:XX
Enter new time (HH:MM:SS)?

To this question you key in the time in the format defined. Press <ENTER> key alone if the current time is right.

As soon as you have done this the BIOS shows you the type of the display on your system.

After that, the setup takes two differet paths depending upon the CMOS being initialized or uninitialized.

2.B.2 CMOS Initialized

Under these conditions you would see the following messages :

Fixed disk drive C type : X (if installed else Not Installed.)
Fixed disk drive D type : X (if installed else Not Installed.)

Diskette drive A is 3 1/2"
Diskette drive B is Double Sided (Other options as above)
Base Memory Size is : XXX KB
Expansion memory size is : XXXX KB

Are these options correct (Y/N)?

Note that the information about Drive A indicates 3 1/2", as CMOS had been set earlier to reflect this status. If on the contrary, CMOS had been set for a 1.2 MB drive, the message in place of 3-1/2" it would be High Capacity.

If you feel that the information displayed above is right, hit <Y> and the <ENTER> key to proceed to system boot with the new information.

2.B.3 CMOS Uninitialised

2.B.3.1 Disk Drive Type Definition

In this case you would have to enter the type of the fixed Drive C in response to the message :

****** WARNING ******
Entering the wrong disk drive TYPE
causes improper operation of the disk.
If disk not installed press <RETURN>
For disk TYPE details press <ESC>

Enter disk drive C type (1-47)?

Note that the disk type details are only a key stroke away. Hit <ESC> key to find for yourself. You could always come back by hitting <ESC> again.

Once you have convinced yourself about the drive type enter the appropriate number and hit <ENTER>.

Note that pressing <ENTER> key alone indicates the absence of the Drive C.

You would then be asked to enter the type of the disk Drive D. The procedure for doing this is the same as that for Drive C. Remember if you do not have disk Drive D on your system, you just have to hit the <ENTER>

key.

Type	Cylinders	Heads	Write-precomp	Landing-zone	Capacity
1	306	4	128	305	10 MB
2	615	4	300	615	21 MB
3	615	6	300	615	31 MB
4	940	8	512	940	64 MB
5	940	6	512	940	48 MB
6	615	4	NONE	615	21 MB
7	462	8	256	511	31 MB
8	733	5	NONE	733	31 MB
9	900	15	NONE	901	115 MB
10	820	3	NONE	820	21 MB
11	855	5	NONE	855	36 MB
12	855	7	NONE	855	51 MB
13	306	8	128	319	21 MB
14	733	7	NONE	733	44 MB
15	000	0	000	000	00 MB
16	612	4	ALL CYLS.	663	21 MB
17	977	5	300	977	42 MB
18	977	7	NONE	977	58 MB
19	1024	7	512	1023	61 MB
20	733	5	300	732	31 MB
21	733	7	300	732	42 MB
22	733	5	300	733	31 MB
23	306	4	ALL CYLS.	336	10 MB
24	925	7	ALL CYLS.	925	56 MB
25	925	9	NONE	925	72 MB
26	754	7	754	754	46 MB
27	754	11	NONE	754	72 MB
28	699	7	256	699	42 MB
29	823	10	NONE	823	71 MB
30	918	7	918	918	55 MB
31	1024	11	NONE	1024	98 MB
32	1024	15	NONE	1024	133 MB
33	1024	5	1024	1024	44 MB
34	612	2	128	612	10 MB
35	1024	9	NONE	1024	80 MB
36	1024	8	512	1024	71 MB
37	615	8	128	615	42 MB
38	987	3	987	987	25 MB
39	987	7	987	987	60 MB
40	820	6	820	820	42 MB
41	977	5	977	977	42 MB
42	981	5	981	981	42 MB
43	830	7	512	830	50 MB
44	830	10	NONE	830	72 MB
45	917	15	NONE	918	115 MB
46	000	00	000	000	00 MB

Diskette drive A is 3 1/2" (Y/N)?

The above question is asked if the drive has been found to have 80 tracks. Since a drive with 80 tracks could either be a
- high capacity i.e 1.2 MB drive
- or 3 1/2" i.e 720 KB drive,

you would have to answer this question.
By entering <N> or <n> you can select the high capacity drive. Alternatively enter <Y> or <y> to select a 720 KB drive. This question could come up for the case of drive B as well provided it has been detected as a 80 track drive by the BIOS.

If you hit the <ENTER> key alone, the BIOS assumes the drive to be a 1.2 MB drive.

At this point you have entered all the information the BIOS requires for starting up the system.

BIOS detects a few details by itself, e.g. the diskette drive type in case of a 360 KB drive as shown below:

Diskette drive B is : Double Sided (Other options as above)
Base Memory Size is : XXX KB
Expansion memory size is : XXXX KB

Are these options correct (Y/N)?

If you are convinced at this stage that all the information you have entered upto this point is right, hit <Y> or <y> key followed by <ENTER> key. When you do this the BIOS goes all over again to boot up the system with the information specified.

However, if you would like to modify some information, then you should hit either <N> or <n> key followed by enter. You would now go through the setup all over again.

2.B.4 Summary of Set-up

The Set-up screen thus requires you to set
a) Date.
b) Time.
c) Hard Disk Type For Drive C (if present).
d) Hard Disk Type For Drive D (if present).

The Set-up procedure also automatically detects the following:
a) Type Of Display Card.
b) Size Of Real Memory.
c) Size of Memory beyond 1 MB.
d) Presence of 360 kb floppy drives.
e) Presence of a 80387.

Also, if a second Hard Disk drive is physically connected but the CMOS is not set for this Drive D, the BIOS informs you about the same and gives you a chance to configure the drive through SETUP.

Having setup the CMOS, the BIOS runs through the diagnostics again, tests the memory, sets up the devices configured and proceeds to boot.

Note that the Set-up option is available even after a soft reset.

2.B.5 When does the BIOS prompt you to run Set-up?

The BIOS prompts you to run Set-up under the following conditions :
a) CMOS options not set.
b) Display Configuration Mismatch.
c) Memory Size mismatch.
d) Hard Disk Set-up error.
e) CMOS battery is low.
f) An additional hard disk presence is detected.

2.C Selecting Clock Speed/Wait States

AMI-BIOS allows you to change Clock Speeds and Wait States through the keyboard at any time. Following are the key combinations and their meanings :-

Key Combinations	Meaning
1. <CNTRL><ALT><+>	Switch to 16Mhz, 0 Wait State - Block Cursor indicates the switch over.
2. <CNTRL><ALT><->	Switch to 6Mhz, 1 Wait State - Double-line Cursor indicates the switch over.
3. <CNTRL><ALT><L-SHIFT><+>	Select Zero Wait State.(Enable Cache) - only at 16MHz.
4. <CNTRL><ALT><L-SHIFT><->	Select One Wait State.(Disable Cache)

At the time of diagnostics the BIOS tests the cache memory. If the cache test fails, the BIOS does not allow the user to enable cache through the key combination.

2.C.1 Default Settings for Clock and Cache

Note that the speed of the system after power-on can be set by a DIP switch SW7. The details of the same can be had under Section 1.3. If the switch is on, the system boots up at 6 MHz with the cache disabled. If it is off, the system boots up at 16 MHz with the cache enabled. If the power-on cache self-test fails, the cache is not enabled, even when the system boots at 16 MHz.

The system returns to this default state after soft reset (warm boot). Note that during a WARM boot the cache memory is not tested.

2.C.2 Low Level Programs for Clock/Cache Selection

The low level programs discussed below will have to be executed under DOS DEBUG program. The user should be familiar with low level programming before he/she attempts the programs given below.

a) Port Definitions : Clock and cache are selected using the following i/o ports:-

CLOCK selection port Address : 0461H
CACHE selection port Address : 0460H

Bit Map : In case of both the ports mentioned above the LSB status (Least Significant Bit i.e BIT 0) determines the selection. The remaining 7 bits i.e BIT 1 thru BIT 7 are don't care.

B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	X	X	X	LSB

Port 461 LSB: 0 -> 6 MHz
1 -> 16 MHz

Port 460 LSB: 0 -> Disable cache
1 -> Enable cache

b) Selecting High or 16 MHz Speed: Under DEBUG prompt - enter the following command:
-O 461,1 <ENTER>

c) Selecting Low or 6 MHz Speed: Under DEBUG prompt - enter the following command:
-O 461,0 <ENTER>

d) Status Of Clock: Under DEBUG prompt - enter the following command:
-I 461<ENTER>

XX

In response the port status is returned in XX. Looking at the LSB the clock speed can be found. If the LSB is set the speed is 16MHz else it is 6 MHz.

e) Enabling the Cache: Enable CACHE using the low level command shown below **only after confirming that the cache is good.** The As described earlier, the cache status is displayed by the BIOS after power-on.

Under DEBUG prompt enter the following command:

-O 460 1<ENTER>

f) Disabling the Cache: Under DEBUG prompt enter the following command:

-O 460 0<ENTER>

g) Status Of Cache: Under DEBUG prompt - enter the following command:

-I 460<ENTER>

XX

In response the port status is returned in XX. Looking at the LSB the cache status can be found. If the LSB is set the cache is enabled else it is disabled.

2.D Errors Reported By AMI-BIOS

AMI-BIOS performs various diagnostic tests at the time the system is powered up. Whenever an error is encountered during these tests, either you hear a few short beeps or see an error display on your monitor. If the error occurs before the display device is initialised the system reports the error by giving a number of short beeps.

If the error is FATAL then system halts after reporting the FATAL error. If the error is NON-FATAL the process continues after reporting the NON--FATAL error.

Fatal Errors

Beep Count	Meaning
1	DRAM refresh failure .
2	Parity Circuit failure.
3	Base 64KB RAM failure.
4	System Timer failure.
5	Processor Failure.
6	Keyboard Controller - Gate A20 error.
7	Virtual Mode Exception Error.
8	Display Memory R/W Test Failure. (*)
9	ROM-BIOS CheckSum Failure.

(*) Non-Fatal Error.

Error Messages

Fatal Errors
1. Channel - 2 of Timer Not functional.
2. Stray Interrupt sensed in controller.
3. Interrupt controller #2 not functional.

Non-Fatal Errors
1. Keyboard Error.
2. Keyboard/Interface Error.
3. CMOS battery state low.
4. CMOS system options not set.
5. CMOS checksum failure.
6. CMOS memory size mismatch.
7. CMOS system time and date not set.
8. CMOS display configuration mismatch.
9. Display setting not proper.
10. Keyboard is locked ..... Unlock it.
11. Floppy disk controller failure.
12. Hard disk unit 0 error.
13. Hard disk unit 1 error.
14. Hard disk unit 0 failure.
15. Hard disk unit 1 failure.
16. Hard disk unit 1 is not defined in CMOS.
17. Cache Memory Bad - Do Not Enable Cache.

2.E Use of 3 1/2" Support Effectively

DOS 3.20 provides support for 3 1/2" drives. For this purpose it needs support from the ROM BIOS. AMI-BIOS release date 12/03/86 onwards provides the necessary support.

The 3 1/2" drive can be freely configured as Drive A or Drive B with this BIOS. Thus it is possible to boot off directly from a 3 1/2" drive.

Earlier versions of DOS would require the use of DRIVER.SYS to provide the necessary support.

A few points would have to be kept in mind when you use the 3 1/2" drive and a 1.2 MB together. Ensure that when you perform the Setup you define the drives correctly. Incorrect definition could make the drive unusable.

The table below describes the valid combinations on a AT:

CMOS Status	Physical Drive Status	Functional
1.2 MB	1.2 MB	YES
3 1/2"	3 1/2"	YES
Undefined	1.2 MB	YES

The remaining combinations are invalid. Please make a note of these combinations before you call us for help.

SECTION 3

System Overview

3.1 Description

The system board is approximately 8.5 by 13 inches and uses very large scale integration (VLSI) technology. It has the following features:

* 80386 Microprocessor

* 16 MHz System Clock

* Optional 80387 Numeric Coprocessor (6/16MHz)

* System support function:
  - -7 Channel Direct Memory Access (DMA)
  - -16 level interrupt
  - -Three programmable timers
  - -System clock

* User selectable 64KB/128KB read only memory (ROM) subsystem

* 64KB Cache Memory which caches 16MB memory address space

* User selectable synchronized system board clock switching option for reducing the processor clock frequency to 6MHz

* 8MHz I/O bus timing compatibility at 16MHz board operation

* Speaker attachment

* Complementary Metal Oxide Semiconductor (CMOS) RAM to maintain system configuration

* Real-Time clock

* Battery backup for CMOS configuration table and Real-Time Clock

* Keyboard attachment

* 8.5 by 13 inch board:Extended XT [1] form-factor

* 6 input/output (I/O) slots:
  - 4 with a 62 + 36 pin card-edge socket
  - 1 with only the 62-pin card-edge socket
  - 1 32bit memory slot

3.2 The Microprocessor

The 80386 is a high performance 32-bit microprocessor designed for Multitasking operating systems. The processor can address up to 4-Gigabytes of physical memory and 64-Terabytes (1-Terabyte = 1-K Gigabyte) of virtual memory (this design limits the physical address to 16MB). It has integrated memory management and protection architecture which includes address translation registers, advanced multitasking hardware and protection mechanism to support operating systems. In addition, it is object code compatible with 8086 family of microprocessor. The 80386 has built-in features to support coprocessors, DMA and interrupts (both maskable and non-maskable). It has two modes of operation: Real address mode and Protected virtual address mode.

In real address mode it operates as a fast 8086 with 32-bit extension if desired. In Protected mode, software can perform a task switch into tasks designated as virtual 8086 mode tasks. The virtual 8086 tasks can be isolated and protected from one another by the use of paging and I/O permission bit map.

3.3 System Performance

Clock Speed

The AMI-386XT can operate at 16MHz, which results in a clock cycle time of 62.5ns. It can run at two different clock rates. The lower clock speed is normally 6 or 8MHz. For convenience, we shall assume this speed to be 6MHz throughout the rest of this manual. If the oscillator U111 on the board is 16MHz instead of 12MHz, all the 6MHz timing will have to be reduced by 25%. Similarly, if Y1 is something other than 32MHz, the 16MHz timings will have to be appropriately rated.

The switch SW-4 determines the initial clock frequency after power-on. Refer to Section 1.3 for details. The clock speed can be switched at any time when the machine is operating. Refer to Section 2.C for details.

The 80387 Numeric processor runs at the processor clock frequency.

Data Access: Bus Width

The 80386 microprocessor supports two types of accesses: Memory, and Input/Output. Each type of access can be 32-, 24-, 16- or 8-bit wide. The memory and I/O devices are 32, 16 or 8 bit wide. The AMI-386 allows any type of access to a device of any width. If necessary, the hardware will split a 80386 bus cycle into a

number of (upto 32 / 8 = 4) cycles to allow access to a 16- or 8-bit device. All the on-board ' devices in the memory space is organized 32-bit wide. These include the on-board DRAM, the high-speed Cache memory and the EPROM containing the BIOS. All the on-board I/O devices are 8-bit wide, with the exception of the 80387 math coprocessor which is a 32-bit device.

The AMI-386XT can support 16- and 8-bit memory and I/O devices on the I/O slots.

The memory space from address 0C0000 thru 0C7FFF is reserved for I/O slot ROM. Most often, only the EGA BIOS (0C0000-0C3FFF), which is accessed through a 8-bit bus, is located in this area. The slow execution of this device driver makes the video I/O sluggish. The AMI-386 provides the option of mapping this space into the 32 bit system board EPROM. The board is shipped with the AMI EGA compatible BIOS in the system board EPROM, which maps into the required memory space if SW1 is ON. Refer to Section 1.3 for SW1 setting. This improves the video I/O speed, since the EGA BIOS can now be accessed through a 32-bit bus. When SW1 is ON, there should not be any I/O slot 16-bit memory in the address space 0C0000 thru 0C7FFF. Also, any I/O slot 8-bit memory in that space will be automatically disabled.

Cache and DRAM access

In 80386, a zero wait-state bus cycle requires two clock cycles. The required number of clock cycles increases by one with every wait-state introduced in the access. Most processor accesses are memory read operations. To speed up the memory reads, the AMI-386 incorporates 64KB of 32-bit wide directly mapped cache, realized with high-speed Static RAM. The cache has byte granularity and a page size of 4 bytes and is implemented with a write-thru algorithm. At 16MHz, with the cache enabled, 81% of data will be available in the cache for memory read operations (this is a statistical value for normal program execution). This improves system speed about twofold, since the cache access requires no wait states, whereas the main memory access would require at least two.

A point to note is that, even the off-board (I/O slot not 32bit memory slot) memory is cached. Hence most read operations, even from a slow off-board memory, will have no wait states. As a result, the speed and bus width of the expansion memory will hardly affect the system speed. However, since an off-board memory always takes longer to access

than the 32 bit memory on the 32bit slot, it is always a good idea to utilize the 32bit memory to its full capacity before resorting to add-on memory boards. Refer to Section 1.3 for 32bit memory switch settings.

Refer to Section 2.C and 3.7 for information on how to enable and disable the cache.

Data Access: Cycle times

The following table gives the number of wait states and the total bus cycle times for different cases of Cache and on-board DRAM access:-

Access Type	6MHz wait states	6MHz time (ns)	16MHz wait states	16MHz time (ns)
Memory Read: Cache hit	-	-	0	125
DRAM Read: Cache disable	1	500	2	250
DRAM Read: Cache miss	1	500	3	312.5
DRAM Write	1	500	2	250

The table below lists the number of wait states and processor access times for on-board EPROM, I/O and off-board accesses:-

Access type	6MHz wait states	6MHz time (ns)	16MHz (MEMW,IORD) wait states	16MHz (MEMW,IORD) time (ns)	16MHz (MEMR,IOWR) wait states	16MHz (MEMR,IOWR) time (ns)
16-bit device	1	500	5	437.5	6	500
8-bit access to 8-bit device	4	1000	10	750	11	812.5
16-bit access to 8-bit device	10	2000	22	1500	24	1625

Refresh Controller and DMA Timing

The refresh controller operates at 6 or 8 MHz for processor clock of 6 or 16MHz respectively. Each refresh cycle requires 5 clock cycles to refresh all the DRAM in the sysytem. 256 refresh cycles are required every 4 ms.

The DMA controller operates at 3 or 4 MHz for CPU clock of 6 or 16 MHz respectively. All DMA transfer bus cycles are 5 clock cycles long, which results in a cycle time of 1660 or 1250 ns.

SECTION - 4

Technical Specifications

4.1 32bit DRAM memory map

SW1	SW2	SW3	MEMORY BELOW 1MB	MEMORY ABOVE 1MB
OFF	OFF	OFF	512K	NIL
OFF	ON	OFF	640K	NIL
OFF	ON	ON	640K	384K
ON	OFF	OFF	512K	1024K
ON	ON	OFF	640K	1024K
ON	ON	ON	640K	1408K

Other than memory on 32bit card, the system memory mapping is like this:

Address	Name	Function
0A0000 - 0BFFFF	128KB video RAM	Reserved for graphics display buffer
0C0000 - 0C7FFF	32KB of ROM	SW1 OFF: adapter card ROM SW1 ON: system board ROM
0C8000 -0CFFFF	32KB of ROM	Rserved for ROM on I/O adapter cards
0D0000 - 0DFFFF	64KB I/O expansion ROM	Reserved for ROM on I/O adapter cards
0E0000 - 0EFFFF	64KB ROM available on system board if SW5 is OFF	Duplicate code assignment at address FE0000-FEFFFF
0F0000 - 0FFFFF	64KB ROM on the system board	Duplicate code assignment at address FF0000-FFFFFF
Address from the end of system board memory to FDFFFF		I/O channel memory
FE0000 - FEFFFF		Duplicate code assignment at address 0E0000-0EFFFF
FF0000 - FFFFFF	64KB ROM on the system board	Duplicate code assignment at address 0F0000-0FFFFF

4.2 I/O Address Map

I/O address hex 000 to 0FF are reserved for the system board I/O. The system board I/O map is as follows:-

Address Range	Device
000-01F	DMA controller 1, 8237A-5
020-03F	Master Interrupt Controller, 8259A
040-05F	Timer, 8254-2
060-07F	Real time clock, NMI(non-maskable interrupt) mask and Keyboard Controller (8742)
080-09F	DMA Page Register, 74LS612
0A0-0BF	Slave Interrupt Controller, 8259A
0C0-0DF	DMA Controller 2, 8237A-5
0E0-0FF	Math Coprocessor
460-46F	Reserved for cache memory enable and system clock switching

I/O address hex 100 to 3FF are available on the I/O channels. The I/O slot address map is as follows:-

Address Range	Device
1F0-1FF	Fixed Disk
200-207	Game I/O
278-27F	Parallel printer port 2
2F8-2FF	Serial port 2
378-37F	Parallel printer port 1
380-38F	SDLC, bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome display and printer adapter
3C0-3CF	Enhanced Graphics Display adapter
3D0-3DF	Color Graphics Monitor adapter
3F0-3F7	Diskette Controller
3F8-3FF	Serial port 1

4.3 System Timers

The system board has three programmable timer/counters controlled by 8254-2 timer/counter chip. The timer channels, defined as channel 0 through 2, are used as follows:-

Channel 0	System timer
Gate 0	Always enabled
Clkin 0	1.190 MHz clock
Clkout 0	Interrupt controller IRQ 0
Channel	Refresh Request Generator
Gate 1	Always enabled
Clkin 1	1.190 MHz clock
Clkout 1	Dynamic memory refresh request
Channel 2	Tone generation for speaker
Gate 2	Controlled by bit 0 of I/O port address 61H
Clkin 2	1.190 MHz clock
Clkout 2	Audio frequency output to speaker

Note: Channel 1 is programmed as a rate generator of 15 microsecond period, to refresh all the DRAM in the system.

The output of Channel 2 is logically ANDed with bit 1 of the I/O port at address 61H to further modulate the output. The 8254-2 timer is programmed by the system through port 40-43H. The address map is as shown:

Address	Register Select
040	Counter 0
041	Counter 1
042	Counter 2
043	Control word register

4.4 System Interrupts

The system processor can be interrupted through NMI (non maskable interrupt), as well as, through two 8259A interrupt controllers (CTLR1 & CTLR2), which provide 16 levels of system interrupt. Any or all interrupt levels, including NMI, can be disabled. The following shows the interrupt level assignments in decreasing order of priority:-

CTLR1	CTLR2	Function
NMI		System board Dynamic Memory parity or I/O channel Check
IRQ 0		Timer Channel 0 output
IRQ 1		Keyboard Controller (output buffer full) interrupt
IRQ 2		CTLR 2 interrupt to CTLR 1 for any interrupt on interrupt levels of CTLR 2
	IRQ 8	Real time clock Interrupt
	IRQ 9	Vertical retrace interrupt from video display adapter. Software redirected to INT 0AH (IRQ 2)
	IRQ 10	Reserved
	IRQ 11	Reserved
	IRQ 12	Reserved
	IRQ 13	Coprocessor Interrupt for any error
	IRQ 14	Fixed Disk Controller
	IRQ 15	Reserved
IRQ 3		Serial port 2
IRQ 4		Serial port 1
IRQ 5		Parallel port 2
IRQ 6		Diskette Controller
IRQ 7		Parallel port 1

The NMI can be disabled by writing into I/O port 70H with bit 7 set and enabled by writing to I/O port 70H with bit 7 reset. There are two sources through which NMI can be generated: (1) System board dynamic RAM parity failure; (2) error reported by I/O channel adapter card through '-I/O channel check (-IOCHCK) signal'. At power-on, the NMI and I/O-check are disabled. Before NMI is enabled, following steps should be taken:-

1. Write data in all system board and I/O adapter memory locations; this will establish good parity at all locations.

2. Enable system board parity check (write into port 61H with data bit 2 set to zero).

3. Enable I/O channel check signal (write into port 61H with data bit 3 set to zero).

Note: All these functions are performed automatically by POST (Power On Self Test)

The status bits (I/O port 61H) indicate whether NMI is due to system-board parity check or I/O-check.

4.5 Description of I/O read/write port 061H

Write port 61H bit definitions

Bit 0	Timer channel 2 GATE input control (1 = GATE is enabled)
Bit 1	Timer channel 2 OUTPUT control (1 = OUPUT will go to audio speaker)
Bit 2	Enable system board parity check (0 = Enable, 1 = Disable)
Bit 3	Enable I/O channel check (0 = Enable, 1 = Disable)
Bit 4-7	Not Used

Read port 61H bit definitions

Bit 0	'Timer channel 2 GATE input control' bit
Bit 1	'Timer Channel 2 OUTPUT control' bit
Bit 2	'enable system board parity check' bit
Bit 3	'enable I/O channel check' bit
Bit 4	System memory refresh determine signal (should toggle at a time period of 30 microseconds if refresh happens properly)
Bit 5	Timer channel 2 OUTPUT
Bit 6	I/O check signal (This bit will be set if there is any I/O channel check error)
Bit 7	System board RAM parity check signal (This bit will be set if there is any system board dynamic memory parity failure)

4.6 Direct Memory Access (DMA)

The system supports seven DMA channels, using four channels each of two 8237A DMA controllers. DMA controller-1 (I/O address 000-01FH) handles channel 0 to 3, which are capable of doing 8 bit data transfers between 8-bit I/O adapters and 8- or 16- bit system

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The system processor can be interrupted through NMI (non maskable interrupt), as well as, through two 8259A interrupt controllers (CTLR1 & CTLR2), which provide 16 levels of system interrupt. Any or all interrupt levels, including NMI, can be disabled. The following shows the interrupt level assignments in decreasing order of priority:-

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IRQ 2		CTLR 2 interrupt to CTLR 1 for any interrupt on interrupt levels of CTLR 2
	IRQ 8	Real time clock Interrupt
	IRQ 9	Vertical retrace interrupt from video display adapter. Software redirected to INT 0AH (IRQ 2)
	IRQ 10	Reserved
	IRQ 11	Reserved
	IRQ 12	Reserved
	IRQ 13	Coprocessor Interrupt for any error
	IRQ 14	Fixed Disk Controller
	IRQ 15	Reserved
IRQ 3		Serial port 2
IRQ 4		Serial port 1
IRQ 5		Parallel port 2
IRQ 6		Diskette Controller
IRQ 7		Parallel port 1

The NMI can be disabled by writing into I/O port 70H with bit 7 set and enabled by writing to I/O port 70H with bit 7 reset. There are two sources through which NMI can be generated: (1) System board dynamic RAM parity failure; (2) error reported by I/O channel adapter card through '-I/O channel check (-IOCHCK) signal'. At power-on, the NMI and I/O-check are disabled. Before NMI is enabled, following steps should be taken:-

1. Write data in all system board and I/O adapter memory locations; this will establish good parity at all locations.

2. Enable system board parity check (write into port 61H with data bit 2 set to zero).

3. Enable I/O channel check signal (write into port 61H with data bit 3 set to zero).

Note: All these functions are performed automatically by POST (Power On Self Test)

The status bits (I/O port 61H) indicate whether NMI is due to system-board parity check or I/O-check.

4.5 Description of I/O read/write port 061H

Write port 61H bit definitions

Bit 0	Timer channel 2 GATE input control (1 = GATE is enabled)
Bit 1	Timer channel 2 OUTPUT control (1 = OUPUT will go to audio speaker)
Bit 2	Enable system board parity check (0 = Enable, 1 = Disable)
Bit 3	Enable I/O channel check (0 = Enable, 1 = Disable)
Bit 4-7	Not Used

Read port 61H bit definitions

Bit 0	'Timer channel 2 GATE input control' bit
Bit 1	'Timer Channel 2 OUTPUT control' bit
Bit 2	'enable system board parity check' bit
Bit 3	'enable I/O channel check' bit
Bit 4	System memory refresh determine signal (should toggle at a time period of 30 microseconds if refresh happens properly)
Bit 5	Timer channel 2 OUTPUT
Bit 6	I/O check signal (This bit will be set if there is any I/O channel check error)
Bit 7	System board RAM parity check signal (This bit will be set if there is any system board dynamic memory parity failure)

4.6 Direct Memory Access (DMA)

The system supports seven DMA channels, using four channels each of two 8237A DMA controllers. DMA controller-1 (I/O address 000-01FH) handles channel 0 to 3, which are capable of doing 8 bit data transfers between 8-bit I/O adapters and 8- or 16- bit system

memory. Each channel can transfer data throughout the 16-megabyte system address space in 64KB blocks.

DMA controller 2 supports channel 4 through 7. Channel 4 is used to cascade DMA Controller 1. Channel 5, 6 and 7 support 16 bit data transfer between 16-bit I/O adapters and 16-bit system memory. These channels can transfer data throughout the 16-megabytes of address space in 128KB blocks. Channels 5, 6 and 7 cannot transfer data on odd byte boundaries.

The following table shows the address generation for the DMA channels. DMA page register supplies upper 8 bits of address for CTLR 1 and 7 bits of address for CTLR 2.

Controller	DMA page register supplied address	DMA controller supplied address
1	A23 through A16	A15 through A0
2	A23 through A17	A16 through A1

For Controller-1, byte high enable (BHE) signal is generated by inverting the signal A0. For Controller-2, both A0 and BHE are forced to logic '0'.

The following table shows the addresses for the page register:

Page register	I/O hex address
DMA Channel 0	087
DMA Channel 1	083
DMA Channel 2	081
DMA Channel 3	082
DMA Channel 5	08B
DMA Channel 6	089
DMA Channel 7	08A
Refresh	08F

For DMA Channels 5 thru 7, the page register data bits D7 through D1 are loaded with address A23 thru A17. Data bit D0 of the page registers, for Channels 5 thru 7, is not used. Since DMA Channels 5 thru 7 do 16-bit data transfer, the count registers for these channels have to be loaded with half the transfer byte-count Also, the base address registers have to be loaded with the real address divided by 2.

Following are the register addresses of DMA controllers 1 and 2:

Command Codes	Hex address for CTLR 1	CTLR 2
CH0 base and current address	000	0C0
CH0 base and current word count	001	0C2
CH1 base and current address	002	0C4
CH1 base and current word count	003	0C6
CH2 base and current address	004	0C8
CH2 base and current word count	005	0CA
CH3 base and current address	006	0CC
CH3 base and current word count	007	0CE
Read Status register/Write command register	008	0D0
Write request register	009	0D2
Write single mask register bit	00A	0D4
Write mode register	00B	0D6
Clear byte pointer flip flop	00C	0D8
Read temporary register/Write master clear	00D	0DA
Clear mask register	00E	0DC
Write all mask register bits	00F	0DE

4.7 I/O PORTS 460 & 461

Setting data bit-0 on write-port 460 enables cache memory. To disable the cache, this bit has to be reset. The cache is disabled at power-on. At least a 64KB block of cachable RAM should be written into, before enabling the cache for the first time after power-on. If cache fault was reported by the POST, the should not be enabled. Refer to Section 4.9 for detail.

The read/write port 461 decides the processor clock frequency.
Reset data bit 0 for 6MHz operation
Set data bit 0 for 16MHz operation

4.8 Real Time Clock/Complementary Metal Oxide Semiconductor (RTC/CMOS) RAM

The RTC/CMOS RAM chip is a MOTOROLA MC146818. It contains the real time clock and 64 bytes of CMOS RAM. The internal clock circuitry uses 14 bytes of RAM and the rest is used to keep system configuration information.

The following table shows the CMOS RAM addresses:-

Addresses	Description
00-0D	Real time clock information
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte - drives A and B
11	Reserved
12	Fixed disk type byte - drives C and D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	Two-byte CMOS checksum
30	Low expansion memory byte
31	High expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-3F	Reserved

Note:The 2-byte CMOS checksum is on address 10H-20H.

These bytes can be read/written by first outputting the address to I/O port 70H and then by reading/writing data from/to I/O port 71H.

REAL TIME CLOCK INFORMATION

The following table describes real-time clock bytes with their addresses:-

Byte	Function	Address
0	Seconds	00
1	Second alarm	01
2	Minutes	02
3	Minute alarm	03
4	Hours	04
5	Hour alarm	05
6	Day of week	06
7	Date of month	07
8	Month	08
9	Year	09
10	Status Register A	0A
11	Status Register B	0B
12	Status Register C	0C
13	Status Register D	0D

Note: The built-in setup program of the system BIOS initializes registers A, B, C and D when the time and date are set. Also, interrupt 1A is the BIOS interface to read/set the time and date. The function of the status register bits is as follows:-

Status Register A

Bit 7	Update in Progress (UIP) - A 1 indicates that an update cycle is in progress or will soon begin. A 0 indicates that the time, calender and alarm information in the RAM is fully available to read/write. Writing a 1 to the SET bit in Register B inhibits any update cycle and then clears the UIP bit.
Bit 6-Bit 4	22-Stage Divider (DV2-DV0) - The divider selection bits identify which of the three time base frequencies (4.194304 MHz, 1.048576 MHz and 32.768 KHz) is in use. The system initializes the divider selection bits by 010, which selects a 32.768 KHz time base.
Bit 3-Bit 0	Rate Selection Bits (RS3-RS0) - These bits select the divider output frequency. The system initializes the rate selection bits by 0110, which selects a 1.024 KHz square wave output frequency

and a 976.562 microsecond periodic interrupt rate if SQWE and PIE bits of register B are enabled.

Status Register B

Bit 7	SET - A 0 updates clock functions normally by advancing the counts once-per-second. A 1 aborts any update cycle in progress and the program can initialize the 14 time and calender bytes without any update occuring in the midst until a 0 is written to this bit.
Bit 6	Periodic Interrupt Enable (PIE) - This is read/write bit which allows an interrupt to occur at a rate specified by the RS3-RS0 bits in Register A. A 1 enables the interrupt and a 0 disables it. The system initializes this bit to 0.
Bit 5	Alarm Interrupt Enable (AIE) - This read/write bit when set to 1 allows an alarm interrupt to occur. A 0 disables the interrupt. The system initializes this bit to 0.
Bit 4	Update Ended Interrupt Enable (UIE) - This read/write bit when set enables the update ended interrupt and a 0 disables it. The system initializes this bit to 0.
Bit 3	Square Wave Enabled (SQWE) - This bit when set to 1, enables a square wave signal at the frequency specified in the rate selection bits RS3-RS0 to appear on the SQW pin. The SQW pin is held low when SQWE bit is set to 0. The system initializes this bit to 0.
Bit 2	Date Mode (DM) - This bit indicates whether time and calender updates are to use binary or BCD formats. This read/write bit, when set to 0 indicates binary and a 1 indicates BCD. The system initializes this bit to 0.
Bit 1	24/12 - This read/write bit establishes the format of the hour bytes. A 1 indicates the 24-hour mode and a 0 indicates the 12-hour mode. The system initializes this bit to 1.
Bit 0	Daylight Savings Enabled (DSE) - This read/write bit when set to 1, allows the program to enable two special updates. On the last Sunday in April

the time increments from 1:59:59AM to 3:00:00AM. On the last Sunday in Octobar when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur if DSE bit is set to 0. The system initializes this bit to 0.

Status Register C

Bit 7	Interrupt Request Flag (IRQF)
Bit 6	Periodic Interrupt Flag (PF)
Bit 5	Alarm Interrupt Flag (AF)
Bit 4	Update Ended Interrupt Flag (UF)
	Bit 7 -Bit 4 are read only flags which are used by the program to determine the source of interrupts when the AIE, PIE and UIE interrupts are enabled in Register B.
Bit 3 - Bit 0	These unused bits are read as 0 and they cannot be written.

Status Register D

Bit 7	Valid RAM and Time bit (VRT) - It indicates the condition of the contents of the RAM through the power sense (PS) pin. A 0 appears on the VRT bit if the power sense pin is low which indicates that the real time clock has lost its power (battery dead). The processor program sets the VRT bit to 1 when the time and calender are initialized to indicate that the RAM and time are valid.
Bit 6-Bit 0	These unused bits are read as 0 and they cannot be written into.

CMOS RAM CONFIGURATION INFORMATION

The following are the bit definitions for the CMOS configuration bytes (addresses hex 0E-3F):-

Diagnostic Status Byte (address hex 0E)

Bit 7	Real time clock chip power status - A 0 indicates that the chip has not lost power and a 1 indicates that the chip has lost power.
Bit 6	Configuration Record Checksum Status Indicator - a 0 indicates that the Checksum is good, and a 1 indicates that it is bad.
Bit 5	Incorrect Configuration Information - This bit is used to check the validity of the content of the equipment byte of the configuration record. A 0 indicates that the configuration information is valid, and a 1 indicates it is invalid.
Bit 4	Memory Size Miscompare - A 0 indicates that the power on diagnostic program check of the system memory size matches with that in the configuration record. A 1 indicates that the memory size is different.
Bit 3	Fixed Disk Adapter/Drive C Initialization Status - A 0 indicates that the fixed disk adapter and drive are functioning properly and the system can attempt to 'boot up'. A 1 indicates that the adapter and/or drive C failed initializtion, which prevents the system from 'boot up'.
Bit 2	Time Status Indicator - A 0 indicates that the time is valid and a 1 indicates that the time is invalid.
Bit 1-Bit 0	Reserved.

Shutdown Status Byte (address hex 0F)

This byte defines the cause of a processor shutdown. This byte is checked by the program, when the SYSTEM FLAG (See in Keyboard Controller description) is set, to determine the cause of the processor shutdown. The following table defines the shutdown byte content:-

Content	Cause
0	Soft Reset or Unexpected shutdown
1	Shut down after memory size
2	Shut down after memory test
3	Shut down with memory error
4	Shut down with boot loader request
5	JMP DWORD request (with INT INIT)
6	Protected mode test passed
7	Protected mode test failed
8	Protected mode test failed
9	Block move shut down request
A	JMP DWORD request (w/o INT INIT)

Diskette Drive Type Byte (address hex 10)

Bit 7-Bit 4 Drive A type:

0000	No drive present
0001	Double Sided Diskette Drive (48 TPI, 360KB)
0010	High Capacity Diskette Drive (96 TPI, 1.2MB)
0011	3 1/2" Diskette Drive (96 TPI, 720KB)
0100-1111	Reserved

Bit 3-Bit 0 Type of second diskette drive installed:

The bit definitions are same as above.

Fixed Disk Type Byte (address hex 12)

Bit 7-Bit 4 — Type of first fixed disk drive installed (drive C):

0000 No fixed disk drive is present
0001 through 1110 define type 1 through type 14, the list of which is given in table below
1111 Hard Disk type between 16 and 255 is indicated in the extended byte (address hex 19)

Bit 3-Bit 0 — Type of second fixed disk drive (drive D):

The bit definitions are same as above, except for 1111 which implies that the Hard Disk type between 16 and 255 is indicated in the extended byte (address hex 1A)

Refer to Section 2.B.3.1 for fixed disk type table.

Equipment Byte (address hex 14)

Bit 7-Bit 6 — Total number of diskette drives installed:
00 1 drive
01 2 drives
10 Reserved
11 Reserved

Bit 5-Bit 4 — Primary Display
00 Primary display is other than Color Graphics Adapter or Monochrome Display adapter.
01 Primary display is Color Graphics Adapter in 40 column mode.
10 Primary display is Color Graphics Adapter in 80 column mode.
11 Primary display is Monochrome Display and Printer Adapter.

Bit 3-Bit 2 — Not used

Bit 1 — Math Coprocessor presence bit:
0 Math Coprocessor not installed
Math Coprocessor installed

Bit 0
1 Diskette drives are installed
0 Diskette drives are not installed

High Base Memory Bytes (address hex 15 and 16)

The size of memory below 1MB is indicated by the 16-bit word formed by these two bytes (address 16H is the higher byte). The content of this word increments by 40H for every 64 KB increment of base memory size. For example, if the system contains 256 KB then content of base memory bytes (15H and 16H together) will be 0100H (content of 16H is 01H and content of 15H is 00H). Maximum possible size of memory below 1 MB is 640KB. So the maximum possible value of base memory bytes is 0280H.

Low and High Memory Expansion Bytes (address hex 17 and 18)

The size of memory above 1MB is indicated by the 16-bit word formed by these two bytes (address 18H is the higher byte). In this case also, the content of this word increments by 40H for every 64 KB increment of expansion memory size. So if the content of memory expansion bytes is 0200H (content of 18H is 02H and content of 17H is 00H), then the amount of memory above MB is 512 Kilobytes. Maximum possible value is 3C00H for a maximum of 15 MB of memory above 1MB.

Drive C Extended Byte (address hex 19)

Bit 7 - 0	Defines the type of Fixed Disk Drive installed (Drive C). 00000000 thru 00001111 are reserved. 00010000 thru 11111111 define the types 16 thru 255.

Drive D Extended Byte (Hex 1A)

Bit 7 - 0	Definition is the same as Drive C extended byte.

Checksum (address hex 2E and 2F)

Address hex 2E - Low byte of checksum
Address hex 2F - High byte of checksum

Checksum is calculated by adding contents of address 10H through 20H and the low byte of checksum is stored in hex 2E and the high byte in hex 2F.

Low and High Expansion Memory Bytes (address hex 30 and 31)

The size of memory above 1MB is indicated by the 16-bit word formed by these two bytes (address 31H is the higher byte), as determined at power-on time. The content of this word increments by 40H for every 64 KB increment of expansion memory size. Maximum possible value is 3C00H for a maximum of 15 MB of memory above 1MB.

Date Century Byte (address hex 32)

Bit 7-Bit 0	BCD value for the century (BIOS interface to read and set).

Information Flag (address hex 33)

Bit 7	Set if memory is present in address space hex 080000-09FFFF
Bit 6	Used by the Setup utility to put out a first user message after initial setup
Bit 5-Bit 0	Reserved

Note: Hex addresses 11, 13, 1B-2D, 34-3F are reserved.

4.9 Keyboard Controller

The keyboard controller is 8742 single chip microcomputer-based and is used to support 386 PC keyboard interface. The controller has the following functions:-

-Receive serial data from the keyboard, check parity of the data and translate it to system scan code, if necessary. Put the received and processed data into the data buffer and interrupt processor.

-Execute system commands through the controller command buffer and place the result, if necessary, in the data buffer and interrupt the processor

-Transmit system data, placed in the data buffer, to the keyboard in a serial format with the parity bit inserted. Get the response from the keyboard and report to the system.

-Report any error to the system through status register at the time of data communication with the keyboard.

Receiving data from the keyboard

The keyboard sends data in a 11-bit serial format. The first bit is a start bit (low level) followed by 8 data bits (least significant data bit first), an odd parity bit and a stop bit (high level). Data sent is synchronized with the keyboard clock. Upon receiving a byte of data from the keyboard, the keyboard controller places the data in its one byte receive-data buffer and disables the keyboard interface until that data is picked up by the system processor. This avoids data overrun. On parity error, the controller requests the keyboard to re-send the data. If the error is repeated, the controller sets the parity error bit in its status register. Time- out error is indicated by setting the time-out bit in the status register, if all the 11 bits are not received within 2 milliseconds from start of transmission. In case of either of these errors, hex FF is placed in the receive-data buffer.

Sending data to the keyboard

Data is sent to the keyboard in the same serial format as data received from the keyboard. If the time between request to send and start of transmission is greater than 15 milliseconds, or if the duration of transmission is greater than 2 milliseconds, then the transmit time-out error bit is set in the status register. The keyboard is required to acknowledge every transmission from the controller. If the acknowledgement has parity error, then the controller sets both the parity and transmit time-out error status bits. Also, if the acknowledgement does not arrive within 25 milliseconds, both the receive and transmit time-out error bits are set. In case of all these errors, hex FE is placed in the data buffer. No retries are made for error at the time of transmitting to the keyboard.

Keyboard Inhibit

The keyboard can be inhibited through keylock jumper J20. When the keyboard is inhibited, although all transmissions from the system to the keyboard will be allowed, the keyboard controller tests all data received from the keyboard. If it is a response to a command sent to the keyboard, then it is placed in the data buffer, otherwise it is ignored.

Keyboard Controller System Interface

The system communicates with the keyboard controller through an input buffer, an output buffer and a status register. The status register can be read through I/O port 64H. The output buffer can

be read through I/O port 60H. The input buffer can be written through both I/O port 64H and 60H. When the input buffer is written through I/O port 64H, the controller interprets it as a command and if it is written through I/O port 60H, then the data is interpreted either as a parameter to a command to the controller or a data to be trans- mitted to the keyboard.

Keyboard Controller Status Register Bit definitions

Bit 0 Output Buffer Full - A 0 indicates that the keyboard controller's output buffer has no data. When the keyboard controller writes to the output buffer, this bit is set to 1. It returns to 0, when the system reads the output buffer (60H).

Bit 1 Input Buffer Full - A 0 indicates that the keyboard controller's input buffer (60H or 64H) is empty. When the system writes to the input buffer this bit is set to 1. It gets reset to 0 when the controller reads the input buffer.

Bit 2 System Flag - The keyboard controller can set this bit to 0 or 1 depending on the command from the system. It is set to 0 after power on reset.

Bit 3 Command/Data - This bit is used by the keyboard controller to determine whether the input buffer contains the command or data. When the system writes to the input buffer through I/O port 64H, this bit is set to 1. When the system write to the input buffer, this bit is set to 0.

Bit 4 Inhibit Switch - This bit reflects the state of the keyboard inhibit switch. This bit is updated whenever the controller writes to the output buffer. A 0 indicates that the keyboard is inhibited.

Bit 5 Transmit Time-Out - A 1 indicates that a data transmission from the keyboard controller to the keyboard was not properly completed within the predefined time limit.

Bit 6 Receive Time-Out - A 1 indicates that a data transmission from the keyboard to the keyboard controller was not properly completed within the predefined time limit.

Bit 7 Parity Error - A 1 indicates that the last byte received from the keyboard had a parity error. The keyboard sends data with odd parity.

be read through I/O port 60H. The input buffer can be written through both I/O port 64H and 60H. When the input buffer is written through I/O port 64H, the controller interprets it as a command and if it is written through I/O port 60H, then the data is interpreted either as a parameter to a command to the controller or a data to be trans- mitted to the keyboard.

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Bit 5 Transmit Time-Out - A 1 indicates that a data transmission from the keyboard controller to the keyboard was not properly completed within the predefined time limit.

Bit 6 Receive Time-Out - A 1 indicates that a data transmission from the keyboard to the keyboard controller was not properly completed within the predefined time limit.

Bit 7 Parity Error - A 1 indicates that the last byte received from the keyboard had a parity error. The keyboard sends data with odd parity.

Keyboard Controller I/O ports

The keyboard controller has two 8-bit I/O ports one of which is used as an input port and the other as an output port. The following tables show bit definitions for the I/O ports and test input ports.

Input Port Definitions

Bit 0-Bit 3	Undefined
Bit 4	RAM on the system board 0=Total 256 KB of on-board RAM 1=512 KB or greater on-board RAM
Bit 5	Undefined
Bit 6	Display type switch 0=Primary display is color graphics adapter 1=Primary display is monochrome display adapter
Bit 7	Keyboard inhibit switch 0=Keyboard inhibited 1=Keyboard not inhibited

Output Port Definitions

Bit 0	Reset to the system processor (software should keep it 1 for the system Processor to work)
Bit 1	Gate addreSs 20 of system proceSsor 0: The system processoR address 20 is inhibited on the system bus. Address 20 will remain zero for any system processor bus cycle* 1* The system processor address 20 is not inhibited on the system bus.
Bit 2	Undefined
Bit 3	Undefined
Bit 4	Output buffer full interrupt to the system
Bit 5	Input buffer full
Bit 6	Keyboard clock (output)
Bit 7	Keyboard data (output)

System Commands to Keyboard Controller(I/O address 64H)

20	Read keyboard controller's command byte - The controller sends its current command byte to its output buffer.
60	Write keyboard controller's command byte - The next byte of data supplied by the system is the controller's command byte, which is written to I/O address Hex 60.

AE Enable Keyboard Interface - This command enables the keyboard interface and also clears bit 4 of the controller's command byte.

C0 Read Input Port - This commands the keyboard controller to read the input port and place the data in the output buffer.

D0 Read Output Port - This commands the keyboard controller to read the output port and place the data in the output buffer.

D1 Write Output Port - This command is used to write the data given through I/O address 60H to the output port. Ensure that the output port bit 0 is not written as it is connected to the reset of the system processor.

E0 Read Test Inputs - Upon receiving this command the controller reads its T0 and T1 inputs and places the data in the output buffer. Data bit 0 represents T0 and bit 1 represents T1.

F0-FF Pulse output port - Bit 0 through 3 of output port can be pulsed for approximately 6 microseconds by this command. Bit 0 through 3 of this command indicates which bits of the output port are to be pulsed. A 0 indicates that the bit is to be pulsed and a 1 indicates that the bit is to be kept unmodified. Note that bit 0 of the output port is connected to the reset of the system microprocessor. So the processor can be reset by pulsing this bit.

Keyboard controller Keyboard Interface

The keyboard controller communicates with the keyboard over a clock line (bit 6 of the output port) and a data line (bit 7 of the output port). The keyboard controller reads the data line through a test input T1 and the clock line through a test input T0. For any type of data transmission with the keyboard, the keyboard clock is used. Data is made available after the rising edge of the clock and is sampled on the falling edge. The hardware protocol for communication with keyboard is given below.

When the keyboard wants to send data, it first checks the clock line for a high level(the keyboard controller can prevent the keyboard from sending data by driving the clock line low through bit 6 of the output port). If the clock and data lines are high(i.e enabled), the keyboard sends the data. Otherwise it stores data in its own buffer.

The keyboard checks the state of the clock line at an interval of 60 microseconds, in order to sense wheather the keyboard controller intends to send data. When the keyboard controller wants to send data, it forces the clock line low for more than 60 microseconds and then releases it with the data line low. This low data is accepted by the keyboard as a start bit(request to send) and it starts clocking the data in. After the tenth bit, the keyboard forces the data line low for one clock period (the stop bit). This action informs the keyboard controller that the keyboard has received its data.

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SECTION - 5

I/O Channel and Connector Specifications

5.1 I/O Channel Features

The I/O channel supports:-

* 24-bit memory addresses to access 16 megabytes of memory address space

* I/O address space hex 100 to hex 3FF

* Selection of data accesses (either 8- or 16-bit)

* 11 levels of interrupts (IRQ3-IRQ7, IRQ9-IRQ12, IRQ14, IRQ15)

* 'I/O channel check' to generate NMI

* 7 DMA channels (Channel 0-3 for 8 bit data transfer and channel 5-7 for 16 bit data transfer)

* I/O wait state generation

* Open-bus structure (allowing multiple microprocessors to share the system's resources, including memory)

* Refresh of system memory from channel microprocessors

There are 6 62-pin (J23-J28), 4 36-pin (J31-J34) and 1 80 pin edge connector sockets for I/O channel adapter cards. In two positions, the 36-pin connector is not present. These positions can support only 62-pin I/O bus adapters.

5.2 I/O Channel Pin Assignment

The following figures summarize pin assignments for the I/O channel connectors:-

I/O Channel (A-Side: J23 through J30)

I/O Pin	Signal Name	I/O
A 1	-IOCHCK	I
A 2	SD7	I/O
A 3	SD6	I/O
A 4	SD5	I/O
A 5	SD4	I/O
A 6	SD3	I/O
A 7	SD2	I/O
A 8	SD1	I/O
A 9	SD0	I/O
A 10	IOCHRDY	I
A 11	AEN	O
A 12	SA19	I/O
A 13	SA18	I/O
A 14	SA17	I/O
A 15	SA16	I/O
A 16	SA15	I/O
A 17	SA14	I/O
A 18	SA13	I/O
A 19	SA12	I/O
A 20	SA11	I/O
A 21	SA10	I/O
A 22	SA9	I/O
A 23	SA8	I/O
A 24	SA7	I/O
A 25	SA6	I/O
A 26	SA5	I/O
A 27	SA4	I/O
A 28	SA3	I/O
A 29	SA2	I/O
A 30	SA1	I/O
A 31	SA0	I/O

I/O Channel (B-Side: J23 THROUGH J30)

I/O pin	Signal Name	I/O
B 1	GND	Ground
B 2	RESETDRV	O
B 3	VCC	Power
B 4	IRQ9	I
B 5	-5V	Power
B 6	DRQ2	I
B 7	-12V	Power
B 8	0WS#	I
B 9	+12V	Power
B 10	GND	Ground
B 11	SMEMW#	O
B 12	SMEMR#	O
B 13	IOWR#	I/O
B 14	IORD#	I/O
B 15	-DACK3	O
B 16	DRQ3	I
B 17	-DACK1	O
B 18	DRQ1	I
B 19	REFRESH#	I/O
B 20	SYSCLK	O
B 21	IRQ7	I
B 22	IRQ6	I
B 23	IRQ5	I
B 24	IRQ4	I
B 25	IRQ3	I
B 26	-DACK2	O
B 27	T/C	O
B 28	BALE	O
B 29	VCC	Power
B 30	OSC	O
B 31	GND	Ground

I/O Channel (C-side: J31 through J38)

I/O Pin	Signal Name	I/O
C 1	SBHE	I/O
C 2	LA23	I/O
C 3	LA22	I/O
C 4	LA21	I/O
C 5	LA20	I/O
C 6	LA19	I/O
C 7	LA18	I/O
C 8	LA17	I/O
C 9	MEMR#	I/O
C 10	MEMW#	I/O
C 11	SD08	I/O
C 12	SD09	I/O
C 13	SD10	I/O
C 14	SD11	I/O
C 15	SD12	I/O
C 16	SD13	I/O
C 17	SD14	I/O
C 18	SD15	I/O

I/O Channel (D-Side: J31 Through J38)

I/O Pin	Signal Name	I/O
D 1	MCS16#	I
D 2	IOCS16#	I
D 3	IRQ10	I
D 4	IRQ11	I
D 5	IRQ12	I
D 6	IRQ15	I
D 7	IRQ14	I
D 8	-DACK0	O
D 9	DRQ0	I
D 10	-DACK5	O
D 11	DRQ5	I
D 12	-DACK6	O
D 13	DRQ6	I
D 14	-DACK7	O
D 15	DRQ7	I
D 16	VCC	Power
D 17	-MASTER	I
D 18	GND	Ground

5.3 I/O Channel signal description

The following is a description of the system board I/O channel signals. All signal lines are TTL compatible. The I/O adapter boards should be designed with a maximum of two (LS) Low-power Schottky loads per line.

SA0-SA19 (I/O)
These address bits are used to address system memory and I/O devices. These lines, alongwith LA17 through LA23, allow upto 16MB of memory access. SA0 through SA19 are gated on the system bus when 'BALE' is high and latched on the falling edge of 'BALE'. These signals are driven by system board microprocessor or DMA controller. They can also be driven by other bus masters residing on the I/O channel, by activating the '-MASTER' signal.

LA17-LA23 (I/O)
These signals are used to address memory and I/O devices within the system. They are not latched, and are valid only when 'BALE' is high. These signals do not remain valid throughout the whole processor cycle. Their purpose is to generate memory decodes for 1 wait state memory cycles. These decodes should be latched by I/O adapters on the falling edge of 'BALE'. These signals may be driven by other microprocessors or DMA controllers, residing on the I/O channel, by activating the '-MASTER' signal.

SBHE (I/O)
'Byte high enable', when low, indicates a transfer of data on the upper byte of the 16-bit data bus (SD8 through SD15). Sixteen bit devices use this signal to condition the data bus buffers connected to SD8 through SD15.

SD0-SD15 (I/O)
These are data bus signals 0 through 15 for memory and I/O devices on the I/O adapter cards. SD0 is the least significant and SD15 is the most significant bit. All communications to 8-bit devices on the I/O channel should be through SD0 to SD7. For 16-bit devices on I/O channel SD0 through SD15 is used. 32- or 24-bit transfers, as well as misaligned 16-bit ones, from the 80386 are split up into two cycles of 16 bit or less. The data is gated to the appropriate part of the 32-bit processor data bus. Similarly, 16 bit transfers to 8-bit devices will be again converted into two 8-bit transfers with SD8 to SD15 gated to SD0 to SD7 whenever necessary.

BALE (Buffered ALE) (O)
'Address latch enable' is used to latch valid addresses and memory decodes on the system board. To the I/O channel, it indicates a valid CPU address. When used with AEN, it indicates a valid DMA address. Microprocessor addresses SA0 to SA19 are gated when

BALE is high and are latched with the falling edge of BALE. BALE is forced high when the system processor goes to hold state, so that the address and memory decode latches become flow-through.

RESETDRV (O)
This active high signal is used to reset or initialize system logic at power-up, during hard reset or a low line-voltage.

SYSCLK (O)
For system board running at 6 or 16 MHz, the time period of this clock is 167 or 125 nanoseconds respectively. At 6 MHz, this is the inverse of the CLK output from 82384. At 16 MHz, it is CLK divided by two. This clock has a 50% duty cycle and is synchronous with the microprocessor clock. This signal should only be used for synchronization. It is not intended for uses requiring a fixed frequency.

-IOCHCK (I)
This signal is used by the I/O adapter channel cards to report any fatal error (e.g, parity error information on I/O channel memory cards or error on I/O devices).

IOCHRDY (I)
'I/O channel ready' is used by memory or I/O devices to extend memory or I/O cycles. A slow device, requiring more than the bus cycle time provided by the system board, should pull IOCHRDY low (not active) immediately after detecting valid address together with Read or Write command. Machine cycles are extented by an integral number of SYSCLK cycles (e.g, 167 ns at 6 MHz). This signal should not be held low for more than 2.5 microseconds.

IRQ3-IRQ7, IRQ9-IRQ12 and IRQ14 to IRQ15 (I)
These positive edge triggered Interrupt Requests are used by I/O channel adapter cards, to indicate to the microprocessor that it requires attention. The interrupt requests are prioritized. The priority is as shown, in decreasing order: IRQ9 through IRQ12, IRQ14, IRQ15 and IRQ3 through IRQ7. An interrupt request is generated by raising an IRQ line from low to high. The line must be held high until the processor acknowledges the interrupt request (Interrupt service routine). IRQ0-IRQ2, IRQ8 and IRQ13 are used by the system board.

IORD# (I/O)
'I/O read', an active low signal, instructs the selected I/O device to drive its data onto the data bus. This signal may be driven by the system microprocessor, system board DMA controllers, or by a microprocessor or DMA controller resident on the I/O channel.

IOWR# (I/O)
'I/O write', an active low signal, instructs the selected I/O device to read data from the data bus. . It may be driven by the system microprocessor, system board DMA controllers, or by a microprocessor or DMA controller resident on the I/O channel.

SMEMR# (O), MEMR# (I/O)
These signals instruct the memory devices to drive data onto the data bus. Both of these signals are active low. SMEMR# signal is generated for any read in low 1MB of memory space, and can be driven by the system board microprocessor and DMA controllers only. MEMR# is active in all memory read cycles and can be driven by any microprocessor or DMA controller in the system. SMEMR# is generated from MEMR# qualified with the decode of the low 1MB of memory. There is one exception. When SW1 is ON, SMEMR# is not generated for address 0C0000 thru 0C7FFF. When a microprocessor or a DMA controller, on the I/O channel, wants to drive the MEMR# signal, it must drive the address lines valid at least one SYSCLK period before driving MEMR# active.

SMEMW# (O), MEMW# (I/O)
These signals, both active low, instruct the memory devices to store the data present on the data bus. MEMW# signal is active in all memory write cycles and can be driven by any microprocessor or DMA controller in the system. SMEMW# signal is active in all memory write cycles in low 1MB of memory space. It is generated from MEMW# signal, qualified with the decode of the low 1MB of memory. This has one exception. When SW1 is ON, SMEMW# is not generated for address 0C0000 thru 0C7FFF. SMEMW# can only be driven by the system board microprocessor and DMA controllers. When a microprocessor or a DMA controller, on the I/O channel, wants to drive the MEMW# signal, it must drive the address lines valid at least one SYSCLK period before driving MEMW# active.

DRQ0-DRQ3 and DRQ5-DRQ7 (I)
DMA requests 0 through 3 and 5 through 7 are asynchronous, active high, channel requests. They are used by peripheral devices and I/O channel microprocessors, to gain DMA service or control of the system. An I/O channel microprocessor can gain control of the system by activating a DMA request line, and then activating -MASTER signal after getting DMA acknowledge (DACK) signal. The DMA request lines are prioritized with DRQ0 having the highest priority and DRQ7 having the lowest. A DMA request is generated by bringing the DRQ line to an active (high) level and keeping it active until the corresponding DACK signal goes active. DRQ0-DRQ3 are used for 8-bit data transfers between 8-bit I/O device and 8/16-bit memory device. DRQ5-DRQ7 are used for 16-bit data transfer between 16-bit I/O device and 16-bit memory device. DRQ4 is used in the system board for cascading the two DMA controllers, and is not available on the I/O channel.

-DACK0 to-DACK3 and -DACK5 to -DACK7 (O)
DMA acknowledge signals 0 through 3 and 5 through 7 are used to acknowledge requests on the corresponding DMA request lines. They are active low.

REFRESH# (I/O)
This active low signal is used to indicate a dynamic memory refresh cycle and can be driven by any microprocessor on the I/O channel. This signal is generated after every 15 microseconds.

AEN (O)
'Address enable', high active, signal is used to degate the microprocessor and other devices from the I/O channel, to enable DMA transfers to take place. When this signal is active, the DMA controller has the control of address bus, data bus, memory control (SMEMR#, SMEMW#, MEMR#, MEMW#) and I/O control (IORD#, IOWR#) signals.

T/C (O)
'Terminal count', normally low, provides a pulse when any DMA channel reaches the terminal count.

-MASTER (I)
This signal is used by a microprocessor or DMA controller residing on the I/O channel to gain control of the system bus. The procedure to gain control of the system bus is as follows:-

-Issue a DRQ to a DMA channel in cascade mode.

-Upon receiving a -DACK, pull the -MASTER signal low to gain control of the system address, data and control lines.

-After -MASTER is low, the I/O microprocessor should wait at least one SYSCLK period before driving the address and data lines and two SYSCLK period before driving the control lines (MEMR#, MEMW#, IORD#, IOWR#).

If -MASTER signal is held low for more than 15 microseconds, system memory data may be lost due to lack of refresh. The I/O microprocessor (in control) can take care of this by activating the REFRESH# signal.

MCS16# (I)
'-MEM 16 chip select' indicates to the system board whether the present data transfer is a 16-bit 1 wait-state memory cycle (true at 6 MHz system board operation). At 16 MHz the number of wait states is increased, to allow at least 500ns for the machine cycle. It must be derived from decoding address LA17 through LA23. 'MCS16#' is an active low signal and should be driven with an open collector or tri-state driver capable of sinking 20mA.

IOCS16# (I)
'-I/O 16 bit chip select' signals to the system board that the present I/O data transfer is a 16-bit I/O cycle, requiring at least 375ns. This active low signal is derived from an address decode, and should be driven with an open collector or tri-state driver capable of sinking 20 mA.

OSC (O)
'Oscillator' is a 14.31818 MHz clock with a duty cycle of 50%.. This signal is not synchronous with SYSCLK. This signal is used in Color Graphics Adapter card.

0WS# (I)
'0-wait state' signal is used to tell the system microprocessor that the present bus cycle can be completed without inserting any additional wait states at 6 MHz. In order to run a memory cycle on a 16-bit memory device, without wait states, 0WS# signal should be derived from an address decode gated with a read or write command (also MCS16# signal has to be activated). At 16 MHz, a minimum cycle time of 330ns is assured. In order to run a memory cycle to an 8-bit device with a minimum of 2-wait states, 0WS# should be driven active one system clock after the read or write command is active, gated with the address decode for the device. Memory read or write commands to an 8-bit device are active on the falling edge of SYSCLK. At 6 MHz, the machine cycle is terminated at the end of the CLK cycle, if 0WS# is sampled low in the middle of the CLK cycle. At 16 MHz, for a 8-bit cycle, the machine cycle is terminated 2 CLK cycles after 0WS# is sampled low. For a 16 bit cycle, a cycle time of 250ns is guaranteed. 0WS# is an active low signal and should be driven with an open collector or tri-state driver capable of sinking 20mA.

5.4 Connectors

The system board contains following connectors:

*** Two power-supply connectors (PS8, PS9)**

Pin assignments are as follows:-

Pin	Assignments	Connector
1	Power Good	
2	VCC	
3	+12V	PS8
4	-12V	
5	Ground	
6	Ground	
1	Ground	
2	Ground	
3	-5V	PS9
4	VCC	
5	VCC	
6	VCC	

*** Reset Push-button Connector (J2)**

It is a 2 pin BERG strip. When shorted, this gives hard reset to the system. The pin assignment is as follows:-

Pin	Assignments
1	Hard reset
2	Ground

*** Battery connector (J21)**

It is a 4-pin, keyed, Berg strip. This is used to supply power to CMOS real time clock when the system is powered off. The pin assignments are as follows:-

Pin	Assignments
1	6V dc
2	Not used
3	Not used
4	Ground

*** Keyboard connector (J22)**

It is a 5-pin, 90 degree PCB mountable DIN connector. The pin assignments are as follows:-

Pin	Assignments
1	Keyboard clock
2	Keyboard data
3	Not used
4	Ground
5	VCC

*** Power LED and keylock connector (J20)**

It is a 5-pin BERG strip. The following are the pin assignments:-

Pin	Assignments
1	LED power
2	Key
3	Ground
4	Keyboard Inhibit
5	Ground

*** Speaker connector (J19)**

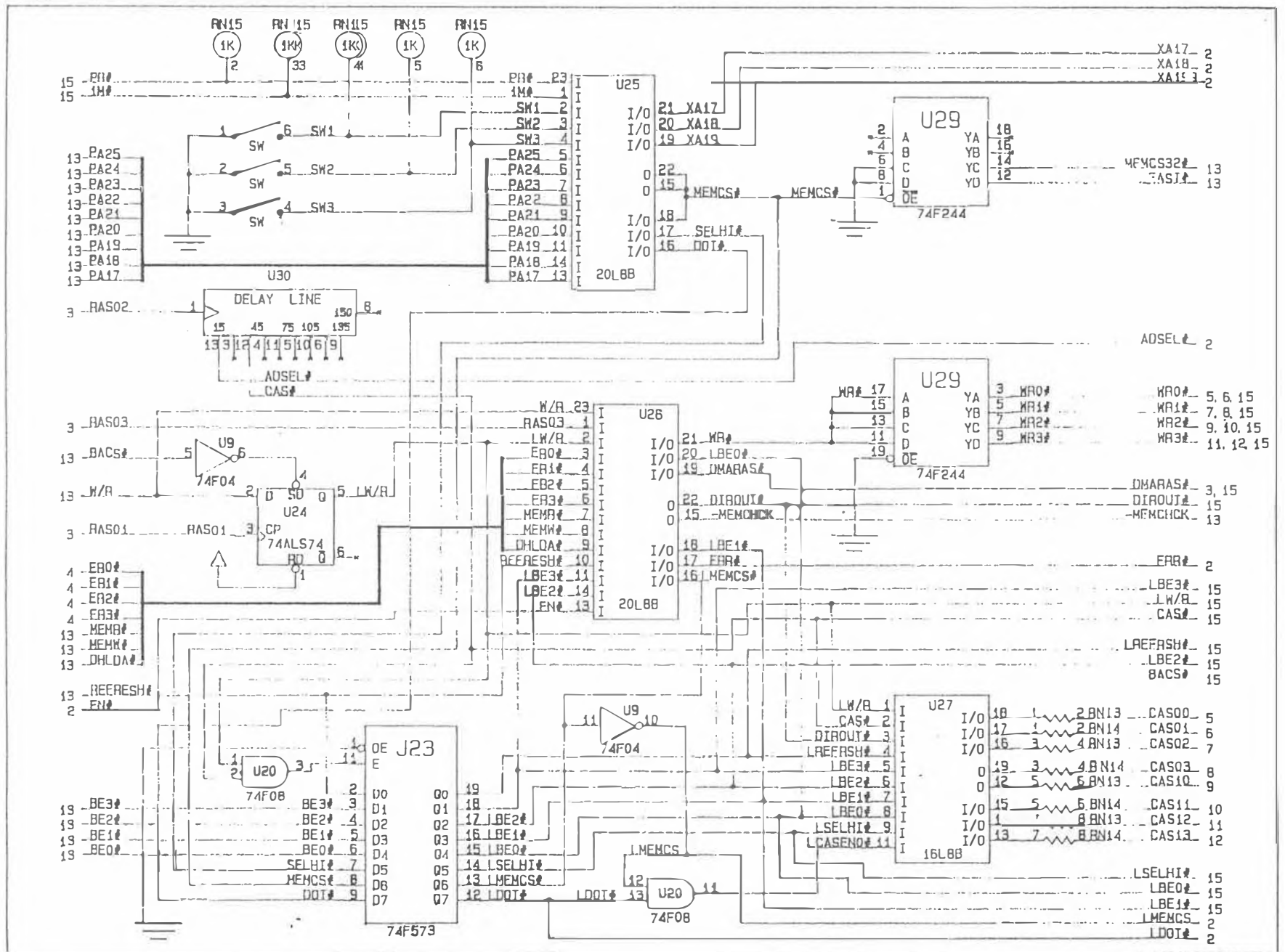
It is a 4-pin, keyed, BERG strip. The pin assignments follow:-

Pin	Assignments
1	Data out
2	Key
3	Ground
4	VCC

*** Turbo LED connector (J1)**

This is a 2-pin BERG strip for connecting the LED indicator for clock speed. The LED glows when pin is low (clock speed is 16MHz). The pin assignment is as follows:-

Pin	Assignment
1	Clock speed
2	LED power



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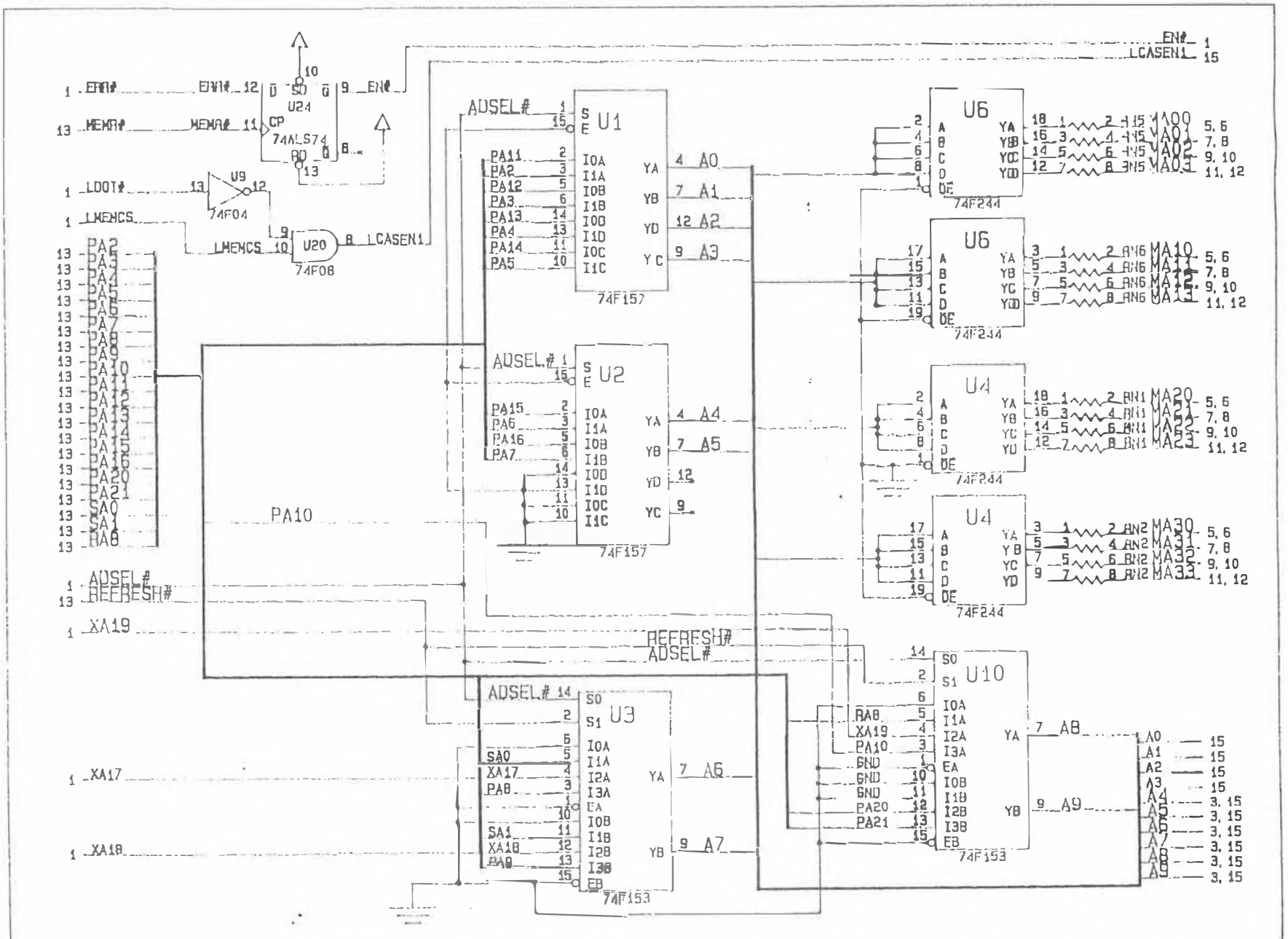
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U9
74F04
U20
74F08
U1
74F157
U2
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U3
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U6
74F244
U4
74F244
U6
74F244
U4
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U10
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REFRESH#
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XA17
XA18
PA10
LDOT#
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EN#
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PA3
PA4
PA5
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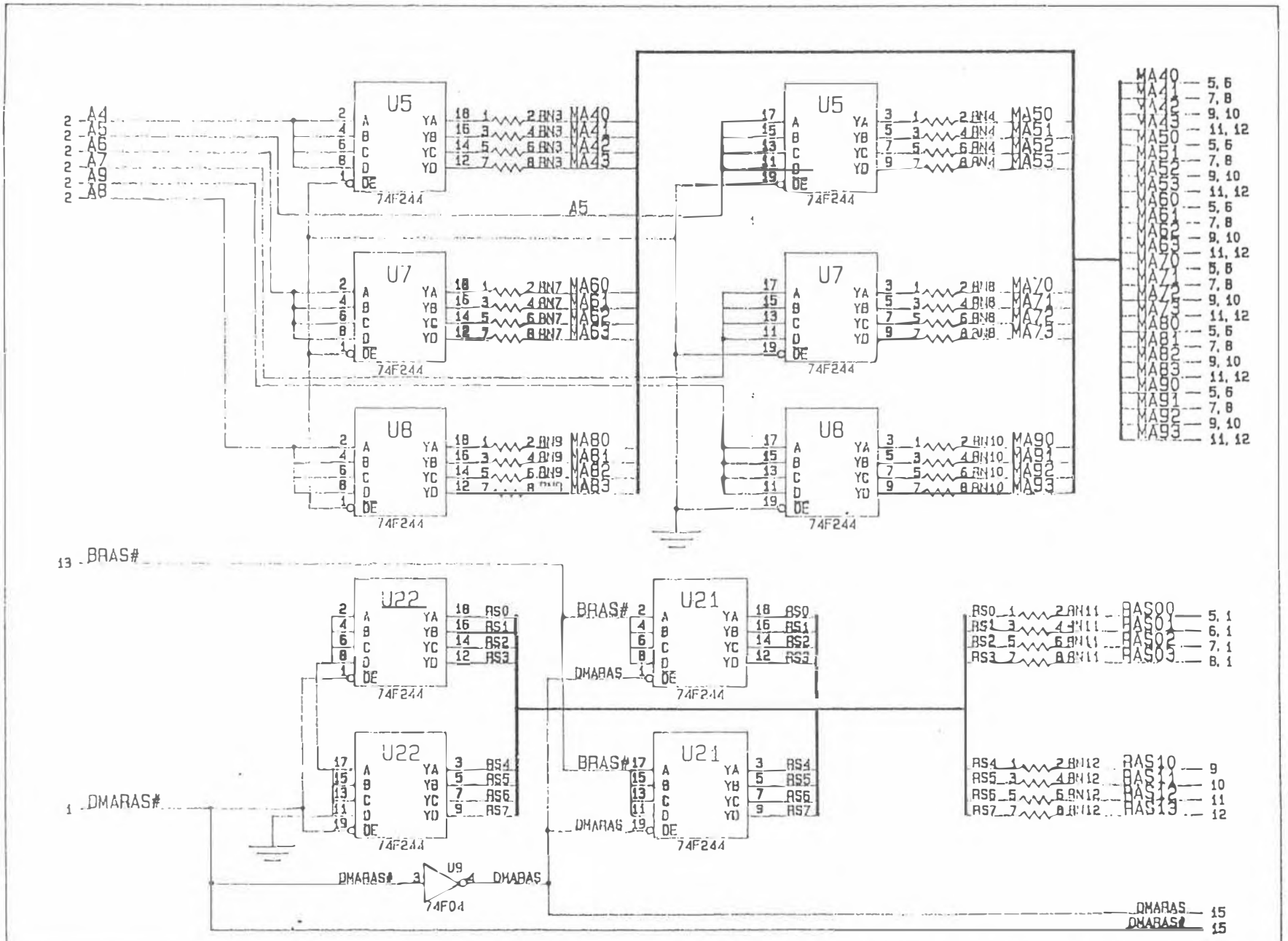
MA30
MA31
MA32
MA33



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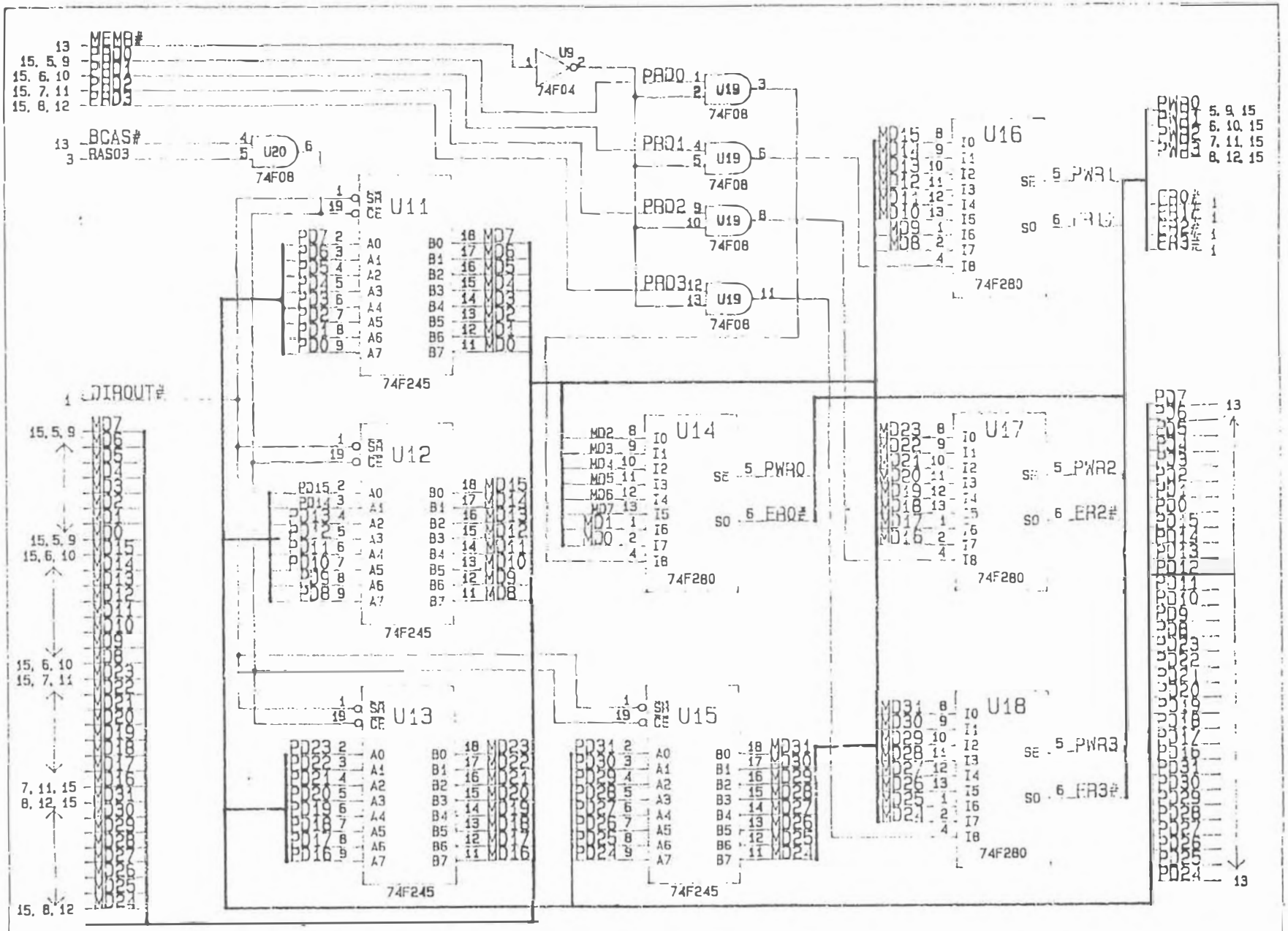

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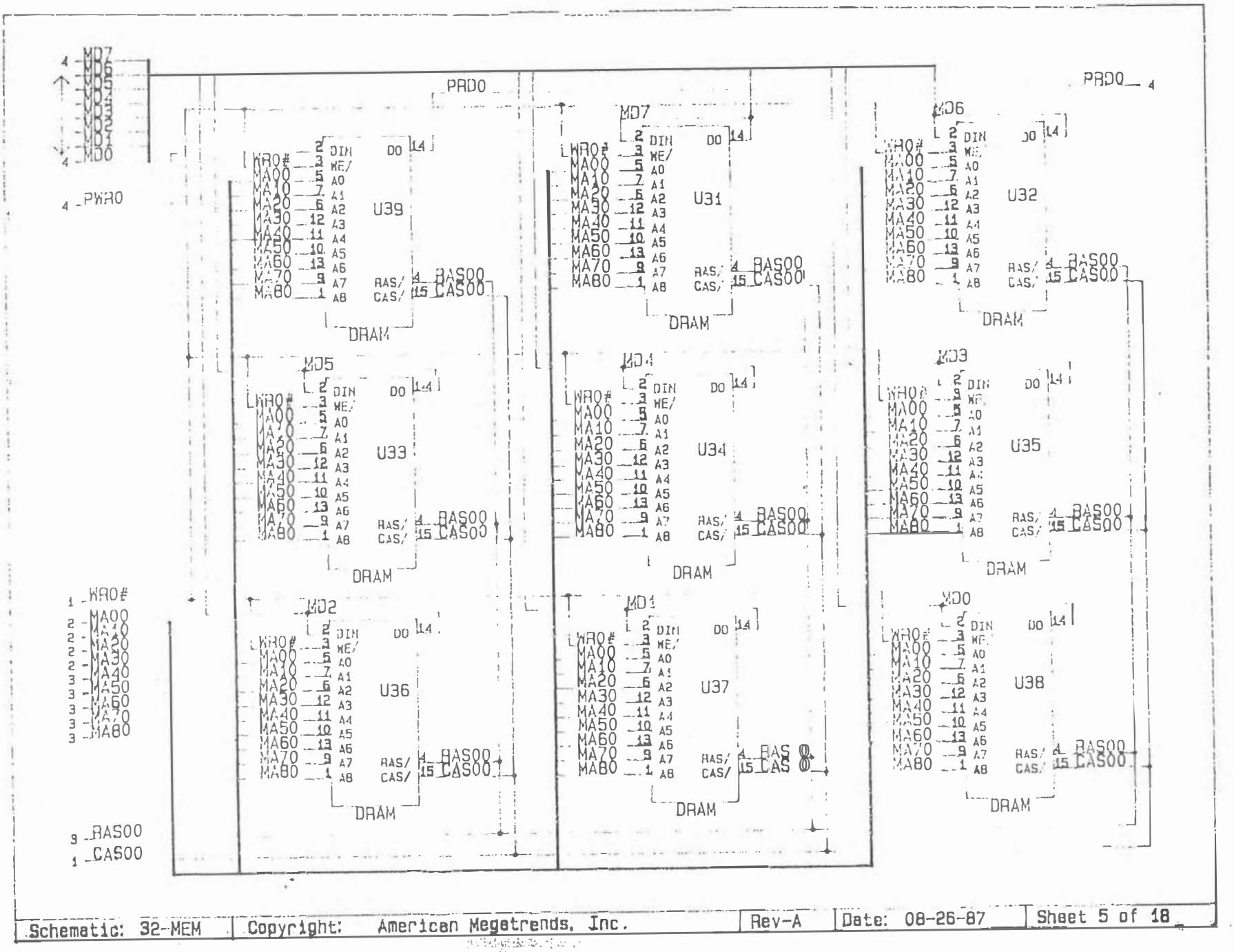

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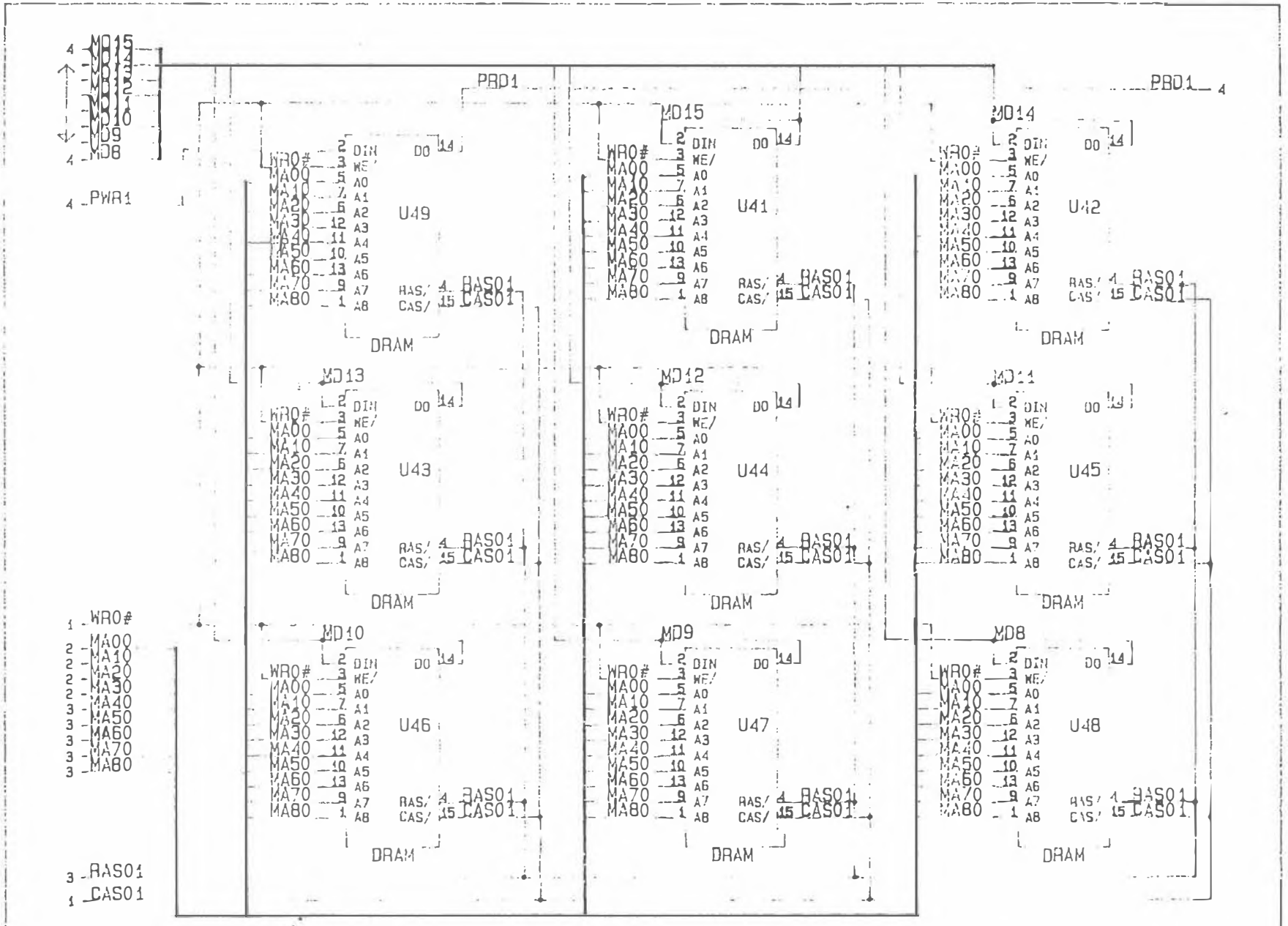
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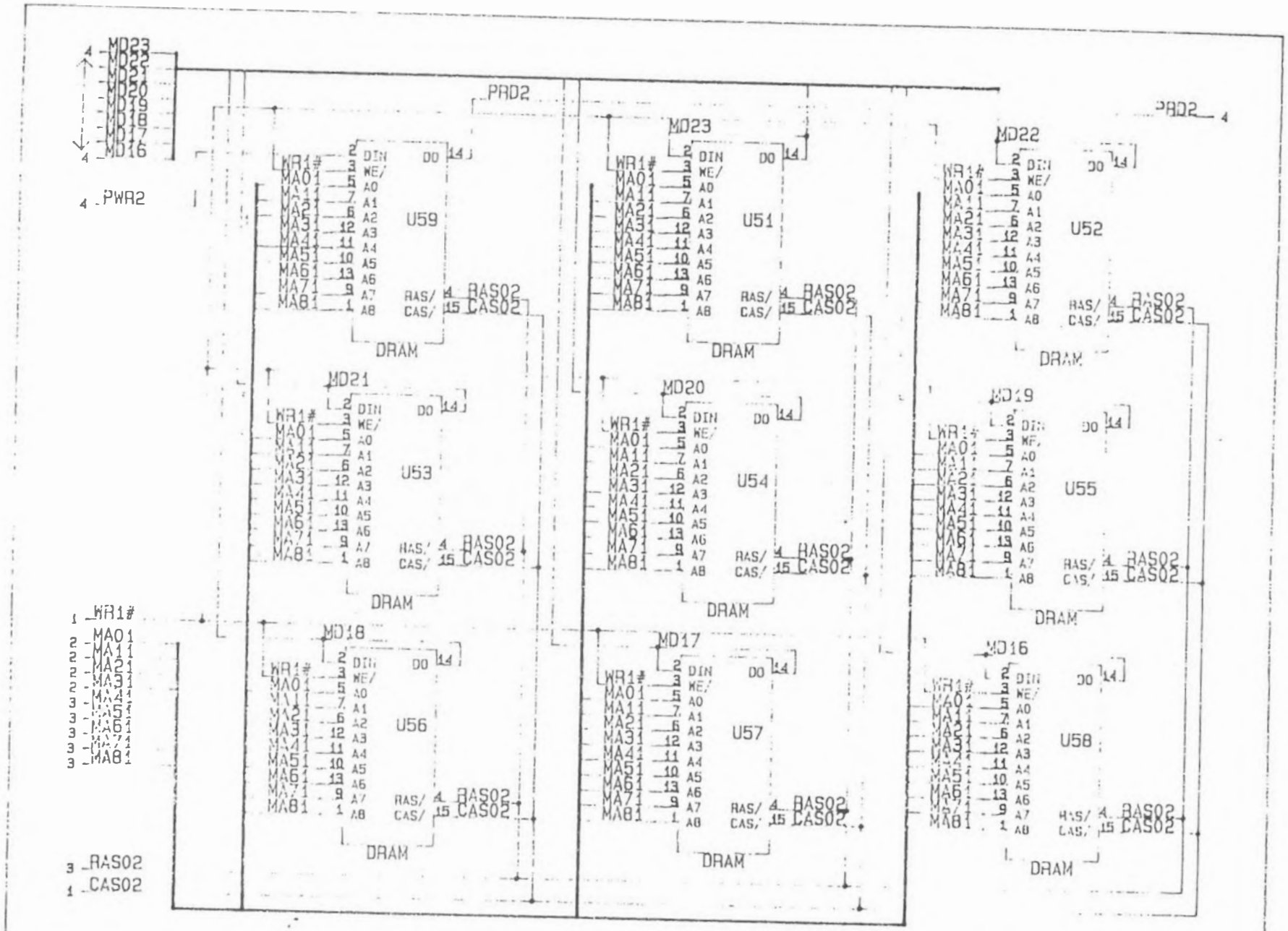
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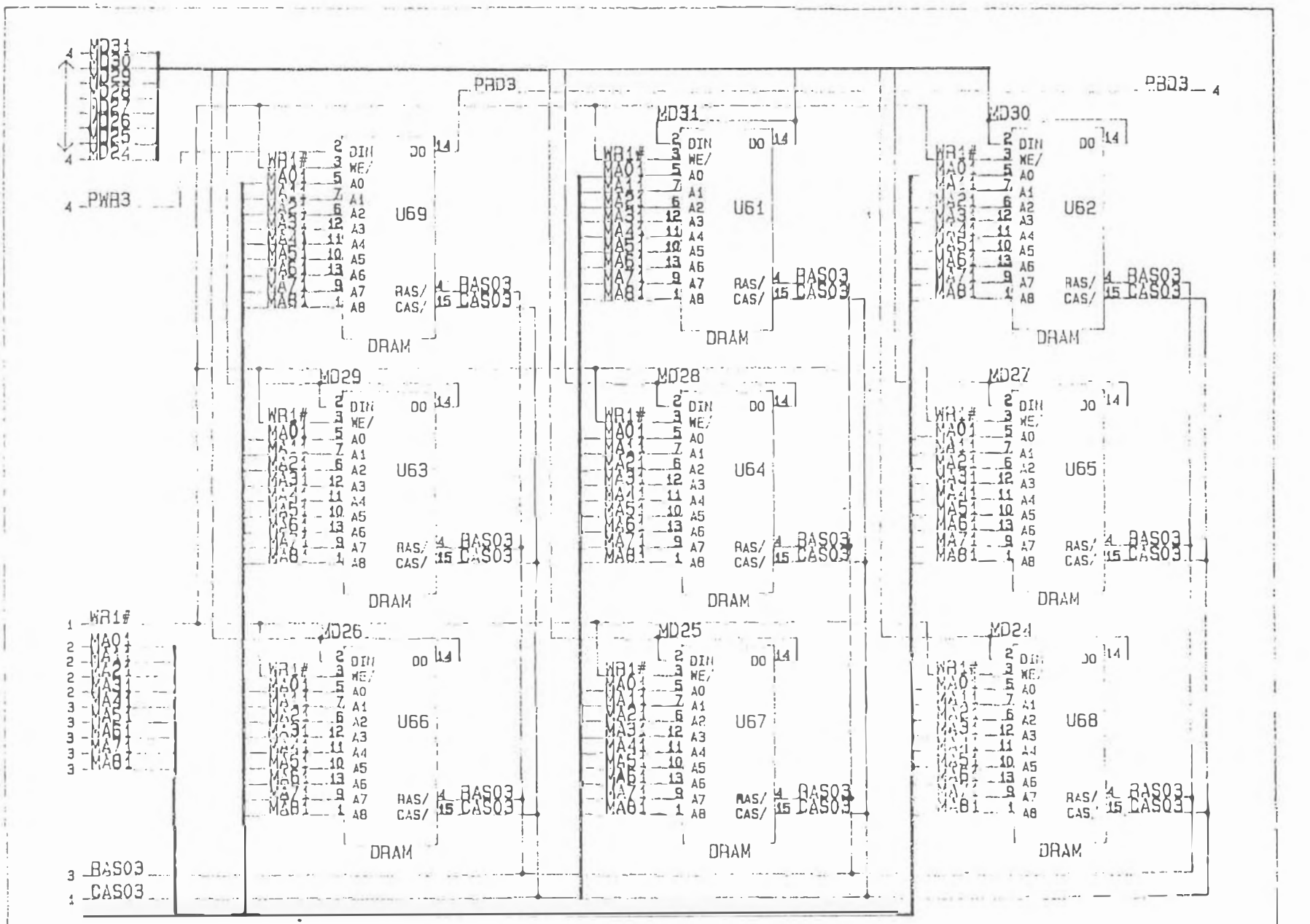

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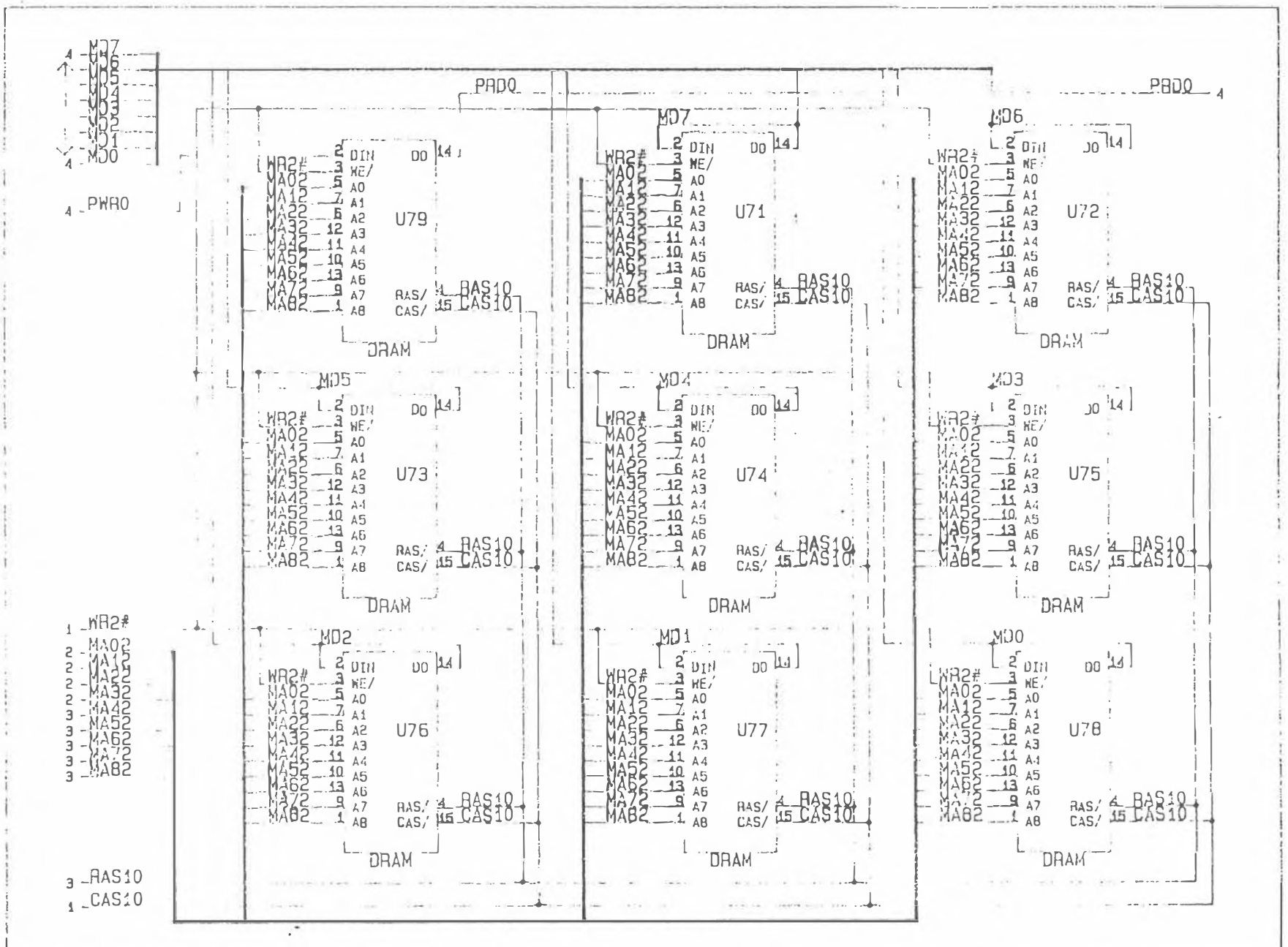
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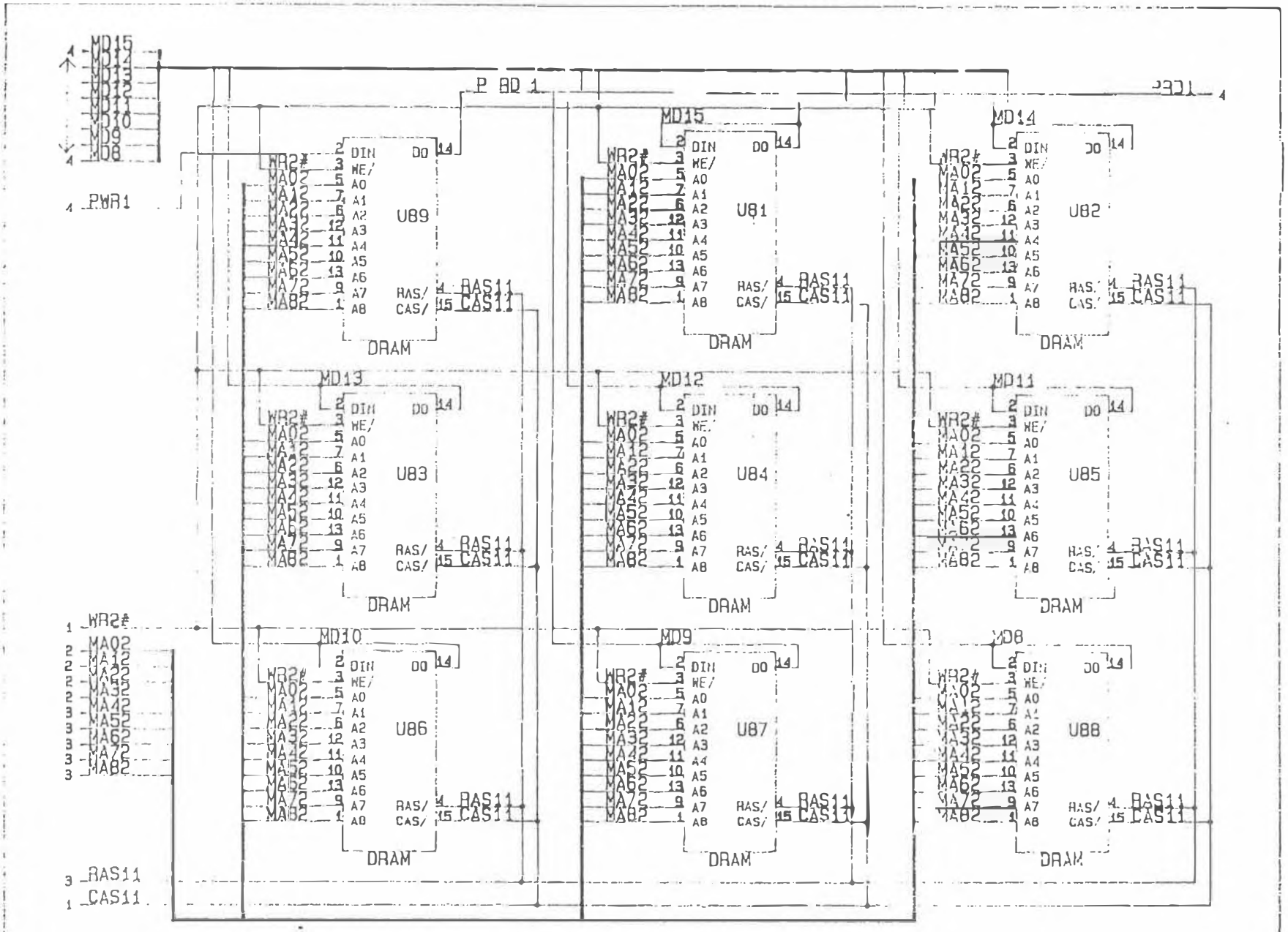

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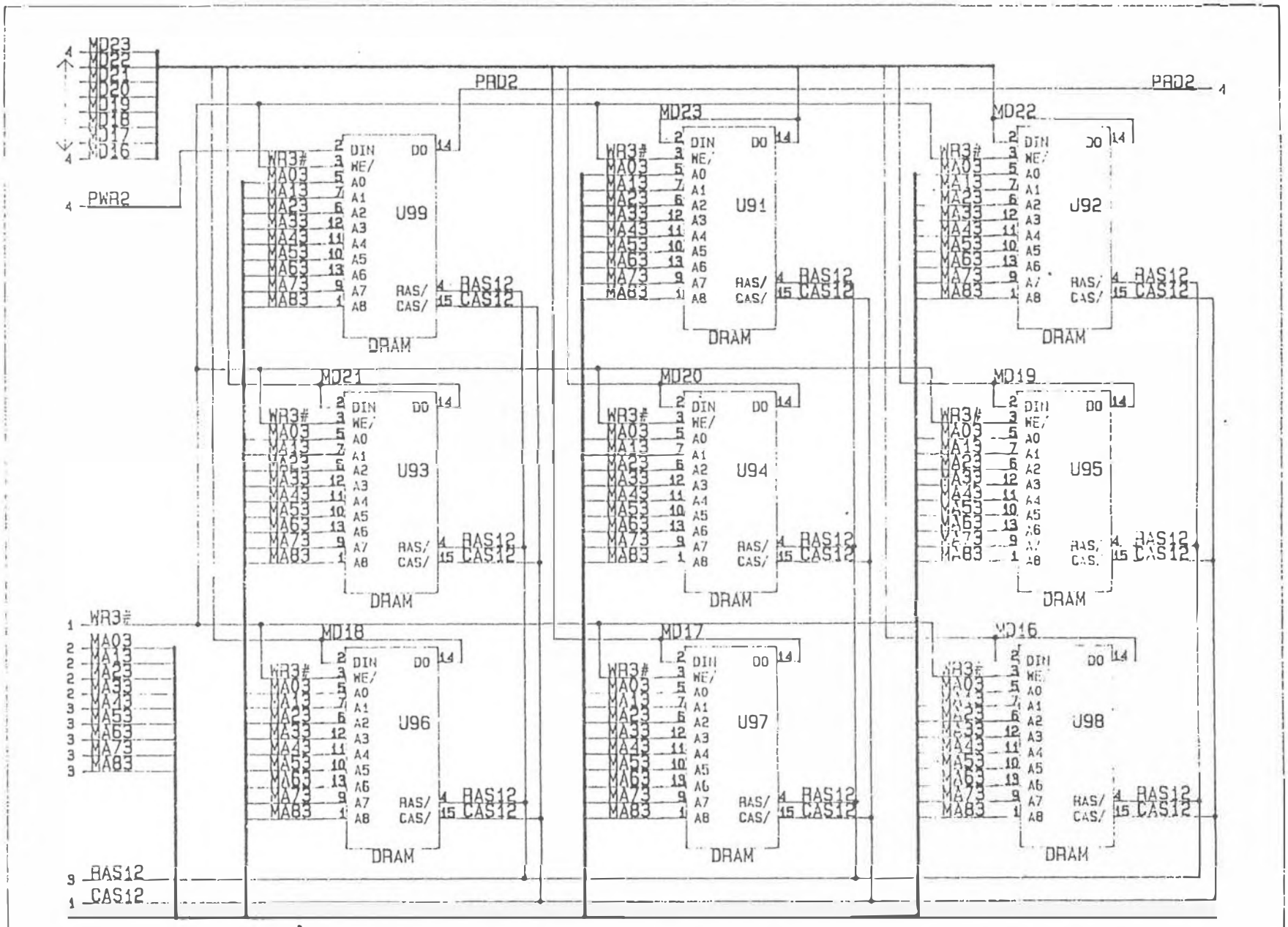
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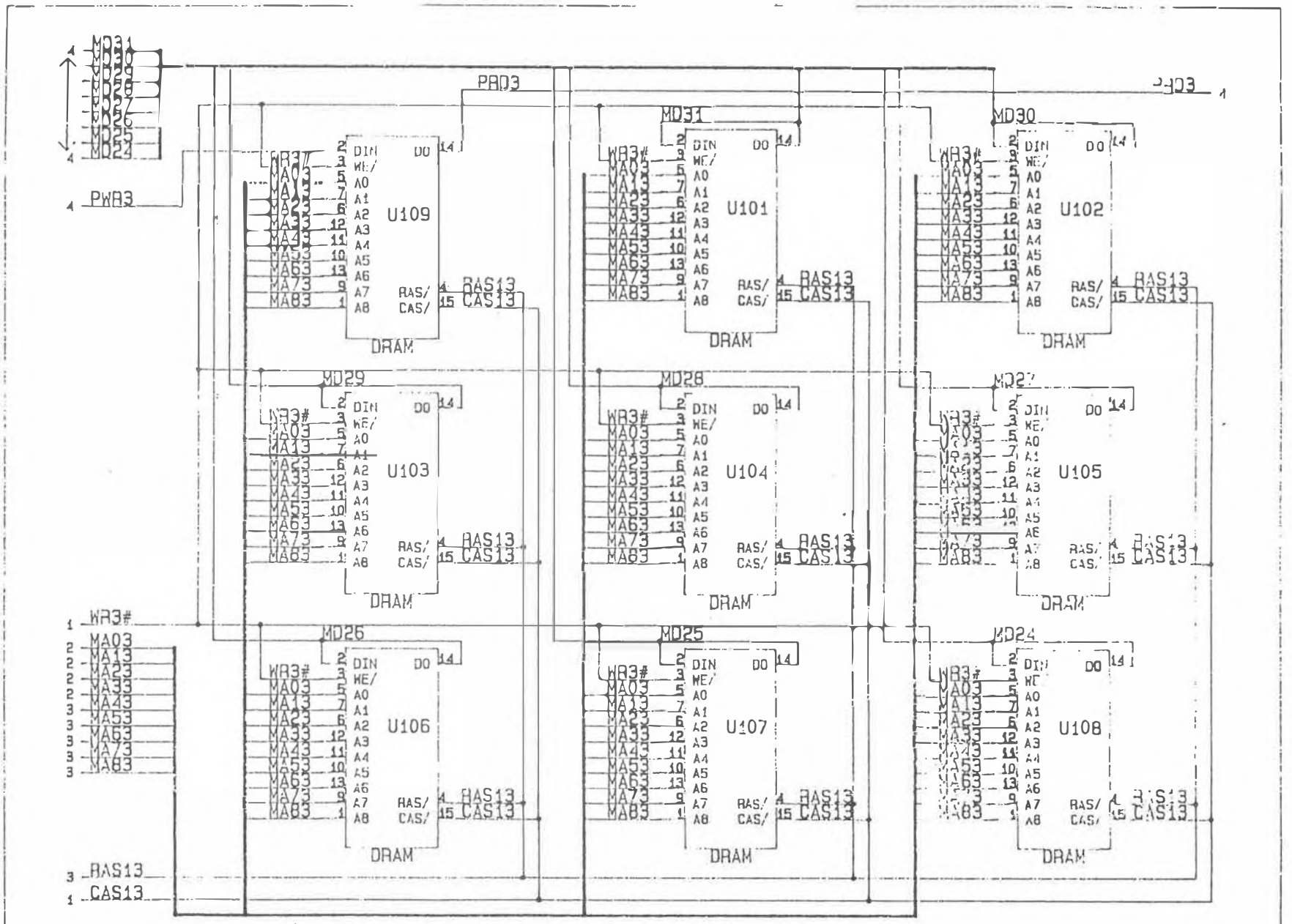

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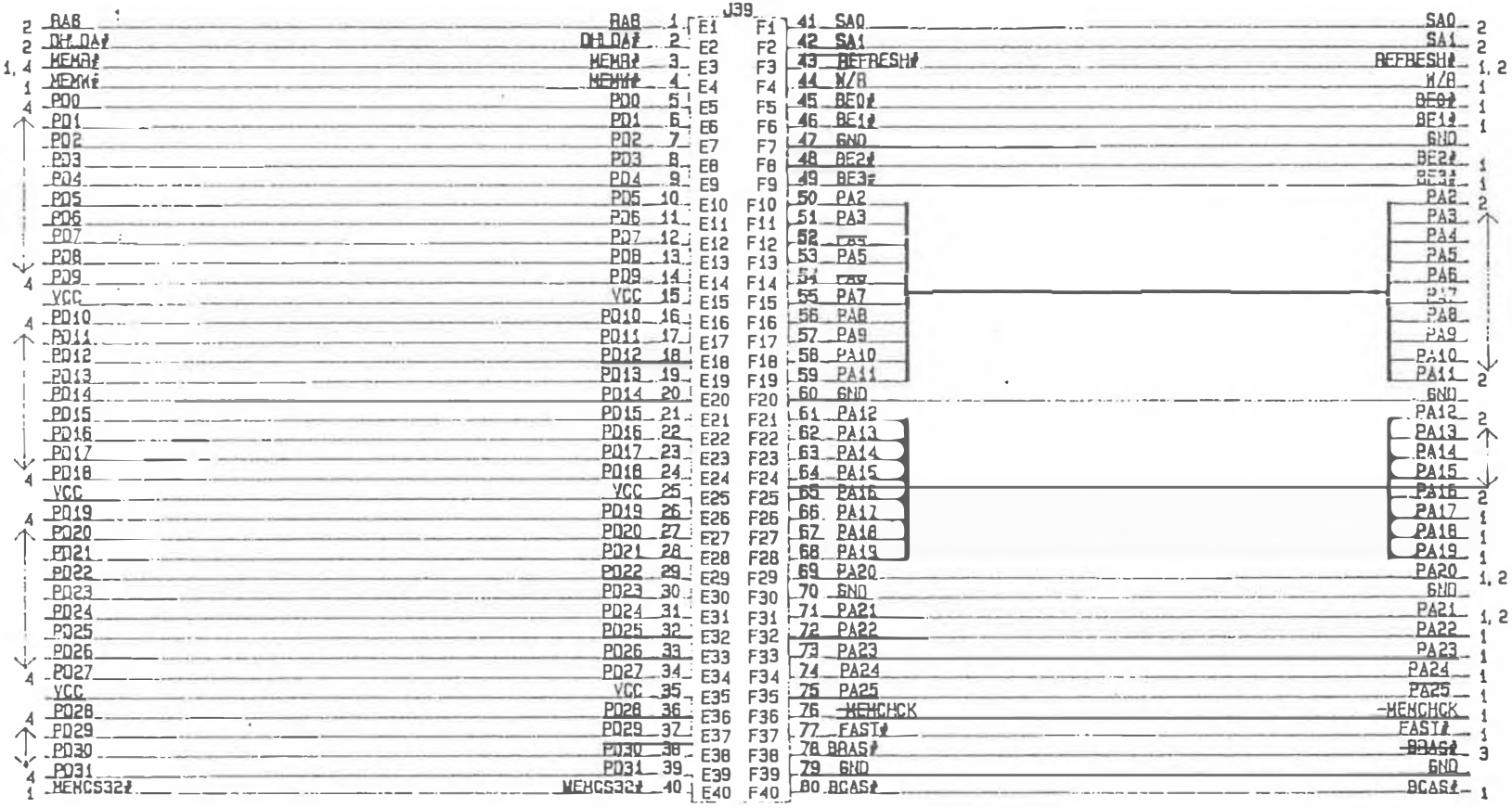

Schematic: 32-MEM	Copyright: American Megatrends, Inc.	Rev-A	Date: 08-26-87	Sheet 13 of 18


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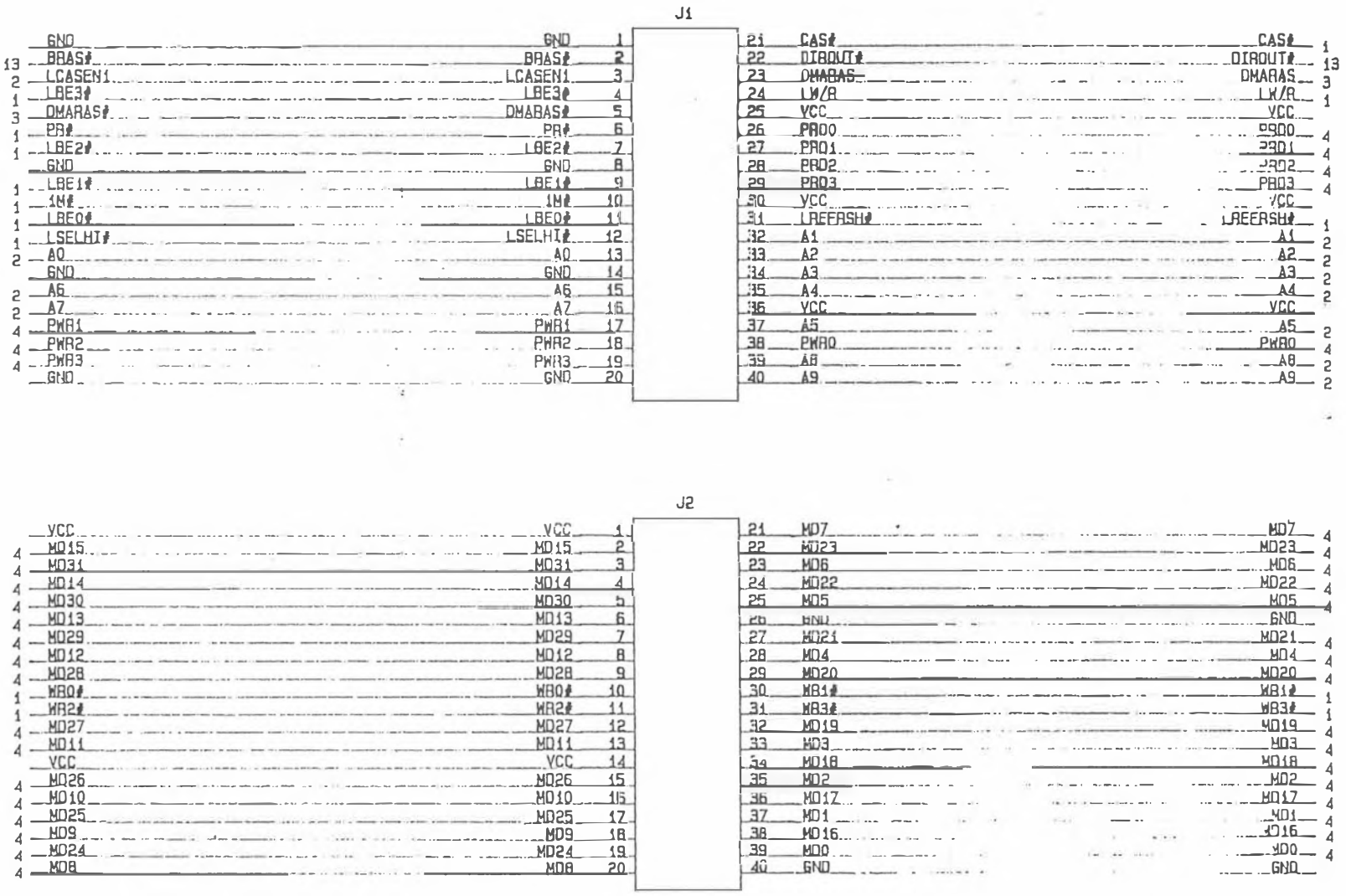
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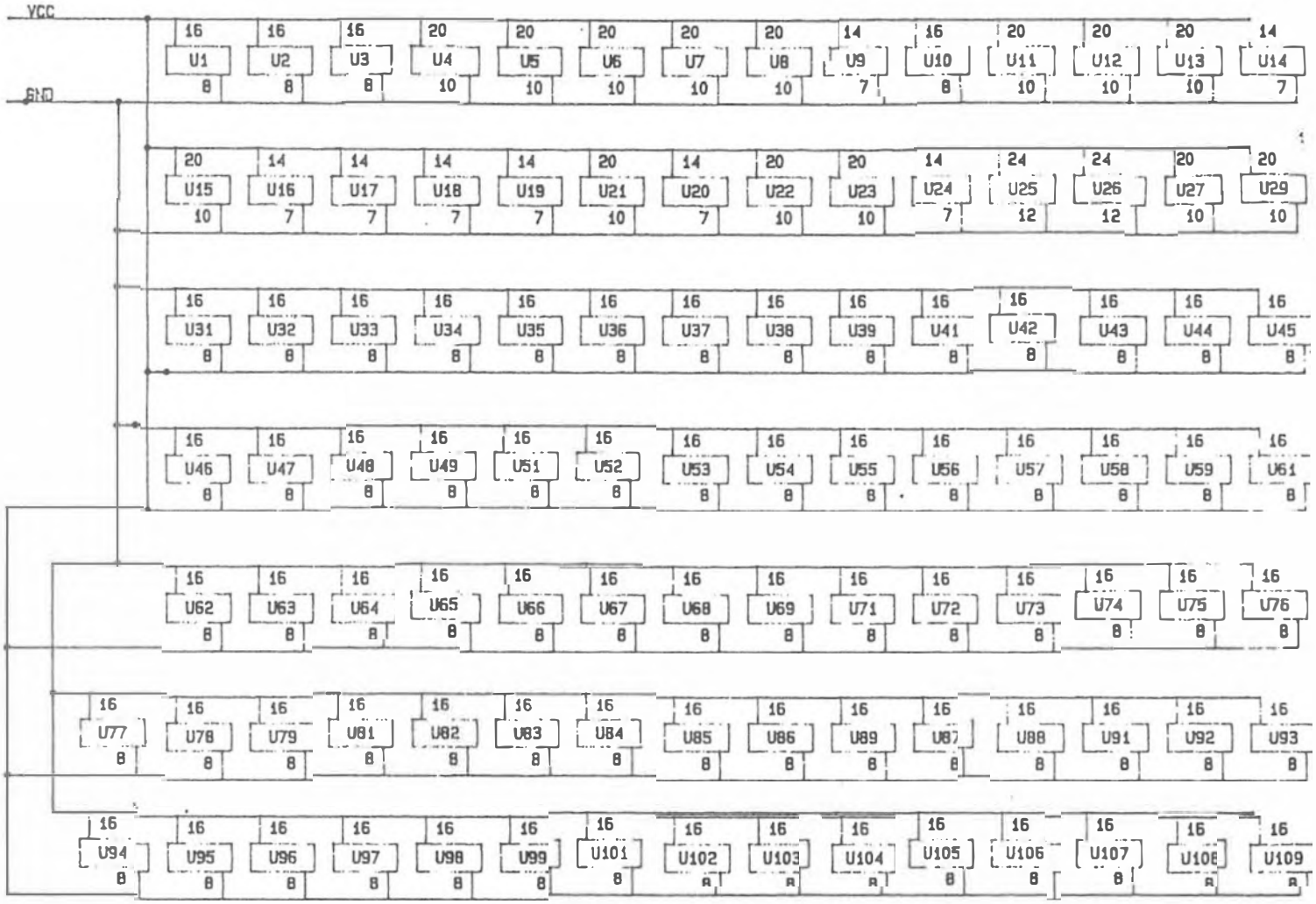

Schematic: 32-MEM	Copyright: American Megatrends, Inc.	Rev-A	Date: 08-26-87	Sheet 16 of 18

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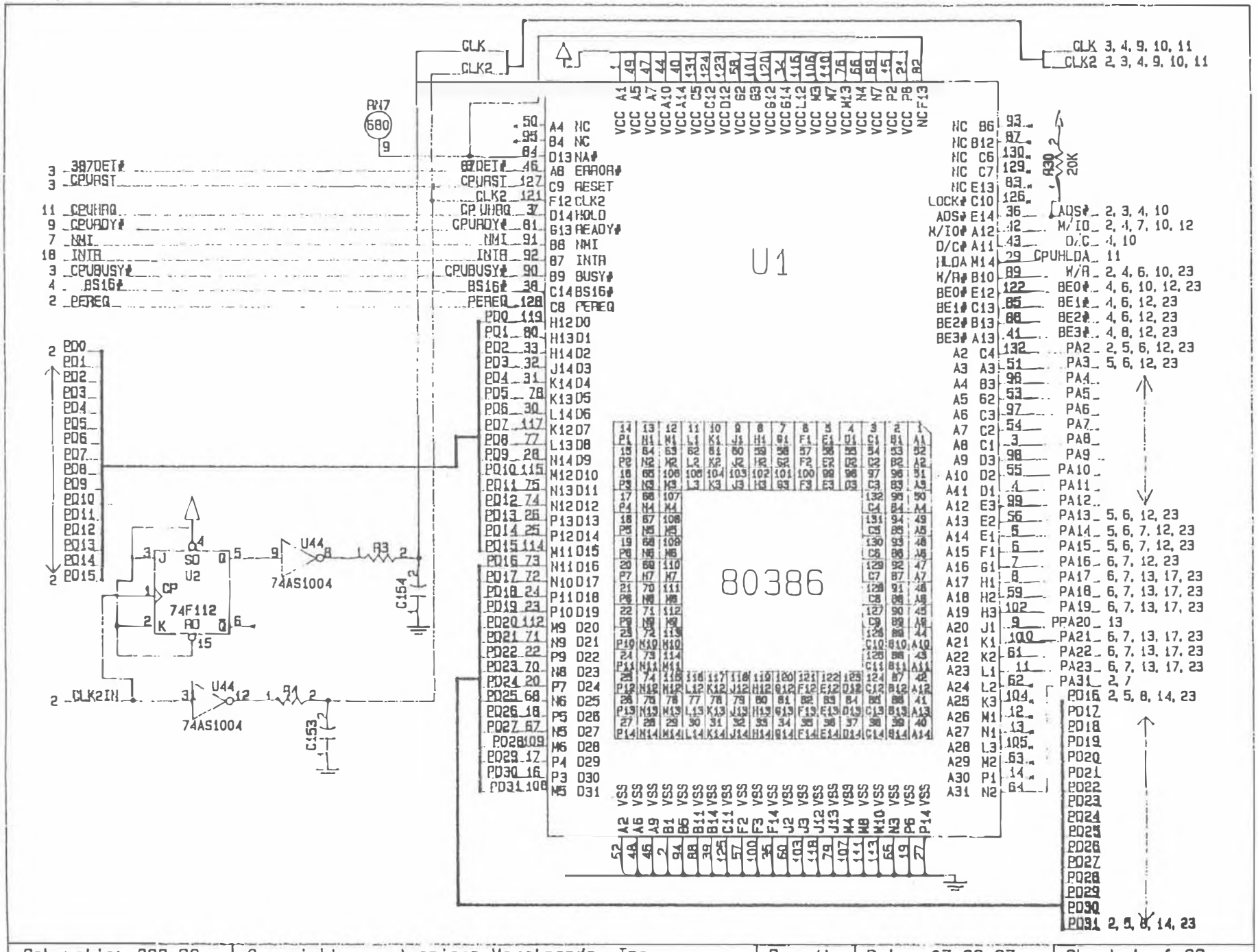

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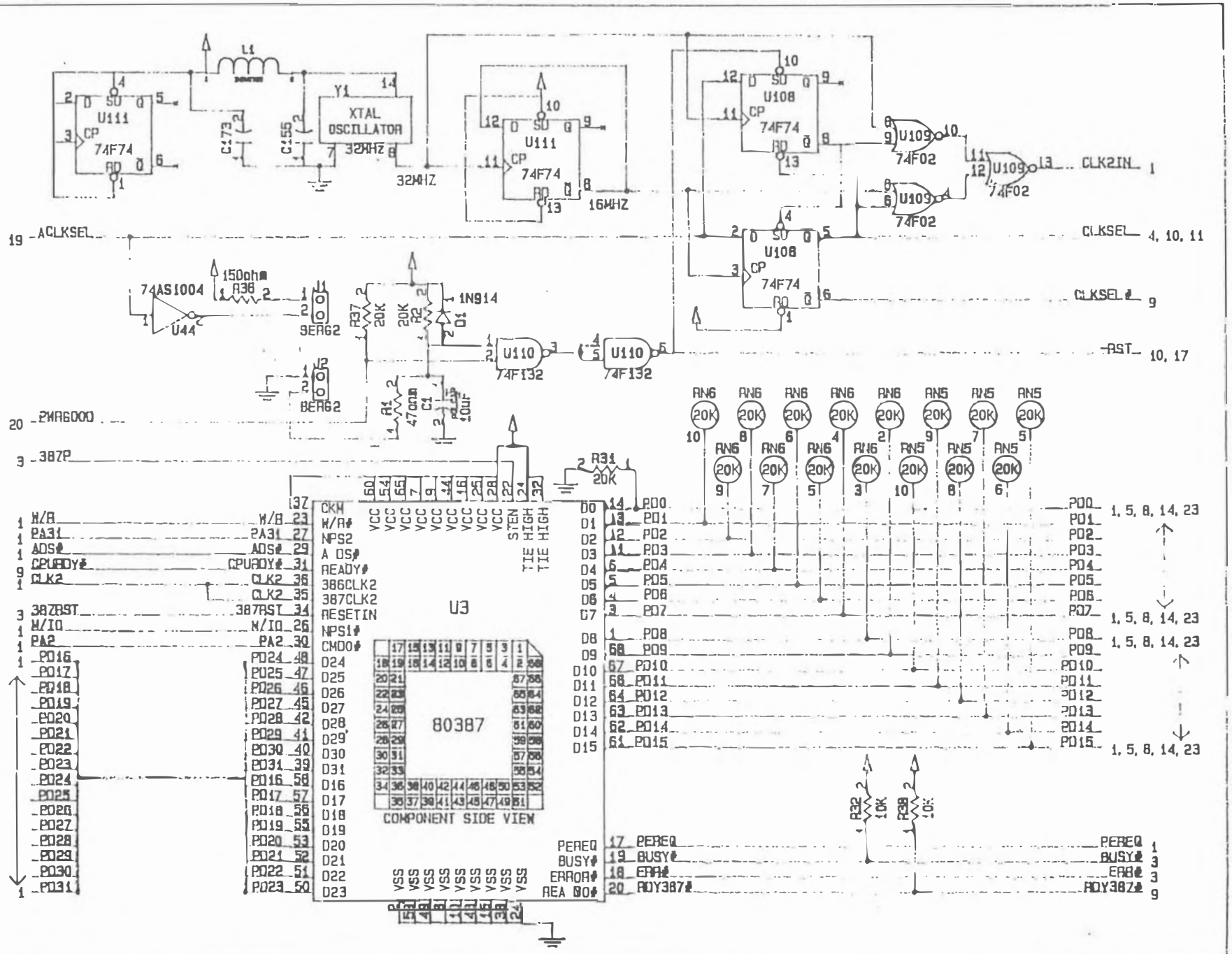

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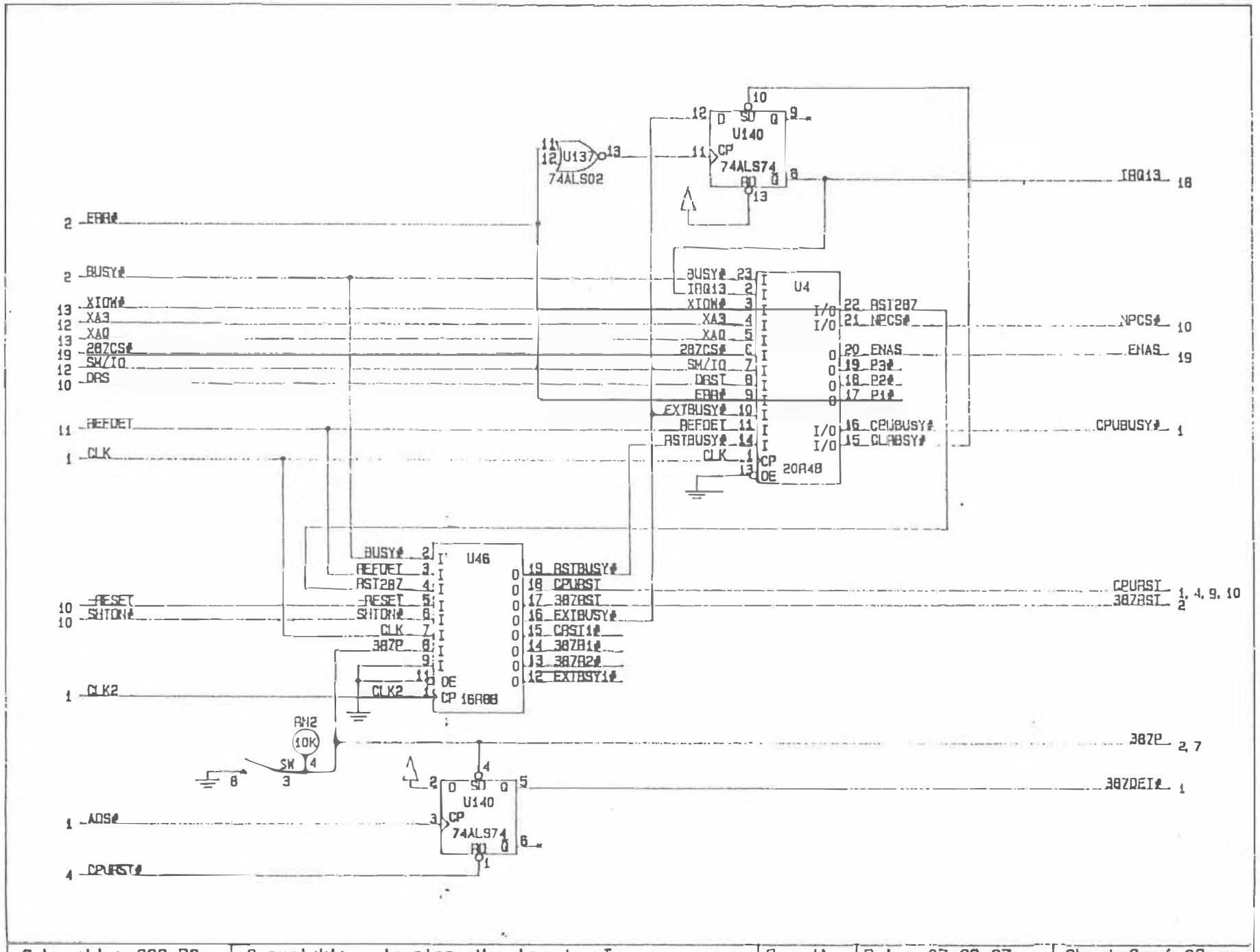

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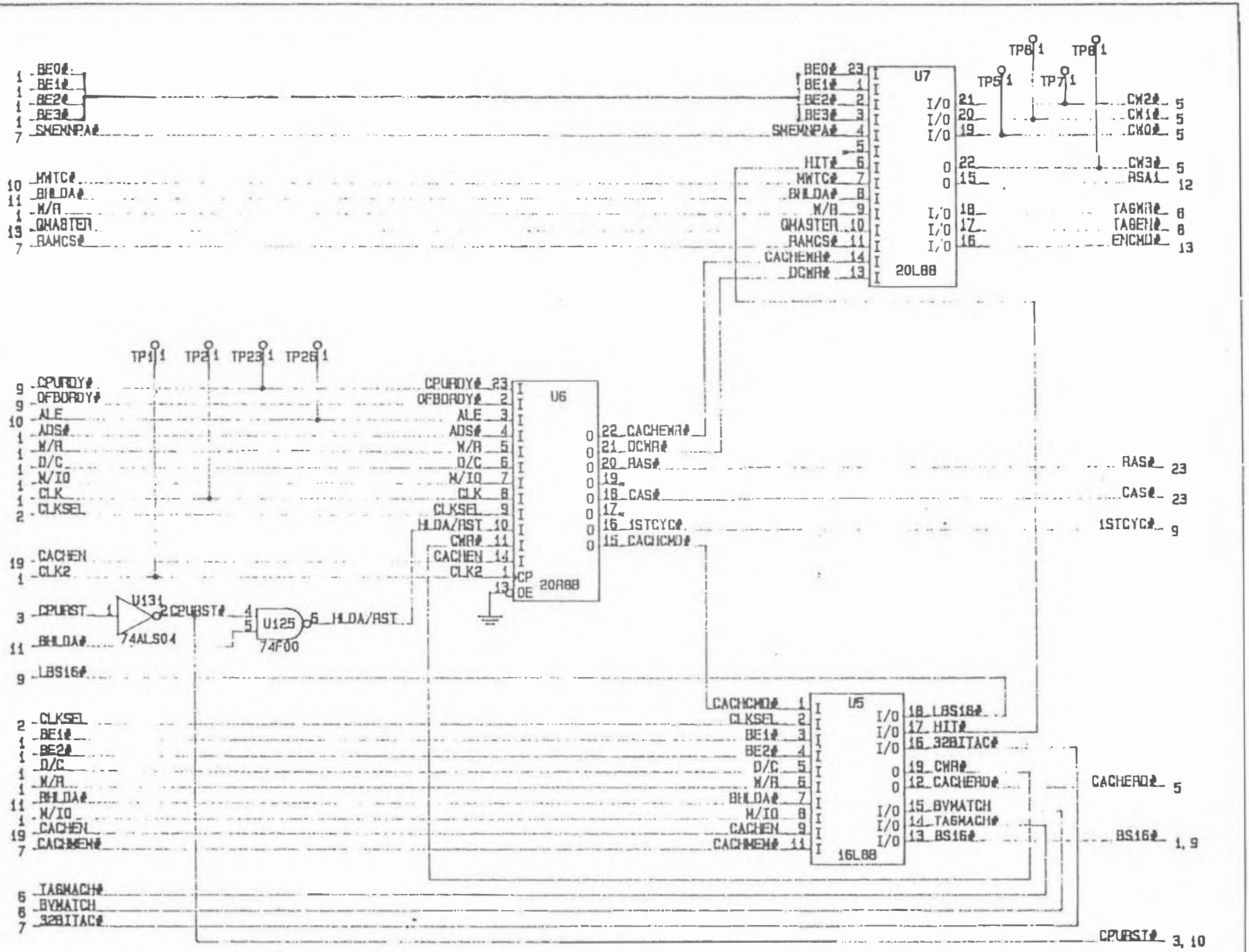

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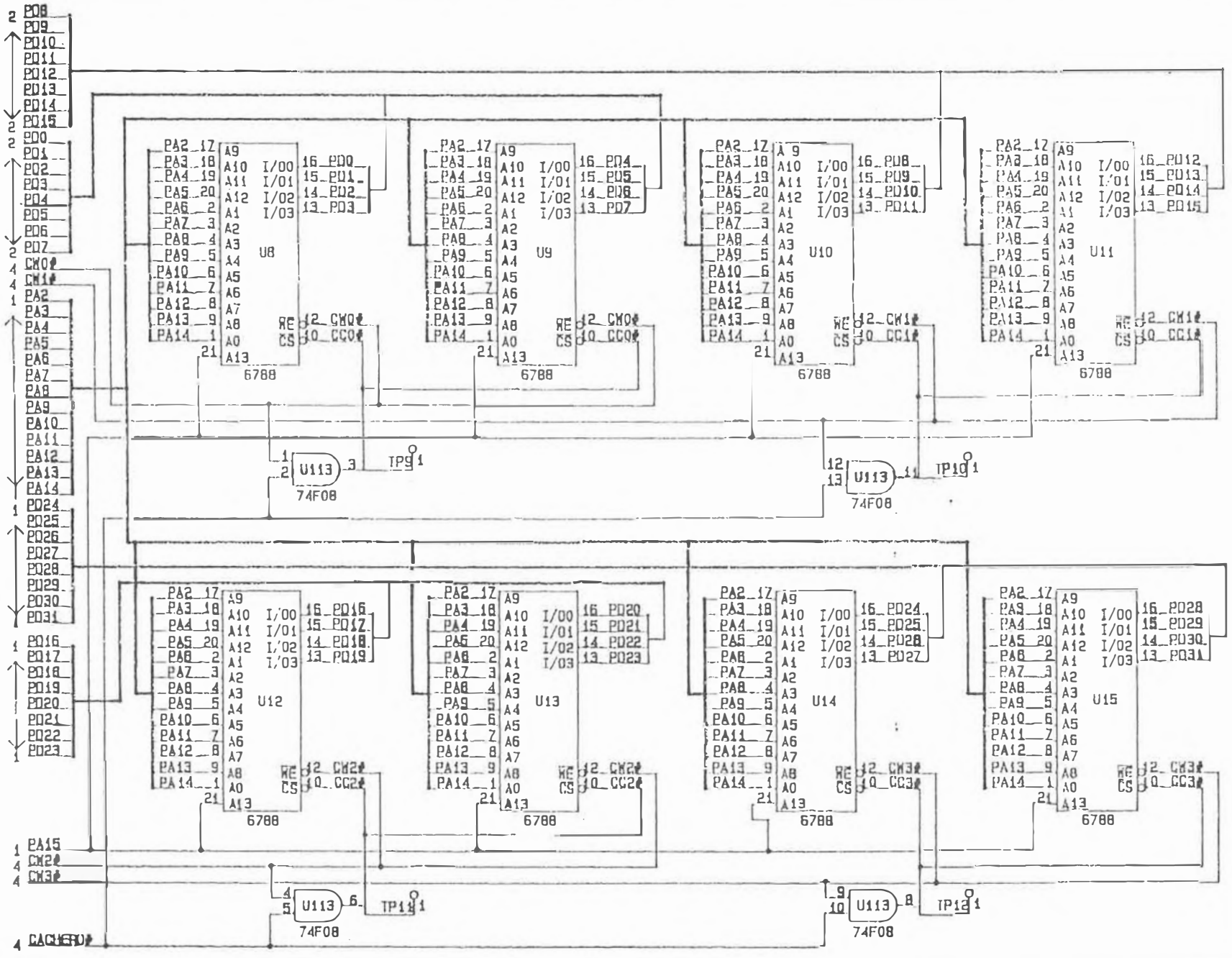

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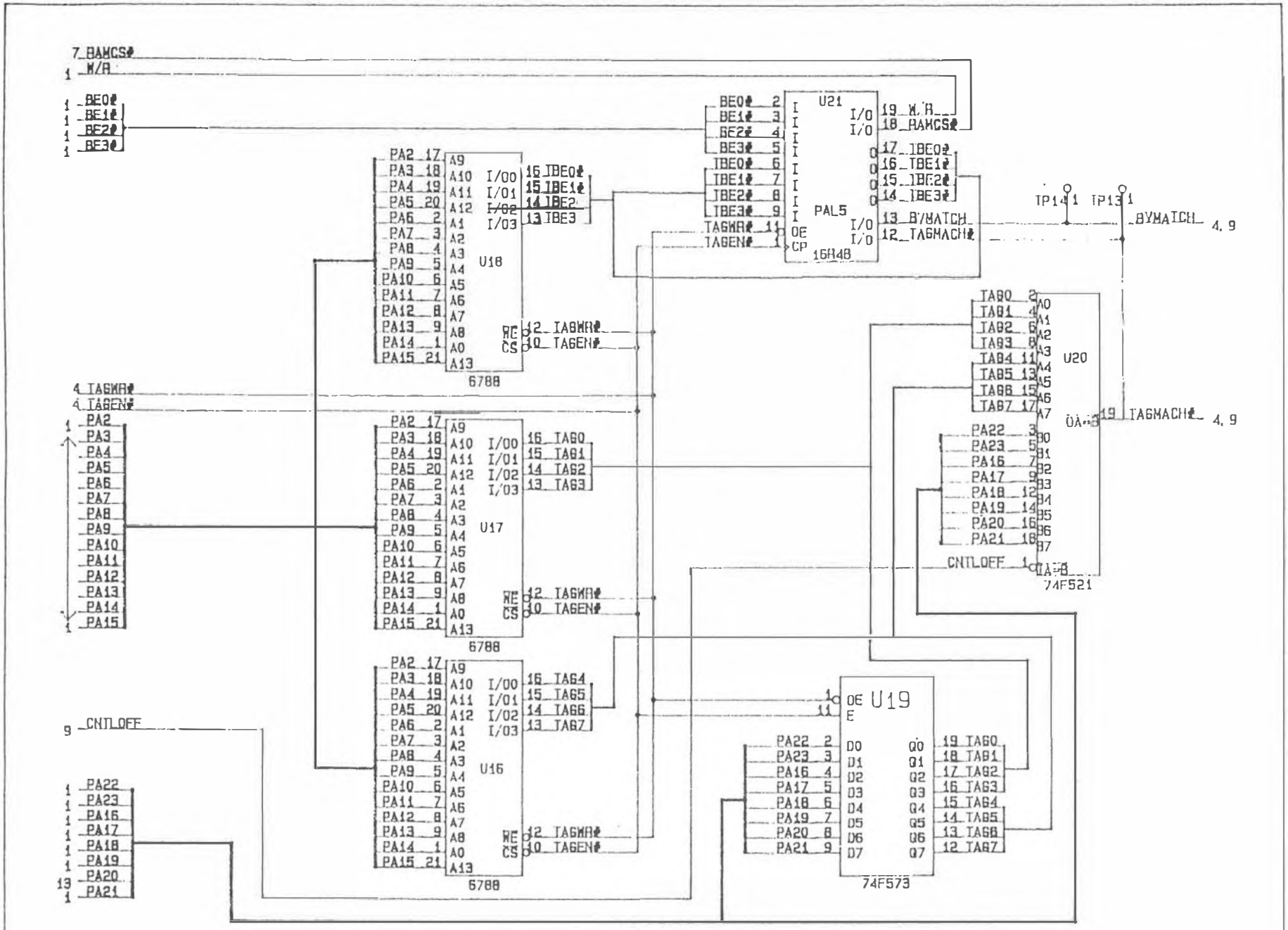

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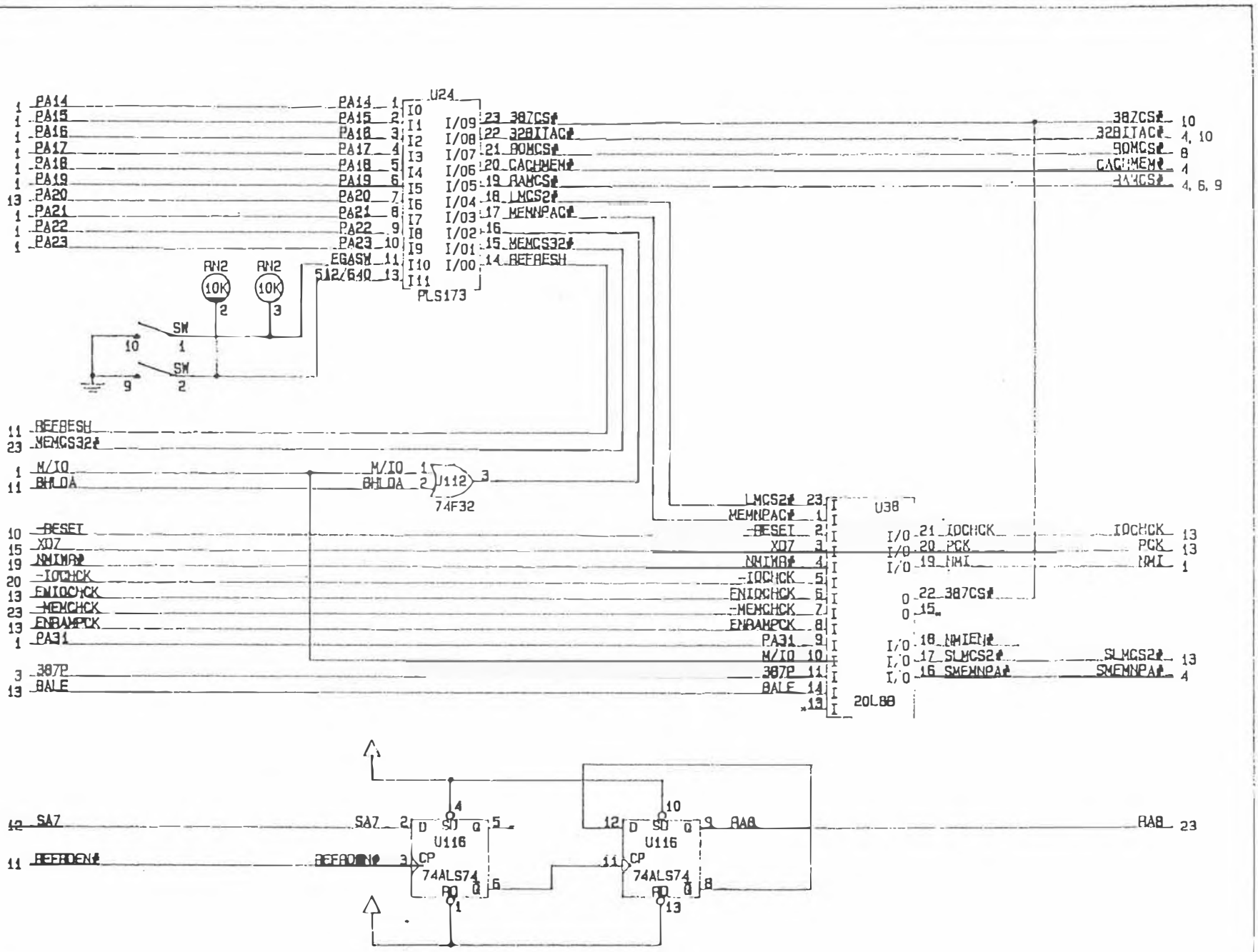
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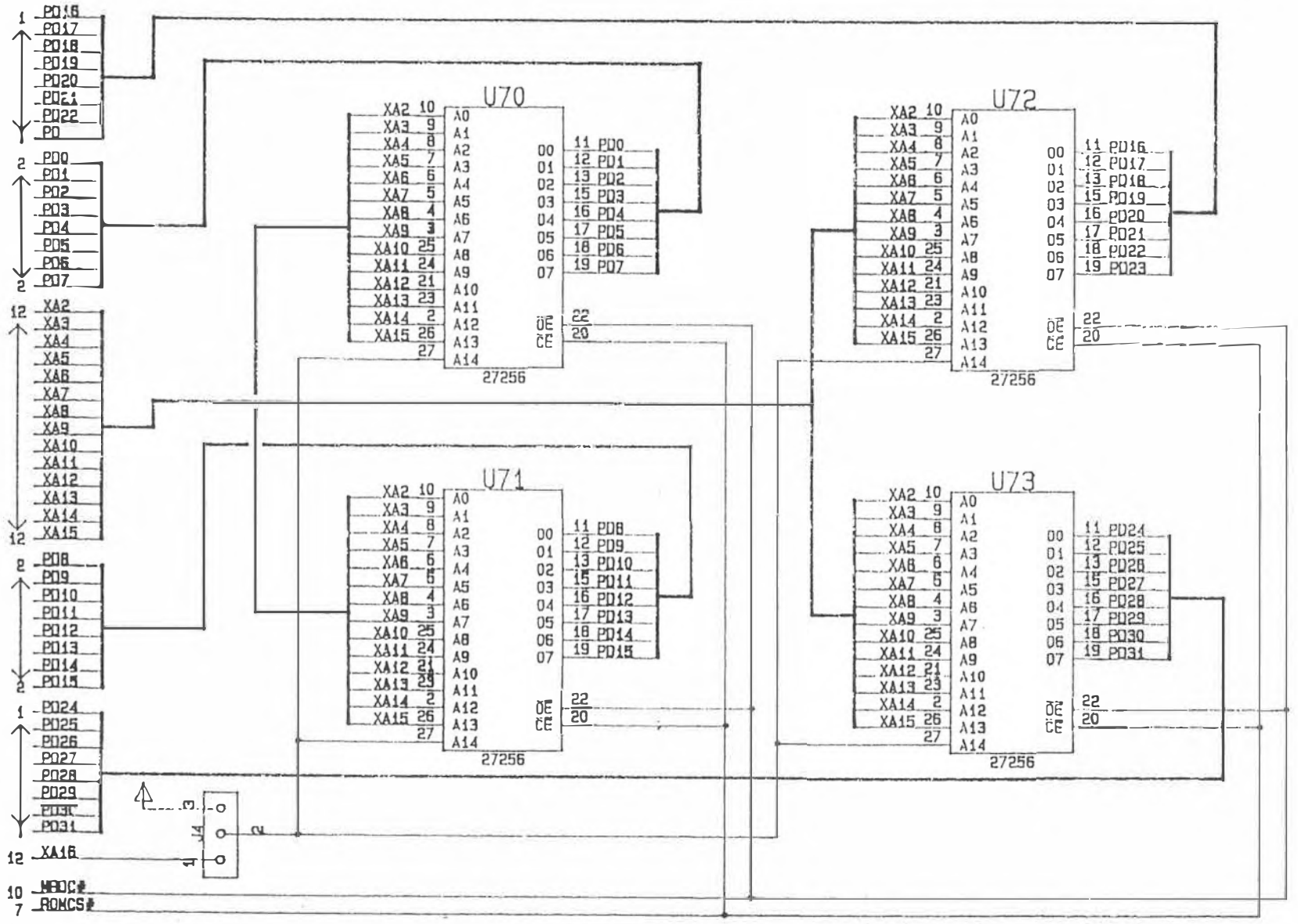
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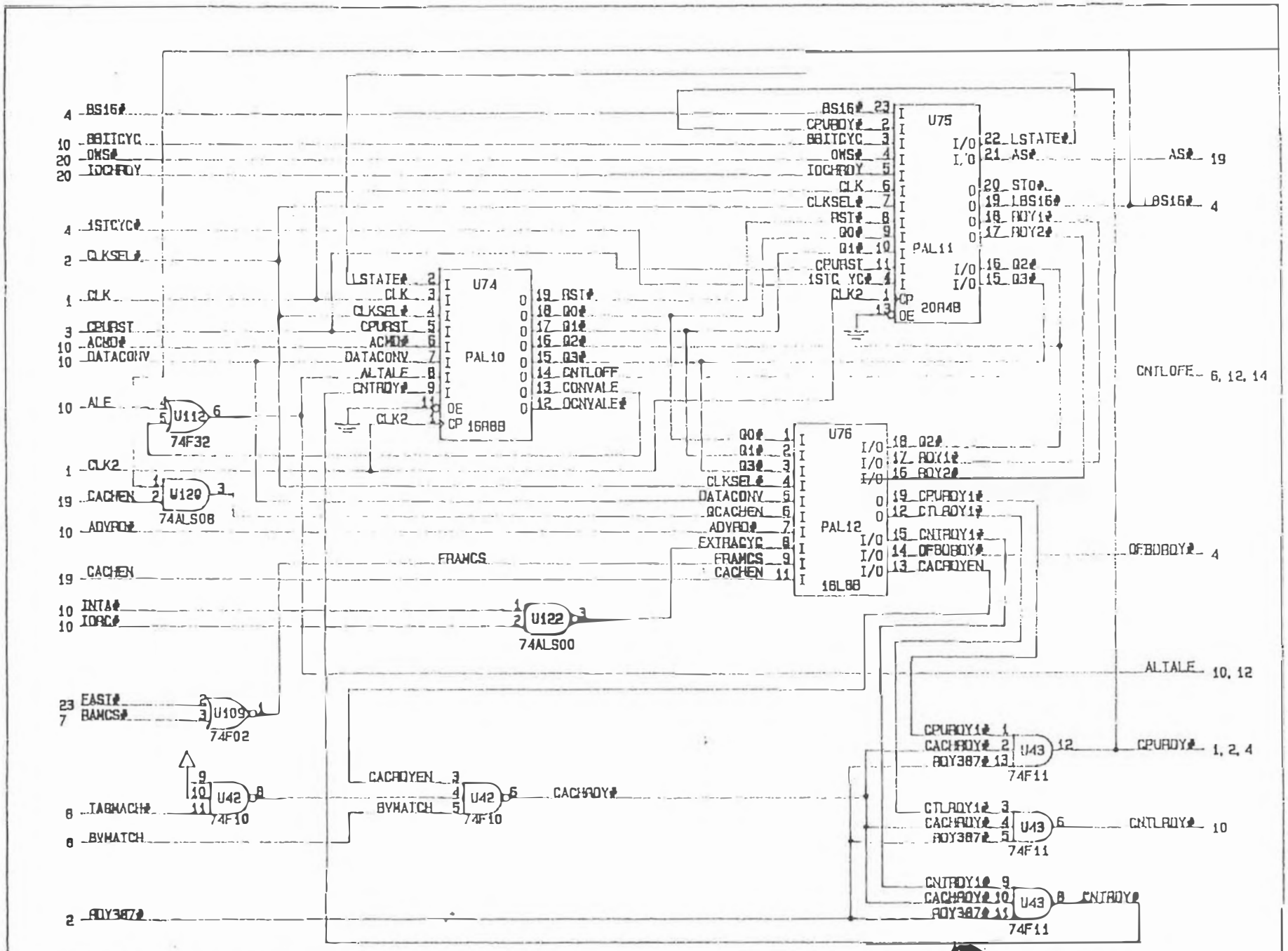

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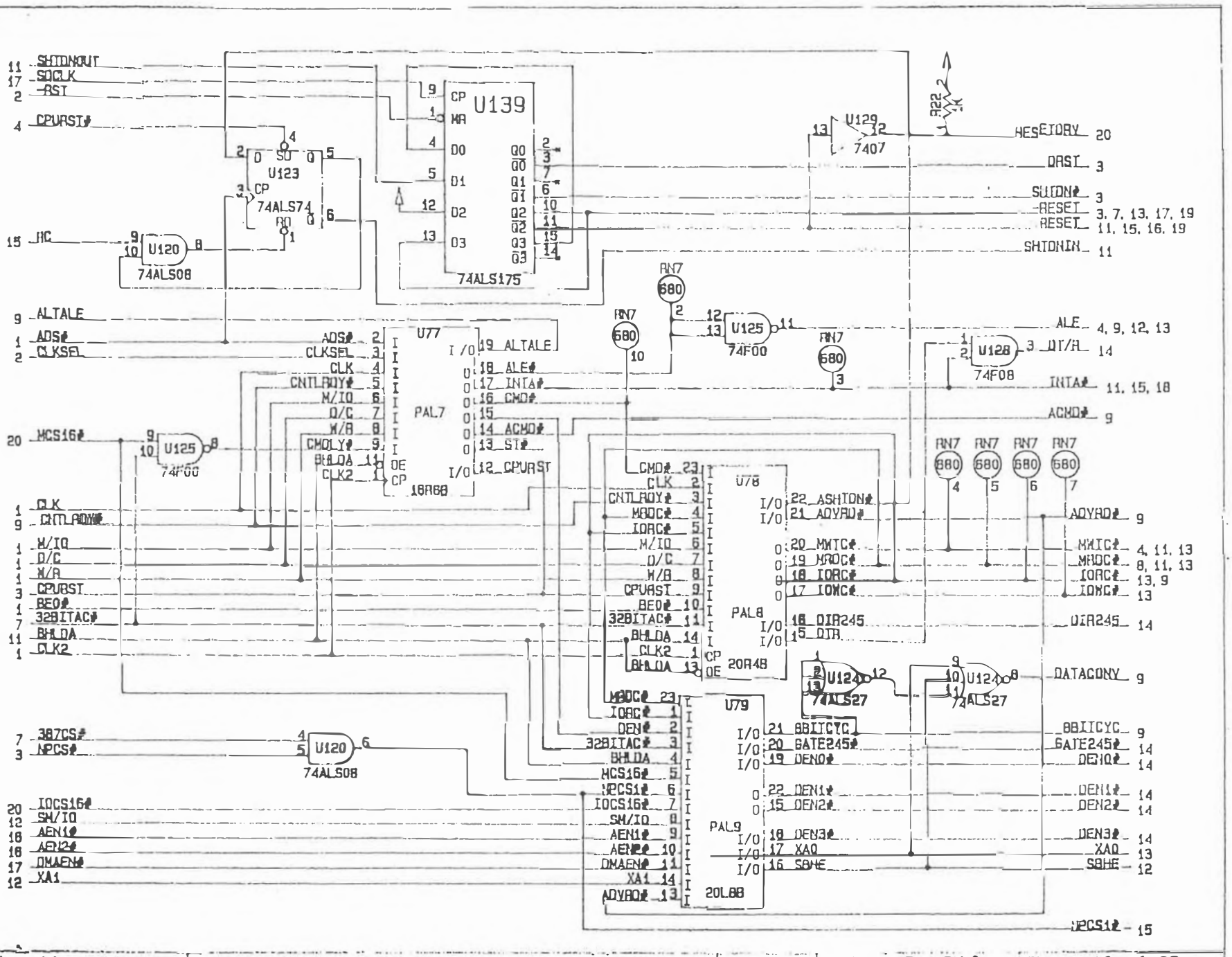
08-14-87



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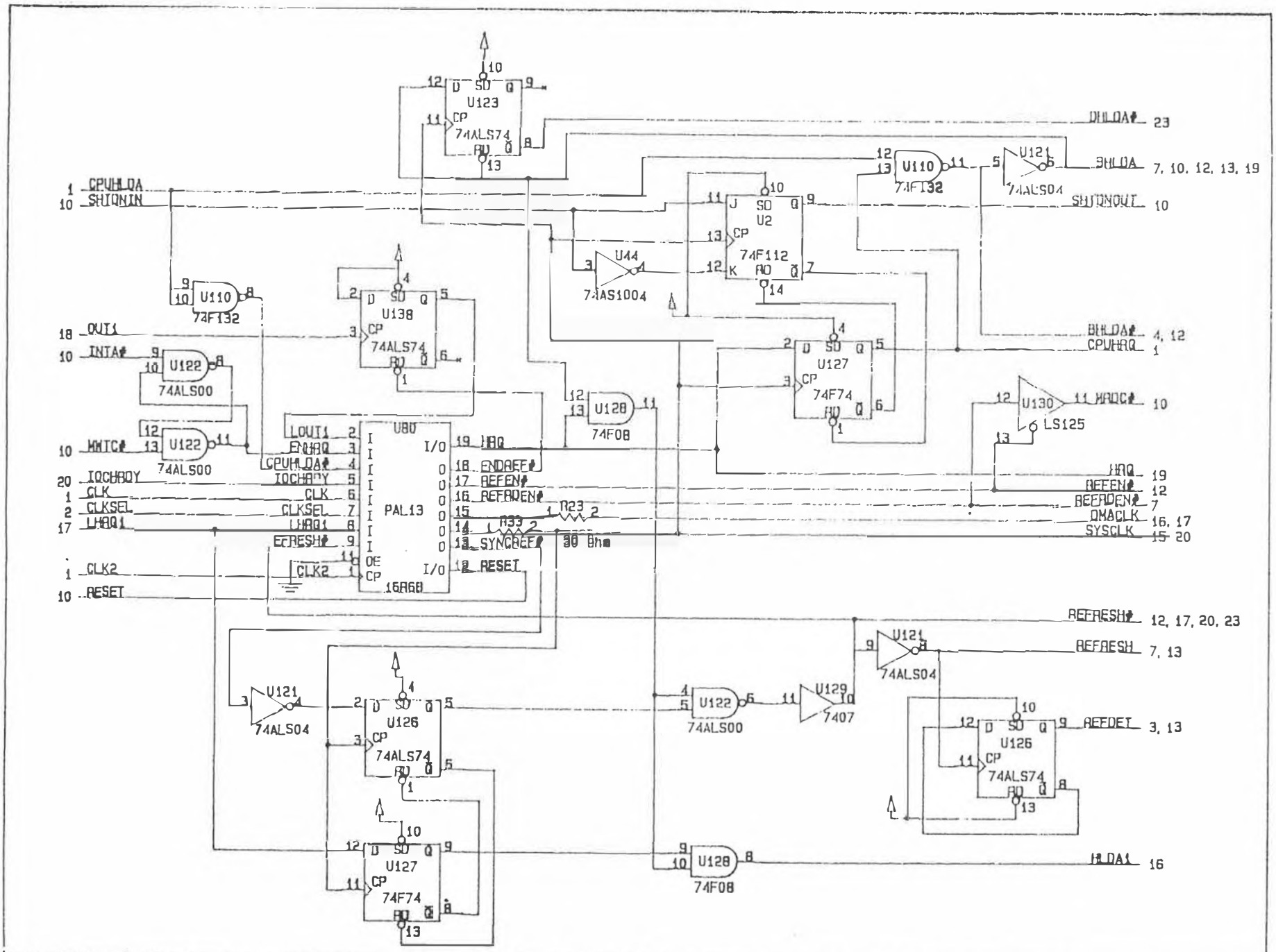
08-14-87



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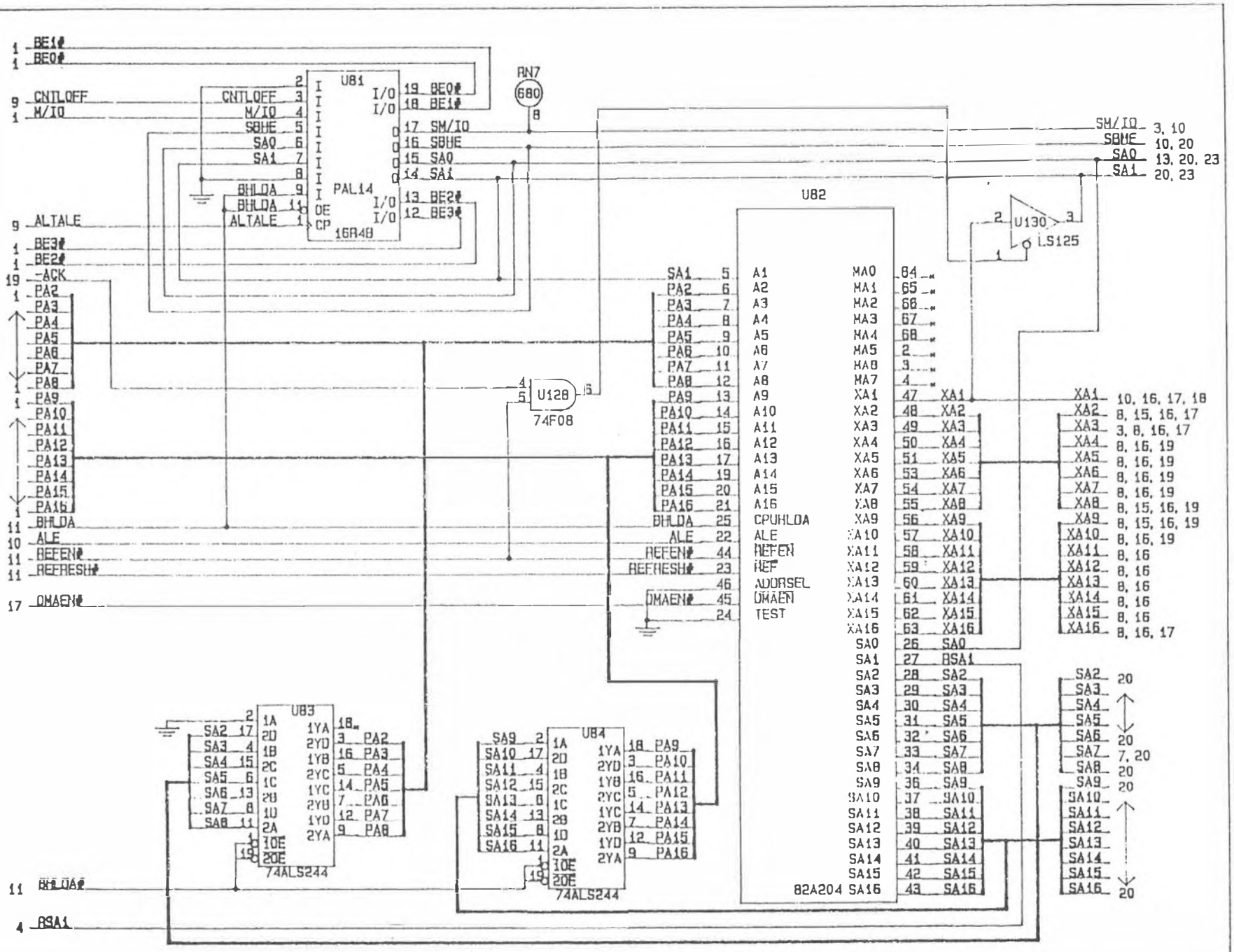

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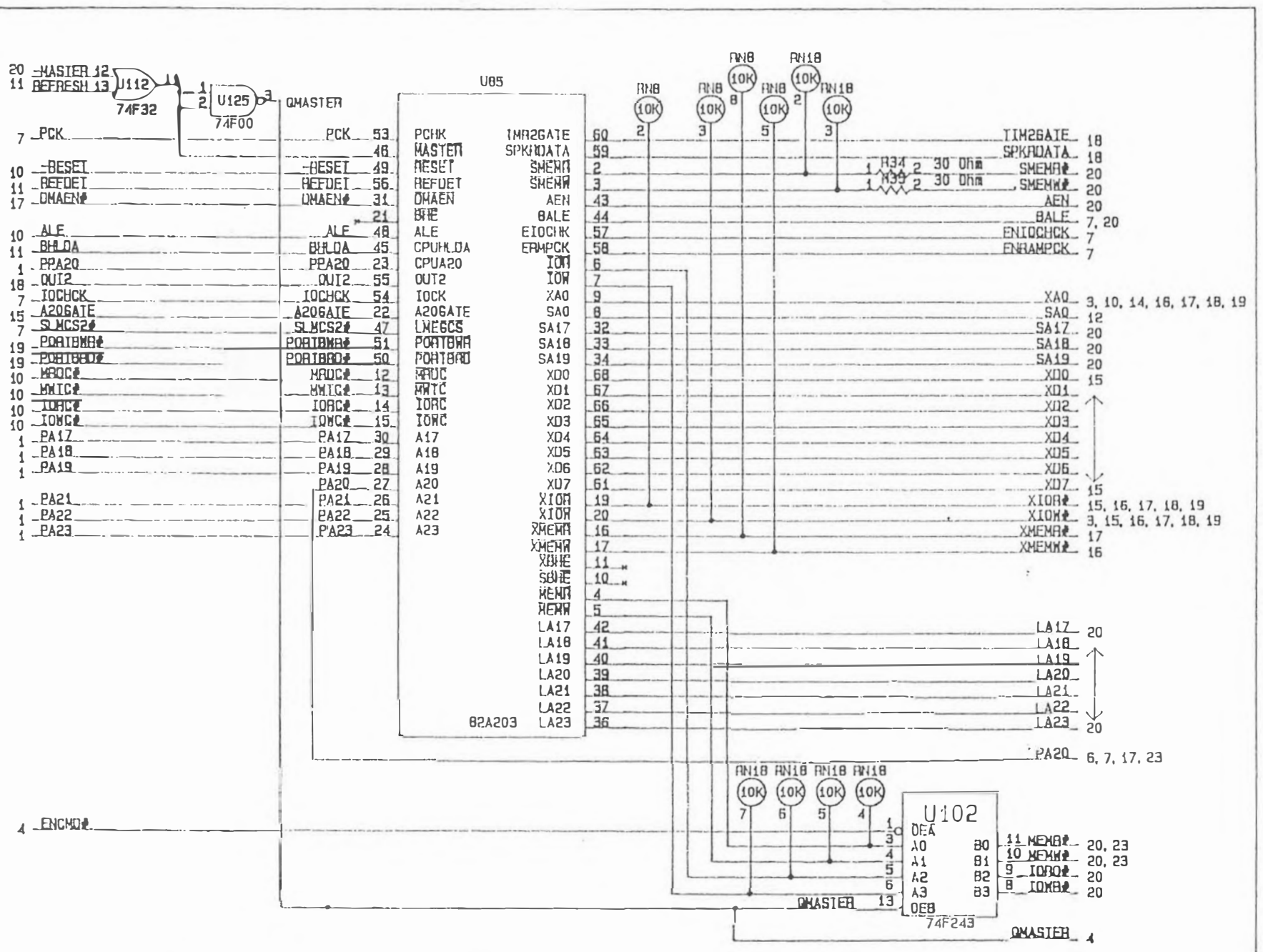

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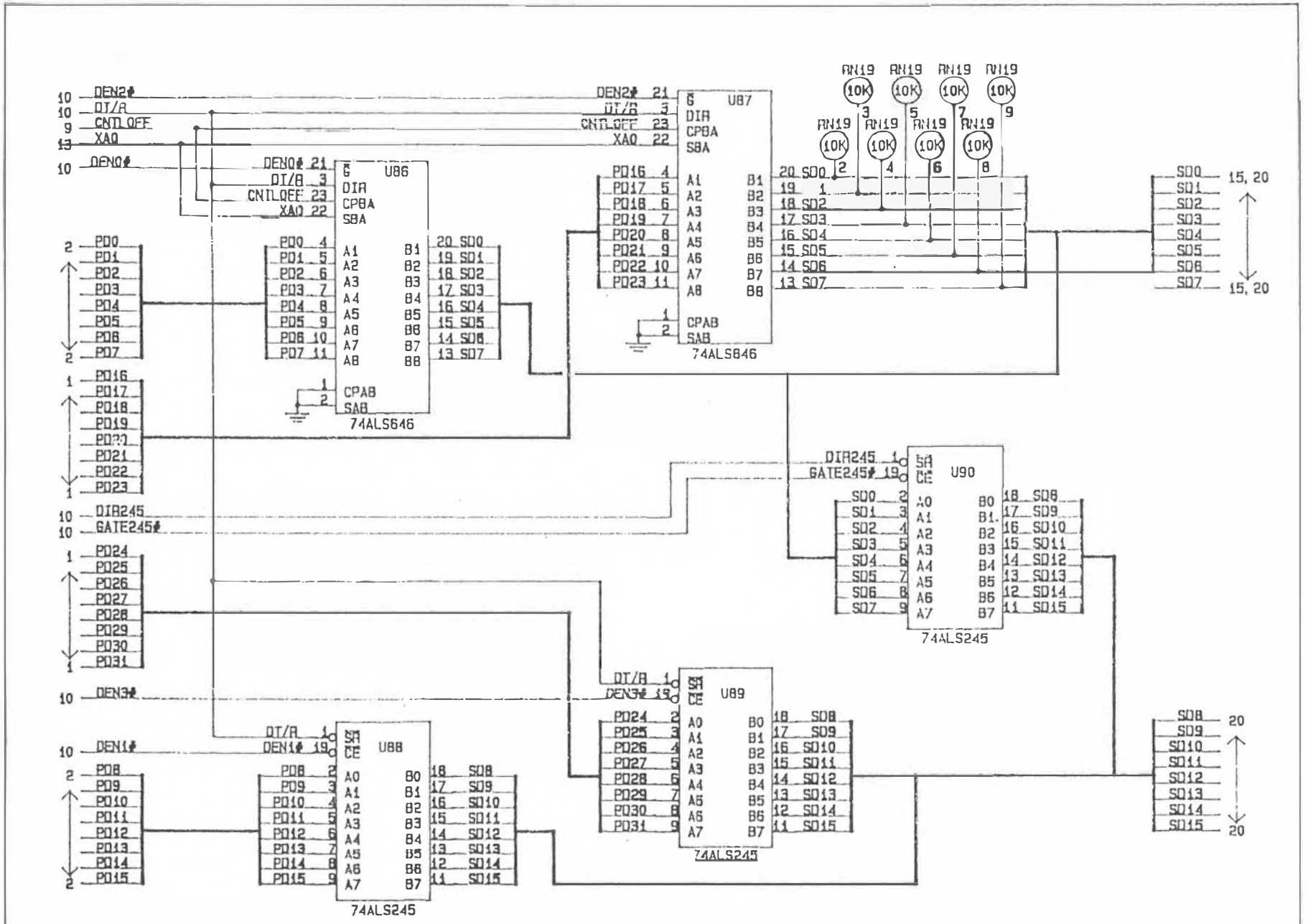

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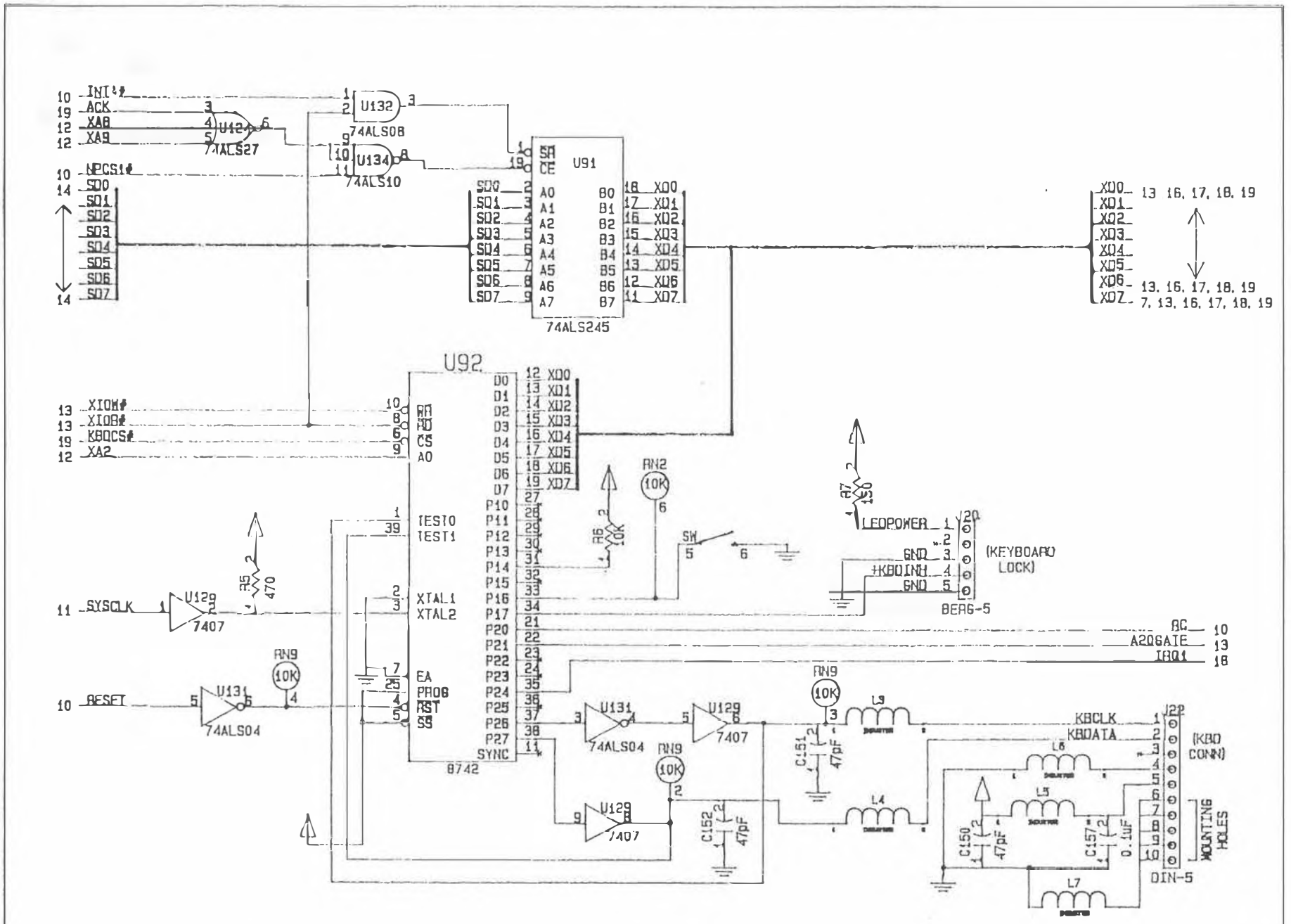

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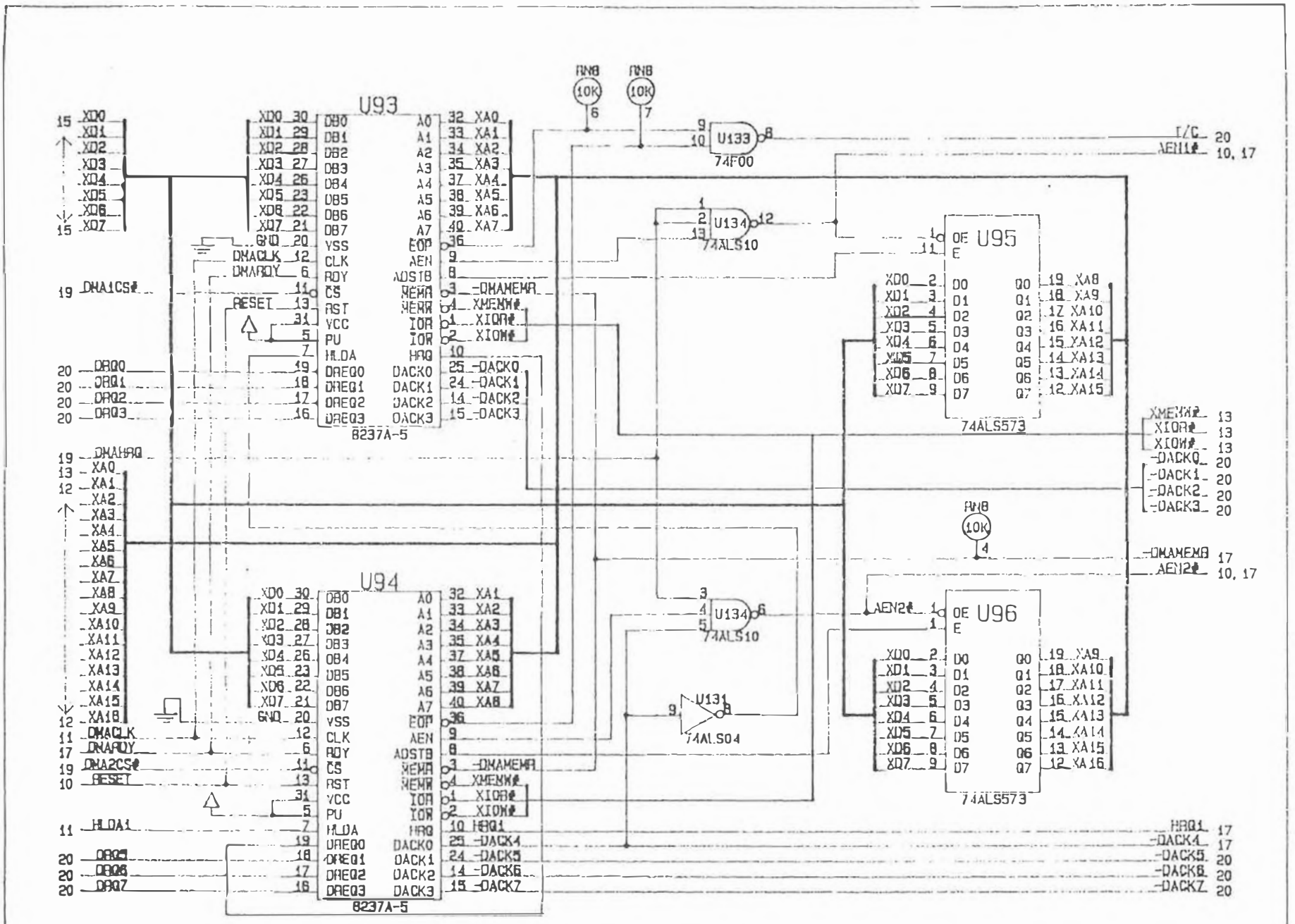

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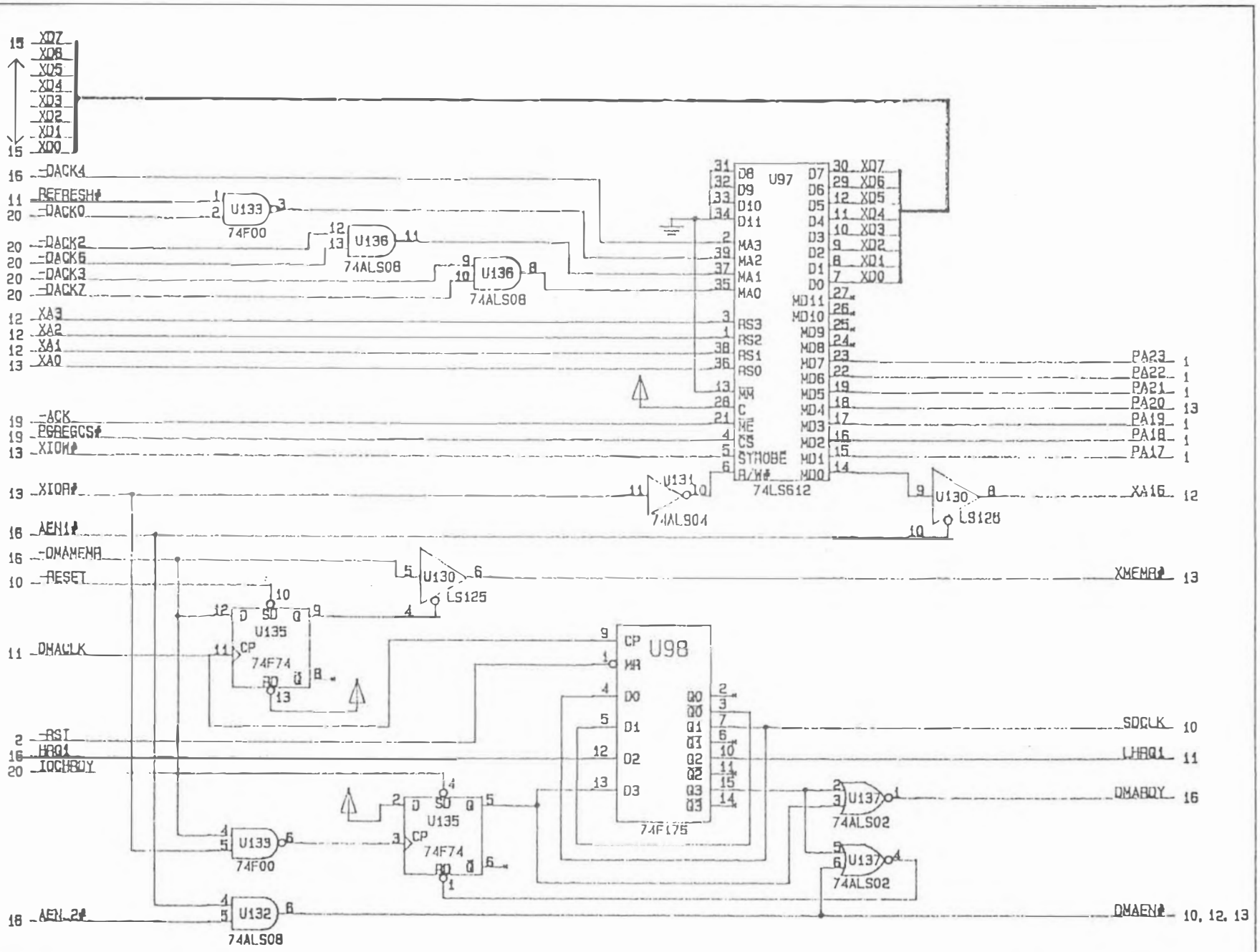
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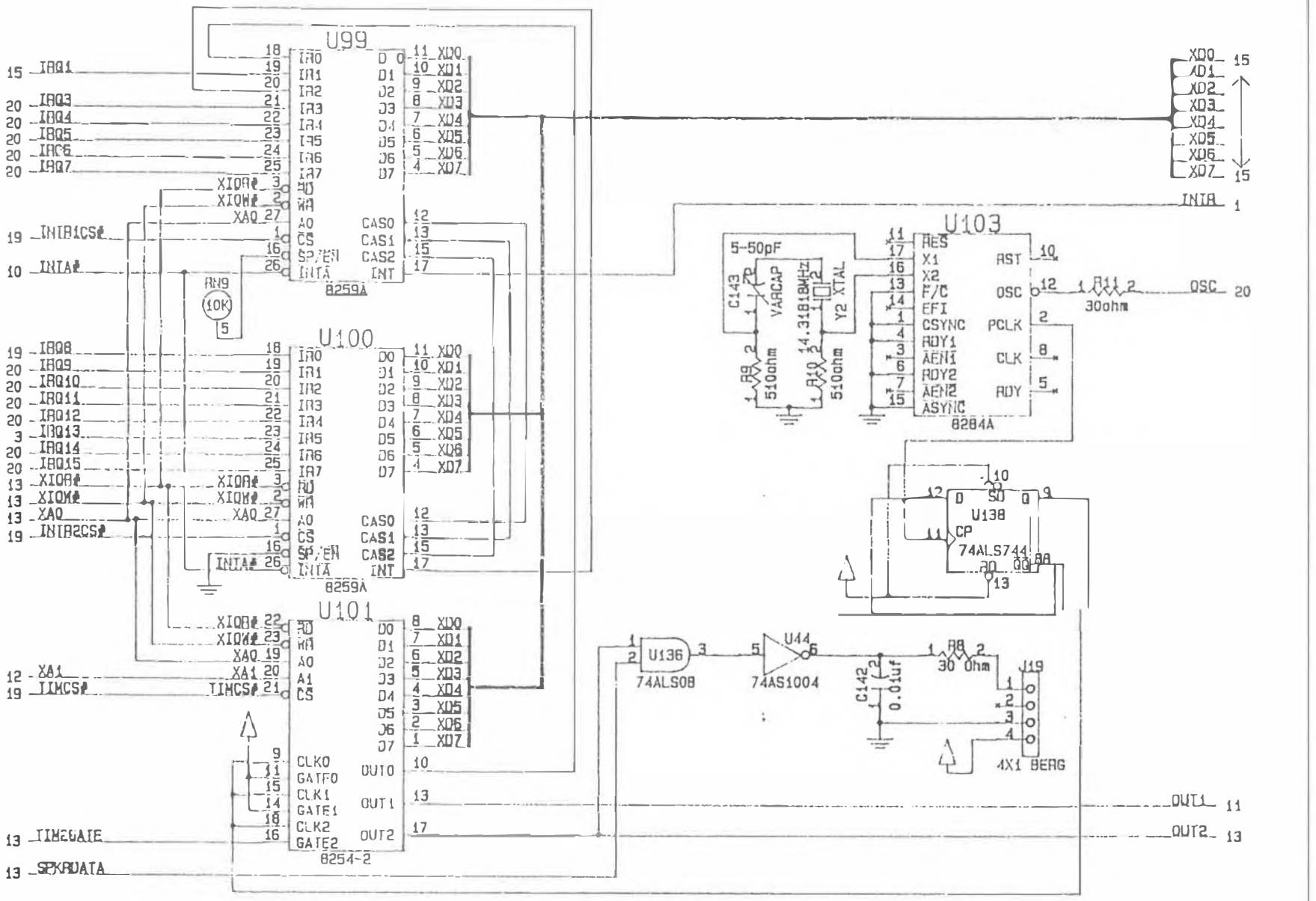

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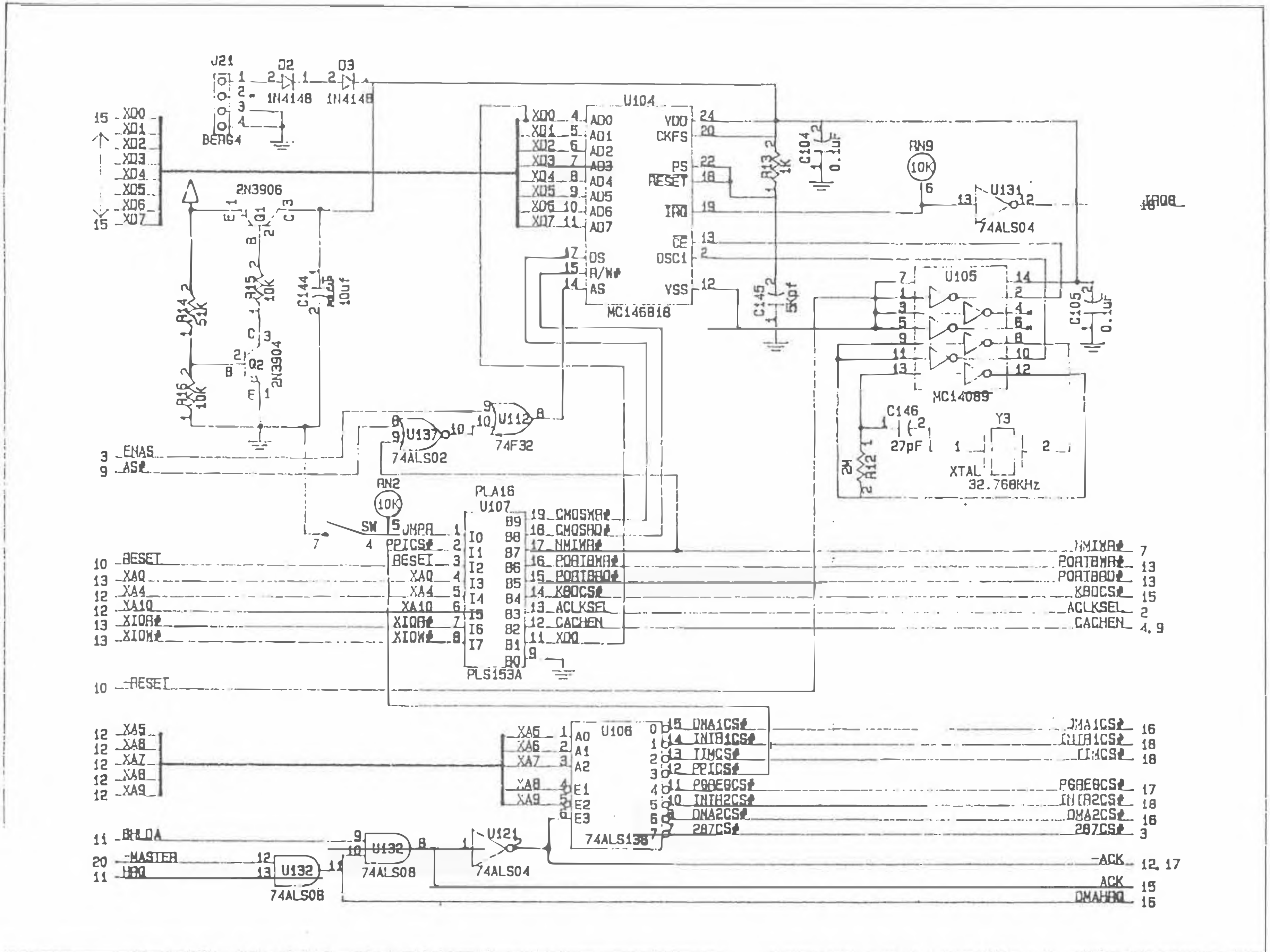

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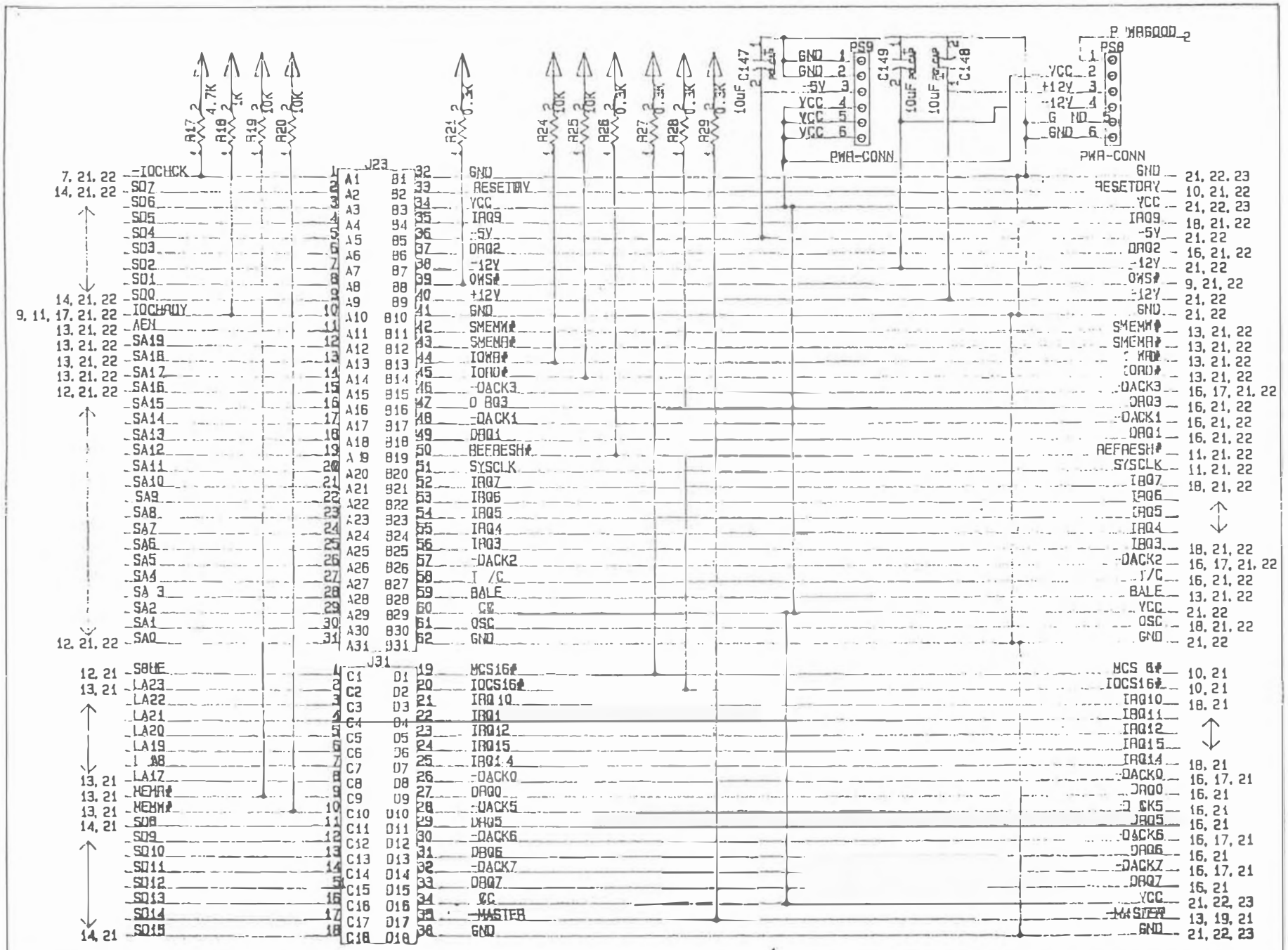

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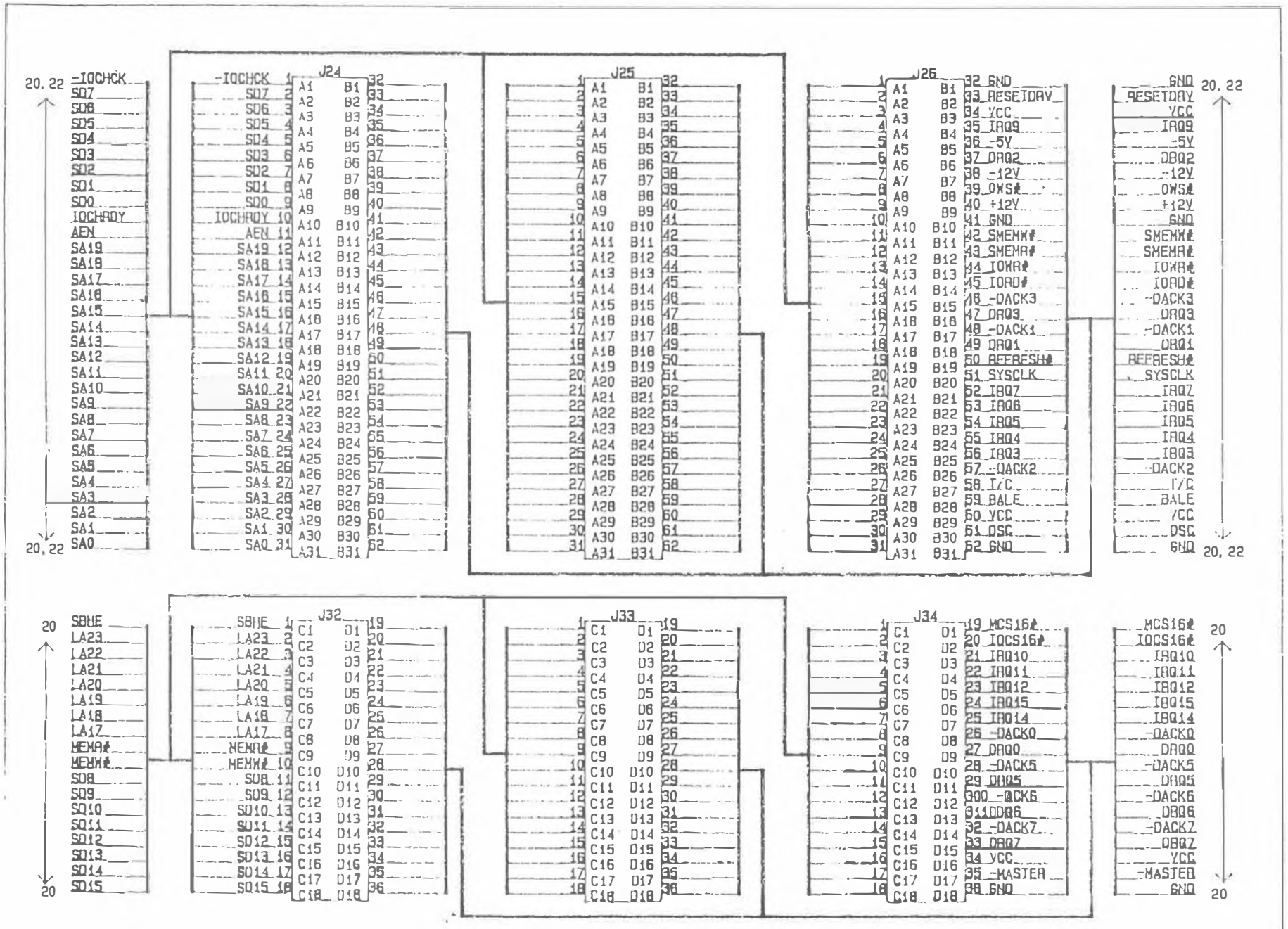

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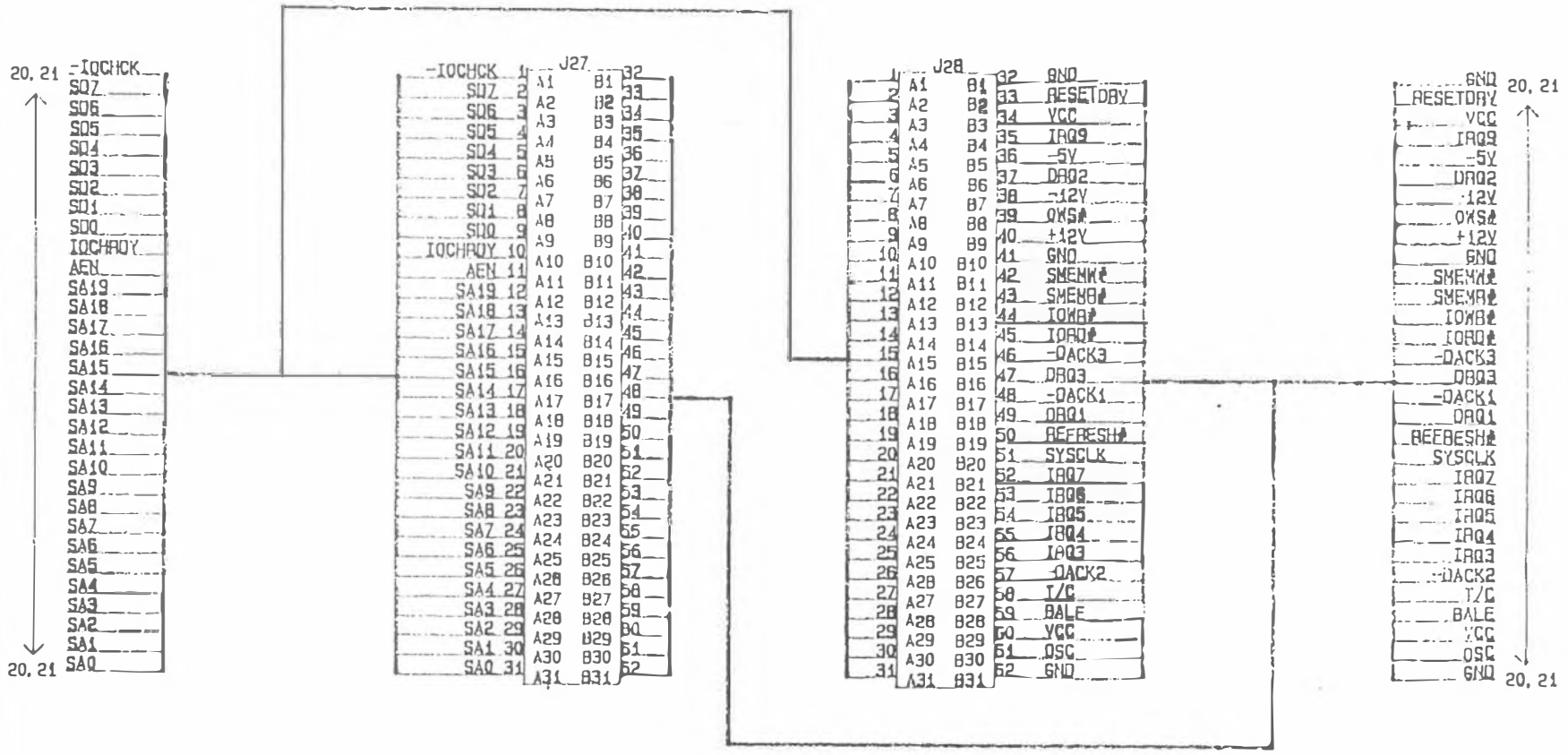
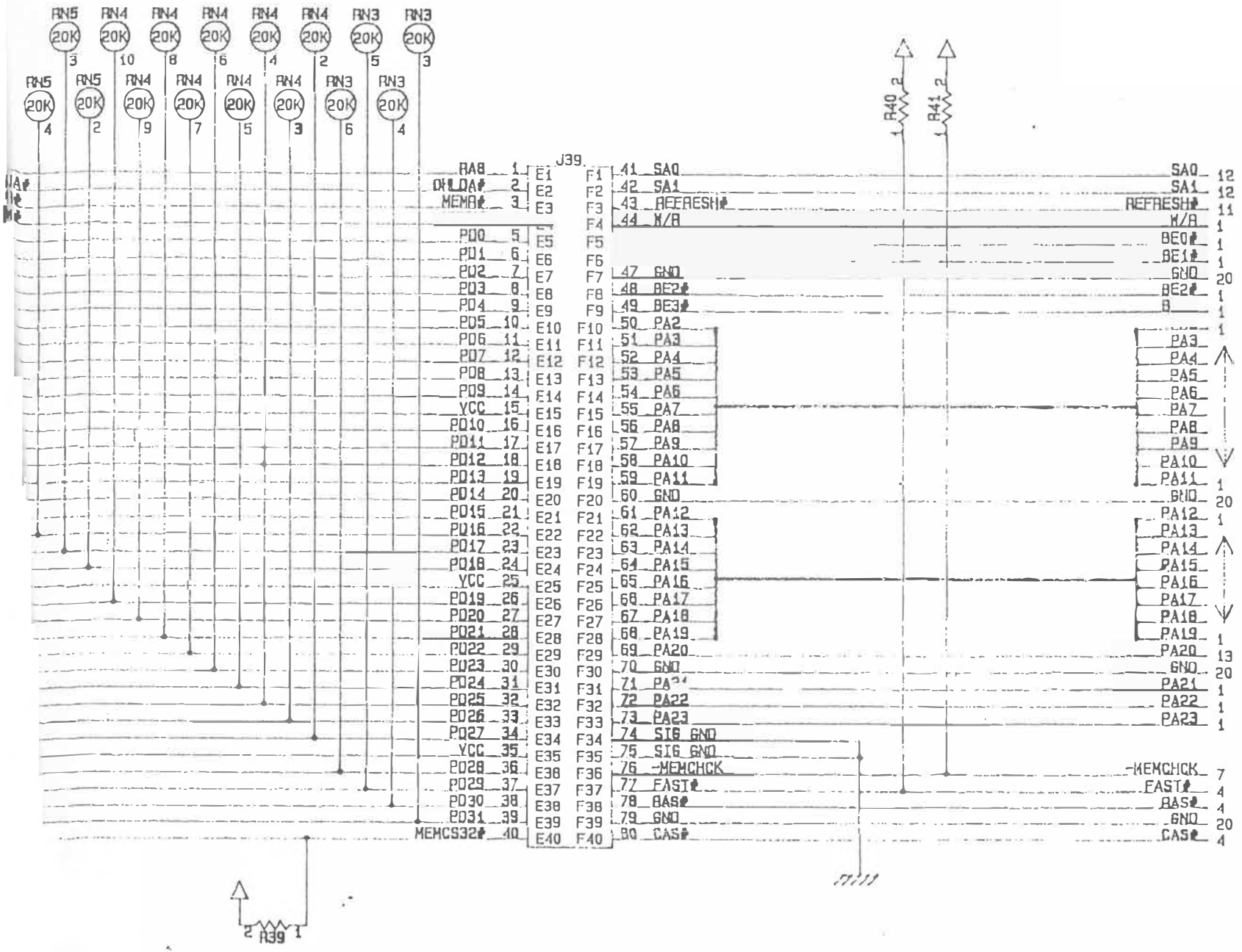

20, 21
-IOCHCK
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
IOCHRDY
AEN
SA19
SA18
SA17
SA16
SA15
SA14
SA13
SA12
SA11
SA10
SA9
SA8
SA7
SA6
SA5
SA4
SA3
SA2
SA1
SA0
20, 21
J27
J28
GND
RESETDRV
VCC
IRQ9
-5V
DRQ2
-12V
OWS#
+12V
GND
SMEMW#
SMEMR#
IOW#
IOR#
-DACK3
DRQ3
-DACK1
DRQ1
REFRESH#
SYSCLK
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
-DACK2
T/C
BALE
VCC
OSC
GND
20, 21


RN5 20K 3
RN4 20K 10
RN4 20K 8
RN4 20K 6
RN4 20K 4
RN4 20K 2
RN3 20K 5
RN3 20K 3
RN5 20K 4
RN5 20K 2
RN4 20K 9
RN4 20K 7
RN4 20K 5
RN4 20K 3
RN3 20K 6
RN3 20K 4
R40 2 1
R41 2 1
R39 2 1
J39
BA8 1 E1 F1 41 SA0 SA0 12
DRQDA# 2 E2 F2 42 SA1 SA1 12
MEMR# 3 E3 F3 43 REFRESH# REFRESH# 11
E4 F4 44 M/B M/B 1
PD0 5 E5 F5 BE0# 1
PD1 6 E6 F6 BE1# 1
PD2 7 E7 F7 47 GND GND 20
PD3 8 E8 F8 48 BE2# BE2# 1
PD4 9 E9 F9 49 BE3# B 1
PD5 10 E10 F10 50 PA2 1
PD6 11 E11 F11 51 PA3 PA3
PD7 12 E12 F12 52 PA4 PA4
PD8 13 E13 F13 53 PA5 PA5
PD9 14 E14 F14 54 PA6 PA6
VCC 15 E15 F15 55 PA7 PA7
PD10 16 E16 F16 56 PA8 PA8
PD11 17 E17 F17 57 PA9 PA9
PD12 18 E18 F18 58 PA10 PA10
PD13 19 E19 F19 59 PA11 PA11 1
PD14 20 E20 F20 60 GND GND 20
PD15 21 E21 F21 61 PA12 PA12 1
PD16 22 E22 F22 62 PA13 PA13
PD17 23 E23 F23 63 PA14 PA14
PD18 24 E24 F24 64 PA15 PA15
VCC 25 E25 F25 65 PA16 PA16
PD19 26 E26 F26 66 PA17 PA17
PD20 27 E27 F27 67 PA18 PA18
PD21 28 E28 F28 68 PA19 PA19 1
PD22 29 E29 F29 69 PA20 PA20 13
PD23 30 E30 F30 70 GND GND 20
PD24 31 E31 F31 71 PA21 PA21 1
PD25 32 E32 F32 72 PA22 PA22 1
PD26 33 E33 F33 73 PA23 PA23 1
PD27 34 E34 F34 74 SIG GND
VCC 35 E35 F35 75 SIG GND
PD28 36 E36 F36 76 -MEMCHCK -MEMCHCK 7
PD29 37 E37 F37 77 FAST# FAST# 4
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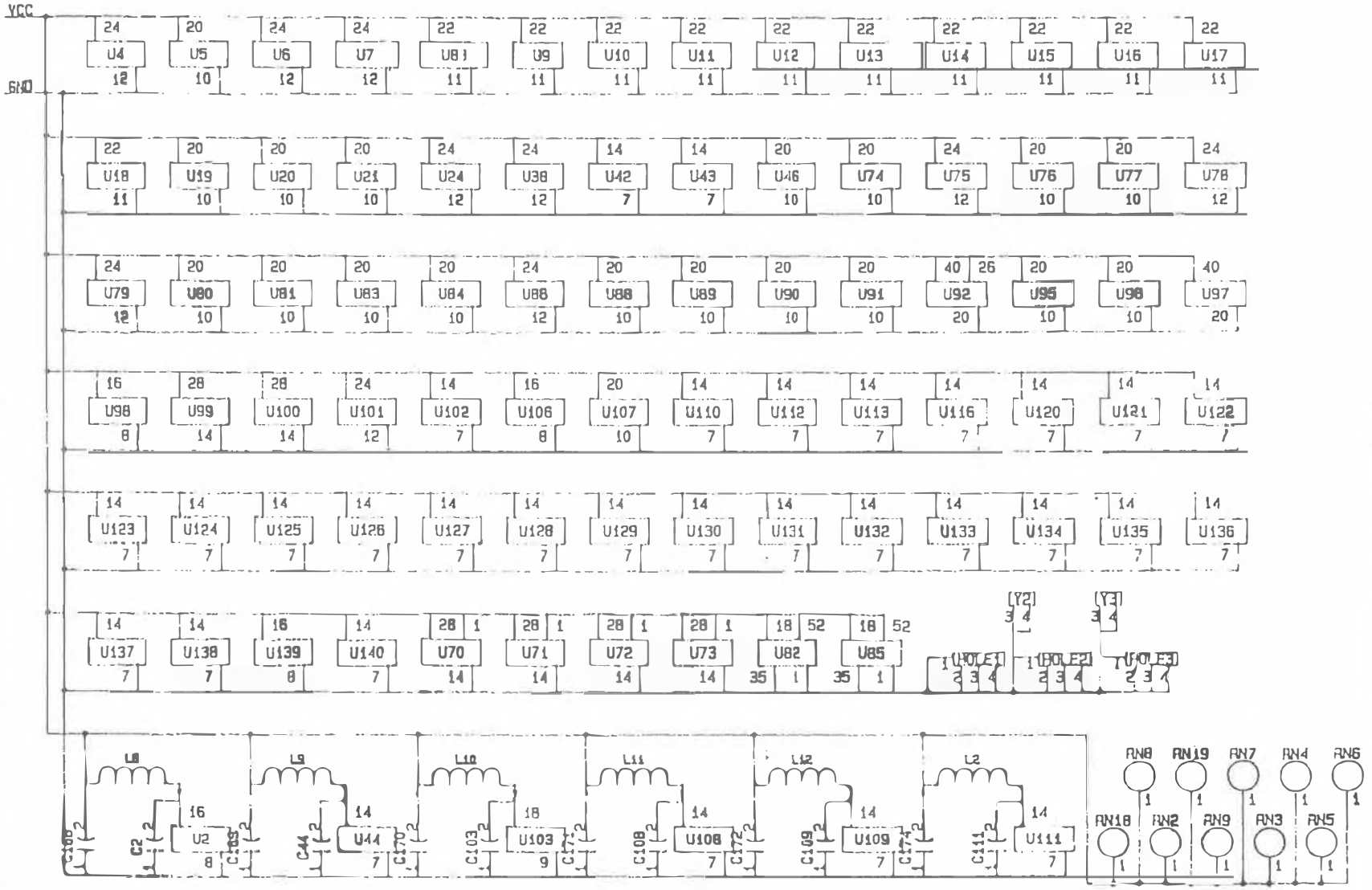
MEMCS32# 40 E40 F40 80 CAS# CAS# 4

08-14-87



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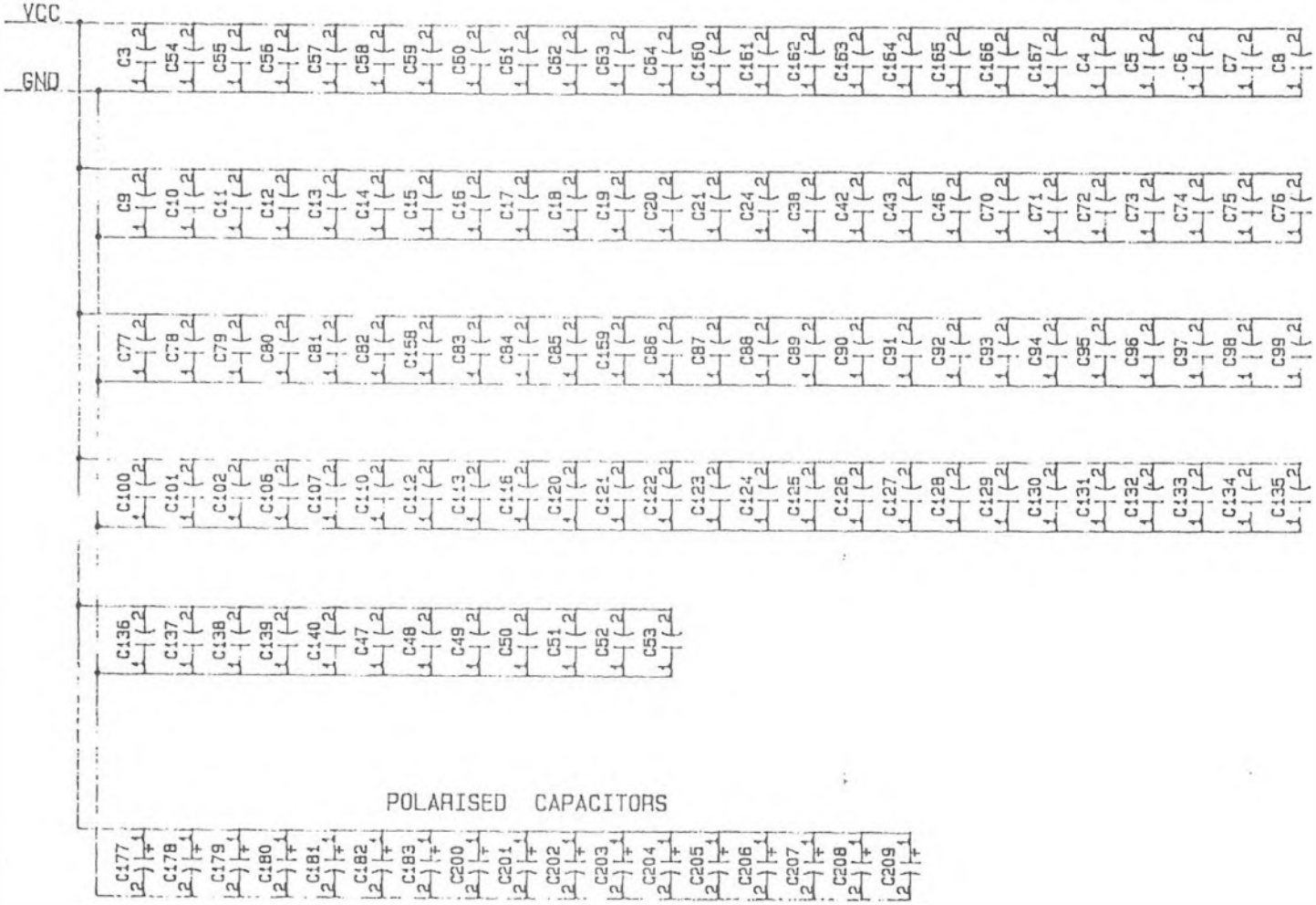
VCC
GND
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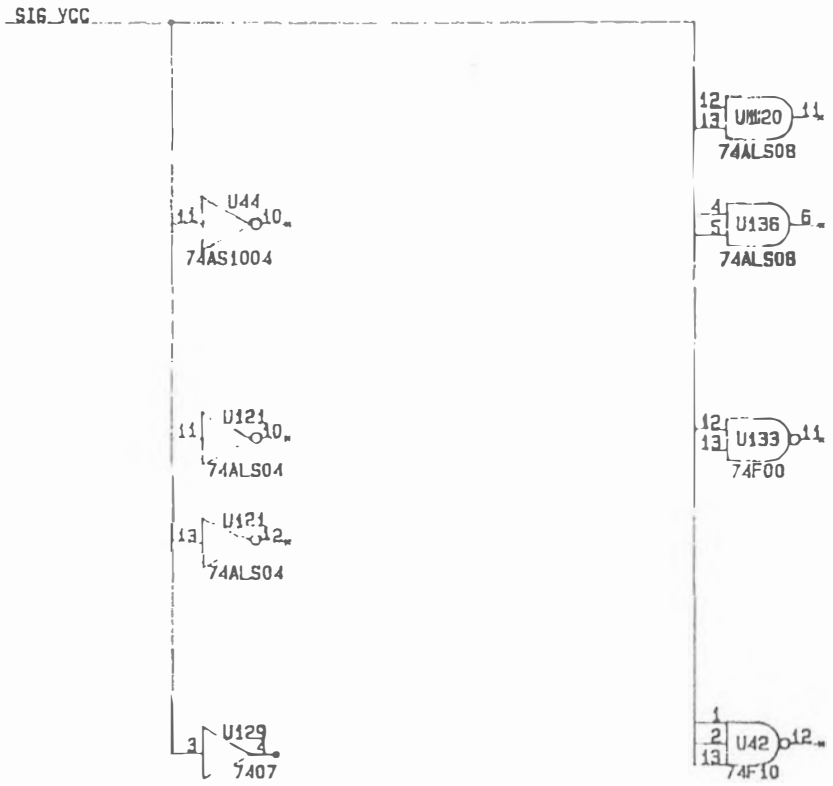
C77 C78 C79 C80 C81 C82 C158 C83 C84 C85 C159 C86 C87 C88 C89 C90 C91 C92 C93 C94 C95 C96 C97 C98 C99
C100 C101 C102 C106 C107 C110 C112 C113 C116 C120 C121 C122 C123 C124 C125 C126 C127 C128 C129 C130 C131 C132 C133 C134 C135
C136 C137 C138 C139 C140 C47 C48 C49 C50 C51 C52 C53
POLARISED CAPACITORS
C177 C178 C179 C180 C181 C182 C183 C200 C201 C202 C203 C204 C205 C206 C207 C208 C209


SI6_VCC
U44
74AS1004
U121
74ALS04
U121
74ALS04
U129
7407
U120
74ALS08
U136
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U133
74F00
U42
74F10