PC-482VN series

Embedded STPC ATLAS 5x86DX2-133 PC/104 CPU Module with on-board VGA/LAN/CF/TFT LCD interface and General Purpose I/O channels

Edition: 1.02

Printed July. 2003

http:/www.inlog.com.tw

Table of contents

Chapter 1
Hardware installation

1.1 Introductions

The PC-482VN is a full-function PC/104 CPU Module which integrates the VGA/TFT LCD panel, CompactFlash,GPIO,Ethernet(PC-482VN Only) and other enhanced I/O interfaces on a PC/104 CPU Module. This Module uses an embedded SGS-THOMSON STPC ATLAS Pentium performance x86-133 low power CPU and embedded 32MB SDRAM on board

The PC-482VN offers power management to minimize power consumption. It complies with the "Green Function" standard and supports three power saving features: doze, sleep, and suspended mode.

Its high performance VGA display supports both CRT and TFT LCD displays with a Display Memory UMA architecture, share system memory up to 4MB and a resolution of up to 1024x768(CRT).

The PC-486V also offers several industrial features such as a 255-level watchdog timer with jumperless setup, supports M-systems DiskOnChip Flash Disk,CompactFlash Slot,GPIO and PC/104 connection for additional functions with PC/104 modules.

1.2 Packing list

- One PC-482VN PC/104 CPU Module
- One Quick Installation Guide
- One CD-ROM for manual (in PDF format), drivers and utility
- One 2mm to 2.54mm IDE flat cable, 44-pin to 40-pin
- One 2mm to 2.54mm FDD cable (34-pin)
- One 2mm to 2.54mm parallel port adapter (26-pin) kit
- One 2mm to 2.54mm serial port(COM1) adapter (10-pin) kit
- One 2mm to 2.54mm 1 to 3 serial port(COM2,3,4) adapter (10-pin) kit
- One Ethernet RJ-45 connector Conversion (For PC-482VN only)
- .One USE cable for two USB port
- One 6-pin DIN to two 6 pin mini-DIN for keyboard,PS/2 Mouse adapter

1.3 Specifications

- **System Chipset :**

  The STPC ATLAS chipset integrates a fully static 5x86-133MHz low power processor, fully compatible with standard x86 processors, and combine it with powerful chipset, graphics and video pipelines to provide a single consumer oriented PC compatible subsystem. The performance of this device is comparable with the performance of a typical P5 generation system.

  The STPC ATLAS includes a powerful x86 processor core along with a 64-bit DRAM controller, advanced 64-bit accelerated graphics and video controller, a high speed PCI chip set functions

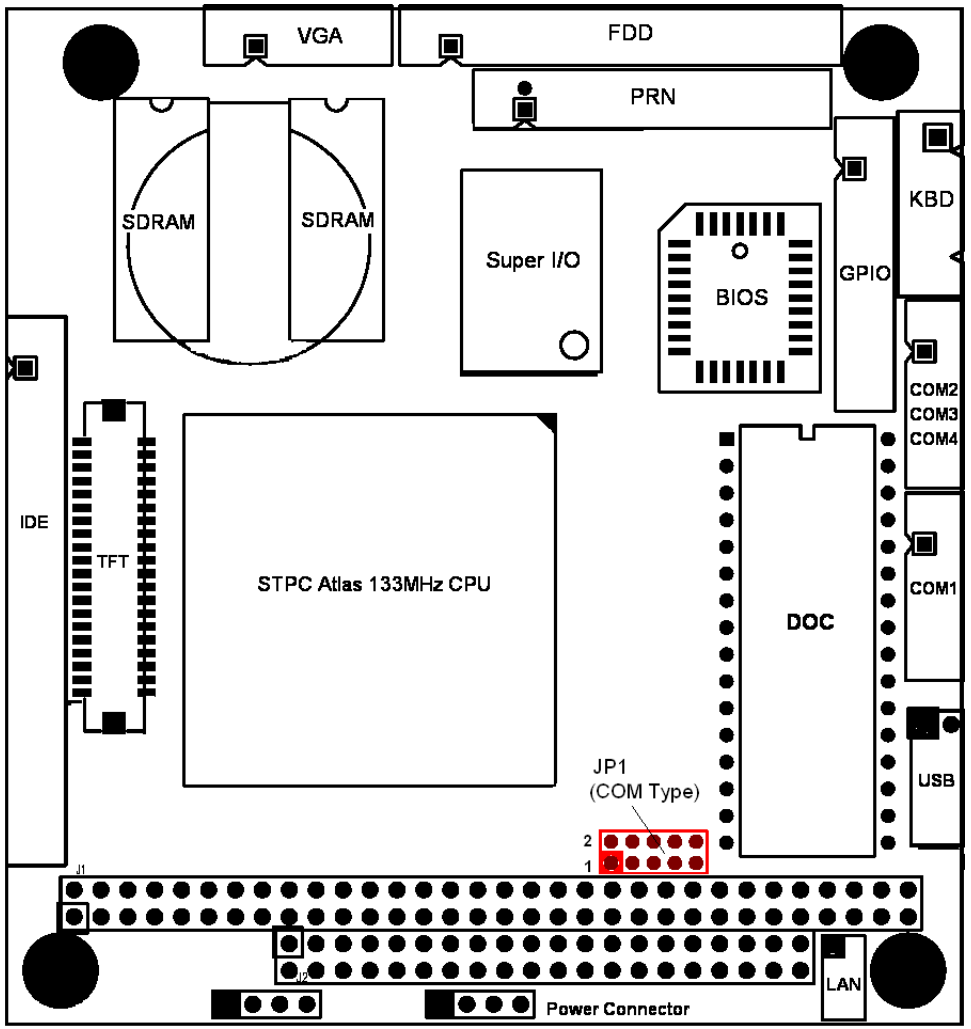
  Graphics functions are controlled through the on-chip graphic engine in the STPC ATLAS and the monitor (or TFT)display is produced through 2D graphics display engine. The graphics resolution supported is a maximum of 1024x768 at 75 Hz refresh rate and is VGA and SVGA compatible

- **System Memory:** On-board 32MB SDRAM(up to 64MB)
- **Bus interface:** PC/104 ISA bus
- **Multi I/O :** Winbond W83977F
- **System BIOS:** Award PnP BIOS with VGA BIOS in a single 256KB FLASH ROM (Year 2000 Compliant BIOS)
- **Plug and Play:** Dual interrupt and DMA signal steering with plug and play control.
- **Display:**
  - Graphics functions are controlled through the on-chip graphic engine in the ST PC ATLAS Chipset
  - The CRT graphics resolution supported is a maximum of 1024x768 at 75 Hz refresh rate and is VGA and SVGA compatible
  - Flat Panel Display: Supports 9/12/18-bit TFT flat panels with resolution up to 800 x 600
- **LAN:** RTL8139C PCI local bus single-chip Fast Ethernet controller and RJ-45 connector. supports 10 Mb/s and 100 Mb/s N-way Auto-negotiation operation (LAN for PC-482VN only)
- **Floppy Disk Drive Interface:** Supports Up to two Floppy Disk Drives,5.25"(360KB or 1.2MB) and/or 3.5"(720KB or 1.44MB/2.88MB)
- **IDE Hard Disk Drive Interface:** One Channel Ultra-DMA 33MB/sec PCI EIDE

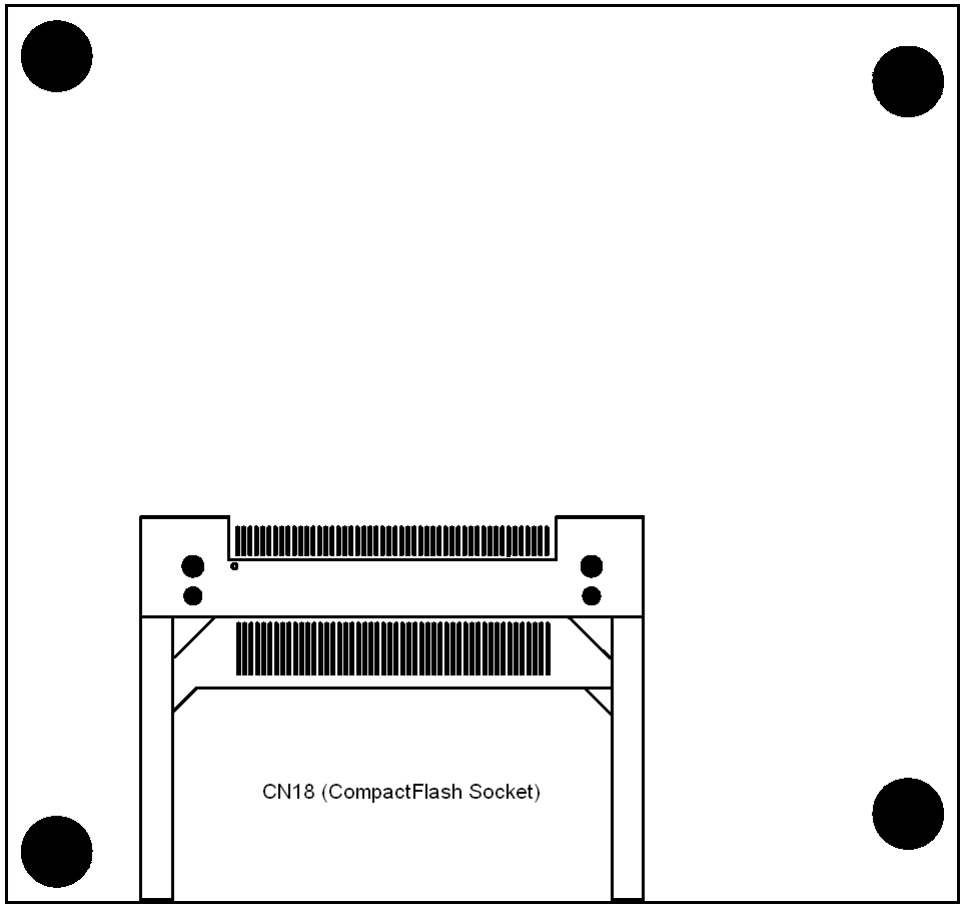
- **CompactFlash Slot:** One Fully IDE CompactFlash Type I/II Compatibility Slot and Support +5VDC or +3.3VDC IDE CompactFlash Card. (CF for PC-482VN only)
- **Serial Ports:**
  - Three RS-232C and One RS-232/422/485 serial Ports. For PC-482VN (One RS-232C and One RS-232/422/485 serial Ports. For PC-482V)
  - Overvoltage protection for RS-422/485 up to 25kV
  - All with 16C550 UART And 16 byte FIFOs
- **Printer Port:** One SPP/ECP/EPP Bi-direction Parallel Port.
- **Solid state disk:** One expended 32-pin Sockets for M-Systems **DiskOnChip**
- **EEPROM :** Provide 256 words(16 bit) EEPROM register for user
- **Real-time clock/calendar:** Lithium battery with 10 year data retention
- **General Purpose I/O interface:**
  - Provide 16 channels TTL level General Purpose I/O interface
  - Each channel can be software programmed to be input or output
  - Individual software programmable interrupt mask.
- **Watch Dog timer:** The watch dog timer range from 0 to 254 sec
- **I/O bus expansion:** PC/104 ISA Bus connector
- **Power Supply Voltage:** + 5VDC
- **Power Consumption:** +5VDC/1.6A (max)
- **Operating Temperature:** 32 to 140F (0 to 60C).
- **Dimensions:** 96(L) x 90(W)mm

Chapter 2
Jumper settings

Locating jumpers



2.1 CompactFlash Slot on solder side



2.2 Jumper Setting

The PC-482VN has a number of jumper that allow you to configure your system to suit your application. The table below lists thefunction of each of the board's jumper:

Label	Function	
JP1	COM1 RS-232/422/485 selection	Ref. 2.3.1

2.3 Setting jumpers

You configure your card to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To <close> a jumper you connect the pins with the clip. To <open> a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case you would connect either pins 1 and 2 or 2 and 3.

The jumper settings are schematically depicted in this manual as follows:

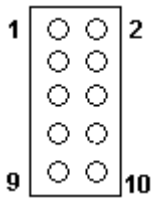
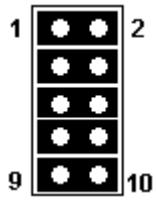
A pair of needle-nose pliers may be helpful when working with jumpers.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

The Jumper settings with background color are factory default

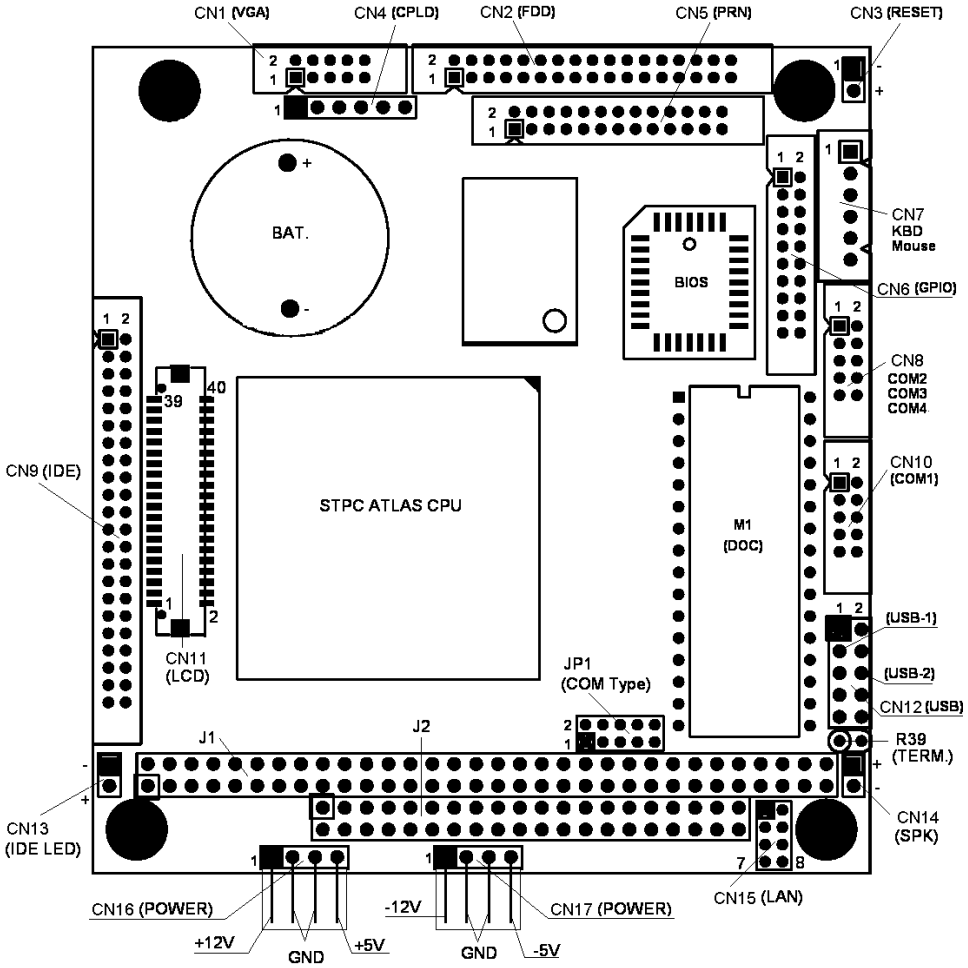
2.3.1 COM1 RS-232/RS-422/RS-485 Selection (JP1)

The COM1 port can be selected as RS-232, RS-422 or RS-485 by setting JP1. The following chart shows the jumper setting.

JP1	COM1 Type
	ALL OPEN for RS-232C **(Default)**
	ALL CLOSED for RS-422/485

Chapter 3
Connecting Peripherals

3.1 Locating Connectors



3.2 Connectors Summary

On-module connectors link the PC-482VN to external devices such as hard disk drives, a keyboard, or floppy drives. The table below lists the function of each of the board's connectors:

Label	Function	Page
CN1	CRT Display connector	3.12
CN2	FDD connector	3.6
CN3	Reset connector	3.3
CN4	CPLD connector	3.11
CN5	Parellel port connector	3.8
CN6	General Purpose I/O connector	3.10
CN7	Keyboard & PS/2 mouse connector	3.4
CN8	Serial Port 2,3,4 (COM2/3/4) connector	3.9
CN9	Hard disk connector	3.7
CN10	Serial Port 1 (COM1) connector	3.9
CN11	Flat panel disply Connector	3.13
CN12	USB connector	3.14
CN13	Hard disk LED	3.5
CN14	Speaker connector	3.15
CN15	Ethernet connector	3.16
CN16	+12V/+5V External Power Input connector	3.17
CN17	-12V/-5V External Power Input connector	3.18
CN18	CompactFlash Slot	3.19

3.3 Hardware reset switch (CN3)

The hardware reset switch button is an active low signal (24 mA sink rate).

Pin	Function
1	Reset SW -
2	Reset SW +

3.4 Keyboard & PS/2 mouse connector (CN7)

The PC-482VN module provides a keyboard connector. The standard PC/AT BIOS will report an error or fail during power-on self-test (POST) after a reset if the keyboard is not present. The PC-482VN's BIOS standard setup menu allows you to select "All, But Keyboard" under the <Halt On> selection. This allows no-keyboard operation in embedded system applications without the system halting under POST.
The PC-482VN module also provides PS/2 mouse connectors, which can be connected to outside world with convert cable.

pin	Signal
1	KBD_CLK
2	KBD_Data
3	MS_CLK
4	GND
5	+5V/DC
6	MS_Data

3.5 Hard disk LED (CN13)

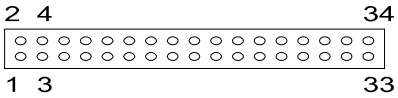
The hard disk LED indicator for hard disk access is an active low signal (24 mA sink rate).

Pin	Function
1	LED -
2	LED +

3.6 Floppy drive connector (CN2)

You can attach up to two floppy drives to the PC-482VN's on-board controller. You can use any combination of 5.25" (360 KB and 1.2 MB) and/or 3.5" (720 KB, 1.44 MB, and 2.88 MB) drives.

1. Plug the 34-pin flat-cable connector into CN2. Make sure that the red wire corresponds to pin one on the connector.
2. Attach the appropriate connector on the other end of the cable to the floppy drive(s). You can use only one connector in the set. The set on the end (after the twist in the cable) connects to the A: drive. The set in the middle connects to the B: drive.

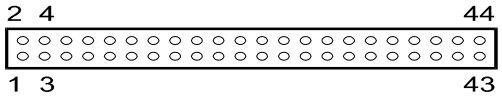


Pin	Signal	Pin	Signal
1	GND	2	DENSITY SELECT*
3	GND	4	N/C
5	GND	6	DRIVE TYPE
7	GND	8	INDEX*
9	GND	10	MOTOR 0*
11	GND	12	DRIVE SELECT 1*
13	GND	14	DRIVE SELECT 0*
15	GND	16	MOTOR 1*
17	GND	18	DIRECTION*
19	GND	20	STEP*
21	GND	22	WRITE DATA*
23	GND	24	WRITE GATE*
25	GND	26	TRACK 0*
27	GND	28	WRITE PROTECT*
29	GND	30	READ DATA*
31	GND	32	HEAD SELECT*
33	GND	34	DISK CHANGE*

* low active

3.7 IDE Hard Drive Connector (CN9)

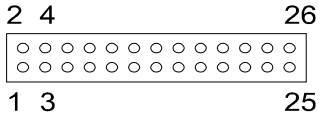
Connect one end of the cable to CN9. Make sure that the red (or blue) wire corresponds to pin 1 on the connector, which is labeled on the board (on the right side).



Pin	Signal	Pin	Signal
1	-RST	2	Ground
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	N.C
21	N.C	22	GND
23	IOW	24	GND
25	IOR	26	GND
27	IORDY	28	BALE
29	N.C.	30	GND
31	IRQ	32	IO16
33	A1	34	N.C.
35	A0	36	A2 CS0
37	CS0	38	CS1
39	-LED	40	GND
41	+5VDC	42	+5VDC
43	GND	44	NC

3.8 Parallel port connector (CN5)

Normally, the parallel port is used to connect the card to a printer. The PC-482VN includes a multi-mode (ECP/EPP/SPP) parallel port, accessed through CN5, a 26-pin flat-cable connector. You will need an adapter cable if you use a traditional DB-25 connector. The adapter cable has a 26-pin connector on one end and a DB-25 connector on the other.
The parallel port is designated as LPT1 and can be disabled or changed to LPT2 or LPT3 in the system BIOS setup. The parallel port interrupt channel is designated to be IRQ7.You can select ECP/EPP DMA channel via BIOS setup.

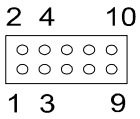


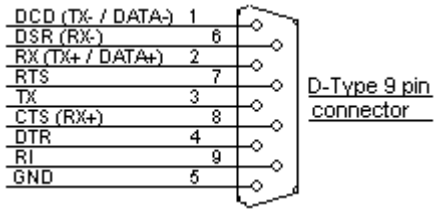
Pin	Signal	Pin	Signal
1	STROBE	2	AUTOFD*
3	D0	4	ERR
5	D1	6	INIT*
7	D2	8	SLCTINI*
9	D3	10	GND
11	D4	12	GND
13	D5	14	GND
15	D6	16	GND
17	D7	18	GND
19	ACK*	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SLCT	26	N/C

3.9 Serial port connectors (CN10, CN8)

The PC-482VN are supported 16C550 compatible UARTs with 16 byte FIFOs

■ Serial Port-1(COM1) RS-232/422/485 Connector (CN10)



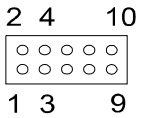


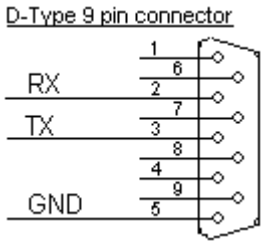
Pin No	RS-232	RS-422	RS-485	Pin No	RS-232	RS-422	RS-485
1	DCD	TX -	DATA -	2	DSR	RX -	
3	RX	TX +	DATA +	4	RTS		
5	TX			6	CTS	RX +	
7	DTR			8	RI		
9	GND			10	NC		

- Terminator Resistor (R39) for RS-422/485
- JP1 ALL CLOSED for RS-422/RS-485 otherwise ALL OPEN [Ref. 2.3.1]

■ Serial Port-2,3,4(COM2/3/4) RS-232 Connector (CN8) - For PC-482VN

- For PC-482V CN8(COM2) pin assigment please Ref. COM1 RS-232 Type
- Ext. Cable to 3 D-type Connector for COM2/COM3/COM4 for PC-482VN
- Serial Port-2,3,4 line shared with CN8





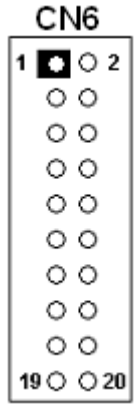
Pin	Name	Pin	Name
1		2	RX (COM3)
3	RX (COM2)	4	TX (COM3)
5	TX (COM2)	6	RX (COM4)
7		8	TX (COM4)
9	GND	10	

3.10 General Purpose I/O Connector(GPIO) (CN6)

- Provide 16 channels General Purpose I/O
- Each channel can be software programmed to input or output
- Individual software programmable interrupt mask.
- All I/O signals confirm to LS-TTL levels and support Pull-Up resistore(4.7K Ω) for each channel
- The GPIO R/W is by software interrupt to function call

  Ref. Appendix D

Pin NO.	Function	Pin NO.	Function
1	GND	2	+5VDC
3	GPIO_0	4	GPIO_8
5	GPIO_1	6	GPIO_9
7	GPIO_2	8	GPIO_10
9	GPIO_3	10	GPIO_11
11	GPIO_4	12	GPIO_12
13	GPIO_5	14	GPIO_13
15	GPIO_6	16	GPIO_14
17	GPIO_7	18	GPIO_15
19	+5VDC	20	GND

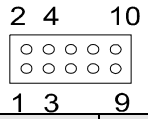


3.11 CPLD Connector (CN4)

pin	Signal
1	TCK
2	TMS
3	GND
4	+5VDC
5	TDO
6	TDI

3.12 CRT display connector (CN1)

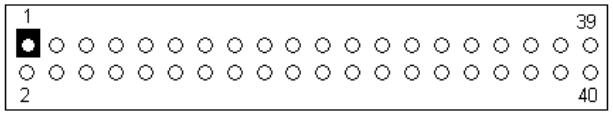
CN1 is a 10-pin header used for conventional CRT displays. A simple one-to-one adapter can be used to match CN1 to a standard 15-pin D-SUB connector commonly used for VGA. Pin assignments for CRT display connector CN1 are detailed in **Chapter 4**



Pin	Signal	Pin	Signal
1	RED	2	GND
3	GREEN	4	GND
5	BLUE	6	GND
7	HSYNC	8	GND
9	VSYNC	10	GND

3.13 Flat panel display connector (CN11)

CN11 is a 20*2-pin connector which can support a 9/12/18bit 640*480 or 800x600 TFT LCD.It is recommended that the LCD bias voltage not be applied to the panel until the logic supply voltage (+5 V) and panel video signals are stable.Pin assignments for connector CN11 are detailed in **Chapter 4**



Pin	Signal	Pin	Signal
1	+12VDC	2	+12VDC
3	GND	4	GND
5	+5VDC	6	+5VDC
7	ENAVEE	8	ENAVDD
9	+3VDC	10	N/C
11	B0	12	B1
13	B2	14	B3
15	B4	16	B5
17	GND	18	N/C
19	G0	20	G1
21	G2	22	G3
23	G4	24	G5
25	GND	26	N/C
27	R0	28	R1
29	R2	30	R3
31	R4	32	R5
33	GND	34	DCLK
35	GND	36	FRAME (VSYNC)
37	FPLINE (HSYNC)	38	TFT_PWM
39	DE	40	+3VDC

3.14 USB1 & USB2 connector (CN12)

The connector CN12 is 8 pins header for USB1 and USB2 port

pin	USB-1	pin	USB-2
1	+5VDC	2	+5VDC
3	USBD1-	4	USBD2-
5	USBD1+	6	USBD2+
7	Signal GND	8	Signal GND
9	GND	10	GND

3.15 Speaker Connector (CN14)

The PC-482VN can drive an 8 Ω speaker at 0.5 watts. Make sure that alternatives to this specification do not overload the card.

Pin	Function
1	+5V DC
2	Speaker Data

3.16 Ethernet 10/100 Base-T connector (CN15)

The Module(PC-482VN Only) is equipped with a high performance PCI-bus Ethernet interface which is fully compliant with IEEE 802.3U 10/100Mbps CSMA/CD standards. It is supported by all major network operating systems.

This connector supports Ethernet 10/100Mbps network data transfer rate operation.

pin	signal	pin	signal
1	TX+	2	TX-
3	RX+	4	
5		6	RX-
7		8	

3.17 External “+12VDC / +5VDC” power input connector (CN16)

The connector CN16 is four pins +12V/GND/+5VDC power input connector

pin	Signal
1	+12VDC
2	GND
3	GND
4	+5VDC

3.18 External “-12VDC / -5VDC” power input connector (CN17)

The connector CN17 is four pins -12V/GND/-5VDC power input connector

pin	Signal
1	-12VDC
2	GND
3	GND
4	-5VDC

3.19 CompactFlash Slot (CN18)

The PC-482VN is equipped with a CompactFlash type I/II Slot on the solder side, which supports at the secondary master IDE interface CompactFlash card and on-board +5VDC to +3.3VDV regulator.

Pin	Signal	Pin	Signal
1	Ground	2	D3
3	D4	4	D5
5	D6	6	D7
7	-CE	8	Ground
9	Ground	10	Ground
11	Ground	12	Ground
13	VCC	14	Ground
15	Ground	16	Ground
17	Ground	18	A2
19	A1	20	A0
21	D0	22	D1
23	D2	24	-IOCS16
25		26	GND
27	D11	28	D12
29	D13	30	D14
31	D15	32	-CE2
33	3.3_GND	34	-IORD
35	-IOWR	36	-WE
37	IRQ	38	-CSEL
39		40	
41	-RESET	42	-IORDY
43		44	VCC
45	-DASP	46	
47	D8	48	D9
49	D10	50	Ground

Chapter 4
VGA BIOS Setup

Introduction

The PC-482VN has an on-board flat panel/VGA interface. The specifications and features are described as follows:

4.1.1 Chipset

The PC-482VN uses a STPC Atals chipset for its SVGA controller. Display Type Supports CRT and TFT LCDs. Able to display both CRT and Flat Panel simultaneously . In addition, it also supports interlaced and non-interlaced analog monitors (color and monochrome VGA) in high-resolution modes while maintaining complete IBM VGA compatibility. Digital monitors (i.e. MDA, CGA, and EGA) are NOT supported. Multiple frequency (multisync) monitors are handled as if they were analog monitors.

4.1.2 Display memory

Display Memory UMA architecture, share system memory up to 4MB, the VGA controller can drive CRT displays or color TFT panel displays with resolutions up to 1024 x 768 (CRT) and 9/12/18 bit 640x480/800x600(TFT Panel)

4.1.3 Flat Panel BIOS and Utility

Below is a list of optional Flat Panel SVGA BIOS. The VGA BIOS is combined with the system BIOS in a single. To change to another BIOS please contact your local dealer.

640480D.BIN -- Award BIOS For 640x480 TFT LCD and run on DOS Mode

640480N.BIN -- Award BIOS For 640x480 TFT LCD and run on normal mode

800600N.BIN -- Award BIOS For 800x6000 TFT LCD and run on normal mode

482CRT.BIN -- Award BIOS For CRT Mode only and run on normal mode

Example : Awdflash 648480d.bin -- For 640x480 TFT LCD and run on DOS Mode

Example : Awdflash 800600N.bin -- For 800x6000 TFT LCD and run on normal mode

Example : Awdflash 482CRT.BIN -- For CRT Mode only and run on normal mode

Appendix A
Flash Disk Setup & EEPROM R/W

A.1 About solid state disk

The PC-482VN provides one extended solid state disk sockets **(M1)** which can accept **DiskOnChip™** device

The **DiskOnChip™** disk occupies 8KB system memory space at CE000h-CFFFFh, D0000h-D1FFFh, DE000h-DFFFFh or E0000h-E1FFFh depends on the setting of Award BIOS Setup "Advanced Chipset->Solid State Disk Address:"

A.2 How to use DiskOnChip Flash disk

The **DiskOnChip™** Flash disk chip is produced by M-Systems. The DiskOnChip™ Flash disk occupies only 8KB system memory address, and can completely emulate a disk in PC system

The PC-482VN module allows the user to install this device on the socket called **M1**.

A.3 How to use EEPROM

The PC-482VN provide a EEPROM for backup system configures and reserved 240 words for user R/W through the software interrupt vector by System BIOS setup "Advanced Chipset->Function Call Entry:"

Write data to EEPROM

Entry : AX = 101h - Write EEPROM
DL - Address (0 - EFh)
BX - data (16bits)

Exi t: none

Read data from EEPROM

Entry : AX = 100h - Read EEPROM
DL - Address (0 - EFh)

Exi t: AX - data (16bits)

Example: EEPROM R/W interrupt vector number is 6Fh

```
; Write data to EEPROM
mov   ax,101h      ; Write data function number
mov   dl,20h       ; Address
mov   bx,3A2Bh     ; data
int   6Fh          ; Write data to EEPROM

; Read data from EEPROM
mov   ax,100h      ; Read data function number
mov   dl,20h       ; Address
int   6Fh          ; Read data from EEPROM (data saved in AX)
```

Appendix B
Programming Watch dog timer

The following steps show how to program the watchdog timer

1. you must write a program which write I/O port address 543(hex) to write timeout value(0-255 sec) to Watchdog REG. and reads I/O port address 443 (hex) to enable watch-dog timer. After enabled, your program must refresh the watchdog timer by reading the I/O port 443 (hex) again perodically.
2. Read I/O port address 43 (hex) to Disabled watch-dog timer..

I/O Address	Function
543H I/O write	Bit(0)=1 – NMI Enabled =0 – NMI Disabled
143H I/O write	Set watchdog timeout value
443H I/O read	Enable watchdog and start to count
443H I/O read	Refresh Cycle
43H I/O read	Disable watchdog

Note: After NMI service routine is process and Disable NMI[Bit(0)=0] then the system will be reseted

The following example shows how you might program the watchdog timer in ASM:

Example-A:

```
Mov   al,5          ; Set timeout Value(5 sec)
Out   143h,al       ; Set to Timer REG.
In    al,443h       ; Enable Watchdog and start to count
…..                 ; do user program
In    al,443h       ; refresh cycle
In    al,43h        ; Disable watchdog timer
```

Example-B:

```
Mov   al,1          ; Set NMI Enabled
Out   543h,al       ; Write Watchdog NMI REG.
Mov   al,8          ; Set timeout Value(8 sec)
Out   143h,al       ; Write to Timer REG.
In    al,443h       ; Enable Watchdog and start to count
…..                 ; do user program
In    al,443h       ; refresh cycle
In    al,43h        ; Disable watchdog timer
```

Appendix C
Award BIOS Setup

C.1 Starting Setup

The Award BIOS is immediately activated when you first power on the computer. The BIOS reads the system information contained in the CMOS and begins the process of checking out the system and configuring it. When it finishes, the BIOS will seek an operating system on one of the disks and then launch and turn control over to the operating system.

While the BIOS is in control, the Setup program can be activated in one of two ways:

1. By pressing <Del> immediately after switching the system on, or

2. by pressing the <Del> key when the following message appears briefly at the bottom of the screen during the POST (Power On Self Test).

   Press DEL to enter SETUP.

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the "RESET" button on the system case. You may also restart by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to...

PRESS F1 TO CONTINUE, DEL TO ENTER SETUP

.

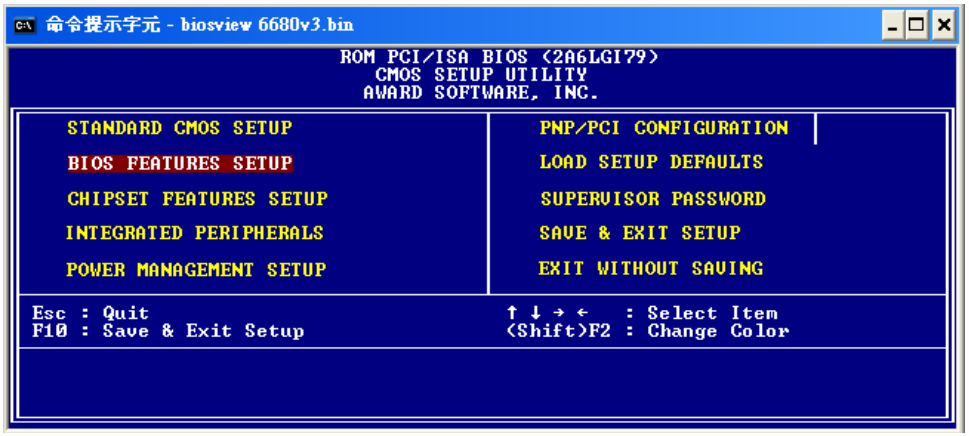
C.2 In Case of Problems

If, after making and saving system changes with Setup, you discover that your computer no longer is able to boot, the Award BIOS supports an override to the CMOS settings which resets your system to its defaults.

The best advice is to only alter settings which you thoroughly understand. To this end, we strongly recommend that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both Award and your systems manufacturer to provide the absolute maximum performance and reliability. Even a seemingly small change to the chipset setup has the potential for causing you to use the override.

C.3 Main Menu

Once you enter the System BIOS CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu.



C.3.1 Setup Items

The main menu includes the following main setup categories. Recall that some systems may not include all entries.

C.3.2 Standard CMOS Features

This setup page includes all the items in a standard, AT-compatible BIOS.

C.3.3 Advanced BIOS Features

This setup page includes all the items of Award special enhanced features.

C.3.4 Advanced Chipset Features Setup

This setup page includes all the items of chipset special features. See Section C.6 for details.

C.3.5 Integrated Peripherals

This section page includes all the items of IDE hard drive and Programmed Input / Output features.

C.3.6 Power Management Setup

This entry only appears if your system supports Power Management, “Green PC”, standards.

C.3.7 PNP / PCI Configuration

This entry appears if your system supports PNP / PCI. See Section 7 for details.

C.3.8 Load Optimized Defaults

The chipset defaults are settings which provide for maximum system performance. While Award has designed the custom BIOS to maximize performance, the manufacturer has the right to change these defaults to meet their needs.

C.3.9 Save & Exit Setup

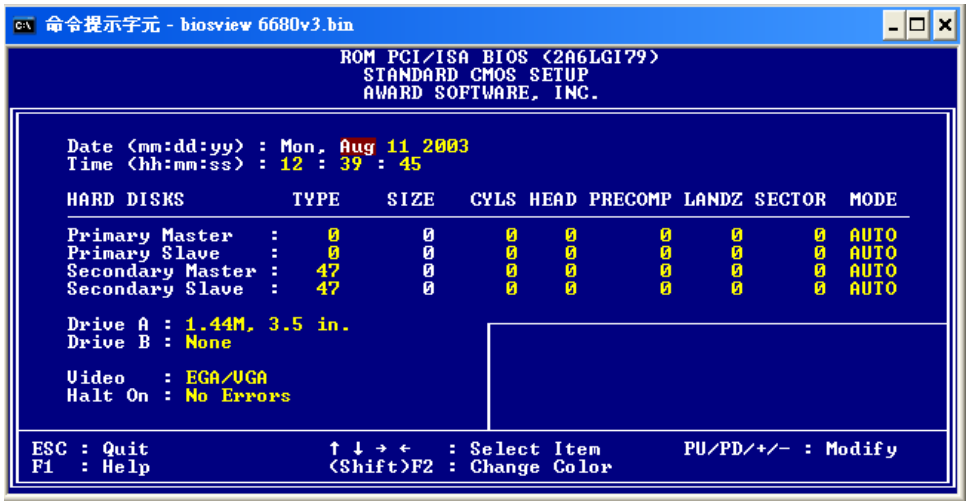
Save CMOS value changes to CMOS and exit setup.

C.3.10 Exit Without Save

Abandon all CMOS value changes and exit setup.

C.4 Standard CMOS Features

The items in Standard CMOS Setup Menu are divided into 10 categories. Each category includes no, one or more than one setup items. Use the arrow keys to highlight the item and then use the <PgUp> or <PgDn> keys to select the value you want in each item.



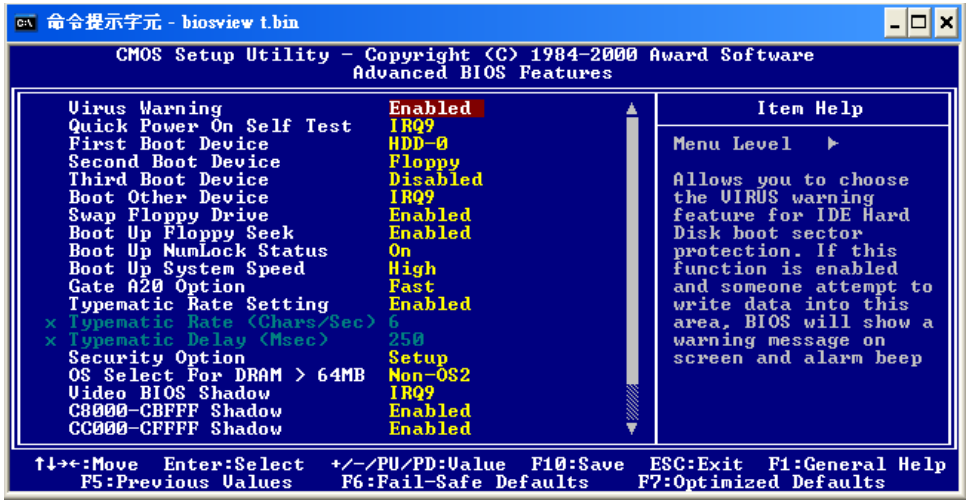
C.4.1 Halt On

The category determines whether the computer will stop if an error is detected during power up.

No errors	The system boot will not be stopped for any error that may be detected.
All errors	Whenever the BIOS detects a non-fatal error the system will be stopped and you will be prompted.
All, But Keyboard	The system boot will not stop for a keyboard error; it will stop for all other errors.
All, But Diskette	The system boot will not stop for a disk error; it will stop for all other errors.
All, But Disk/Key	The system boot will not stop for a keyboard or disk error; it will stop for all other errors.

C.5 Advanced BIOS Features

This section allows you to configure your system for basic operation. You have the opportunity to select the system's default speed, boot-up sequence, keyboard operation, shadowing and security.



C.5.1 Quick Power On Self Test

This category speeds up Power On Self Test (POST) after you power up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST.

Enabled	Enable quick POST
Disabled	Normal POST

C.5.2 Gate A20 Option

This entry allows you to select how the gate A20 is handled. The gate A20 is a device used to address memory above 1 Mbytes. Initially, the gate A20 was handled via a pin on the keyboard. Today, while keyboards still provide this support, it is more common, and much faster, for the system chipset to provide support for gate A20.

Normal	keyboard
Fast	chipset

C.5.3 PCI / VGA Palette Snoop

It determines whether the MPEG ISA/VESA VGA Cards can work with PCI/VGA or not.

Enabled	When PCI/VGA working with MPEG ISA/VESA VGA Card.
Disabled	When PCI/VGA not working with MPEG ISA/VESA VGA Card.

C.5.4 Video BIOS Shadow

Determines whether video BIOS will be copied to RAM. However, it is optional depending on chipset design. Video Shadow will increase the video speed.

Enabled	Video shadow is enabled
Disabled	Video shadow is disabled

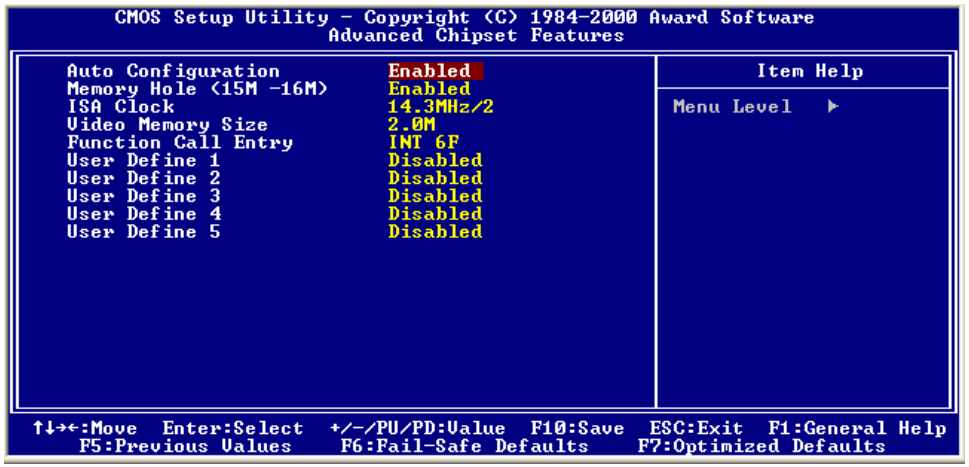
C.5.5 C8000 - CBFFF Shadow/DC000 - DFFFF Shadow

These categories determine whether option ROMs will be copied to RAM. An example of such option ROM would be support of on-board SCSI.

Enabled	Optional shadow is enabled
Disabled	Optional shadow is disabled

C.6 Advanced Chipset Features Setup

This section allows you to configure the system based on the specific features of the installed chipset. This chipset manages bus speeds and access to system memory resources, such as DRAM and the external cache. It also coordinates communications between the conventional ISA bus and the PCI bus. It must be stated that these items should never need to be altered. The default settings have been chosen because they provide the best operating conditions for your system. The only time you might consider making any changes would be if you discovered that data was being lost while using your system.



C.6.1 Auto Configuration

Pre-defined values for DRAM, cache.. timing according to CPU type & system clock.
The Choice: Enabled, Disabled.
Note: When this item is enabled, the pre-defined items will become SHOW-ONLY.

C.6.2 Memory Hole At 15M-16M

In order to improve performance, certain space in memory can be reserved for ISA cards. This memory must be mapped into the memory space below 16 MB.

Enabled	Memory hole supported.
Disabled	Memory hole not supported.

C.6.3 ISA Clock

This item allows you to select the ISA clock type.

14.3MHz / 2	System clock type
PCI CLK / 4	PCI clock type

C.6.4 Video Memory Size

This item allows you to select the Video Memory Size

Memory Size
512KB
1MB
2MB
4MB

C.6.5 Function Call Entry

This item allows you to select the Software Interrupt Number for GPIO,EEPROM of Driver Function Call Entry. [Ref. Appendix D]

INT. No.
INT 6Fh
INT 7Fh
INT 8Fh,
INT 9Fh
INT AFh
INT BFh
INT CFh
INT DFh
INT EFh

C.6.6 Solid State Disk Address

This item allows you to select The Solid State Disk **(DiskOnChip™)** occupies system memory area

Address
CE000h - CFFFFh
D0000h – D1FFFh
DE000h - DFFFFh
E0000h – E1FFFh

C.6.7 User Define 1

This item is reserved for user define and read from CMOS RAM address 5Eh (bit-4)

Enabled	CMOS RAM Address 5Eh (bit-4) = 0
Disabled	CMOS RAM Address 5Eh (bit-4) = 1

C.6.8 User Define 2

This item is reserved for user define and read from CMOS RAM address 5Eh (bit-3)

Enabled	CMOS RAM Address 5Eh (bit-3) = 0
Disabled	CMOS RAM Address 5Eh (bit-3) = 1

C.6.9 User Define 3

This item is reserved for user define and read from CMOS RAM address 5Eh (bit-2)

Enabled	CMOS RAM Address 5Eh (bit-2) = 0
Disabled	CMOS RAM Address 5Eh (bit-2) = 1

C.6.10 User Define 4

This item is reserved for user define and read from CMOS RAM address 5Eh (bit-1)

Enabled	CMOS RAM Address 5Eh (bit-1) = 0
Disabled	CMOS RAM Address 5Eh (bit-1) = 1

C.6.11 User Define 5

This item is reserved for user define and read from CMOS RAM address 5Eh (bit-0)

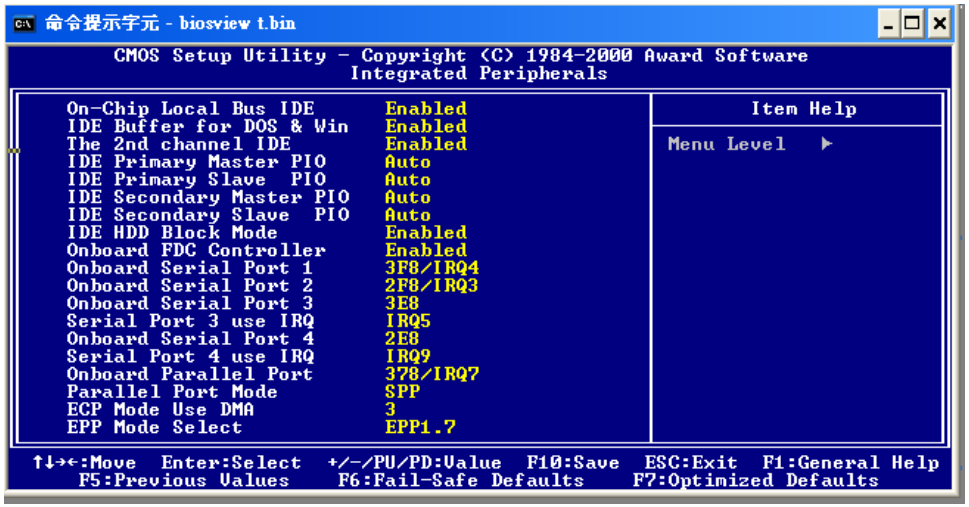
Enabled	CMOS RAM Address 5Eh (bit-0) = 0
Disabled	CMOS RAM Address 5Eh (bit-0) = 1

C.6.12 CPU Internal Cache

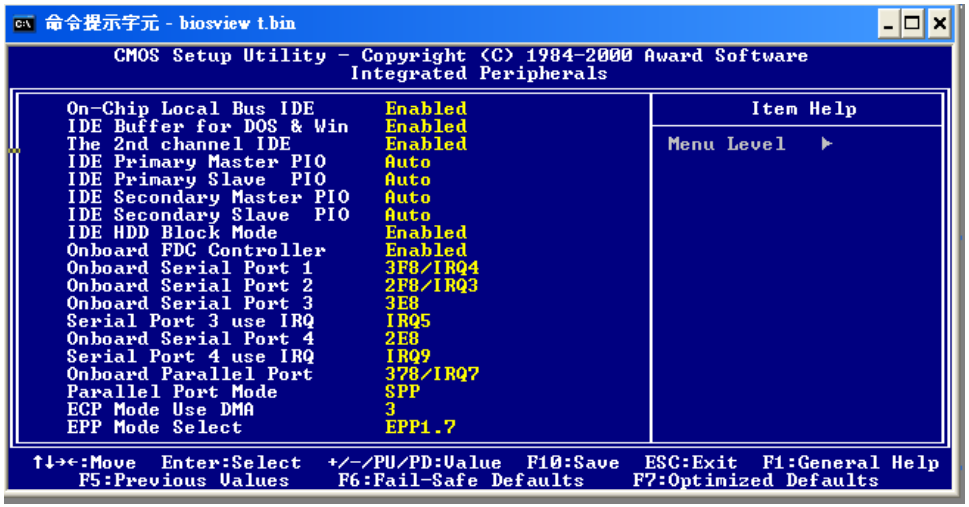
This categorie speed up memory access. However, it depends on CPU. The default value is enable.

Enabled	Enable cache
Disabled	Disable cache

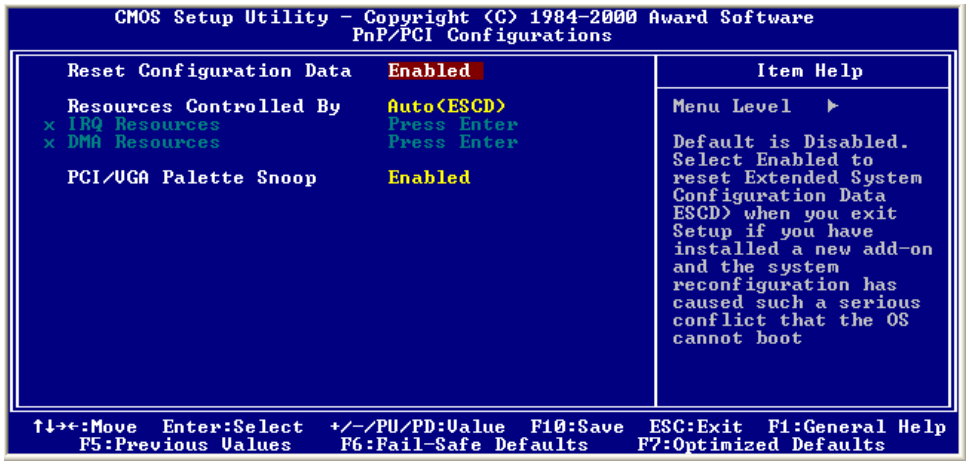
C.7 Integrated Peripherals



C.8 Power Management Setup



C.9 PnP/PCI Configuration Setup



C.10 Load Optimized Defaults

When you press <Enter> on this item you get a confirmation dialog box with a message similar to:

Load Optimized Defaults (Y/N) ? N

Pressing 'Y' loads the default values that are factory settings for optimal performance system operations.

Appendix D
Programer's Reference

D.1 How to use this driver

The PC-482 driver is Called by software interrupts INT 6Fh, 7Fh, 8Fh, 9Fh, AFh, BFH, CFh, DFh or EFh and selected by Award BIOS setup "Advanced Chipset--> Function Call Entry:" [Ref. C.6.5]

● (AH) = 01h Read & Write data from/to EEPROM

➢ (AL) = 00h - Read data from EEPROM
(DX) - Address (00h to EFh)

On Return: (AX) - Data

➢ (AL) = 01h - Write data to EEPROM
(DX) - Address (00h to EFh)
(BX) - Data

On Return: none

● (AH) = 02h General Purpose I/O (GPIO)

➢ (AL) = 00h - Set GPIO Port direction control register
(DL) - Port Number
= 0 - Port-0 (Channels 7-0)
= 1 - Port-1 (Channels 15-8)
(DH) - This 8-bit registers sets the direction, input or output of GPIO channels
= 0 - Output
= 1 - Input

On Return: none

➢ (AL) = 01h - Read GPIO input port

(DL) - Port Number
= 0 - Port-0 (Channels 7-0)
= 1 - Port-1 (Channels 15-8)

On Return: (AL) - Data

➢ (AL) = 02h - Write Data to GPIO output port

(DL) - Port Number
= 0 - Port-0 (Channels 7-0)
= 1 - Port-1 (Channels 15-8)

(DH) - Data

On Return: none

➢ (AL) = 03h - Write Interrupt edge select bits for selected GPIO input

(DL) - Port Number
= 0 - Port-0 (Channels 7-0)
= 1 - Port-1 (Channels 15-8)

(DH) - Write Interrupt edge register(bits 7-0)
= 0 - Rising edge
= 1 - Falling edge

On Return: none

➢ (AL) = 04h - Write Interrupt mask bits for selected GPIO input channels

(DL) - Port Number
= 0 - Port-0 (Channels 7-0)
= 1 - Port-1 (Channels 15-8)

(DH) - Write Interrupt unmask register (bits 7-0)
= 0 - Disabled
= 1 - Enabled

On Return: none

➢ (AL) = 05h - Set GPIO Interrupt Number (IRQ)

(DL) - Interrupt Number (IRQ 1-15)
bit(7) – Interrupt Enabled/Disabled
= 0 – Disabled
= 1 – Enabled
bit(6-4) – Reserved
bit(3-0) – IRQ number(0-15)
(Reserved IRQ0,IRQ2,IRQ9 for system)

On Return: none

➢ (AL) = 06h - Clear interrupt for selected GPIO channel

(DL) - Port Number
= 0 - Port-0 (Channels 7-0)
= 1 - Port-1 (Channels 15-8)

(DH) - Write 1 to clear Interrupt for selected channel (bits 7-0)

On Return: none

● (AH) = 03h Watch-Dog Reset

➢ (AL) = 00h - Set Watch-Dog tmie-out value

(DL) - Watch-dog time-out value
= 0 - Watch-dog Disabled
> 0 - Time-out value (1-255 second)

On Return: none

➢ (AL) = 01h - Set Watch-dog NMI Enabled/Disabled

(DL) - Watch-dog NMI Enabled/Disabled
= 1 - Enabled
= 0 - Disabled

On Return: none

➢ (AL) = 02h - Enabled Watch-dog and Refresh Cycle

On Return: none

➢ (AL) = 03h - Disabled Watch-dog Reset

On Return: none

● (AH) = 04h PassWord

➢ (AL) = 00h - Set PassWord
(DX,BX) - Password

On Return: none

➢ (AL) = 01h - Verify Password
(If Error 5 times then auto clear Password)
(DX,BX) - Password

On Return: (AX) = 0 - Valid
= FFFFh - Invalid

● (AH) = 06h Read User define status from CMOS RAM
(Ref. C.6.7)

➢ (AL) = 1 - Read User Define 1 Status
= 2 - Read User Define 2 Status
= 3 - Read User Define 3 Status
= 4 - Read User Define 4 Status
= 5 - Read User Define 5 Status

On Return: AL = 0 - Enabled
= 1 - Disabled

Appendix E
System configuration

E.1 System I/O ports

Addr. range (Hex)	Device
000-01F	DMA controller
020-021	Interrupt controller 1, master
040-05F	8254 timer
060-06F	8042 (keyboard controller)
070-07F	Real-time clock, (NMI) mask
080-09F	DMA page register,
0A0-0BF	Interrupt controller 2
0C0-0DF	DMA controller
0F0	Clear math co-processor
0F1	Reset math co-processor
0F8-0FF	Math co-processor
100	SSD bank register
143	Watchdog time
1F0-1F8	Fixed disk
200-207	Reserved (Game I/O)
278-27F	Reserved
2E8-2EF	Serial port 4
2F8-2FF	Serial port 2
300-31F	Prototype card
320	Ethernet controller(PC-486VN)
360-36F	Reserved
378-37F	Parallel printer port 1 (LPT 2)
380-38F	SDLC, bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome display and LPT1
3C0-3CF	Reserved
3D0-3DF	Color/graphics monitor adapter
3E8-3EF	Serial port 3
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1
443	Watchdog timer enabled
543	Watchdog timeout value REG.
500	SSD control register

E.2 DMA channel assignments

Channel	Function
0	Available
1	Available
2	Floppy disk (8-bit transfer)
3	Available (Parallel Port)
4	Cascade for DMA controller 1
5	Available
6	Available
7	Available

E.3 IRQ mapping chart

IRQ no.	Device used
0	Interval timer
1	Keyboard
2	Interrupt from Controller 2
3	COM2
4	COM1
5	Reserved
6	FDD
7	LPT1
8	RTC
9	Software Redirected to INT 0AH (IRQ2)
10	Reserved
11	Reserved
12	PS/2 mouse
13	Co-processor
14	Primary IDE
15	Secondary IDE