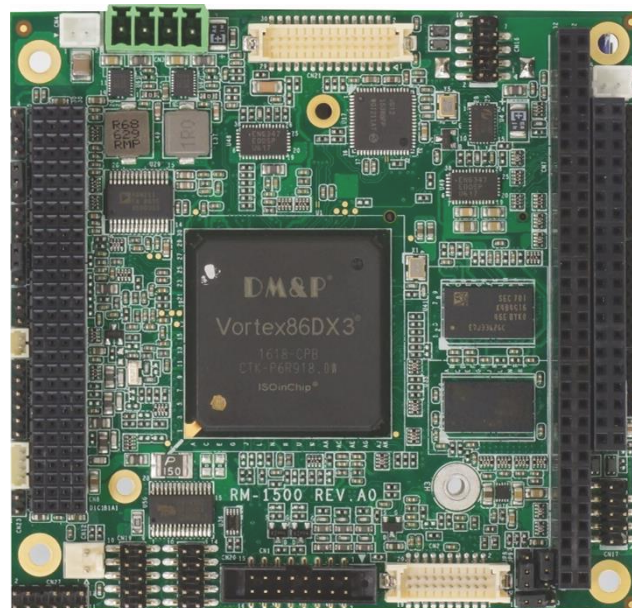


Portwell

PB-VORTEX-DX3

Manual

Rev. 1.3



Change Index

Revision	Changes
1.0a	Release (05.10.2017)
1.1	Connector pinning at 6.3 changed
1.2	CN4 added (01.04.2019)
1.3	Tables updated, BIOS configuration added

Table 1: Change Index

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1. Introduction

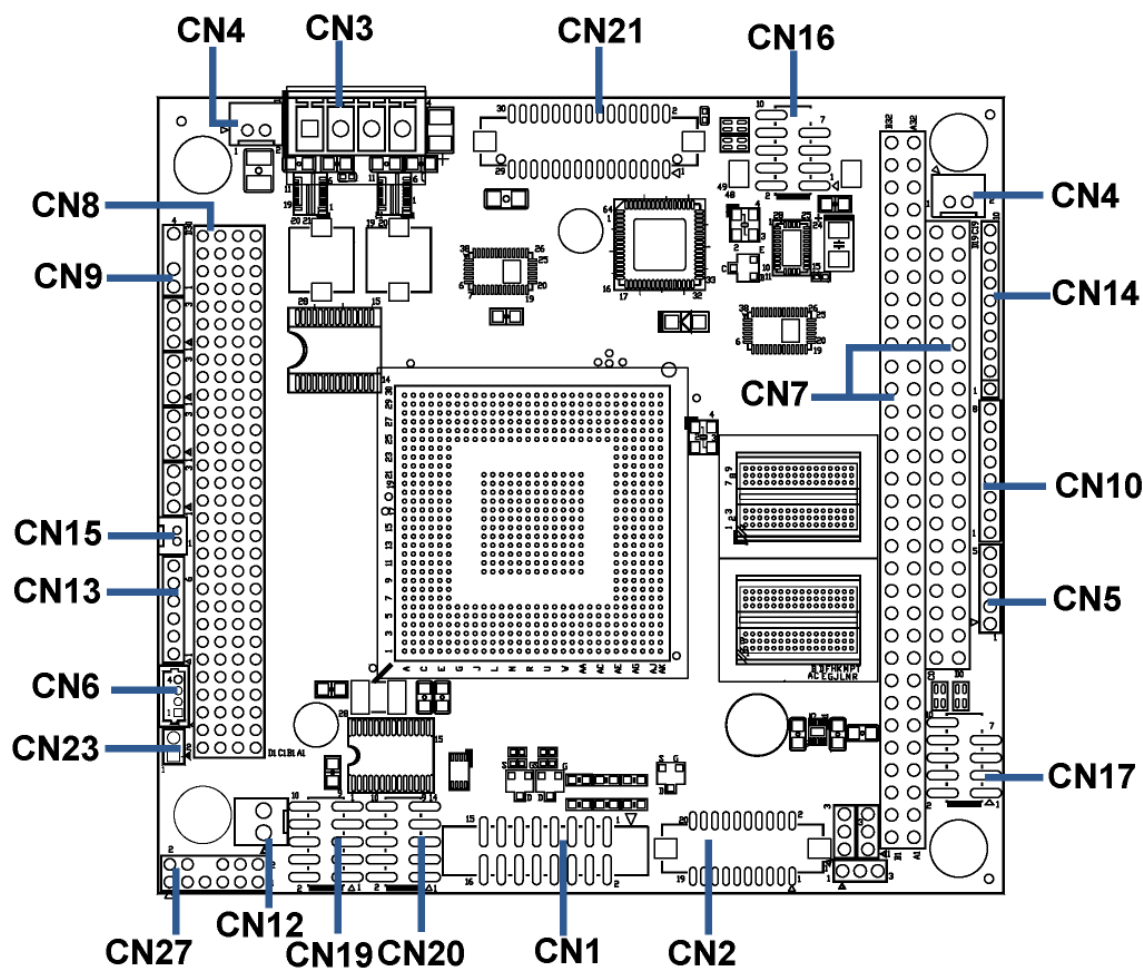
The PB-Vortex-DX3 with the dimensions 90x96mm is based on the DM & P Vortex86-DX3 system on chip (SoC). The clock frequency of the Vortex86-DX3 dual core processor is 1GHz. The soldered 2GB (DDR3L, 1333) memory allows the use in rough industrial environment. A complete ISA bus and PCI interface make the PC/104 board an all-rounder and a perfect replacement of discontinued x86-based PC/104 boards. Serial bus interfaces are available via SM and I²C. The single 5V voltage power supply AT/ATX mode is via jumper settings. The power consumption TDP is about 6 watts, which allows passive cooling. Dual display via CRT and 18/24bit single-channel LVDS is support. The board has 2x Ethernet (10/100 and 10/100/1000 Mbit) ports, one SATA connector for HDD, and M.2 socket (2242, Socket for "B key"). Additional interfaces are 4x USB 2.0 and 2x COM, of which COM1 are designed as RS232 and COM2 as RS232 / 422/485. An absolute highlight is the soldered mass memory with up to 64GB eMMC Flash, as well as an I/O interface GPIO with 4 in & 4 out lines.

1.1 Features

- PC/104 Specification 2.6
- Very Ultra low power consumption (Around 6W)
- DMP Vortex86 DX3-9126 CPU Onboard (SOC)
- Supports the PC/104+ and PC/104 connector onboard
- DDR3L 1333 2GB Memory IC onboard (1.35V,256Mbitx16*4)
- VGA output with 2x8 pin header
- 18/24bit single channel LVDS connector with 2 x 15 pin header
- Dual LAN connector with 2x10 pin header (1 x GbE,1 x Fast Ethernet)
- 4xUSB 2.0,2xCOM Port (COM2 Port is RS-232/422/485, COM1 is RS232 Only)
- 1xSATA Port (1x7 Pin),1xM.2 Socket (2242 Only)
- 4GB eMMC Flash onboard (optional)
- 4 in & 4 out GPIO
- DC 5V Power input.
- -20~70 degrees Operating Temperature

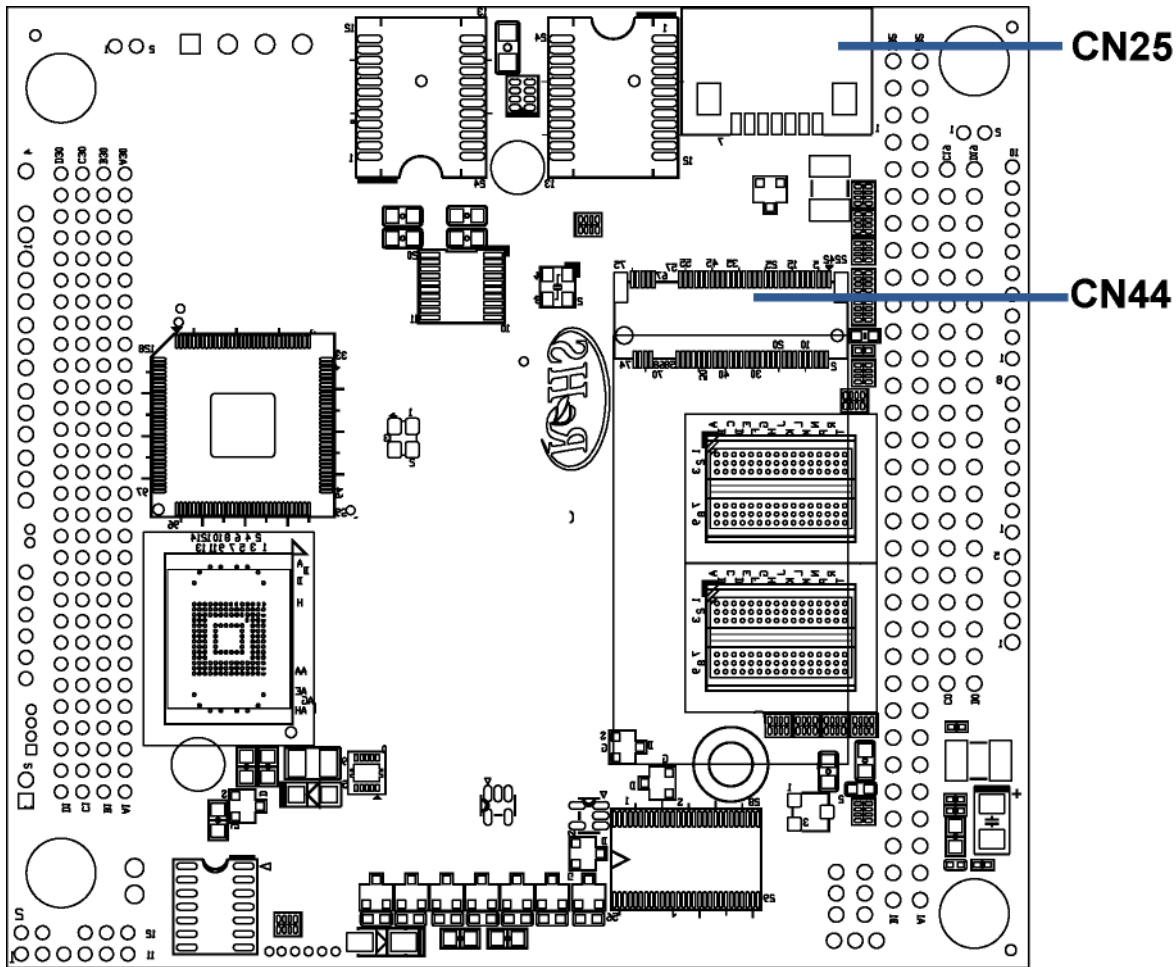
2. Hardware Briefing

2.1 Onboard Connectors



TOP View

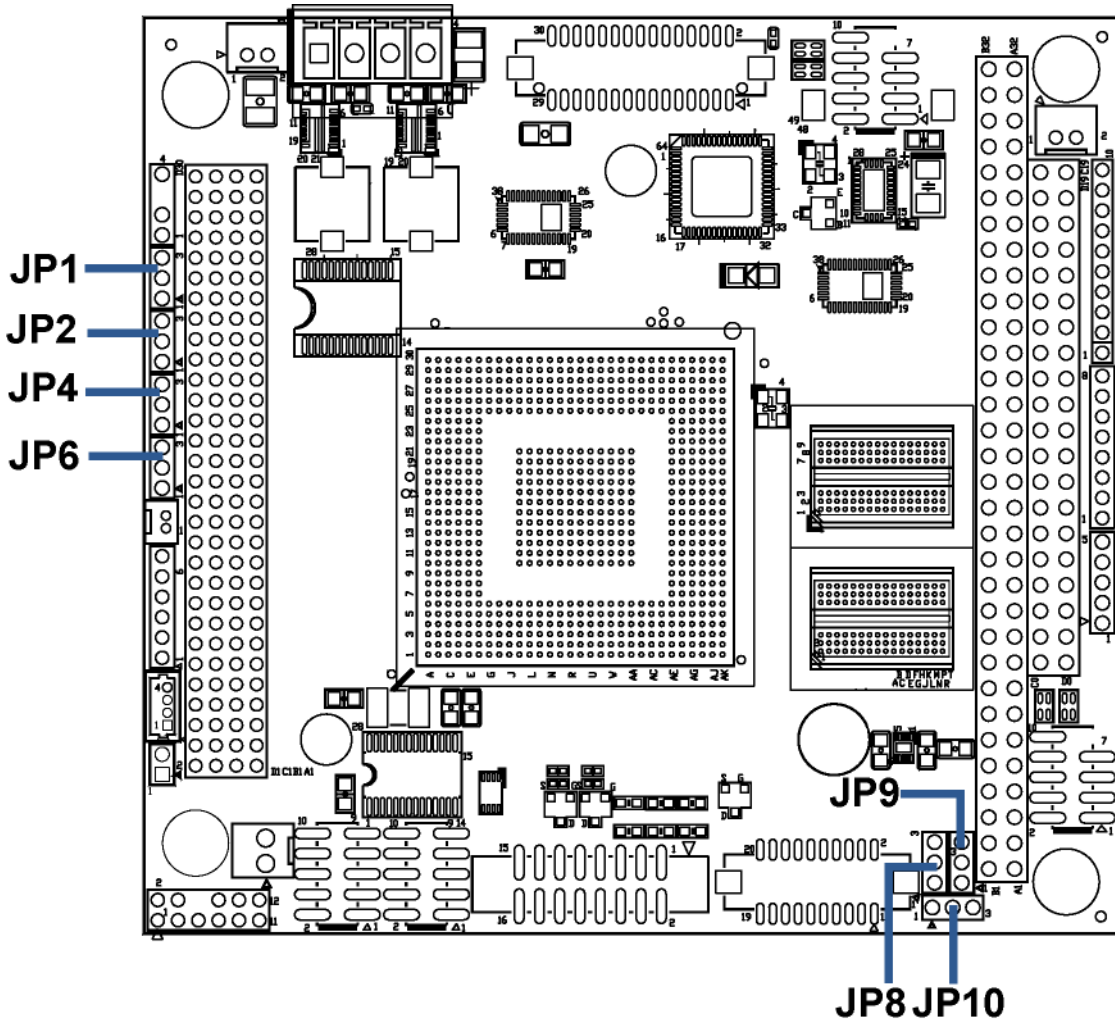
CN1	VGA Connector	CN2	LVDS CONNECTOR
CN3	+V5P0 CONNECTOR	CN4	+V 12 P0 CONNECTOR
CN5	LVDS BACKLIGHT CONNECTOR	CN6	+V5VP0_STBY CONNECTOR
CN7	ISA BUS CONNECTOR	CN8	PCI104 CONNECTOR
CN9	-5V &12V CONNECTOR	CN10	FRONT PANNEL CONNECTOR
CN11	N/A	CN12	FAN CONNECTOR
CN13	KB/MS CONNECTOR	CN14	GPIO CONNECTOR
CN15	BATTERY CONNECTOR	CN16	USB Pin header
CN17	USB Pin header	CN18	N/A
CN19	COM1 PINHEADER	CN20	COM2 PINHEADER
CN21	LAN1/2 PIN HEADER	CN22	N/A
CN23	POWER BUTTON	CN24	SATA POWER CONNECTOR
CN27	HDA PINHEADER	CN26	N/A



BOTTOM View

CN25	SATA CONNECTOR	CN44	M.2 CONNECTOR (2242 Only)
-------------	-----------------------	-------------	----------------------------------

2.2 Jumper Settings



JP1	LVDS VOLTAGE	JP1	PCI VOLTAGE
	1-2: +V3P3		1-2: +V5P0
	2-3: +V5P0 (Default)		2-3: +V3P3 (Default)

JP4	AT/ATX	JP6	Clear CMOS
	1-2: AT MODE		1-2: NORMAL (Default)
	2-3: ATX MODE (Default)		2-3: CLEAR CMOS

		GPIO74	JP9	JP8	
JP8	1-2: HIGH	0	0	0	RS422 Full Duplex
JP9	2-3: LOW	0	1	1	Pure RS232 (Default)
		0	1	0	RS485 DE#/RE Half Duplex
		0	1	1	RS485 DE#/RE Half Duplex
		1	X	X	Shutdown Mode

JP10

**1-2: HIGH
2-3: LOW**

JP10:

Slew rate control pin, Logical Low Input will limit driver slew from either RS-232 to 1Mbps or RS-485 to 10Mbps.

JP10=1-2 (Default)

RS232 = 1Mbps

RS422/RS485 = 10Mbps

JP10=2-3

RS232=250kbps

RS422/RS485=250kbps

3. Specifications

3.1 System

Form Factor	PC/104 Specification 2.6
Processor	DMP Vortex86 DX3-9126 CPU
Base Frequency	1.0 Ghz Processor
Turbo Boost Frequency	N/A
Core/Tread	2
Onboard L2 Cache	512KB
CPU TDP	6W TDP
Chipset	Integrated in SoC
BIOS	AMI 64Mbits SPI Flash

3.2 Memory

Technology	DDR3L 1333
ECC Support	N/A
Channel/Socket	Memory IC Onboard
Max. Capacity	2GB

3.3 Graphics Specifications

Controller	UMA architecture, VGA controller, 2D Graphics engine support
Base/Turbo Freq. (MHz)	N/A
Graphic Memory	N/A
HW Acceleration	N/A

3.4 Display

LVDS Output	Single channel with 18/24 bit LVDS output
Digital Display Interface (DDI)	N/A
Multiple Display	VGA+LVDS output

3.5 I/O Interface

PCIex1 Bus	N/A
SATA	1xSATA I Port(1.5Gb/sec)/ M.2 Socket (2242 only)
USB3.0	N/A
USB2.0	4xUSB 2.0
GPIO	4 in & 4 out
COM Port	2 x port
TPM	N/A
Smart Fan	N/A

3.6 Storage

Mass Storage	SMI 4GB eMMC Flash onboard(Optional)
--------------	--------------------------------------

3.7 Expansion Slot

PCIe x16	N/A
PCIe x1	N/A
Audio Interface	Reserved 2x6 pin connector
LPC Bus	N/A

3.8 Serial Bus

SMBus	Yes
I2C Bus	Yes

3.9 Ethernet

Ethernet	1 x integrated PHY (10/100 Mbit) 1 x Intel i211It (10/100/1000 Mbit)
----------	---

3.10 Power Requirement

Power Type	AT/ATX power mode by Jumper Setting
Supply Voltage	DC 5V Input with 1x4 pin phoenix contact connector
Power Consumption	approx~6 to 7W

3.11 Operating System

Operating Systems	DOS 6.22 and XPE (Standard support) WES7, Linux, QNX (by request)
-------------------	--

3.12 Mechanical & Environment

Temperature	-20~70 degrees Operating Temperature
Humidity	Operating: 10 - 90% r. H. non condition Storage: 5 - 95% r. H. non-condition.
Vibration Resistance	TBD
Dimensions	96 mm x 90 mm (LxW")

3.13 Packing contents

- USB cable x 1
- COM port cable x 1
- SATA cable x 1
- Audio cable x 1

3.14 Ordering Information

PB-VORTEX-DX3

DMP Vortex DX-3 SOC/2GB DDR3L/VGA/
LVDS/Dual LAN/4xUSB 2.0/2xCOM port/
SATA/M.2 Socket /DC 5V Input

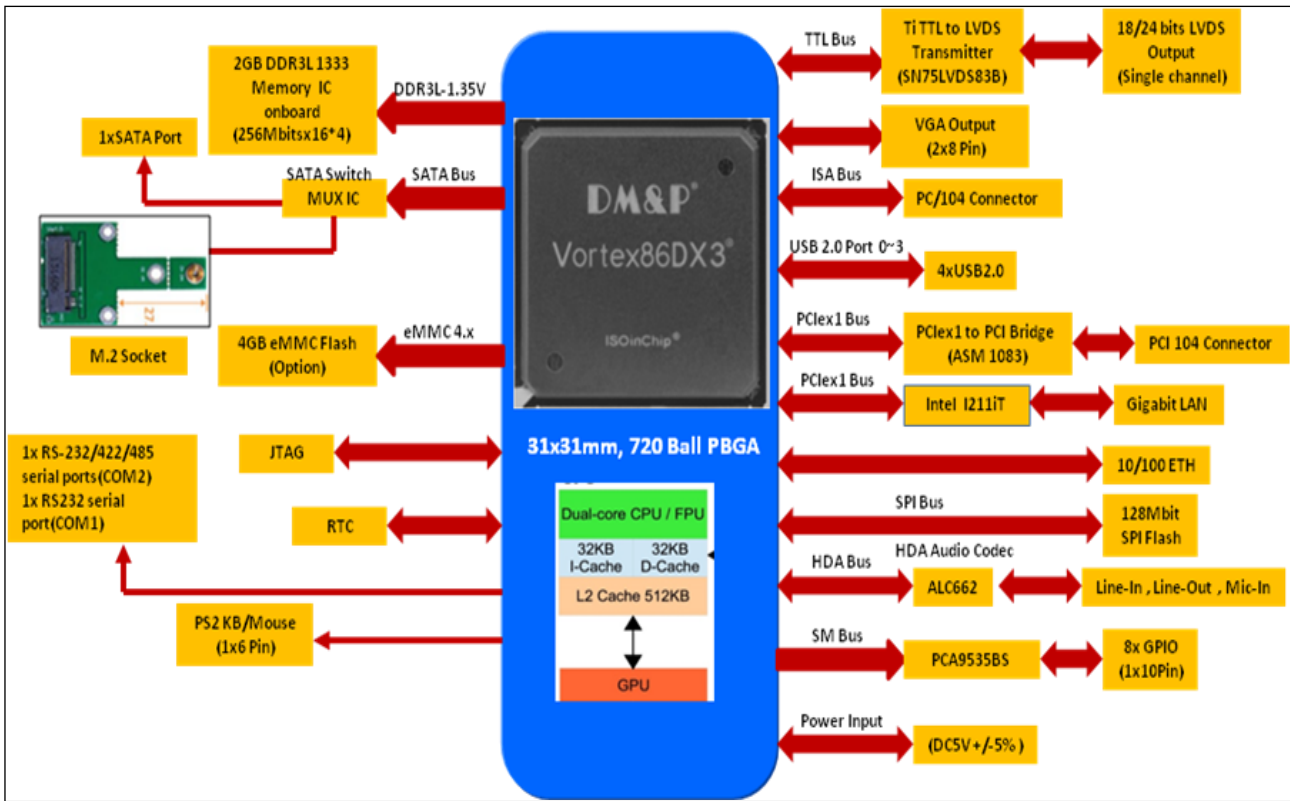
3.15 Regulatory Compliance



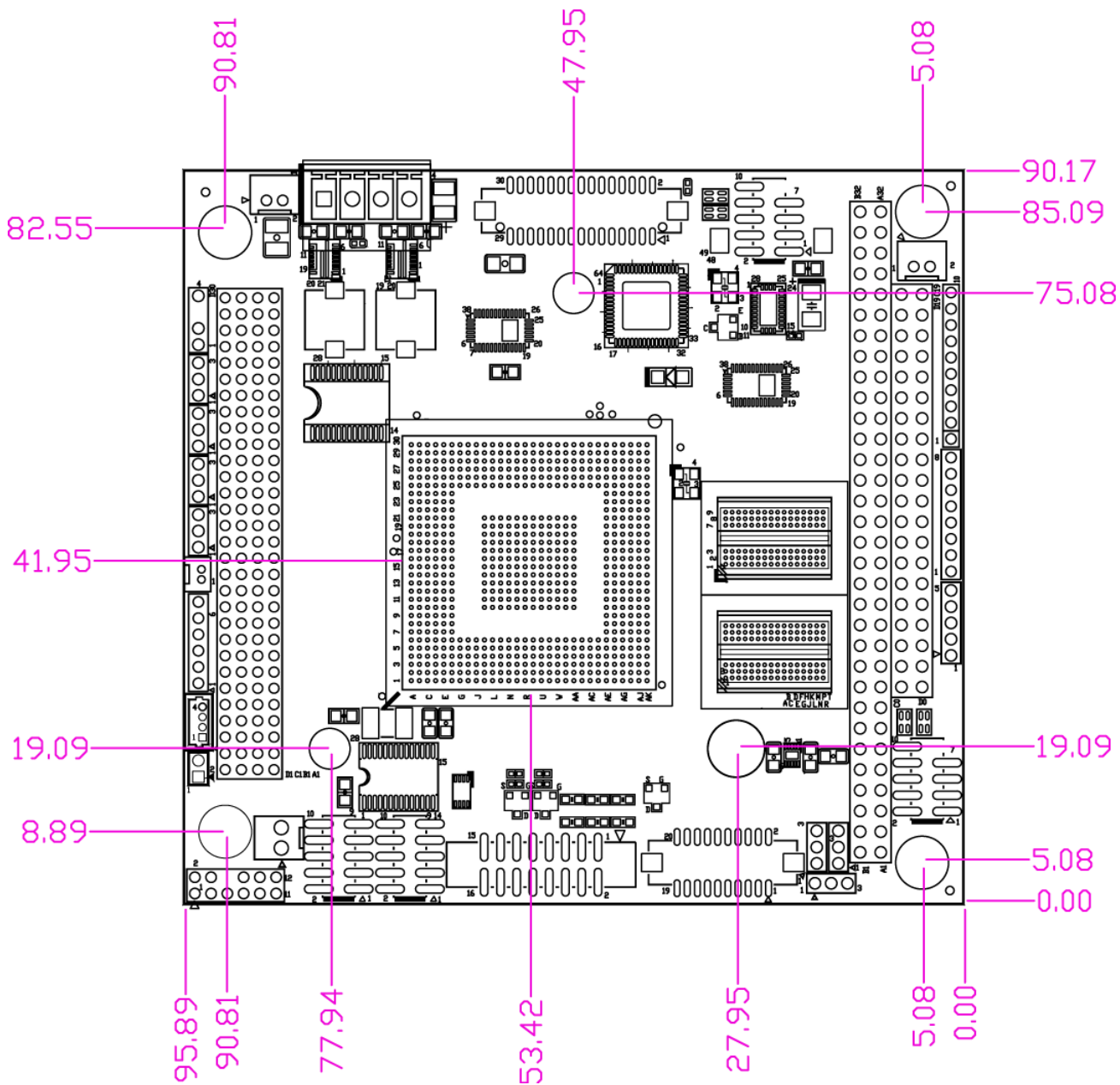
Hazardous substance-Free (RoHS) Compliant

This product is designed and developed on hazardous substance-free components and parts and totally RoHS (Restriction of Hazardous Substances Directive 2002/95/EC) compliant.

4. Functional Diagram



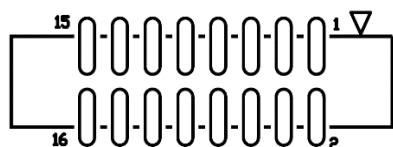
5. Mechanical Dimensions



Unit: mm

6. Pinout Definitions

6.1 CN1 CRT CONNECTOR



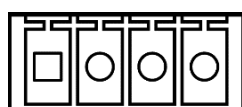
PIN	Description	PIN	Description
1	CRT_RED	2	CRT_GREEN
3	CRT_BLUE	4	+5VP0
5	GND	6	GND
7	GND	8	GND
9	+V_CRTCON	10	GND
11	V5P0	12	CRT_DDC_SDA
13	CCRT_HSYNC	14	CRT_VSYNC
15	CRT_DDC_SCL	16	N/C

6.2 CN2 LVDS CONNECTOR



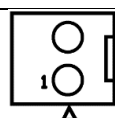
PIN	Description	PIN	Description
1	TX0+	2	TX0-
3	GND	4	GND
5	TX1+	6	TX1-
7	GND	8	VCC_LCD
9	TX2+	10	TX2-
11	LVDS_Clock+	12	LVDS_Clock-
13	GND	14	GND
15	N/C	16	N/C
17	Backlight enable	18	VCC_LCD
19	DDC_Data	20	DDC_Clock

6.3 CN3 +V5P0 CONNECTOR



PIN	Description	PIN	Description
1	+V5P0	2	+V5P0
3	GND	4	GND

6.4 CN4 12 volt DC-in



PIN	Description	PIN	Description
1	GND	2	+V12 P0

6.5

6.6 CN5 LVDS BACKLIGHT CONNECTOR



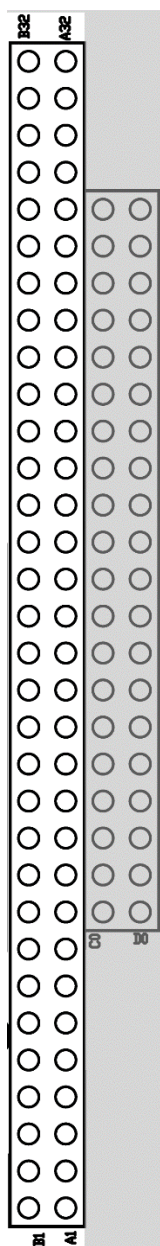
PIN	Description	PIN	Description
1	+12VP0	2	GND
3	LBKLT_EN_DELAY	4	LCD_BKB_CTRL
5	+5VP0		

6.7 CN6 +V5P0_STBY CONNECTOR



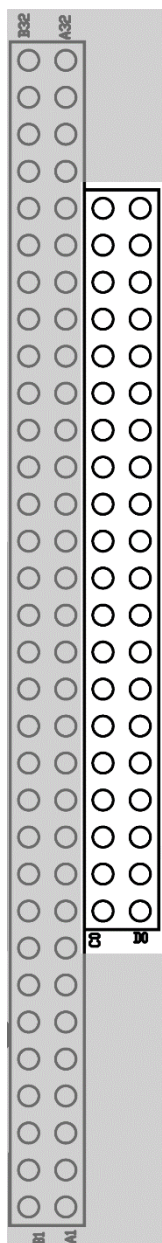
PIN	Description	PIN	Description
1	+V5P0_STBY	2	+V5P0_STBY
3	GND	4	PS_ON

6.8 CN7 ISA BUS CONNECTOR



XT Slot Connector

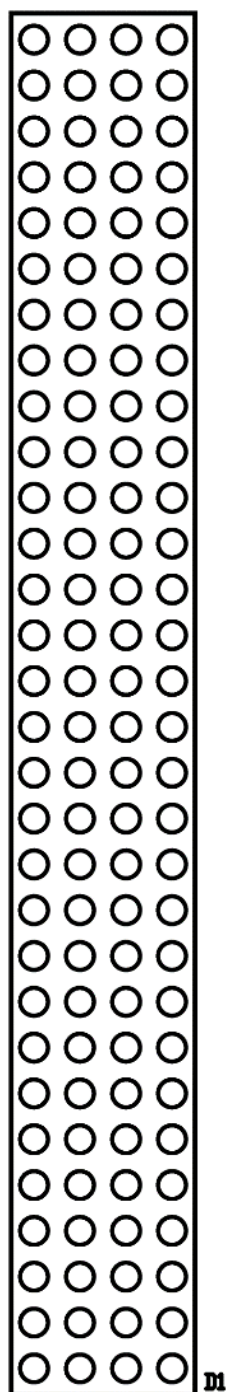
PIN	A	B
1	IOCHK#	GND
2	SD7	RSTDRV
3	SD6	+5V
4	SD5	IRQ9
5	SD4	-5V
6	SD3	DRQ2
7	SD2	-12V
8	SD1	OVS
9	SD0	+12V
10	IOCHRDY	(KEY2)
11	AEN	SMEMW#
12	SA19	SMEMR#
13	SA18	IOW#
14	SA17	IOR#
15	SA16	DACK3#
16	SA15	DRQ3
17	SA14	DACK1#
18	SA13	DRQ1
19	SA12	REFRESH#
20	SA11	SYSCLK
21	SA10	IRQ7
22	SA9	IRQ6
23	SA8	IRQ5
24	SA7	IRQ4
25	SA6	IRQ3
26	SA5	DACK2#
27	SA4	TC
28	SA3	BALE
29	SA2	+5V
30	SA1	OSC
31	SA0	GND
32	GND	GND



AT Slot Connector


PIN	C	D
0	GND	GND
1	SBHE#	MEMCS16#
2	LA23	IOCS16#
3	LA22	IRQ10
4	LA21	IRQ11
5	LA20	IRQ12
6	LA19	IRQ15
7	LA18	IRQ14
8	LA17	DACK0#
9	MEMR#	DRQ0
10	MEMW#	DACK5#
11	SD8	DRQ5
12	SD9	DACK6#
13	SD10	DRQ6
14	SD11	DACK7#
15	SD12	DRQ7
16	SD13	+5V
17	SD14	MASTER#
18	SD15	GND
19	(KEY2)	GND

6.9 CN8 PCI CONNECTOR

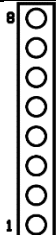


PIN	A	B	C	D
1	GND	Reserved	+5V	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0#	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1#	AD15	+3.3V
9	SERR#	GND	SBO#	PAR
10	GND	PERR#	+3.3V	SDONE
11	STOP#	+3.3V	LOCK#	GND
12	+3.3V	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	+3.3V
14	GND	AD16	+3.3V	C/BE2#
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0#	GND	REQ1#	VI/O
24	GND	REQ2#	+5V	GNT0*
25	GNT1#	VI/O	GNT2#	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD#	+5V	RST#
29	+12V	INTA#	INTB#	INTC#
30	-12V	REQ3#	GNT3#	GND

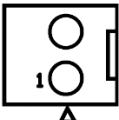
6.10 CN9 5V &12V CONNECTOR

	PIN	Description	PIN	Description
	1	-V5P0	2	GND
	3	N/C	4	-V12P0


6.11 CN10 FRONT PANNEL CONNECTOR

	PIN	Description	PIN	Description
	1	PWR_LED_N	2	GND
	3	HDD_LED_N	4	N/C
	5	SYS_PWRGD	6	GND
	7	SPKR_PU	8	BEEP_SPKR_R_N

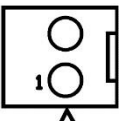
6.12 CN12 FAN CONNECTOR

	PIN	Description	PIN	Description
	1	GND	2	+V5P0

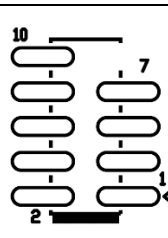
6.13 CN14 GPIO CONNECTOR

	PIN	Description	PIN	Description
	1	+V3P3	2	GPO0
	3	GPO1	4	GPO2
	5	GPO3	6	GPI0
	7	GPI1	8	GPI2
	9	GPI3	10	GND

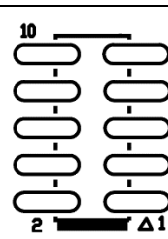
6.14 CN15 BATTERY CONNECTOR

	PIN	Description	PIN	Description
	1	+BATTERY	2	GND

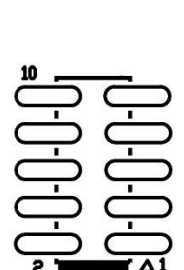
6.15 CN16/CN17 USB2.0 PIN HEADER

		PIN	Description	PIN	Description
1	VCC	2	VCC		
3	USB_PN	4	USB_PN		
5	USB_PP	6	USB_PP		
7	GND	8	GND		
9	N/C	10	GND		

6.16 CN19/CN20 COM1/COM2 PINHEADER

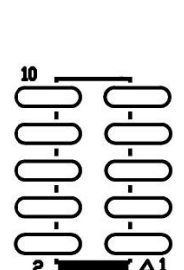
		PIN	Description	PIN	Description
1	DCD_N_CON	2	DSR_N_CON		
3	SIN_CON	4	RTS_N_CON		
5	SOUT_CON	6	CTS_N_CON		
7	DTR_N_CON	8	RI_N_CON		
9	GND	10	N.C		

6.17 CN20 COM2 PINHEADER(RS232)

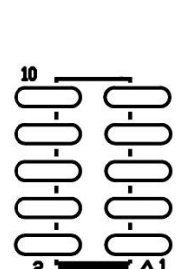
		PIN	Description	PIN	Description
1	DCD_N_CON	2	DSR_N_CON		
3	SIN_CON	4	RTS_N_CON		
5	SOUT_CON	6	CTS_N_CON		
7	DTR_N_CON	8	RI_N_CON		
9	GND	10	N.C		

6.18

6.19 CN20 COM2 PINHEADER(RS422)

		PIN	Description	PIN	Description
1	TX-	2	N.C		
3	TX+	4	N.C		
5	RX+	6	N.C		
7	RX-	8	N.C		
9	GND	10	N.C		

6.20 CN20 COM2 PINHEADER(RS485)

		PIN	Description	PIN	Description
1	DATA-	2	N.C		
3	DATA+	4	N.C		
5	N.C	6	N.C		
7	N.C	8	N.C		
9	GND	10	N.C		

6.21 CN21 LAN1/2 PIN HEADER



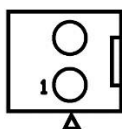
PIN	Description	PIN	Description
1	LAN1_L_MDIP2	2	LAN1_L_MDIPO
3	LAN1_L_MDIN2	4	LAN1_L_MDINO
5	LAN1_L_MDIP3	6	LAN1_L_MDIP1
7	LAN1_L_MDIN3	8	LAN1_L_MDIN1
9	+V3P3	10	GND
11	LAN1_ACT_N_R	12	LAN1_LINK_N
13	LAN1_LINK100_N_R	14	LAN1_LINK1000_N
15	GND	16	GND
17	LAN2_L_MDIPO	18	LAN2_L_MDI2
19	LAN2_L_MDINO	20	LAN2_L_MDI2
21	LAN2_L_MDIP1	22	LAN2_L_MDI3
23	LAN2_L_MDIN1	24	LAN2_L_MDI3
25	LAN2_ACT_N_R	26	LAN2_LINK_N
27	LAN2_LINK100_N	28	N.C
29	GND	30	GND

6.22 CN23 POWER BUTTON



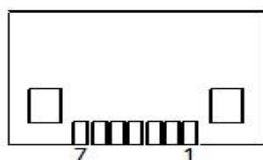
PIN	Description	PIN	Description
1	GND	2	PWR_BUTTON

6.23 CN24 SATA POWER CONNECTOR



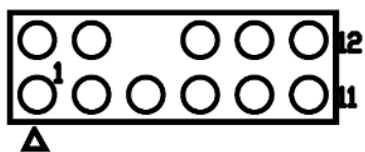
PIN	Description	PIN	Description
1	GND	2	+V5P0

6.24 CN25 SATA CONNECTOR



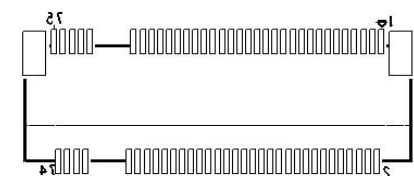
PIN	Description	PIN	Description
1	GND	2	SATA_TX_P
3	SATA_TX_N	4	GND
5	SATA_RX_N	6	SATA_RX_P
7	GND	GND1	GND
GND2	GND		

6.25 CN27 HDA PINHEADER



PIN	Description	PIN	Description
1	+V5P0	2	GND
3	GND	4	HD_BCLK
5	+V3P3	6	N.C
7	HDA_SDIN0	8	HDA_SYNC
9	GND	10	HDA_RST#
11	HDA_SDOUT	12	HDA_SDI

6.26 CN44 M.2 CONNECTOR



PIN	Description	PIN	Description
1	GND	2	+V3P3
3	GND	4	+V3P3
5	N.C	6	
7	N.C	8	
9	GND	10	
11	N.C	12	+V3P3
13	N.C	14	+V3P3
15	GND	16	+V3P3
17	N.C	18	+V3P3
19	N.C	20	N.C
21	GND	22	N.C
23	N.C	24	N.C
25	N.C	26	N.C
27	GND	28	N.C
29	N.C	30	N.C
31	N.C	32	N.C
33	GND	34	N.C
35	N.C	36	N.C
37	N.C	38	N.C
39	GND	40	N.C
41	SATA_RXP	42	N.C
43	SATA_RXN	44	N.C
45	GND	46	N.C
47	SATA_TXN	48	N.C
49	SATA_TXP	50	PERST#
51	GND	52	CLKRQ#_V3
53	N.C	54	N.C
55	N.C	56	N.C
57	GND	58	N.C
59	N.C	60	N.C
61	N.C	62	N.C
63	N.C	64	N.C
65	N.C	66	N.C
67	N.C	68	N.C
69	N.C	70	+V3P3
71	GND	72	+V3P3
73	GND	74	+V3P3
75	GND		

7. BIOS Setup

Follow steps below to enter the BIOS setup utility:

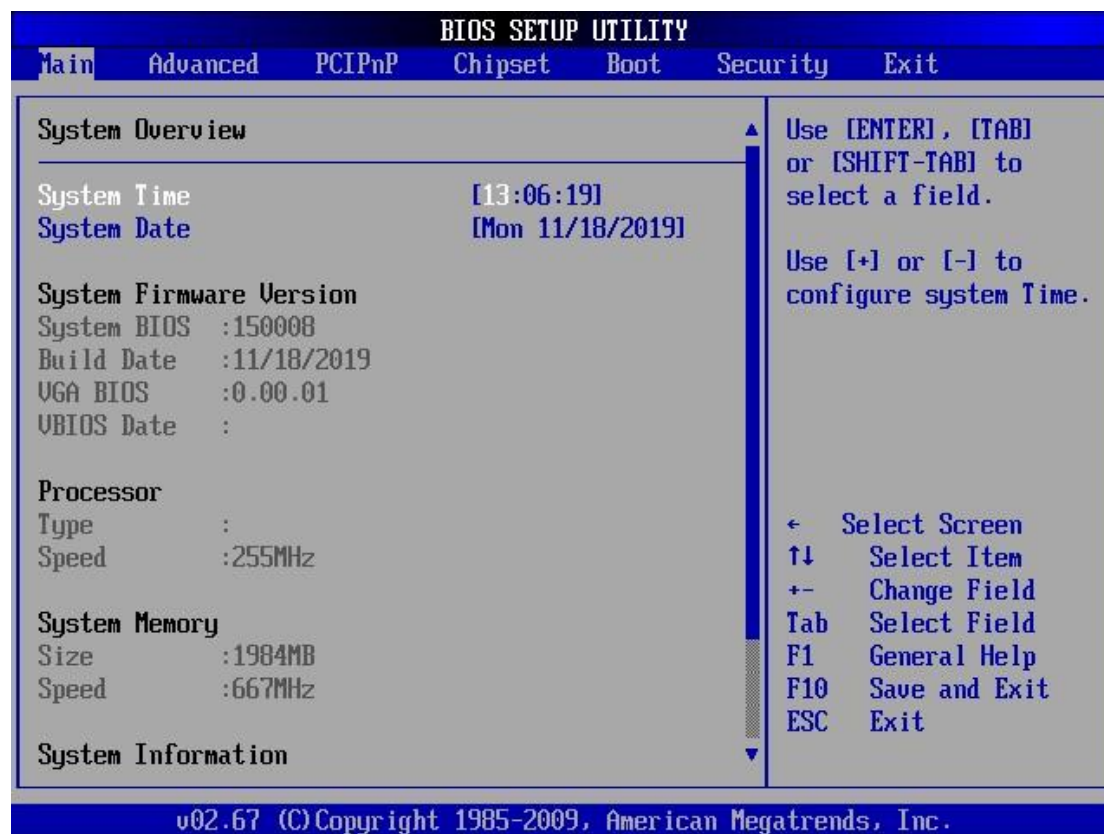
1. Connect a computer keyboard and Display to the device.
2. Power on the device.
3. Press the <Delete> key during the boot-up.
4. Then the BIOS main screen shows.

Operation instructions:

- ★ Arrow key [←] [→]: Navigate through setup screens, e.g. [Main], [Advanced], [Chipset], [Boot], [Security], [Save & Exit] and [Server Mgmt]
- ★ Arrow key [↑] [↓]: Highlight an item/option on a setup screen
- ★ [Enter]: select the highlighted item/option or enter the sub-menu under the highlighted item/option
- ★ [ESC]: exit the current screen
- ★ [+]/[-] = to adjust values for the selected setup item/option

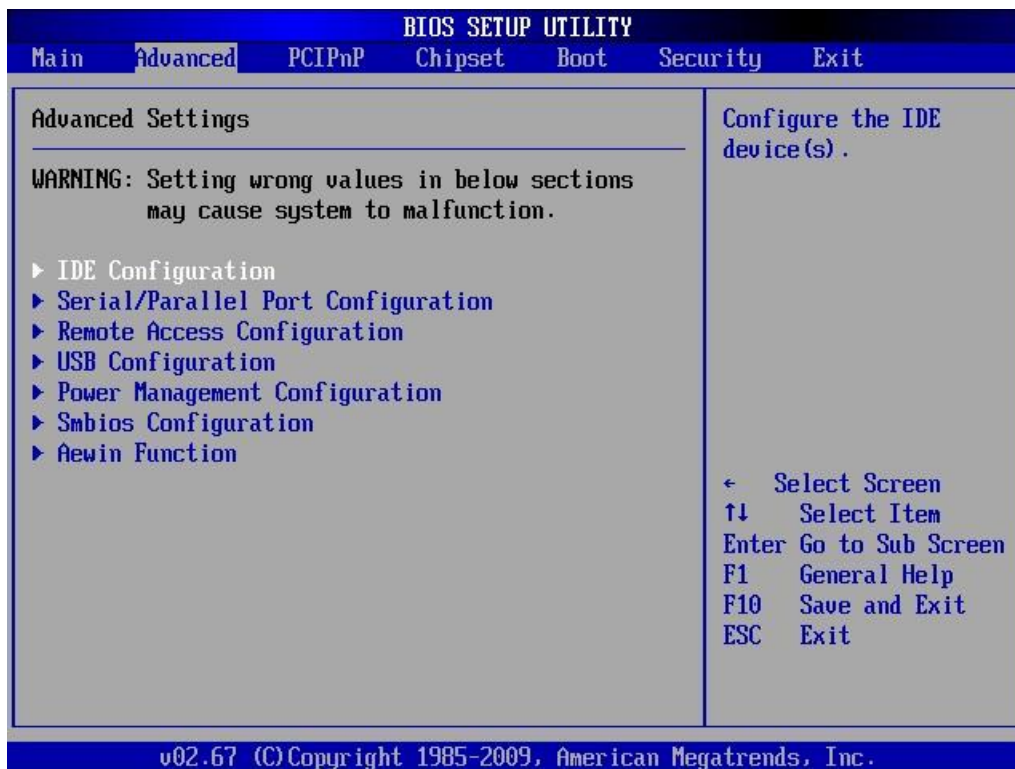
The following sections describe the BIOS setup. BIOS settings of this module can be viewed and set via BIOS settings. It is strongly recommended that only users with profound experiences are allowed to change the default BIOS settings.

7.1 Main



Feature	Options	Description
System Overview		
System Time	HH/MM/SS	
Weekday, System Date	MM/DD/YYYY	Requires the alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Weekday, MM/DD/YYYY)
System Firmware Version		
System BIOS	150008	
Build Date	11/18/2019	
VGA BIOS	0.00.01	
Processor		
Type		Information only
Speed		Information only
System Memory		
Size		Information only
Speed		Information only
System Information		

7.2 Advanced



	Option
Advanced	IDE Configuration
	Serial/Parallel Port Configuration
	Remote Access Configuration
	USB Configuration
	Power Management Configuration
	Smbios Configuration
	Aewin Function

7.2.1 IDE Configuration

BIOS SETUP UTILITY	
Advanced	
IDE Configuration	
OnBoard PCI IDE Controller	[Both]
▶ Primary IDE Master	: [Hard Disk]
▶ Primary IDE Slave	: [Not Detected]
▶ Secondary IDE Master	: [Not Detected]
▶ Secondary IDE Slave	: [Not Detected]
Hard Disk Write Protect	[Disabled]
IDE Detect Time Out (Sec)	[35]
ATA (PI) 80Pin Cable Detection	[Host & Device]
Hard Disk Delay	[Disabled]
OnBoard IDE Operate Mode	[Legacy Model]
Not Program PIO mode	[Disabled]
Primary IDE Pin Select	[SD Card]
SATA PHY Speed	[Auto]

DISABLED: disables the integrated IDE Controller.
 PRIMARY: enables only the Primary IDE Controller.
 SECONDARY: enables only the Secondary IDE Controller.
 BOTH: enables both IDE Controllers.

← Select Screen
 ↑↓ Select Item
 +- Change Option
 F1 General Help
 F10 Save and Exit
 ESC Exit

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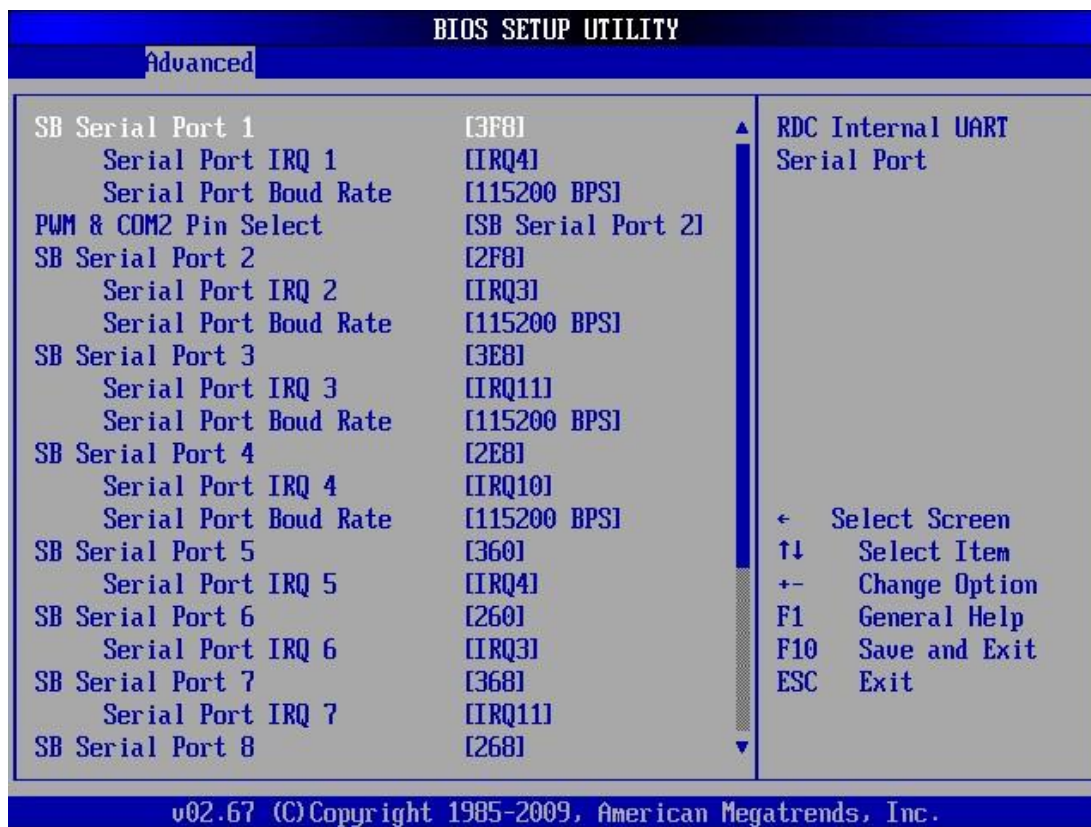
Feature	Options
	Not Installed
	Auto
Type	CD/DVD
	ARMED
LBA/Large Mode	Disabled
	Auto
Block (Multi-Sector Transfer)	Disabled
	Auto
	Auto
	0
PIO Mode	640x480
	24bit(800x600)
	18bit(800x600)
	4
	Auto
	SWAMA0
	SWAMA1
	SWAMA2
	MWAMA0
DMA Mode	MWAMA1
	MWAMA2
	UDMA0
	UDMA1
	UDMA2
	UDMA3

IDE Configuration Primary IDE Master

Feature		Options
		UDMA4
		UDMA5
		UDMA6
	S.M.A.R.T	Auto
		Disabled
		Enabled
	32Bit Data Transfer	Disabled
		Enabled
Primary IDE Slave		Not Installed
	Type	Auto
		CD/DVD
		ARMD
	LBA/Large Mode	Disabled
		Auto
	Block (Multi-Sector Transfer)	Disabled
		Auto
		Auto
		0
	PIO Mode	640x480
		24bit(800x600)
		18bit(800x600)
	4	
	DMA Mode	Auto
	S.M.A.R.T	Auto
		Disabled
		Enabled
	32Bit Data Transfer	Disabled
		Enabled
Secondary IDE Master		Not Installed
	Type	Auto
		CD/DVD
		ARMD
	LBA/Large Mode	Disabled
		Auto
	Block (Multi-Sector Transfer)	Disabled
		Auto
		Auto
		0
	PIO Mode	640x480
		24bit(800x600)
		18bit(800x600)
	4	
	DMA Mode	Auto
	S.M.A.R.T	Auto
		Disabled
		Enabled
	32Bit Data Transfer	Disabled
		Enabled
Secondary IDE Slave		Not Installed
	Type	Auto
		CD/DVD
		ARMD
	LBA/Large Mode	Disabled
		Auto
Block (Multi-Sector Transfer)	Disabled	
	Auto	
	Auto	
	PIO Mode	0
		640x480

Feature	Options
	24bit(800x600)
	18bit(800x600)
	4
	DMA Mode
	Auto
	Auto
	S.M.A.R.T
	Disabled
	Enabled
	32Bit Data Transfer
	Disabled
	Enabled
Hard Disk Write Protect	Disabled
	Enabled
	0
	5
	10
	15
IDE Detect Time Out (Sec)	20
	25
	30
	35
	Host & Device
ATA (PI) 80Pin Cable Detection	Host
	Device
	Disabled
	1 Second
Hard Disk Delay	2 Second
	4 Second
	8 Second
	Legacy Mode
OnBoard IDE Operate Mode	Native Mode
	Disabled
Not Program PIO mode	Primary Channel
	Secondary Channel
	Parallel IDE
Primary IDE Pin Select	SD Card
	Gen 1 Only
SATA PHY Speed	Auto

7.2.2 Serial/Parallel Port Configuration



Feature	Options
	Disabled
	3F8
	2F8
	3E8
	2E8
SB Serial Port1	360
	260
	368
	268
	3E0
	2E0
	IRQ3
	IRQ4
	IRQ5
	IRQ6
	IRQ7
Serial Port IRQ 1	IRQ8
	IRQ9
	IRQ10
	IRQ11
	IRQ12
	IRQ13
	IRQ14

	IRQ15
	2400BPS
	4800BPS
	9600BPS
Serial Port Boud Rate	19200BPS
	38400BPS
	57600BPS
	115200BPS
PWM & COM2 Pin Select	SB Serial Port 2
	8254 PWM
	Disabled
	3F8
	2F8
	3E8
	2E8
SB Serial Port2	360
	260
	368
	268
	3E0
	2E0
	IRQ3
	IRQ4
	IRQ5
	IRQ6
	IRQ7
	IRQ8
Serial Port IRQ 2	IRQ9
	IRQ10
	IRQ11
	IRQ12
	IRQ13
	IRQ14
	IRQ15
	2400BPS
	4800BPS
	9600BPS
Serial Port Boud Rate	19200BPS
	38400BPS
	57600BPS
	115200BPS
	Disabled
	3F8
	2F8
	3E8
SB Serial Port3	2E8
	360
	260
	368
	268

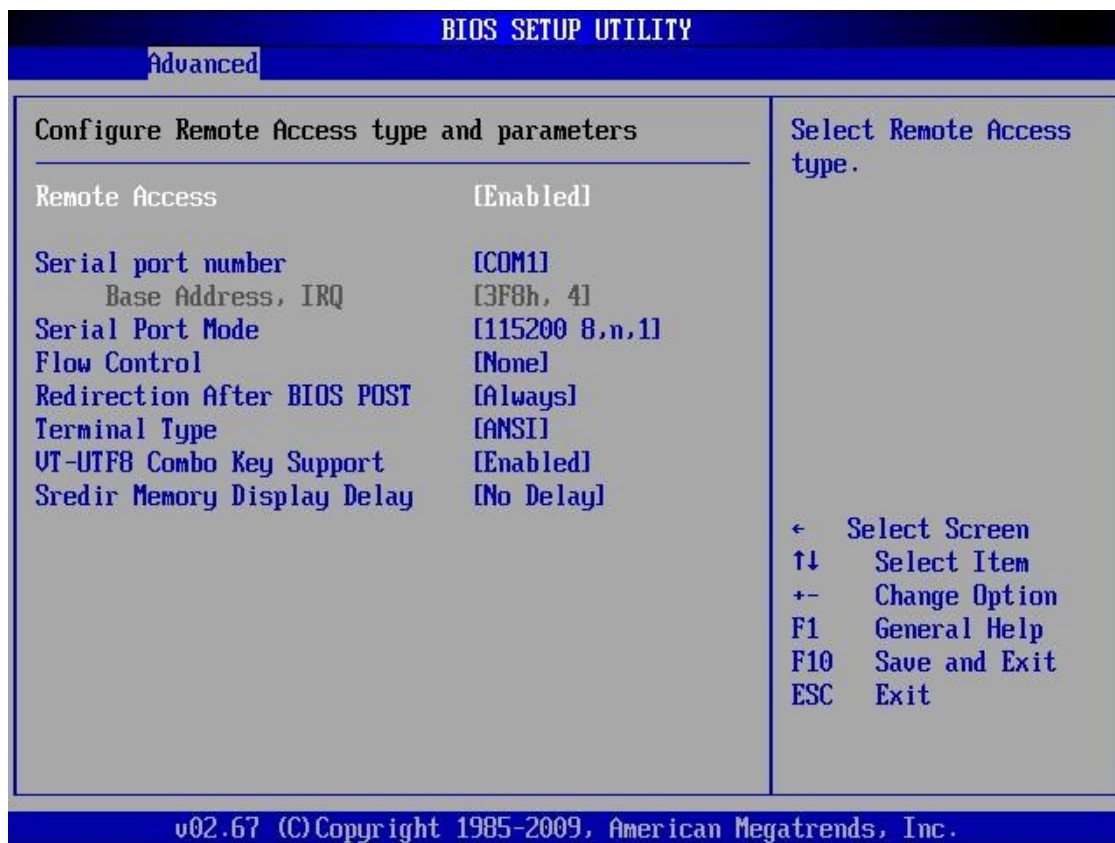
	3E0
	2E0
Serial Port IRQ 3	IRQ3
	IRQ4
	IRQ5
	IRQ6
	IRQ7
	IRQ8
	IRQ9
	IRQ10
	IRQ11
	IRQ12
	IRQ13
	IRQ14
	IRQ15
	Serial Port Boud Rate
4800BPS	
9600BPS	
19200BPS	
38400BPS	
57600BPS	
115200BPS	
SB Serial Port4	Disabled
	3F8
	2F8
	3E8
	2E8
	360
	260
	368
	268
	3E0
	2E0
Serial Port IRQ 4	IRQ3
	IRQ4
	IRQ5
	IRQ6
	IRQ7
	IRQ8
	IRQ9
	IRQ10
	IRQ11
	IRQ12
	IRQ13
	IRQ14
	IRQ15
	Serial Port Boud Rate
4800BPS	
9600BPS	
19200BPS	

	38400BPS
	57600BPS
	115200BPS
SB Serial Port5	Disabled
	3F8
	2F8
	3E8
	2E8
	360
	260
	368
	268
	3E0
	2E0
Serial Port IRQ 5	IRQ3
	IRQ4
	IRQ5
	IRQ6
	IRQ7
	IRQ8
	IRQ9
	IRQ10
	IRQ11
	IRQ12
	IRQ13
Serial Port Boud Rate	2400BPS
	4800BPS
	9600BPS
	19200BPS
	38400BPS
	57600BPS
	115200BPS
SB Serial Port6	Disabled
	3F8
	2F8
	3E8
	2E8
	360
	260
	368
	268
	3E0
	2E0
Serial Port IRQ 6	IRQ3
	IRQ4
	IRQ5
	IRQ6
	IRQ7

	IRQ8
	IRQ9
	IRQ10
	IRQ11
	IRQ12
	IRQ13
	IRQ14
	IRQ15
Serial Port Boud Rate	2400BPS
	4800BPS
	9600BPS
	19200BPS
	38400BPS
	57600BPS
	115200BPS
SB Serial Port7	Disabled
	3F8
	2F8
	3E8
	2E8
	360
	260
	368
	268
	3E0
2E0	
Serial Port IRQ 7	IRQ3
	IRQ4
	IRQ5
	IRQ6
	IRQ7
	IRQ8
	IRQ9
	IRQ10
	IRQ11
	IRQ12
	IRQ13
IRQ14	
IRQ15	
Serial Port Boud Rate	2400BPS
	4800BPS
	9600BPS
	19200BPS
	38400BPS
	57600BPS
115200BPS	
SB Serial Port8	Disabled
	3F8
	2F8
	3E8

	2E8	
	360	
	260	
	368	
	268	
	3E0	
	2E0	
Serial Port IRQ 8	IRQ3	
	IRQ4	
	IRQ5	
	IRQ6	
	IRQ7	
	IRQ8	
	IRQ9	
	IRQ10	
	IRQ11	
	IRQ12	
	IRQ13	
	IRQ14	
	IRQ15	
	Serial Port Boud Rate	2400BPS
		4800BPS
9600BPS		
19200BPS		
38400BPS		
57600BPS		
115200BPS		
SB Parallel Port Address	37B	
	27B	
Parallel Port Mode	BPP	
	EPP 1.9 AND SPP	
	ECP	
	ECP AND EPP 1.9	
	SPP	
	EPP 1.7 and SPP	
	ECP AND EPP 1.7	
EPP Version	1.7	
	1.9	
ECP Mode DMA Channel	DMA0	
	DMA1	
	DMA3	
Parallel Port IRQ	IRQ5	
	IRQ7	

7.2.3 Remote Access Configuration



Remote Access Configuration	Remote Access	Disabled
		Enabled
	Serial Port number	COM1
	Base Address, IRQ	115200, 8, n, 1
		57600, 8, n, 1
		38400, 8, n, 1
		19200, 8, n, 1
		09600, 8, n, 1
	Flow Control	None
		Hardware
		Software
	Redirection after BIOS Post	Disabled
		Boot Loader
		Always
Terminal Type	ANSI	
	VT100	
	VT-UTF8	
VT-UTF8 Combo Key Support	Disabled	
	Enabled	
Sredir Memory Display Delay	No Delay	
	Delay 1 Sec	
	Delay 2 Sec	
	Delay 3 Sec	

7.2.4. USB Configuration

USB Configuration	USB Support	Disabled
		Enabled
	Legacy USB Support	Disabled
		Enabled
		Auto
	USB 2.0 Control Mode	Fullspeed
		HighSpeed
	BIOS EHCI Hand-off	Disabled
		Enabled
	USB Beep Message	Disabled
		Enabled
	Support USB Device Wakeup	Disabled
		Enabled
	USB Storage Device Reset Delay	10 Sec
20 Sec		
30 Sec		
40 Sec		
Emulation Type	Auto	
	Floppy	
	Forced FDD	
	Hard Disk	
	CDROM	

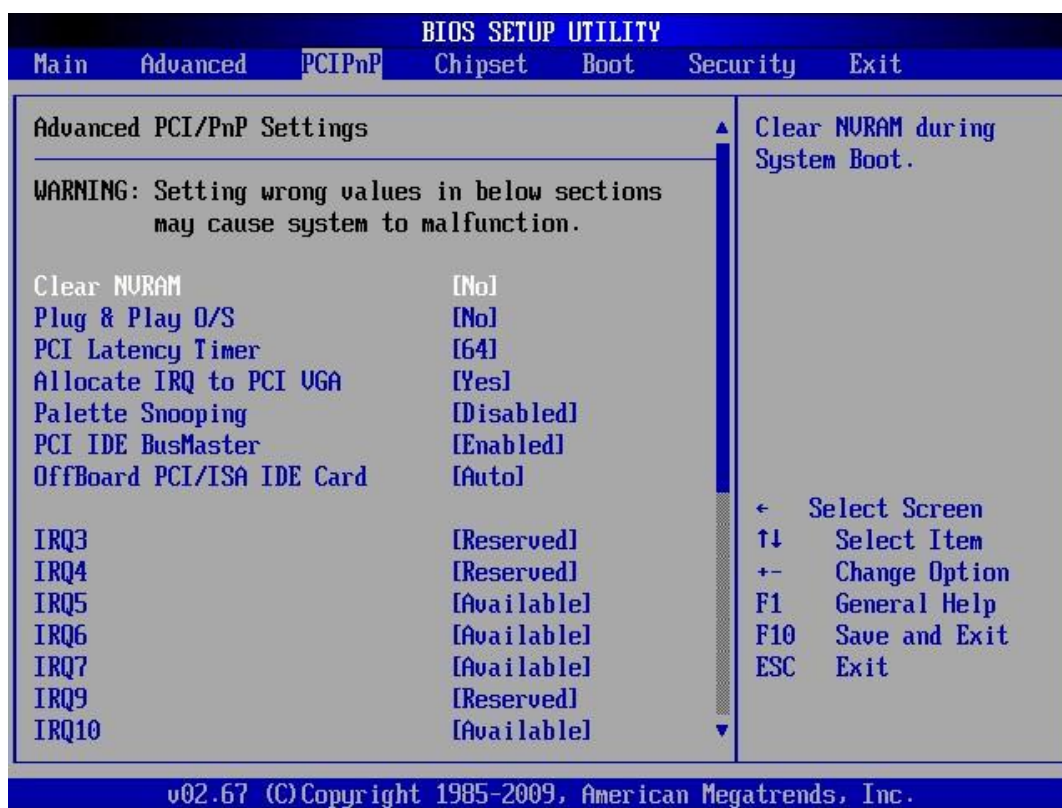
7.2.5. Smbios Configuration

Smbios Configuration	Disabled
	Enabled

7.2.6. Aewin Functions

Aewin Functions	SATA Selection	M.2
		SATA
	Combo Switch	RS-232
		RS-422
		RS-485

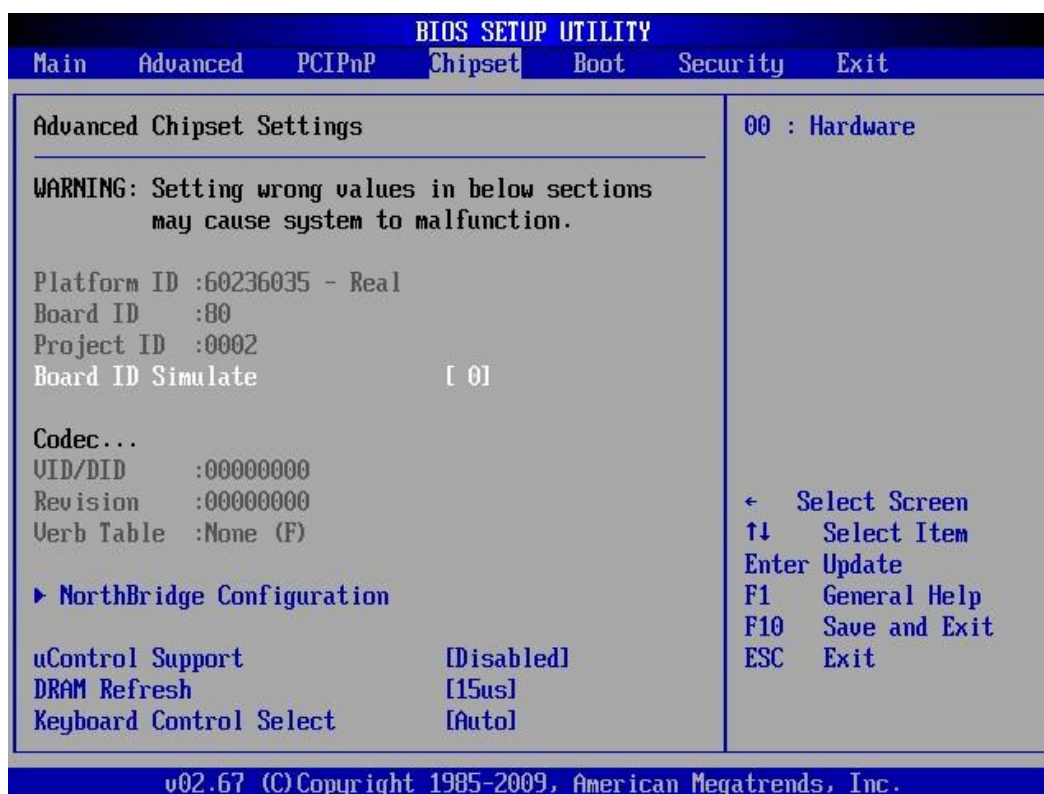
7.3 PCIPnP



Feature	Options
Clear NURAM	No
	Yes
Plug & Play O/S	No
	Yes
PCI Latency Timer	32
	64
	96
	128
	160
	192
	224
	248
Allocate IRQ to PCI VGA	Yes
	No
Palette Snooping	Disabled
	Enabled
PCI IDE BusMaster	Disabled
	Enabled
OffBoard PCI/ISA IDE Card	Auto
	PCI Slot1
	PCI Slot2
	PCI Slot3
	PCI Slot4

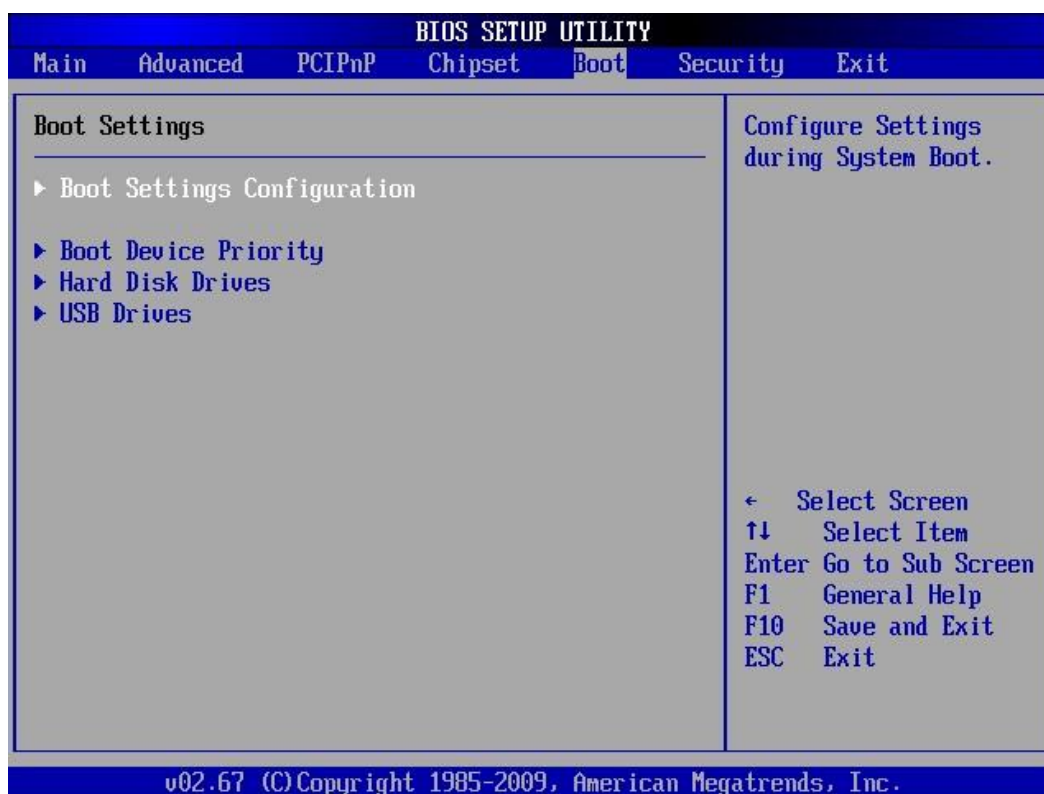
Feature	Options
	PCI Slot5
	PCI Slot6
IRQ3	Available
	Reserved
IRQ4	Available
	Reserved
IRQ5	Available
	Reserved
IRQ6	Available
	Reserved
IRQ7	Available
	Reserved
IRQ9	Available
	Reserved
IRQ10	Available
	Reserved
IRQ11	Available
	Reserved
IRQ12	Available
	Reserved
IRQ14	Available
	Reserved
IRQ15	Available
	Reserved
DMA Channel 0	Available
	Reserved
DMA Channel 1	Available
	Reserved
DMA Channel 3	Available
	Reserved
DMA Channel 5	Available
	Reserved
DMA Channel 6	Available
	Reserved
DMA Channel 7	Available
	Reserved
Reserved Memory Size	Disabled
	Enabled

7.4 Chipset



Feature	Options
Board ID Simulate	VBIOS
	640x480
NorthBridge Configuration	24bit(800x600)
	18bit(800x600)
	NB Function 0 Register 51
	Disabled
uControl Support	Mode 1
	Mode 2
DRAM Refresh	7.8uS
	15uS
Keyboard Control Select	Internal KBC
	External KBC
	Auto

7.5 Boot



Feature

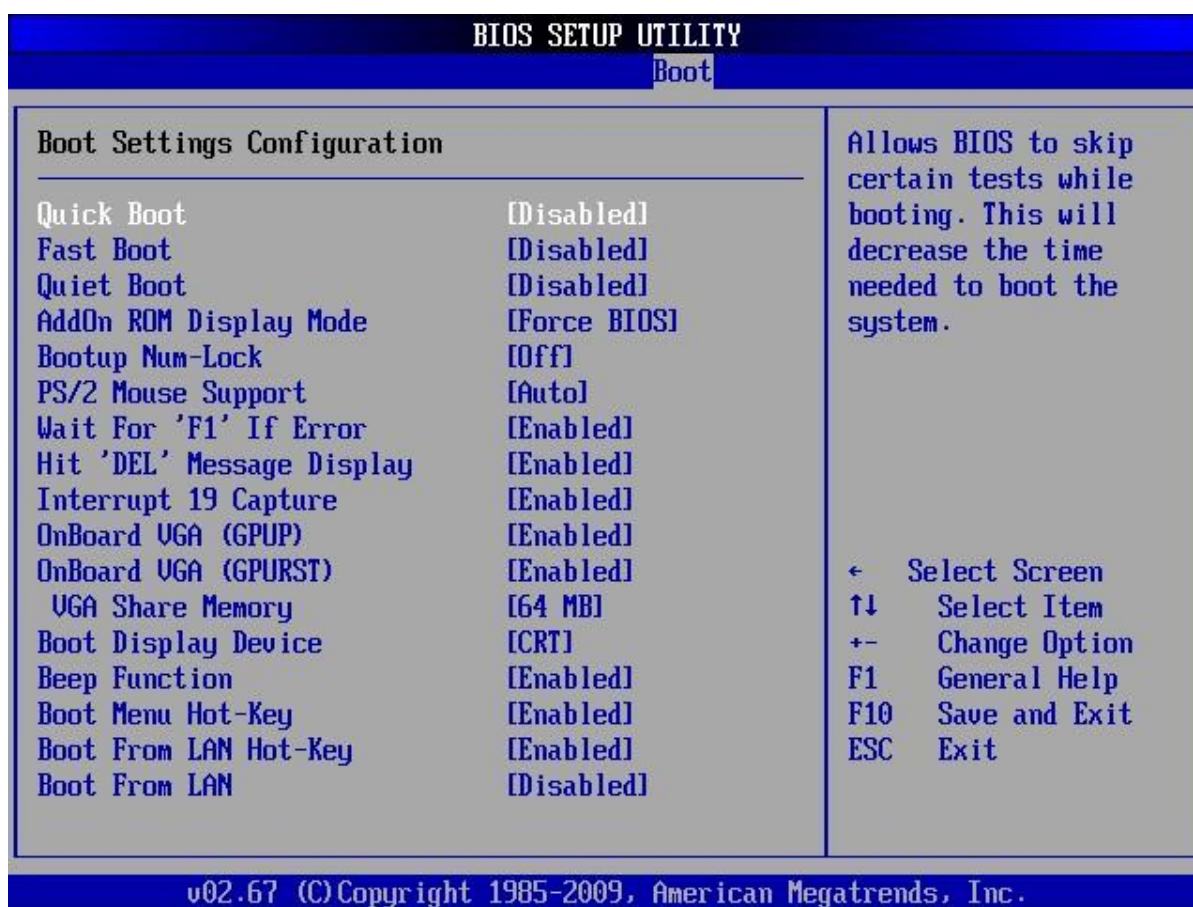
Boot Settings Configuration

Boot Device Priority

Hard Disk Drives

USB Drives

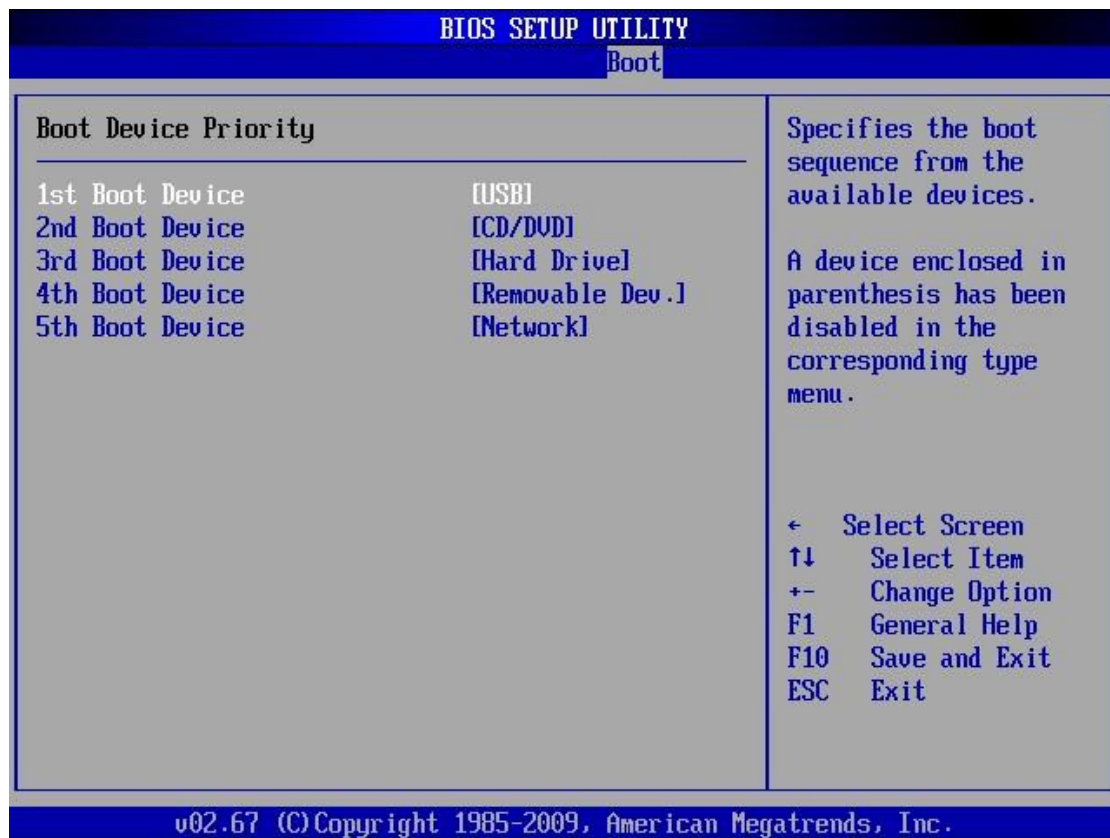
7.5.1 Boot Settings Configuration



Feature	Options	
Boot Setting Configuration	Quick Boot	Disabled
		Enabled
	Fast Boot	Disabled
		Enhanced 1
		Enhanced 2
	Quiet Boot	Disabled
		Enabled
	AddOn ROM Display Mode	Force BIOS
		Keep Current
	Bootup Num-Lock	Off
		On
	PS/2 Mouse Support	Disabled
		Enabled
Auto		
Wait For 'F1' If Error	Disabled	
	Enabled	
Hit 'DEL' Message Display	Disabled	
	Enabled	
Interrupt 19 Capture	Disabled	
	Enabled	
OnBoard VGA (GRUP)	Disabled	

	Enabled
OnBoard VGA (GRURST)	Disabled
	Enabled
VGA Share Memory	16MB
	32 MB
	64 MB
	128 MB
	256 MB
	512 MB
Boot Display Device	VBIOS
	IPD
	DVI
	CRT
	HDMI
	HDTV
	TV
Beep Function	Disabled
	Enabled
Boot Menu Hot-Key	Disabled
	Enabled
Boot LAN Hot-Key	Disabled
	Enabled
Boot From LAN	Disabled
	Used INT 18h
	Used INT 19h
	PnP/BEV(BBS)
	RPL

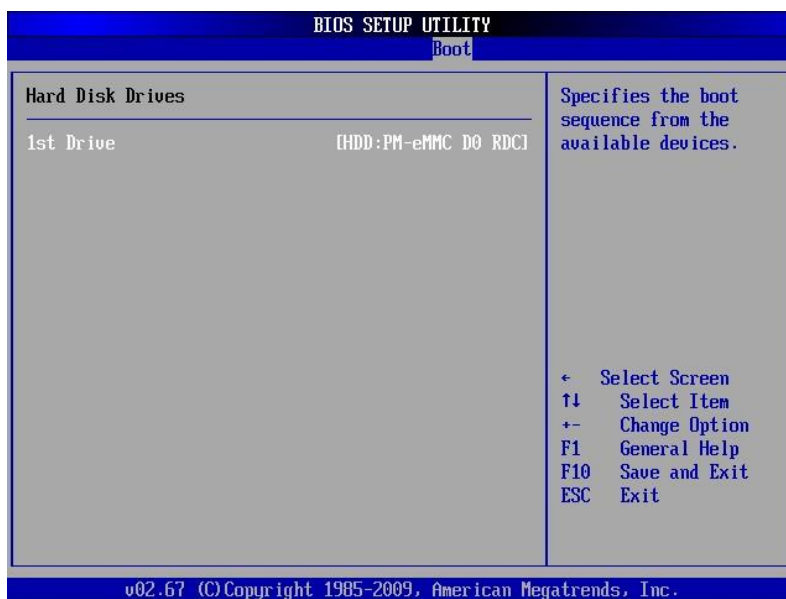
7.5.2 Boot Device Priority



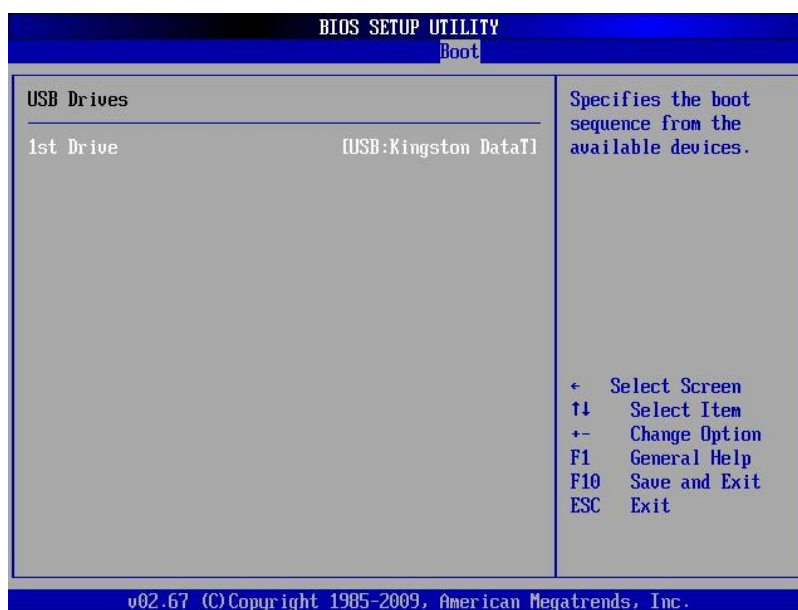
Boot Device Priority	
1st Boot Device	USB CD/DVD Hard Drive Removable Dev. Network Disabled
2nd Boot Device	USB CD/DVD Hard Drive Removable Dev. Network Disabled
3rd Boot Device	USB CD/DVD Hard Drive Removable Dev. Network Disabled
4th Boot Device	USB CD/DVD Hard Drive Removable Dev. Network Disabled

5th Boot Device	USB
	CD/DVD
	Hard Drive
	Removable Dev.
	Network
	Disabled

7.5.3 Hard Disk Drives

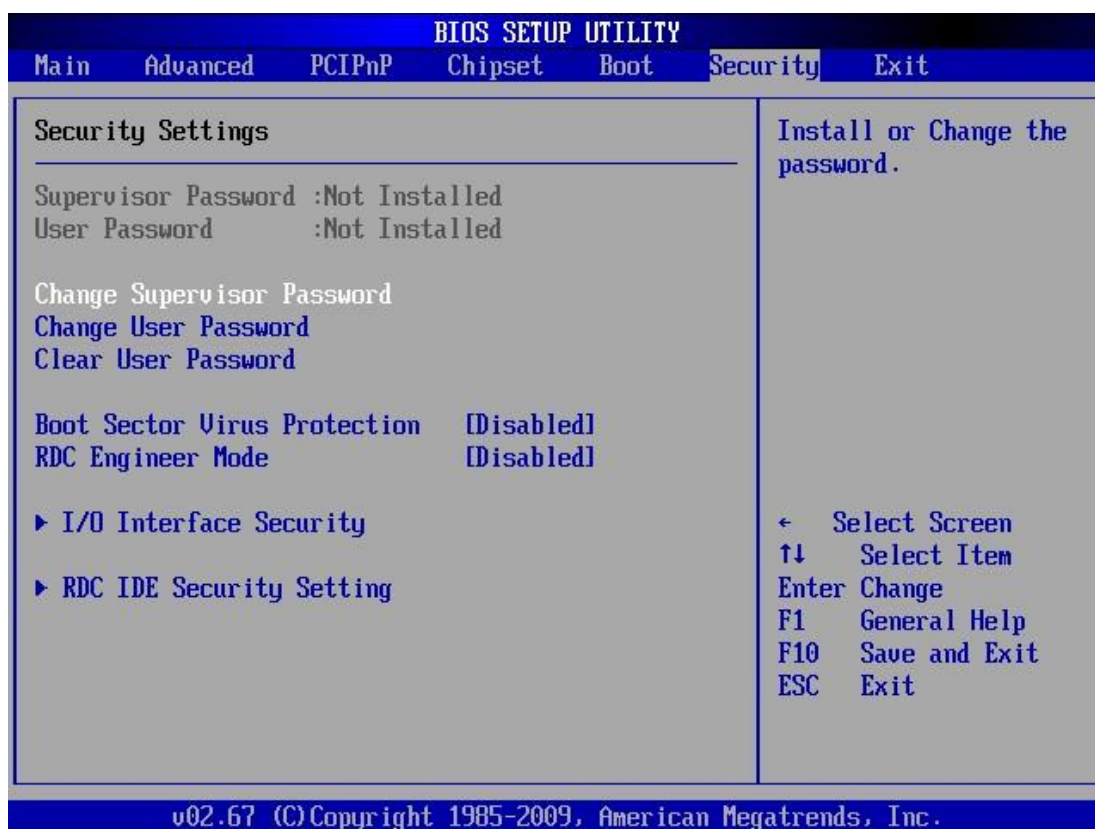


Hard Disk Drives	1st Drive	Depends on the device installed Disabled
------------------	-----------	---



USB Device	1st Drive	Depends on the device installed Disabled
------------	-----------	---

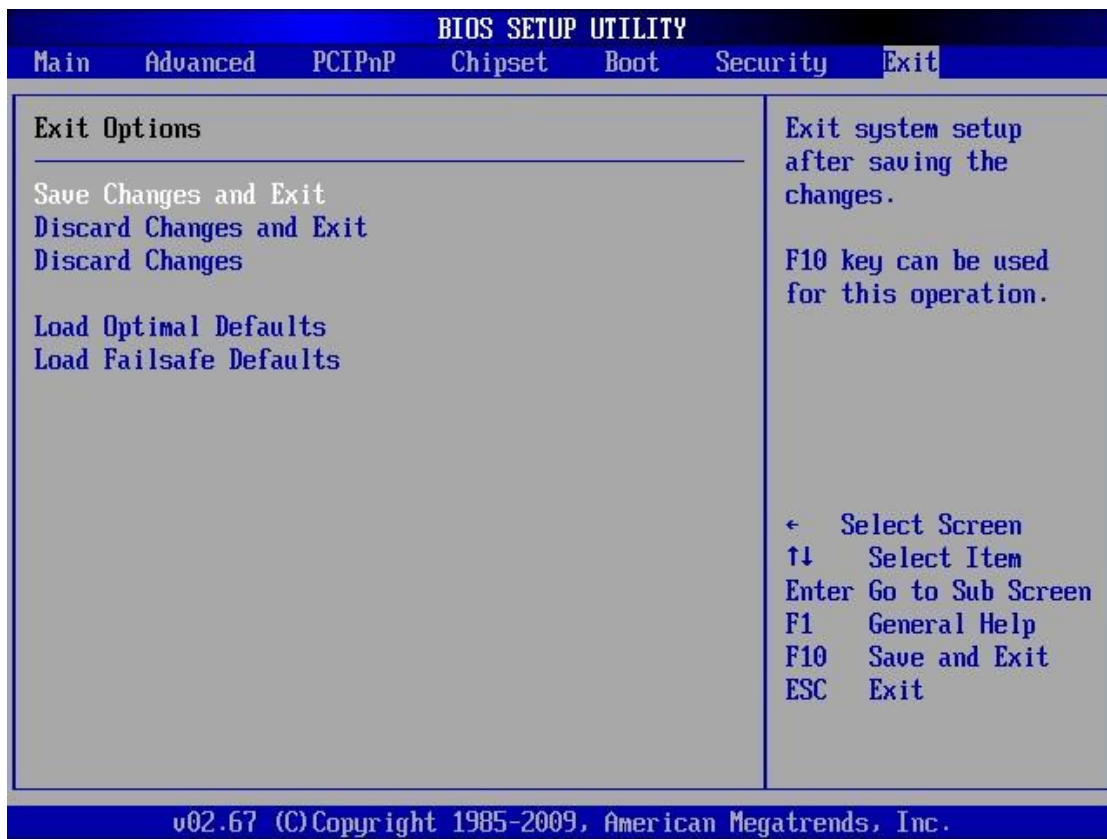
7.6 Security



Feature	Options
Supervisor Password	
User Password	
Change Supervisor Password	Enter New Password
Change User Password	Enter New Password
Clear User Password	Clear Password? OK Cancel
Boot Sector Virus Protection	Disabled Enabled
RDC Engineer Mode	Disabled Enabled
I/O Interface Security	USB Control 1 Interface
	USB Control 2 Interface
	USB Device Interface
	LAN Network Interface
	COM1 Port Interface
	COM2 Port Interface
	COM3 Port Interface
	COM4 Port Interface
	COM5 Port Interface
COM6 Port Interface	
COM7 Port Interface	
COM8 Port Interface	
COM9 Port Interface	

Feature	Options
	Parallel Port Interface
	AUDIO/MODEM Interface
RDC IDE Security Setting	AES Key Length
	PM-HDD Encryption Mode

7.7 Save & Exit



Feature	Options
Save Changed and Exit	OK
	Cancel
Discard Changes and Exits	OK
	Cancel
Discard Changes	OK
	Cancel
Load Optimal Defaults	OK
	Cancel
Load Failsafe Defaults	OK
	Cancel

8. 8. PIO and WatchDog Timer sample code

8.1 8.1. GPIO Sample Program for DOS environment

```
// ***** //  
//      GPIO Sample Code  
//      Version No : 1.0.0  
// ***** //  
  
//#include <stdio.h>  
//#include <sys/io.h>  
//#include <termios.h>  
//#include <unistd.h>  
//#include <assert.h>  
//#include <string.h>  
//#include <stdlib.h>  
//#include <sys/ioctl.h>  
//#include <sys/time.h>  
//#include <sys/types.h>  
  
#include <fcntl.h>  
  
#include <stdio.h>  
#if __linux__  
#include <sys/io.h>  
#include <unistd.h>  
#else  
#include <dos.h>  
#endif  
#include <string.h>  
#include "ESDKERRR.h"  
  
#define IO_PERMOFF 0  
#define IO_PERMON 3  
  
#if __linux__  
void outportb(unsigned short int ulport, unsigned char data);  
unsigned char inportb(unsigned short int ulport);  
void outportl(unsigned short int ulport, unsigned int data);  
unsigned int inportl(unsigned short int ulport);  
void delay(int secs);  
#endif  
  
void help(void);  
unsigned int IsVortex86DX3(void);  
  
#if __linux__
```

```
void outportb(unsigned short int ulport, unsigned char data)
{
    outb_p(data, ulport);
}

unsigned char inportb(unsigned short int ulport)
{
    //int data_rw8 = 0;
    //data_rw8 = inb_p(ulport);
    //return data_rw8;
    return inb_p(ulport);
}

void outportl(unsigned short int ulport, unsigned int data)
{
    outl_p(data, ulport);
}

unsigned int inportl(unsigned short int ulport)
{
    //int data_rw32 = 0;
    //data_rw32 = inl_p(ulport);
    //return data_rw32;
    return inl_p(ulport);
}

void delay(int secs)
{
    usleep(secs * 1000);
}
#endif

unsigned int IsVortex86DX3(void)
{
    unsigned long val;
#ifdef __linux__
    iopl(IO_PERMON);
#endif // __linux
    //outl(0x80000090, 0xcf8);
    outportl(0xcf8, 0x80000090);
    val = inportl(0xcfc);
#ifdef __linux__
    iopl(IO_PERMOFF);
#endif // __linux__
    if(val == 0x36504D44)
        return 1;

    return 0;
}
```

```
}

void help(void)
{
    printf("=====\r\n");
    printf("    GPIO Test program        \r\n");
    printf("=====\r\n");
    printf("gpio -r  Show All Data        \r\n");
    printf("gpio -0h set GPO0 N25 high \r\n");
    printf("gpio -0l set GPO0 N25 low  \r\n");
    printf("gpio -1h set GPO1 M26 high \r\n");
    printf("gpio -1l set GPO1 M26 low  \r\n");
    printf("gpio -2h set GPO2 M25 high \r\n");
    printf("gpio -2l set GPO2 M25 low  \r\n");
    printf("gpio -3h set GPO3 N27 high \r\n");
    printf("gpio -3l set GPO3 N27 low  \r\n");
    printf("gpio -f13h set SATA_SEL F13 high \r\n");
    printf("gpio -f13l set SATA_SEL F13 low  \r\n");
    printf("=====\r\n");
}

int main(int argc, char* main_argv[])
{
    int result = 0;

    if(IsVortex86DX3())
    {
        printf("Vortex86DX3 found.\r\n");
    }

#ifdef __linux__
    iopl(IO_PERMON);
#endif // __linux__

    switch(argc)
    {
    case 2:
        /* set GPIO port0[7-4] as input mode GPIO port0[3-0] as output mode */
        outportb(0x98, 0x0F);

        /* set GPIO port8[7] as output mode */
        unsigned char regData = inportb(0x95);
        regData |= 0x80;
        outportb(0x95, regData);

        // Get GPIO value.
        if(!strcmp(main_argv[1], "-r"))
        {
            // Read all GPIO value.

```

```
regData = inportb(0x78);

printf("GPIO J26 : %d\n", (regData & 0x10)>>4);
printf("GPIO P27 : %d\n", (regData & 0x20)>>5);
printf("GPIO L26 : %d\n", (regData & 0x40)>>6);
printf("GPIO L27 : %d\n", (regData & 0x80)>>7);
printf("GPO0 N25 : %d\n", regData & 0x01);
printf("GPO1 M26 : %d\n", (regData & 0x02)>>1);
printf("GPO2 M25 : %d\n", (regData & 0x04)>>2);
printf("GPO3 N27 : %d\n", (regData & 0x08)>>3);

regData = inportb(0x88);

printf("GPO SATA_SEL F13 : %d\n", (regData & 0x80)>>7);
}
// Set GPIO output value.
else if(!strcmp(main_argv[1], "-0h"))
{
    regData = inportb(0x78);
    regData |= 0x01;
    outportb(0x78, regData);
    regData = inportb(0x78);
    if(0x01 == (regData & 0x01))
        printf("Set GPO0 N25 to high.\n");
    else
    {
        result = -1;
        printf("Set GPIO N25 high Failed return %d\n", regData & 0x01);
    }
}
else if(!strcmp(main_argv[1], "-0l"))
{
    regData = inportb(0x78);
    regData &= 0xFE;
    outportb(0x78, regData);
    regData = inportb(0x78);
    if(!(regData & 0x01))
        printf("Set GPO0 N25 to low.\n");
    else
    {
        result = -1;
        printf("Set GPIO N25 low Failed return %d\n", regData & 0x01);
    }
}
else if(strcmp(main_argv[1], "-1h") == 0)
{
    regData = inportb(0x78);
    regData |= 0x02;
```

```
    outportb(0x78, regData);
    regData = inportb(0x78);
    if(0x02 ==(regData & 0x02))
        printf("Set GPO1 M26 to high.\n");
    else
    {
        result = -1;
        printf("Set GPO1 M26 high Failed return %d\n", (regData & 0x02)>>1);
    }
}
else if(strcmp(main_argv[1], "-1l") == 0)
{
    regData = inportb(0x78);
    regData &= 0xFD;
    outportb(0x78, regData);
    regData = inportb(0x78);
    if(!(regData & 0x02))
        printf("Set GPO1 M26 to low.\n");
    else
    {
        result = -1;
        printf("Set GPO1 M26 low Failed return %d\n", (regData & 0x02)>>1);
    }
}
else if(strcmp(main_argv[1], "-2h") == 0)
{
    regData = inportb(0x78);
    regData |= 0x04;
    outportb(0x78, regData);
    regData = inportb(0x78);
    if(0x04 ==(regData & 0x04))
        printf("Set GPO2 M25 to high.\n");
    else
    {
        result = -1;
        printf("Set GPO2 M25 high Failed return %d\n", (regData & 0x04)>>2);
    }
}
else if(strcmp(main_argv[1], "-2l") == 0)
{
    regData = inportb(0x78);
    regData &= 0xFB;
    outportb(0x78, regData);
    regData = inportb(0x78);
    if(!(regData & 0x04))
        printf("Set GPO2 M25 to low.\n");
    else
    {
```

```
        result = -1;
        printf("Set GPO2 M25 low Failed return %d\n", (regData & 0x04)>>2);
    }
}
else if(strcmp(main_argv[1], "-3h") == 0)
{
    regData = inportb(0x78);
    regData |= 0x08;
    outportb(0x78, regData);
    regData = inportb(0x78);
    if(0x08 ==(regData & 0x08))
        printf("Set GPO3 N27 to high.\n");
    else
    {
        result = -1;
        printf("Set GPO3 N27 high Failed return %d\n", (regData & 0x08)>>3);
    }
}
else if(strcmp(main_argv[1], "-3l") == 0)
{
    regData = inportb(0x78);
    regData &= 0xF7;
    outportb(0x78, regData);
    regData = inportb(0x78);
    if(!(regData & 0x08))
        printf("Set GPO3 N27 to low.\n");
    else
    {
        result = -1;
        printf("Set GPO3 N27 low Failed return %d\n", (regData & 0x08)>>3);
    }
}
else if(strcmp(main_argv[1], "-f13h") == 0)
{
    regData = inportb(0x88);
    regData |= 0x80;
    outportb(0x88, regData);
    regData = inportb(0x88);
    regData &= 0x80;
    if(0x80 == regData)
        printf("Set SATA_SEL F13 to high.\n");
    else
    {
        result = -1;
        printf("Set SATA_SEL F13 high Failed return %d\n", regData>>7);
    }
}
else if(strcmp(main_argv[1], "-f13l") == 0)
```



```
{
    regData = inportb(0x88);
    regData &= 0x7F;
    outportb(0x88, regData);
    regData = inportb(0x88);
    regData &= 0x80;
    if(!regData)
        printf("Set SATA_SEL F13 to low.\n");
    else
    {
        result = -1;
        printf("Set SATA_SEL F13 low Failed return %d\n", regData>>7);
    }
}
else
    help();
break;

default:
    help();
break;
}

#if __linux__
    iopl(IO_PERMOFF);
#endif
}
else
{
    result = -1;
    printf("Vortex86DX3 not found.\r\n");
}

return result;
}
```

8.2 Watchdog timer Sample Program for DOS environment

```
// *****//  
//      Watch Dog Timer Sample Code  
//      Version No : 1.0.0  
// *****//  
  
//#include <stdio.h>  
//#include <sys/io.h>  
#include <termios.h>  
//#include <unistd.h>  
#include <assert.h>  
//#include <string.h>  
#include <stdlib.h>  
#include <sys/ioctl.h>  
#include <sys/time.h>  
#include <sys/types.h>  
  
#include <fcntl.h>  
  
#include <stdio.h>  
#if __linux__  
#include <sys/io.h>  
#include <unistd.h>  
#else  
#include <dos.h>  
#endif  
#include <string.h>  
#include "ESDKERRR.h"  
  
#define IO_PERMOFF 0  
#define IO_PERMON 3  
  
#define INDEX_PORT 0x22  
#define DATA_PORT 0x23  
  
#if __linux__  
#define PORT_TYPE unsigned short int  
#define DATA_L_TYPE unsigned int  
#else  
#define PORT_TYPE unsigned short  
#define DATA_L_TYPE unsigned long  
#endif // __linux__  
  
#if __linux__  
void outportb(unsigned short int ulport, unsigned char data);  
unsigned char inportb(unsigned short int ulport);
```

```
void outportl(unsigned short int ulport, unsigned int data);
unsigned int inportl(unsigned short int ulport);
void delay(int secs);
#endif

void Write_SIO(PORT_TYPE ulportIdx, PORT_TYPE ulportData, unsigned char reg, unsigned char val);
unsigned char Read_SIO(PORT_TYPE ulportIdx, PORT_TYPE ulportData, unsigned char reg);
void Write_SIO32(PORT_TYPE ulportIdx, PORT_TYPE ulportData, DATA_L_TYPE reg, DATA_L_TYPE val);
DATA_L_TYPE Read_SIO32(PORT_TYPE ulportIdx, PORT_TYPE ulportData, DATA_L_TYPE reg);
void help(void);
unsigned int IsVortex86DX3(void);

#if __linux__
void outportb(unsigned short int ulport, unsigned char data)
{
    outb_p(data, ulport);
}

unsigned char inportb(unsigned short int ulport)
{
    //int data_rw8 = 0;
    //data_rw8 = inb_p(ulport);
    //return data_rw8;
    return inb_p(ulport);
}

void outportl(unsigned short int ulport, unsigned int data)
{
    outl_p(data, ulport);
}

unsigned int inportl(unsigned short int ulport)
{
    //int data_rw32 = 0;
    //data_rw32 = inl_p(ulport);
    //return data_rw32;
    return inl_p(ulport);
}

void delay(int secs)
{
    usleep(secs * 1000);
}
#endif

void Write_SIO(PORT_TYPE ulportIdx, PORT_TYPE ulportData, unsigned char reg, unsigned char val)
{
    outportb(ulportIdx, reg);
}
```

```

    outportb(ulportData, val);
}

unsigned char Read_SIO(PORT_TYPE ulportIdx, PORT_TYPE ulportData, unsigned char reg)
{
    outportb(ulportIdx, reg);
    return inportb(ulportData);
}

void Write_SIO32(PORT_TYPE ulportIdx, PORT_TYPE ulportData, DATA_L_TYPE reg, DATA_L_TYPE val)
{
    outportl(ulportIdx, reg);
    outportl(ulportData, val);
}

DATA_L_TYPE Read_SIO32(PORT_TYPE ulportIdx, PORT_TYPE ulportData, DATA_L_TYPE reg)
{
    outportl(ulportIdx, reg);
    return inportl(ulportData);
}

void help(void)
{
    printf("=====\n");
    printf("    Watchdog Timer Program ver1.00    \n");
    printf("=====\n");
    //printf("Usage: WDT -r  (Show Watchdog Register Settings) \n");
    //printf("Usage: WDT -info (Show Watchdog Current Status) \n");
    printf("Usage: WDT -s xxx (Set Time-out Value)    \n");
    printf("    xxx = 1 ~ 512 seconds, 0 is stop.    \n");
    //printf("Usage: WDT -m xxx (Set Time-out Value)    \n");
    //printf("    xxx = 1 ~ 255 minutes, 0 is stop.    \n");
    printf("=====\n");
}

unsigned int IsVortex86DX3(void)
{
    unsigned long val;
#ifdef __linux__
    iopl(IO_PERMON);
#endif // __linux
    //outl(0x80000090, 0xcf8);
    outportl(0xcf8, 0x80000090);
    val = inportl(0xcfc);
#ifdef __linux__
    iopl(IO_PERMOFF);
#endif // __linux
    if(val == 0x36504D44)

```

```
    return 1;

    return 0;

#if 0
    unsigned long val;
    iopl(IO_PERMON);
    outl(0x80000090, 0xcf8);
    val = inl(0xcfc);
    iopl(IO_PERMOFF);
    if(val == 0x35504d44)
        return 1;
    else
        return 0;
#endif

    //return 1;
}

int main(int argc, char* main_argv[])
{
    int result = 0;

    if(IsVortex86DX3())
    {
        printf("Vortex86DX3 found.\r\n");

        int ucWDTTime;

#if __linux__
        iopl(IO_PERMON);
#endif // __linux__

        switch(argc)
        {
#if 0
        case 2:
            // Get WDT time.
            if(!strcmp(main_argv[1], "-r"))
            {
                //outportb(0x22, 0x13); // Lock register
                //outportb(0x23, 0xc5); // Unlock config. register
                Write_SIO(INDEX_PORT, DATA_PORT, 0x13, 0xc5);

                unsigned char c = Read_SIO(INDEX_PORT, DATA_PORT, 0x3B);

                unsigned int lTime = 0;
                lTime += (c & 0xFF) << 16;
            }
#endif
        }
    }
}
```

```

    c = Read_SIO(INDEX_PORT, DATA_PORT, 0x3A);

    lTime += (c & 0xFF) << 8;

    c = Read_SIO(INDEX_PORT, DATA_PORT, 0x39);

    lTime += (c & 0xFF);

    lTime /= 0x20L * 1000L;

    //outportb(0x22, 0x13); // Lock register
    //outportb(0x23, 0x00); // Lock config. register
    Write_SIO(INDEX_PORT, DATA_PORT, 0x13, 0x00);

    printf("Second mode: %d second\n", lTime);
}
else if(!strcmp(main_argv[1], "-info"))
{
    if(!ucWDTTime)
        printf("Watchdog status : Stopped\r\n");
    else
        printf("Watchdog status : Countdown Running\r\n");
}
else
{
    help();
}
break;
#endif

case 3:
    // Set WDT second mode time.
    if(!strcmp(main_argv[1], "-s"))
    {
        // Set WDT time.
        sscanf(main_argv[2], "%d", (int *)&ucWDTTime);

        if((0 < ucWDTTime) && (512 >= ucWDTTime))
        {
            //outportb(0x22, 0x13); // Lock register
            //outportb(0x23, 0xc5); // Unlock config. register
            Write_SIO(INDEX_PORT, DATA_PORT, 0x13, 0xc5);

            // 500 mini-second
            unsigned int lTime = 0x20L * ucWDTTime * 1000L;
            //outportb(0x22, 0x3b);

```

```

//outportb(0x23, (ITime >> 16) & 0xff);
Write_SIO(INDEX_PORT, DATA_PORT, 0x3b, ((ITime >> 16) & 0xff));
//outportb(0x22, 0x3a);
//outportb(0x23, (ITime >> 8) & 0xff);
Write_SIO(INDEX_PORT, DATA_PORT, 0x3a, ((ITime >> 8) & 0xff));
//outportb(0x22, 0x39);
//outportb(0x23, (ITime >> 0) & 0xff);
Write_SIO(INDEX_PORT, DATA_PORT, 0x39, (ITime & 0xff));

// Reset system
//outportb(0x22, 0x38);
//unsigned char c = inportb(0x23);
unsigned char c = Read_SIO(INDEX_PORT, DATA_PORT, 0x38);
c &= 0x0f;
c |= 0xd0;
// Reset system. For example, 0x50 to trigger IRQ7
//outp(0x22, 0x38);
//outp(0x23, c);
Write_SIO(INDEX_PORT, DATA_PORT, 0x38, c);

// Enable watchdog timer
//outportb(0x22, 0x37);
//c = inportb(0x23);
c = Read_SIO(INDEX_PORT, DATA_PORT, 0x37);
c |= 0x40;
//outportb(0x22, 0x37);
//outportb(0x23, c);
Write_SIO(INDEX_PORT, DATA_PORT, 0x37, c);
//outportb(0x22, 0x13); // Lock register
//outportb(0x23, 0x00); // Lock config. register
Write_SIO(INDEX_PORT, DATA_PORT, 0x13, 0x00);

//printf("Watchdog Timer will count down for %d second(s)\n", ucWDTTime);
printf("System will reboot after %d seconds.\r\n", ucWDTTime);
}
else if(!ucWDTTime)
{
//outportb(0x22, 0x13); // Unlock register
//outportb(0x23, 0xc5);
Write_SIO(INDEX_PORT, DATA_PORT, 0x13, 0xc5);
//outportb(0x22, 0x3c);
//unsigned char c = inportb(0x23);
//unsigned char c = Read_SIO(INDEX_PORT, DATA_PORT, 0x3c);
unsigned char c = Read_SIO(INDEX_PORT, DATA_PORT, 0x37);
//outportb(0x22, 0x3c);
//outportb(0x23, c | 0x40);
//Write_SIO(INDEX_PORT, DATA_PORT, 0x3c, (c | 0x40));

```

```
Write_SIO(INDEX_PORT, DATA_PORT, 0x37, (c & 0xBF));
//outportb(0x22, 0x13); // Lock register
//outportb(0x23, 0x00);
Write_SIO(INDEX_PORT, DATA_PORT, 0x13, 0x00);

printf("Watchdog Timer is Stopping now\r\n");
}
if((0 > ucWDTTime) || (512 <= ucWDTTime))
{
    result = -1;
    printf("Timer duration is 1~512sec, type wrong value %d\r\n", ucWDTTime);
}
}
else
{
    help();
}
break;

default:
    help();
    break;
}
}

#if __linux__
    iopl(IO_PERMOFF);
#endif
}
else
{
    result = -1;
    printf("Vortex86DX3 not found.\r\n");
}
}

return result;
}
```


9. Contact Information

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