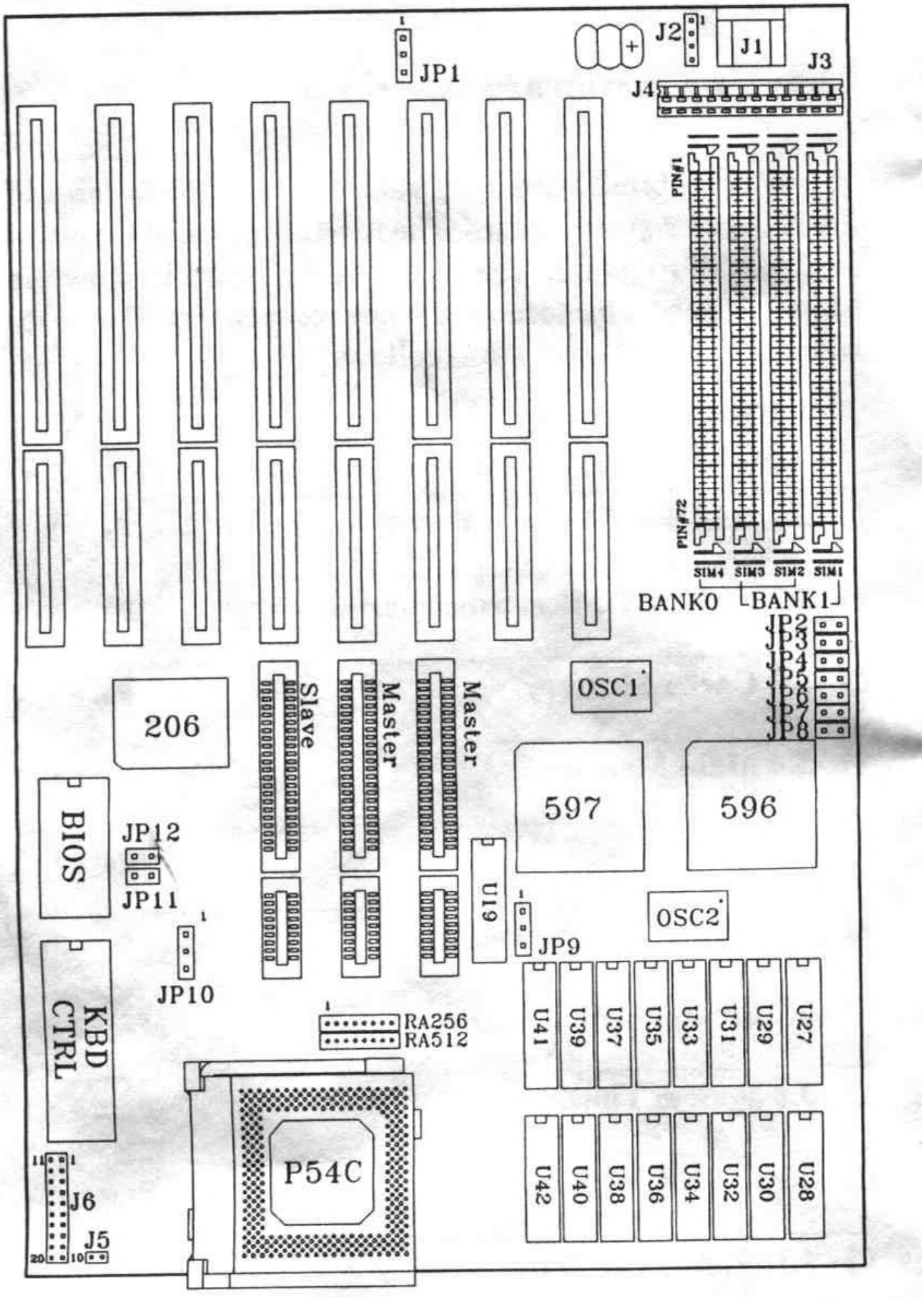


Figure 2: Layout and connector locations of the PAT54PV

Table 1: Memory configurations of the PAT54PV

Total Memory	Bank 0	Bank 1
2MB	256K x 36	----
4MB	512K x 36	----
6MB	256K x 36	512K x 36
8MB	1M x 36	----
8MB	512K x 36	512K x 36
10MB	256K x 36	1M x 36
12MB	512K x 36	1M x 36
16MB	1M x 36	1M x 36
16MB	2M x 36	----
18MB	256K x 36	2M x 36
20MB	512K x 36	2M x 36
24MB	1M x 36	2M x 36
32MB	4M x 36	----
32MB	2M x 36	2M x 36
34MB	256K x 36	4M x 36
36MB	512K x 36	4M x 36
40MB	1M x 36	4M x 36
48MB	2M x 36	4M x 36
64MB	4M x 36	4M x 36
64MB	8M x 36	----
66MB	256K x 36	8M x 36
68MB	512K x 36	8M x 36
72MB	1M x 36	8M x 36
80MB	2M x 36	8M x 36
96MB	4M x 36	8M x 36
128MB	8M x 36	8M x 36

Chapter 4 Configuring the PAT54PV

The following sections describe the necessary procedures and proper jumper settings to configure the PAT54PV system board. For the locations of the jumpers and Resistor Arrays, refer to *Figure 2* on *page 3 - 2*.

The following configuration options can be selected:

4.1 AT Bus Clock Selection Jumpers: JP2 & JP3

The PAT54PV generates the AT Bus clock ***(ATCLK)*** from an internal division of the ***Local Bus(VL-Bus) Clock (VLCLK)***.

Refer to the following table for the necessary settings.

Table 7: VLCLK to ATCLK relationship

JP2	JP3	ATCLK Frequency	VLCLK Frequency
		10MHz	50MHz
		8MHz	40MHz
		8MHz	33MHz

Note

VLCLK can be derived from a clock synthesizer in U53 Refer to ***Section 4.7, "VL-Bus Frequency Selection"*** *for details.*

4.2 VL-Bus Signal Sample Selection Jumper: JP4

A VL-Bus device, to indicate that the current cycle is a VL-Bus cycle, generates a signal called ***LDEV#***. This signal, depending on how JP4 is set, can be sampled by the P54C/CT CPU at two different time intervals.

Refer to the following table for the recommended settings.

Table 8: Local bus signal sample selection

JP4	Condition
	Recommended for 33MHz VLCLK
	Recommended for 40/50MHz VLCLK

4.3-1 VL-Bus Wait State Selection Jumper: JP5

This *2-pin* header, **JP5**, determines whether or not an additional local bus clock cycle is necessary to perform a write to a VL-Bus peripheral device. Read cycles are unaffected by this setting.

Refer to the following table for the necessary settings.

Table 9-1: VL-Bus write wait state selection settings

JP5	Condition
	0 wait state writes *(Recommended for 33MHz VLCLK)*
	1 wait state writes *(Recommended for 40MHz/50MHz VLCLK)*

4.3-2 VL-Bus Speed Indication Jumper: JP6

This *2-pin* header, **JP6**, is used to indicate the VL-Bus clock speed (VLCLK) of the PAT54PV

Refer to the following table for the necessary setting

Table 9-2: VL-Bus speed indication settings

JP6	Condition
	33MHz VLCLK
	40/50MHz VLCLK

4.4 Video Adapter Selection Jumper: JP7

This jumper setting is checked by the system BIOS during system boot-up to decide what type of video card is primary card in the system board. This jumper setting is also checked against the configuration information stored in the CMOS RAM by the Setup program.

If there is only one video card installed in the PAT54PV system, set this jumper to reflect its type.

If more than one video card is installed in the PAT54PV system, set this jumper to indicate which card is the primary one.

Table 10: Video adapter selection jumper settings

JP7	Function
	Monochrome
	Color

Note

s jumper is set to indicate the type of primary display nt in the PAT54PV, an error message will appear g boot-up. Also, note that for a videoless application, as a dedicated file server, it is not necessary to set JP7. nay specify videoless application during the system program.

4.5 Back-to-Back I/O Delay Selection: JP8

This 2-pin header must be set according to the following table.

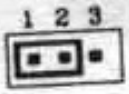
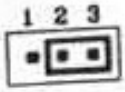
Table 11: Back-to-back I/O delay selection setting

JP8	Function
	Enable back-to-back I/O delay *(default)*
	Disable back-to-back I/O delay

4.6 Local Device Indication Jumper: JP9

Set this 3-pin header, JP9, according to the following table.

Table 12: Local device indication settings

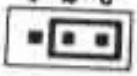
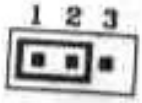
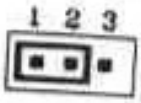
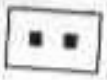
JP9	Function
	33MHz or 40MHz VLCLK
	50MHz VLCLK

4.7 VL-Bus Frequency Selection : JP10 - JP12

The VESA Local(VL) Bus Clock*(VLCLK)* of the PAT54PV can be derived from ***a clock synthesizer installed in U53.***

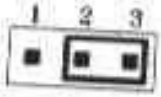
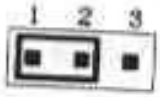
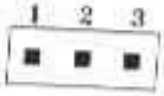
JP10 - JP12 are used to determine the VLCLK frequency of the PAT54PV.

Table 13: VLCLK frequency

VLCLK Frequency	JP10	JP11	JP12
33MHz			
40MHz			
50MHz			

4.9 Battery Selection Jumper: JP1

This *3-pin* header allows the user to select whether the on board battery or an external battery for the CMOS RAM and the Real Time Clock is being used.

JP1	Function
	Use the on board battery
	Clear CMOS RAM
	Use an external battery connected to J2

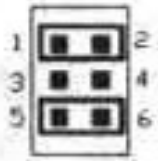
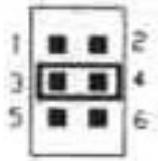
Note

No external battery can be connected to J2 when the on board battery setting is chosen. Doing so will damage the on board battery.

If you are having difficulty booting up due to invalid Setup configuration, you may clear the contents of the CMOS RAM by shorting pins 1 & 2 for a few seconds.

This procedure, however, must be perform

4.10 P54C CPU Core/Bus Frequency Selection

CPU	JP18
P54C 100/66	
P54C 90/60	
P54C 75/50