PAT38PI

Version 1.0A

User's Manual

PAT38PI
System Board
User's Manual

(ver 1.0)

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User's Manual
PAT38PI System Board
1st Edition (April 1990)
TMC Research Corporation

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This manual is organized as follows:

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Chapter 3 Hardware Description - Describes each of the major features of the PAT38PI system board.

Chapter 4 Configuring the PAT38PI - Describes the necessary procedures and jumper settings to configure the PAT38PI system board.

Chapter 5 Installation - Describes the interface the PAT38PI provides for creating a working system.

Chapter 6 Options - Describes the installation and configuration procedures for the options of the PAT38PI.

NOTES

1. INTRODUCTION

The PAT38PI is a high performance system board that is functionally compatible with the system board in the IBM AT. The brain of the PAT38PI system board is the powerful Intel 32-bit 80386. The PAT38PI is designed with a highly integrated chipset using VLSI technology to achieve high reliability, small footprint, and low power consumption.

The memory controller provides the user with the following features: for even bank configurations, it provides 2-way or 4-way interleaving; for odd banks it provides paging. The page-interleaved system memory of the PAT38PC ensures the user zero wait state access without the use of high speed DRAMs.

Memory expansion on the PAT38PI is easy as the system board accepts up to 8MB of SIP memory. And for your memory hungry applications, the PAT38PI's Page Interleave memory can be increased to 16MB by using an optional high-speed memory card. There are two 32-bit memory cards available for the PAT38PI: DIP8P and SIM16P. The DIP8P accepts 1M x 1 DIP chips and the SIM16P accommodates 256KB or 1MB SIM modules.

The PAT38PI has a coprocessor socket which can accommodate either an Intel 80387 or a Weitek 3167 numeric coprocessor. With its high performance and reliability, the PAT38PI is the solution to your computing needs.

2. SPECIFICATIONS

Main Processor
Intel 80386 CPU

Coprocessor Support
A socket to accommodate Intel 80387 or Weitek 3167

Memory Controller
Supports 2-way or 4-way page-interleaved memory

System Memory(on board)
Eight SIP sockets for 256K x 9 or 1M x 9 SIPs

System Memory(on memory card)
One 32-bit memory slot
Optional 8MB or 16MB 32-bit memory card
DIP8P: Up to 8MB of 1M x 1 DIPs
SIM16P: Up to 16MB(256K x 9 or 1M x 9 SIMMs)

BIOS
Licensed BIOS in a single 27C512 EPROM

Clock Calendar
Battery backed RTC and CMOS RAM

Interrupts
Sixteen levels of hardware interrupts

Timers
Three programmable timers

Expansion Slots
One 32-bit slot, can be used as a 16-bit slot when not used by a 32-bit memory card
Five 16-bit slots
Two 8-bit slots

Connectors
Connectors for: power supply, keyboard, reset switch, keylock and power LED, speaker, turbo switch, and turbo LED

Physical Dimensions
8.5"(Width) x 13"(Length)

Power Requirement
+ 5V 2.5 AMP

Two Versions
25MHz and 20MHz **PAT38PI**

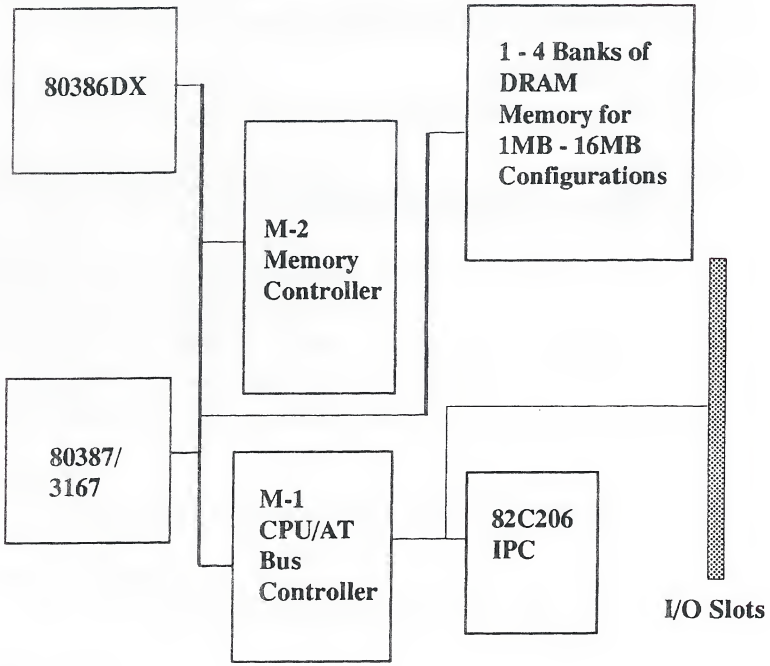


Figure 1: PAT38PI function block

3. HARDWARE DESCRIPTION

This section briefly describes each of the major features of the PAT38PI system board. A layout of the board is shown in Figure 2 to show the locations of the key components. The topics covered in this section are as follows:

Main Processor - Intel 80386

Math Coprocessor - Intel 80387 or Weitek 3167

Page Interleaved Operation

System Memory

I/O Port Address Map

Memory Mapping

BIOS ROM

Timer

DMA Channels

Interrupt Controllers

Real Time Clock and CMOS RAM

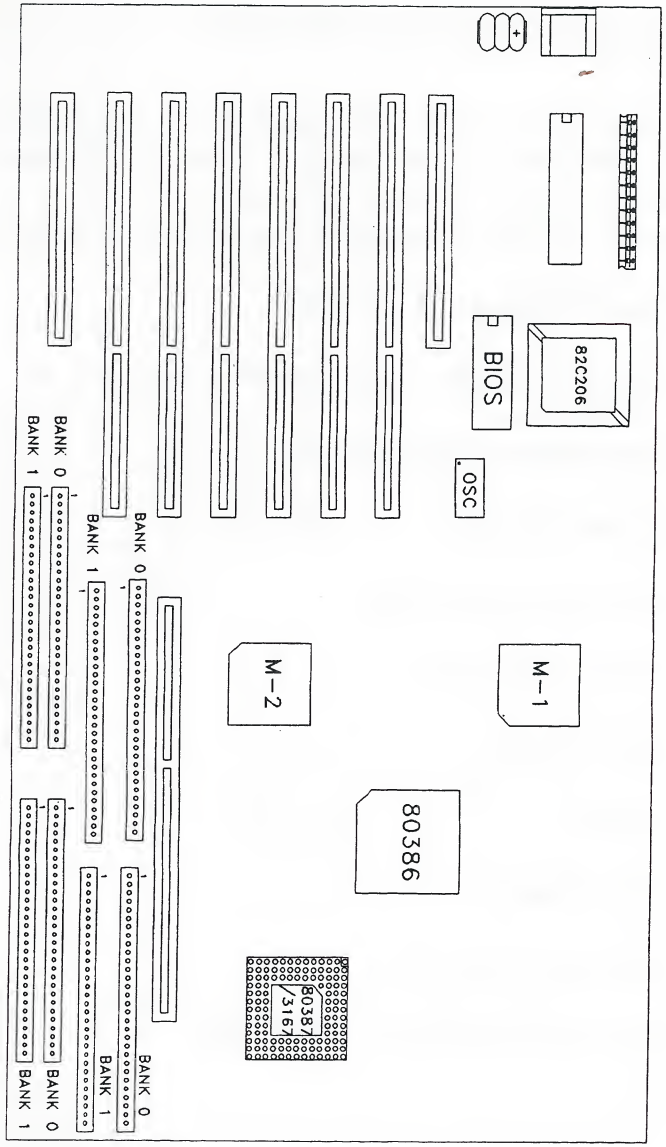


Figure 2: Layout of the PAT38PI

3.1 System Board

The PAT38PI is designed by implementing an 80386 CPU and a highly integrated chipset. The chipset consists of the **M-1 CPU/BUS controller** and the **M-2 memory controller**. Combined with the **82C206, Integrated Peripherals Controller**, the chipset integrates the 386/AT system board with under 20 devices, plus memory.

The **M-1** provides system logic and data bus conversion logic. The control logic consists of 386 CPU control logic, AT bus cycle control, 387 Numeric coprocessor control logic, synchronous clock divide logic and control of the local peripheral bus.

The **M-2** performs the Memory Management functions. It supports page-interleaved operations for the system memory.

The **82C206** Integrated Peripheral Controller (IPC) incorporates the DMA controller, Interrupt controller, Timer, and Clock/Calendar functions.

3.2 80386 CPU

The Central Processing Unit of the PAT38PI system board is Intel's 80386 microprocessor. It provides unprecedented performance, and is upward compatible with Intel's 8088, 8086, and 80286 microprocessors. The 80386 CPU has 32-bit wide internal and external data paths. The 32-bit address lines provide a physical memory capacity of four gigabytes. The design of the PAT38PI implements 24 address lines, limiting the actual physical address space to 16 MB. The virtual 8086 mode permits concurrent execution of multiple software to support the multi-tasking operating system.

3.3 Math Coprocessor (Optional)

The PAT38PI has a 121-pin PGA socket to accommodate either the Intel 80387 or the Weitek 3167 coprocessor. The Intel 80387 or the Weitek 3167 will be running in synchronous mode with respect to the CPU. For details on the installation of the 80387 or the 3167, refer to **Section 6.3 Math Coprocessor.**

3.4 Page Interleaved Operations

The memory controller, M-2, provides flexible implementation of paging for the system memory. For even bank configurations, it provides 2 or 4-way page-interleaving; for odd banks, it provides page mode accesses.

The M-2, uses a page-interleaved design that is different from most interleaved designs. Normal 2-way interleaving scheme uses two banks of DRAMs with even(double word) addresses stored in one bank and odd addresses in the other. If accesses are sequential(or at least two alternating even and odd addresses) the RAS precharge time of one bank can be overlapped with the access time of the second bank. Typically the hit rate (fraction of the time that the required bank is available) is 50%. This is especially true since operand accesses(which tend to be more random) can be interspersed with instruction fetches (which are most likely to be sequential).

Page mode operation available with most DRAMs operates because the access to the row address of the internal DRAM array makes available a large number of bits(512 bits in a 256K x 1) that are subsequently selected using the column address. Once a row access has been made, higher speed random access can be made to any bit(1 of 512) within the row. Page mode accesses and cycle times are typically half that of the normal accesses and cycle times, respectively.

If 36 256K x 1 DRAMs are used to implement a bank, a page would have 512 x 4 bytes == 2KB. Thus, memory could be interleaved on a 2KB page rather than a 4 byte

basis. Any access to the currently active RAS active page would occur in the page access rather than the normal access time and any subsequent access could be to anywhere in the same 2KB page without incurring any penalty due to RAS precharge.

The effectiveness of page-mode operation depends heavily on the page-size. A larger page size increases the chance of a hit. Therefore, if 4-way page-interleaving is implemented instead of 2-way, system performance is further improved.

3.5 System Memory

The memory controller, M-2, of the PAT38PI can control up to four 32-bit memory banks. To maximize the on board memory capacity and still provide flexibility in expanding the system memory, the PAT38PI provides 2 banks of SIP memory and a 32-bit memory expansion slot to accommodate an optional 32-bit memory card. Together they provide up to 16MB of Page Interleaved memory. The on board memory consists of two 32-bit banks with four memory sockets for each bank. The SIP sockets are designed to accept either 256KB or 1MB modules, giving the user great flexibility in memory configurations. An optional 32-bit memory card can be installed in the system to increase the memory capacity of the PAT38PI up to 16 MB.

Refer to the following subsections for details on the possible memory configurations of the PAT38PI with the DIP8P and SIM16P.

The following table illustrates the possible on board memory configurations of the PAT38PI.

Total Memory	PAT38PI	
	Bank 0	Bank 1
1MB	4 of 256K x 9 SIP	---
2MB	4 of 256K x 9 SIP	4 of 256K x 9 SIP
4MB	4 of 1M x 9 SIP	---
8MB	4 of 1M x 9 SIP	4 of 1M x 9 SIP

3.5.1 Memory Expansion

There are two 32-bit memory cards available for the PAT38PI, the DIP8P and the SIM16P. The DIP8P consists of two 32-bit banks, with each bank consisting of 36 1M x 1 bit DRAMs. The SIM16P has four 32-bit memory banks, Banks 0 through 3. Each bank consists of four SIMM sockets which are designed to accept 256K x 9 or 1M x 9 SIMMs.

The following table summarizes the memory bank assignments of the PAT38PI, DIP8P, and SIM16P.

PAT38PI memory banks	On board SIP memory	DIP8P		SIM16P
		JP1 - JP10 1, 2 Short	JP1 - JP10 2, 3 Short	
Bank 0	X	X		X
Bank 1	X	X		X
Bank 2			X	X
Bank 3			X	X

Note: The memory banks of the PAT38PI are assigned as Banks 0 and 1 and cannot be reassigned.

General Rules for PAT38PI's Memory Expansion

1. No Partial Banks

For example, when installing SIPs on Bank 0 of the PAT38PI, all four SIP sockets must be populated.

2. No Bank Overlap

For example, you cannot install SIPs on Bank 0 on the PAT38PI system board and at the same time install DIP chips on Bank 0 of the DIP8P.

3. No Mix of Memory Sizes in the Same Bank

For example, you cannot mix 256K SIPs with 1M SIPs in the same bank.

4. No Bank Gap

For example, you cannot populate Banks 0 and 2 and leave Bank 1 unpopulated.

For details on possible memory configurations with the SIM16P or the DIP8P, refer to **Sections 6.1 and 6.2.**

3.6 I/O Port Address Map

The 80386 CPU communicates via I/O ports. There is a total of 1K port address space defined. The following table lists the I/O port addresses used in the PAT38PI and those assigned to other devices that can be used by I/O expansion cards.

Devices on the System Board

Address	Device
000 - 01F	DMA Controller #1
020 - 03F	Interrupt Controller #1
040 - 05F	Timer
060 - 06F	Keyboard Controller
070 - 07F	Real Time Clock, NMI
080 - 09F	DMA Page Register
0A0 - 0BF	Interrupt Controller #2
0C0 - 0DF	DMA Controller #2
0F0	Clear Math Coprocessor Busy Signal
0F1	Reset Math Coprocessor

Devices on the I/O Slots

Address	Description
1F0 - 1F8	Fixed Disk Controller
200 - 207	Game Port
278 - 27F	Parallel Port #2 (LPT2)
2F8 - 2FF	Serial Port #2 (COM2)
300 - 31F	Prototype Card
360 - 36F	Reserved
378 - 3FF	Parallel Port #1 (LPT1)
380 - 38F	SDLC #2
3A0 - 3AF	SDLC #1
3B0 - 3BF	MDA Video Card (including LPTO)
3C0 - 3CF	Reserved.
3D0 - 3DF	CGA Video Card
3F0 - 3F7	Floppy Disk Controller
3F8 - 3FF	Serial Port #1 (COM1)

3.7 Memory Map

The PAT38PI has a maximum memory capacity of 16MB. The first megabyte is divided into four blocks with each block dedicated to a fixed function. The following table illustrates the memory map for the PAT38PI.

Address		Description
0KB	000000H	Conventional RAM
	09FFFFH	
640KB	0A0000H	128 KB Video RAM
	0BFFFFH	
768KB	0C0000H	192KB I/O Expansion ROM
	0EFFFFH	
960KB	0F0000H	64KB System BIOS ROM
	0FFFFFH	
1 MB	100000H	15 MB User RAM
	FEFFFFH	
	FF0000H	Duplicated 64KB System BIOS ROM at 0F0000H
16MB	FFFFFFH	

3.8 BIOS

The PAT38PI contains a single 27C512 EPROM that contains the system BIOS. The BIOS resides at the upper 64KB of address space in the first megabyte. In protected mode, the BIOS is also mapped to the upper 64KB of the 16MB space and can be accessed at either location.

The BIOS on the PAT38PI is compatible with the BIOS in the IBM AT with the exception that it does not contain the BASIC interpreter. The BASIC and BASICA on IBM PC-DOS will not run on the PAT38PI. To run BASIC in systems based on the PAT38PI, the user should use the GW-BASIC interpreter provided with the Microsoft DOS diskette.

3.9 Timer

The PAT38PI has three channels of timer/counter in the 82C206, which is Intel 8254 compatible. The function of each channel is listed as follows:

Channel	Function
0	System timer - This timer generates the time base for the system timer. Its output is tied to IRQ0.
1	Memory Refresh Request - This timer is used to generate memory refresh requests. It triggers the memory refresh cycle.
2	Tone Generator for speaker - This timer provides the speaker tone. Various sounds can be generated by programming the timer.

3.10 DMA Channels

The PAT38PI contains the equivalent of two 8237A DMA controllers in the 82C206. The 82C206 provides the user with two DMA controllers and four channels of DMA (DMA #1) for 8-bit transfers and three channels of DMA (DMA #2) for 16 bit transfers.(The first 16-bit DMA channel is used for cascading.)

Channel		Function
Controller #1	Controller #2	
0		DRQ0, Reserved
1		DRQ1, SDLC
2		DRQ2, Floppy Disk Controller
3		DRQ3, Reserved
	4	DRQ4, Cascade for DMA
	5	DRQ5, Reserved
	6	DRQ6, Reserved
	7	DRQ7, Reserved

3.11 Interrupt Controller

The PAT38PI contains two Intel 8259A compatible interrupt controllers in the 82C206. Sixteen channels are partitioned into the cascaded controllers (INTC1, INTC2) with 8 inputs each. Of these 16 channels, three are connected internally to various devices, allowing 13 user definable channels of interrupt. Any or all of these interrupts can be masked.

Level	Function
NMI	RAM Parity Check
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ8	Real Time Clock
IRQ9	Software Redirected to Int 0AH
IRQ10	Reserved
IRQ11	Reserved
IRQ12	Reserved
IRQ13	80287
IRQ14	Fixed Disk Controller
IRQ15	Reserved
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Parallel Port #2
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1

3.12 Real Time Clock and CMOS RAM

The PAT38PI contains an MC146818 compatible Real Time Clock (RTC) and 128 bytes of CMOS RAM in the 82C206. The CMOS RAM stores the system's configuration information entered via the Setup program. The RTC and the CMOS RAM are kept active by a battery when the system power is turned off.

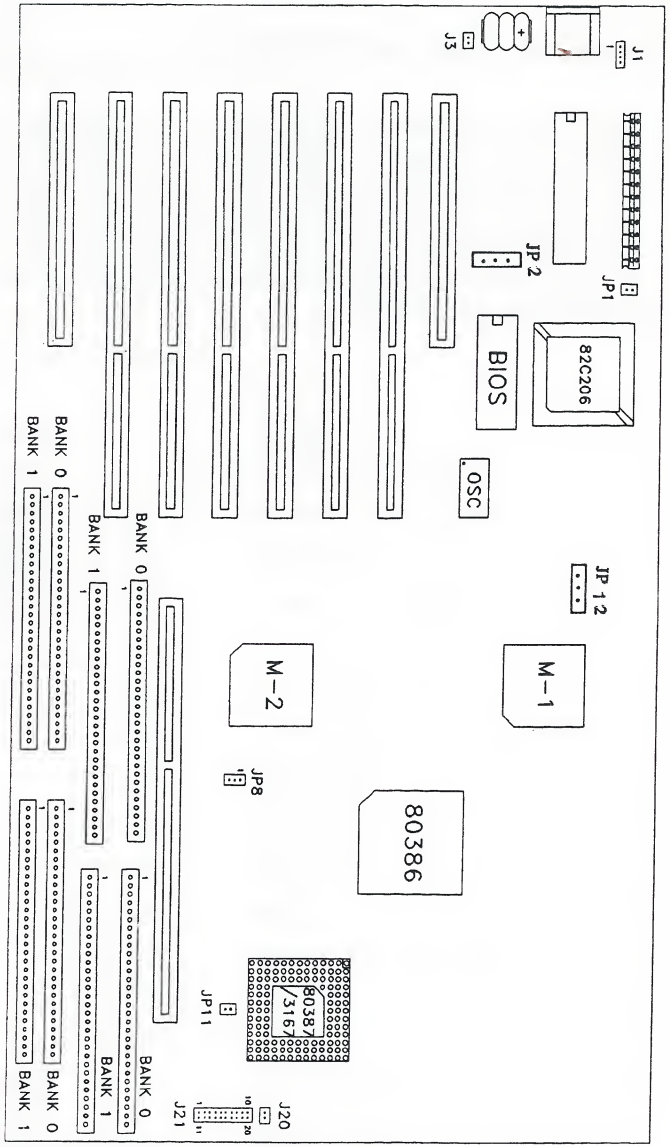


Figure 3: Layout & connector locations of the PAT38PI

4. CONFIGURING THE PAT38PI

The following sections describe the necessary procedures and proper jumper settings to configure the PAT38PI system board. The following configuration options can be selected:

Video Adapter Card Selection: JP1

ROM BIOS SIZE Selection : JP2

Battery Selection: J3

Pipelined Mode Selection: JP8

Weitek 3167 Presence Indication: JP11

Math Coprocessor Presence Indication : JP12

For locations of the jumpers, refer to Figure 3.

4.1 Video Adapter Card Selection: JP1

This jumper setting is checked by the system BIOS during system boot-up to decide what type of video card is the primary card on the system board. This jumper setting is also checked against the configuration information stored in the CMOS RAM by the Setup program. If you have only one video card in your system, set the jumper to reflect its type. If more than one video card is installed in your system, set the jumper to indicate which video card is the primary one.

Color(CGA, EGA, VGA)

Monochrome(MDA, HGC)

4.2 Battery Selection: J3

This jumper setting allows the user to select whether the on board battery or an external battery for the CMOS RAM and the RTC is being used.

Use the on board battery

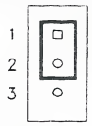
Use an external battery connected to J1

Note:

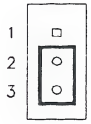
1. *No external battery can be connected to J1 when the on board battery is chosen. Doing so will damage the on board battery.*
2. *The on board battery is a rechargeable battery. It will always be charged whenever the system is running. The on board battery is fully charged at the factory as a part of the burn in process. The on board battery should be able to hold the contents of the CMOS RAM and keep the RTC running for 3 months without recharge.*

4.3 Pipelined Mode Selection: JP8

This jumper setting allows the user to select between two choices of address timing: **non-pipelined** and **pipelined**. Pipelining increases the time that a memory has to respond without lengthening the bus cycle. To maximize performance, enable the pipelined mode.



Pipelined Mode Disabled



Pipelined Mode Enabled

4.4 Weitek 3167 Presence Indication: JP11

This jumper must be set to indicate whether the Weitek 3167 is present or not present.

Note: The presence of an 80387 will be automatically detected by the CPU.

Weitek 3167 Present

No Weitek 3167

4.5 ROM BIOS SIZE Selection : JP2

This setting allows the user to select ROM size used in the ROM sockets, U9.

Setting for 27512 EPROM

Setting for 27256 EPROM

4.6 Math Coprocessor Presence Indication : JP12

This jumper must be set to indicate whether the math coprocessor is present or not present. Not setting this jumper properly will cause difficulty during system bootup

80387 Installed

No Installed

5. INSTALLATION

This section describes the interface that the PAT38PI provides for creating a working system. Please refer to Figure 3 for location of the connectors.

The following items are covered in this section.

External Battery Connector: J1

Keyboard Connector: J2

Power Supply Connectors: J4, J5

Speaker Interface: J21(Pins 1 - 4)

Power LED and Keylock Connector: J21(Pins 11 - 15)

Turbo Switch: J21(Pins 7 & 17)

Turbo LED Connector: J21(Pins 8 & 18)

Reset Switch: J21(Pins 9 & 19)

Hard Disk Drive Access Indicator LED: J20, J21

5.1 External Battery Connector: J1

This four pin connector, J1, allows the user to connect an external battery to maintain the information stored in the CMOS RAM.

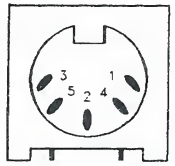
Pin #	Description
1	Vcc
2	N.C.
3	N.C.
4	Ground

Note: The external battery should be a 6V battery.

5.2 Keyboard Connector: J2

The keyboard connector, J2, is a 5-pin DIN connector for connecting an IBM AT or an IBM Enhanced 101-key compatible keyboard.

The following table describes the pin-out assignments of this connector.



Pin #	Function
1	Clock
2	Data
3	N.C.
4	Ground
5	Vcc

5.3 Power Supply Connectors: J4, J5

When using an AT compatible power supply, plug both of the power supply connectors into J4 and J5.

Caution: Extreme care must be taken when plugging in the power supply connectors. If the connectors are not connected in the right orientation, both the system board and the power supply will be damaged.

The following figure indicates the pin-out assignments of the power supply connectors:

Power Supply Connectors: J4, J5

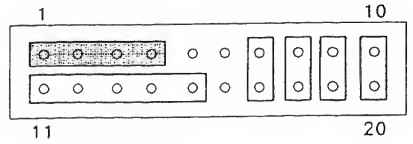
Pin #	Description	Wire Color
1	Power Good	Orange
2	+ 5 V	Red
3	+ 12 V	Yellow
4	- 12 V	Blue
5	Ground	Black
6	Ground	Black
7	Ground	Black
8	Ground	Black
9	- 5 V	White
10	+ 5 V	Red
11	+5 V	Red
12	+5 V	Red

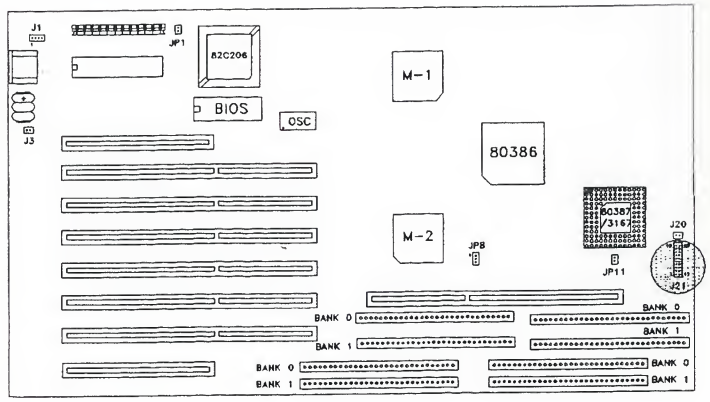
5.4 Speaker Interface: J21 (Pins 1-4)

Pins 1-4 of the 20-pin connector, J21, provide an interface to a speaker for audio tone generation. This connector provides four pins but only two pins are used. A speaker with 8-Ohm or higher impedence is recommended.

Note: Orientation is not required when connecting a speaker to pins 1-4.

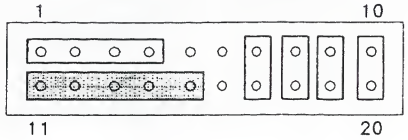
J21 Pin #	Function
1	Speaker Out
2	N. C.
3	Ground
4	+ 5V





5.5 Power LED and Keylock Connector: J21(Pins 11-15)

Pins 11 - 15 of the 20-pin connector, J21, allow the user to connect the power LED and keylock switch of the system's front panel. The power LED indicates the **on/off** status of the system. The keylock switch, when closed, will **disable** the keyboard function.

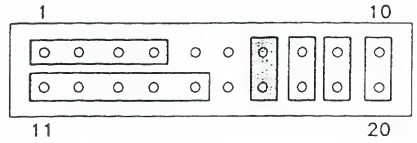


J21 Pin #	Function
11	Power LED
12	N.C.
13	Ground
14	Keylock
15	Ground

5.6 Turbo Switch: J21(Pins 7 & 17)

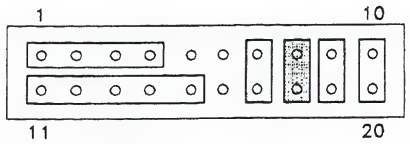
Pins 7 and 17 of the 20-pin connector, J21, allow the user to connect a turbo switch on the front panel of the system chassis. A turbo switch is usually a push-on switch. When the switch is **on**, Pins 7 & 17 are shorted and the CPU will be running at **full** speed. To switch to **low(non-turbo)** speed, simply depress the switch. To return to **high(turbo)** speed mode, press the switch again.

Note: Orientation is not required when connecting a turbo switch.



5.7 Turbo LED Connector: J21(Pins 8 & 18)

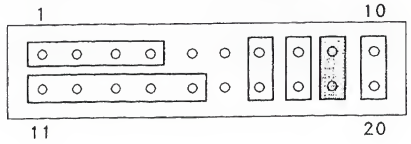
Pins 8 and 18 of the 20-pin connector, J21, provide the user with an interface for connecting a turbo LED indicator in the system's front panel. This LED, when on, indicates the turbo(high) speed mode of the PAT38PI.



Pin #	Function
8	Anode
18	Cathode

5.8 Reset Switch: J21(Pins 9 & 19)

Pins 9 and 19 of the 20-pin connector, J21, provide an interface for a reset switch. The reset switch allows the user to reset the system without turning the power switch off and on.

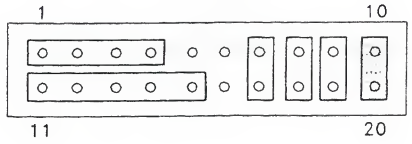


Note: Orientation is not required when connecting a reset switch.

5.9 Hard Disk Drive Access LED: J20, J21(Pins 10 & 20)

These connectors allow the user to connect the hard disk access LED indicator on the system's front panel. The LED will be on whenever the system is accessing the hard drive. Connect the 2-pin connector from the system chassis to pins 10 and 20 of J21. Also, make a connection from J20 to the hard disk controller's LED interface.

Note: You may also connect HDD LED indicator on the system's front panel directly to the hard disk controller without using these connectors.



J21 (Pins 10 & 20)	J20
LED in	LED out

6. OPTIONS

This section describes the installation and configuration of the options for the PAT38PI. The optional boards and equipment include the following:

DIP8P

SIM16P

Math Coprocessors - Weitek 3167 and Intel 80387

6.1 DIP8P

The DIP8P is a high-speed 32-bit memory card designed for the PAT38PI. The DIP8P consists of two memory banks with each bank containing 36 DIP chip sockets. The DIP sockets of the DIP8P accept 1M x 1 DRAMs, and when fully populated, will extend the PAT38PI's Page Interleave memory by an additional 8MB.

Jumper Settings

The DIP8P can be used in two ways, depending on how its memory banks are assigned. There are ten jumpers, JP1 through JP10, on the DIP8P which allow the user to configure the memory banks on the DIP8P as Banks 0 and 1 or as Banks 2 and 3.

Assigning the memory banks on the DIP8P as Banks 0 and 1 will allow the user to utilize DIP memory chips for Banks 0 and 1 instead of SIPs.

Assigning the memory banks on the DIP8P as Banks 2 and 3 will allow the user to add an additional 8MB to the system.

Figures 4 and 5 show the necessary jumper settings.

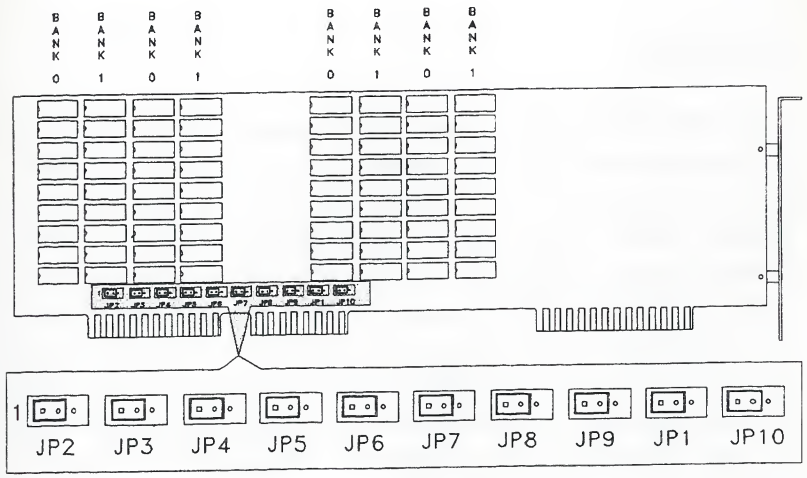


Figure 4: DIP8P configured as Banks 0 & 1 of the PAT38PI

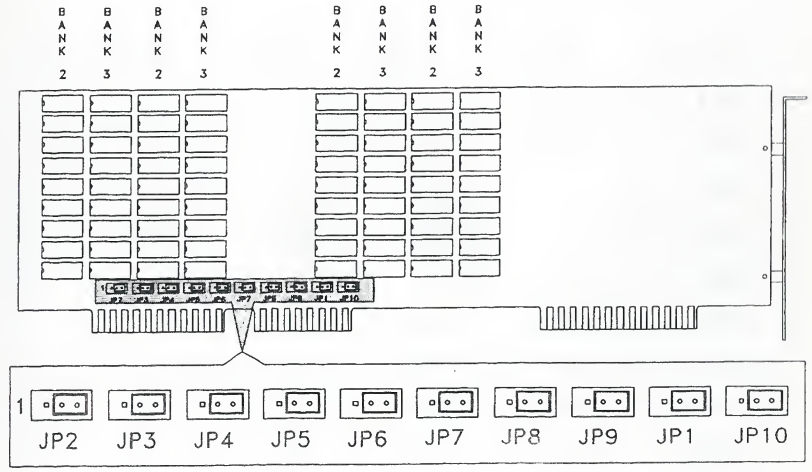


Figure 5: DIP8P configured as Banks 2 & 3 of the PAT38PI

6.2 SIM16P

The SIM16P is a high speed 32-bit memory card designed to increase the Page Interleave memory of the PAT38PI up to 16Mbytes. The SIM16P has four 32-bit memory banks, Banks 0 through 3. Each bank consists of four SIMM sockets which are designed to accept 256K x 9 or 1M x 9 SIMMs. This feature gives the user maximum flexibility during memory configurations. The user may also choose to populate the SIP sockets on the PAT38PI or those on the SIM16P for system memory Banks 0 and 1. The following table illustrates the possible memory configurations of the SIM16P.

Total Memory	BANK 0 SIMM	BANK 1 SIMM	BANK 2 SIMM	BANK 3 SIMM
1MB	256K	---	---	---
2MB	256K	256K	---	---
3MB	256K	256K	256K	---
4MB	256K	256K	256K	256K
4MB	1M	---	---	---
6MB	1M	256K	256K	---
8MB	1M	1M	---	---
10MB	1M	1M	256K	256K
12MB	1M	1M	1M	---
16MB	1M	1M	1M	1M

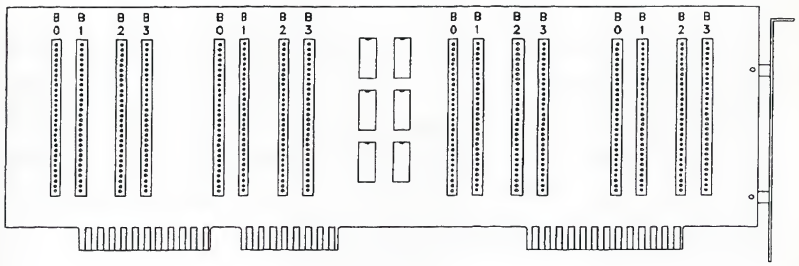


Figure 6: Layout & bank identification of the SIM16P

Note:

1. *A memory bank on the SIM16P consists of 4 SIMM sockets.*
2. *The SIM16P contains four 32-bit memory banks. Therefore if you populate Banks 0 and 1, the SIP sockets on the PAT38PI must remain empty to avoid bank overlap. The reverse is also true. For details on memory banks, refer to Section 3.5.1 "Memory Expansion."*

6.3 Math Coprocessors

The PAT38PI provides a PGA socket to accommodate an Intel 80387 or a Weitek 3167 math coprocessor.

To install an 80387, orient the 80387 so that the notch on the socket aligns with the notch on the 80387. Align the 80387 so the pins of the coprocessor are in alignment with the **two inner rows** of the socket and press evenly and firmly on the 80387 to "seat" it in the socket. Figure 7 illustrates the installation procedure.

Synchronous Operation of the 80387

The PAT38PI is designed so that the 80387 runs in synchronous mode with respect to the CPU speed. For example, if your CPU speed is 25MHz, the speed of the 80387 should also be 25MHz.

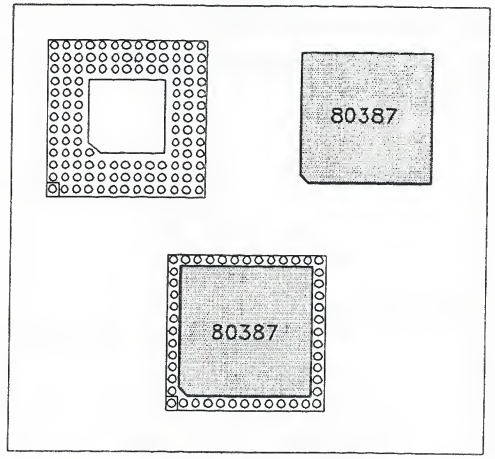


Figure 7: Installing an 80387

Note: The 80387 has a total of 68 pins. Therefore, you must align the 80387 with the two inner rows of the PGA socket. Also note that the CPU will automatically recognize the presence of an 80387 and no jumper change is required.

To install a Weitek 3167, align the notch of the Weitek 3167 with the notch on the socket and press firmly and evenly on the 3167 coprocessor. Figure 8 illustrates the installation procedure.

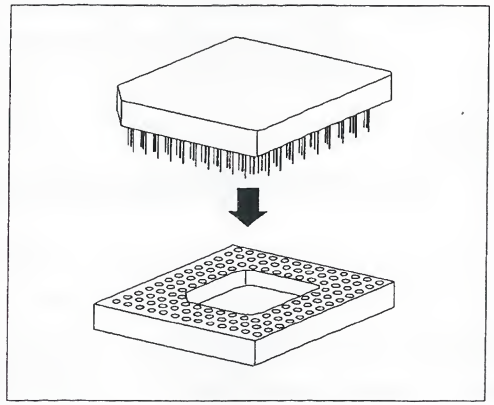


Figure 8: Installation of a Weitek 3167

Note: Refer to Section 4.4, " Weitek 3167 Presence Indication" and properly set the jumper to indicate the presence of a Weitek 3167.

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A.1 SIM64P

The SIM64P is a high speed 32-bit memory card designed to increase page Interleave memory of the PAT38PC or PAT38PI up to 16Mbytes, the PAT48PA up to 32 Mbytes and the PAT38PX or PAT48PX up to 64Mbytes. The SIM64P has four 32-bit memory banks, Banks 0 through 3. Each bank consists of four SIMM sockets which are designed to accept 256K x 9, 1M x 9 or 4M x 9 SIMMs. The feature gives the user maxium flexibility during memory configurations. The following table illustrates the possible memory configurations of the SIM64P.

CAPACITY MEMORY	BANK 0 SIMM	BANK 1 SIMM	BANK 2 SIMM	BANK 3 SIMM
1MB	256K	---	---	---
2MB	256K	256k	---	---
3MB	256K	256K	256K	---
4MB	256K	256K	256K	256K
4MB	1M	---	---	---
6MB	1M	256K	256K	---
8MB	1M	1M	---	---
10MB	1M	1M	256K	256K
12MB	1M	1M	1M	---
16MB	1M	1M	1M	1M
32MB	4M	4M	---	---
64MB	4M	4M	4M	4M

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