586 MOTHERBOARD LAYOUT AND CONFIGURATION S=SHORTED 0=0PEN 1-2 = PINS 1 AND 2 SHORTEDCONNECTORS AND JUMPERS: HARDWARE RESET (J1) KEYLOCK AND POWER LED (J3) 1 = GROUND1 = LED POWER2 = RESET2 = NOT USED3 = GROUNDSPEAKER CONNECTOR (J2) 4 = KEYBOARD INHIBITOR 1 = SIGNAL5 = GROUND2 = VCC3 = SIGNAL FAN POWER CONNECTOR (J4) 4 = VCC1 = +12 VDC 2 = GROUNDVESA BUS WAIT STATE (JP3) 3 = GROUND4 = +5 VDC S = ONE WAIT STATE O = ZERO WAIT STATECPU SPEED ID FOR VL-BUS (JP4) CPU TYPE SELECTION (JP1, JP2) S = HIGHER THAN 33MHZJP1 JP2 0 = EQUAL OR UNDER 33386 0 S S 0 486 TURBO SWITCH CONNECTOR (JP9) S S X86 1 = SELECT PIN2 = GROUNDCPU CLOCK SELECTION (JP6 - JP8) JP7 JP6 JP8 50MHZ S TURBO LED CONNECTOR (JP10) 0 0 S 60MHZ 0 0 1 = +5 VDC 66MHZ S 0 S 2 = INDICATE PINMONITOR STANDBY TIMER SELECTION (JP11 - JP13) JP11 JP12 JP13 12MTN S 0 0 S 0 6MIN 0 0 S 3MIN 0 SYSTEM POWER MANAGEMENT SLECTION (JP14 - JP16) JP14 JP15 JP16 S 0 24MTN 0 S 0 0 12MIN 6MIN 0 0 S CACHE SIZE SELECTION (JP17 - JP21, JP24) JP18 JP19 JP20 JP17 JP21 JP24 64KB 0 0 0 2-3 2-3 2-3 128KB S 0 0 1-2 1-2 1-2

MB-PAM-0030P

 
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INTERNAL/EXTERNAL VL-BUS LCLK SELECTION (JP22, JP23, JP28) JP22 JP23 JP26 ASYNC 1-2 1-2 S SYNC 2-3 2-3 0 MDHDOE# INACTIE SELECTION (JP25) BACK TO BACK IO DELAY (JP29) S = END OF LAST T2S = ENABLEO = BEGINNING OF LAST T2 0 = DISABLEAT CLK SELECTION (JP27 - JP28) LDEV# SAMPLE SELECTION (JP30) JP27 S = END OF SECOND T2JP28 S LCLK/5 S O = END OF FIRST T2LCLK/4 0 S LCLK/3 S 0 LOCAL BUS SELECTION (JP31) LCLK/2 0 0 S = VL-BUS DISABLED0 = VL-BUSENABLED VIDEO SELECTION (JP32) S = COLORPOWER MANAGEMENT IRQ (JP34) O = MONOCHROME2-3 = IRQ 151-2 = IRQ 12BATTERY SELECTION (JP33) 1-2 = DISCHARGETESTING SELECTION (JP35) 2-3 = INTERNAL BATTERYS = FOR QUICK TESTONLY 0 = DEFAULT0 = NORMALAPPLICATION EXTERNAL BATTERY CONNECTOR (J20) KEYBOARD CONNECTOR (J23) 1 = 6 VDC2 = NOT USED3 = GROUND4 = GROUNDPOWER SUPPLY CONNECTOR (J21 - J22)

MEMORY INSTALLATION:

THIS MOTHERBOARD HAS 4 SIMM SOCKETS. THE USER CAN INSTALL 256KB, 1/4MB SIMMS. 70 ns SIMMS OR FASTER IS REQUIRED.