Little Board ™/P5x
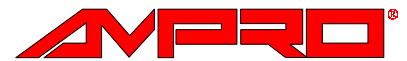
Interactive Manual

PLEASE SELECT:

- *Table of Contents*
- *Index*

- *Mechanical Diagrams*
- *Jumper Settings*

AMPRO ®

Little Board™/P5*x*

P/N 5001351 Revision B

REVISION HISTORY

Revision	Reason for Change	Date
1/A	Pre-Production Release	11/98
B	Production Release	5/99

Table of Contents

Preface

Introduction

Product Reference

Technical Specifications

Appendix A

Appendix B

Preface

Introduction

This manual is for integrators and programmers of systems based on the Ampro Little Board/P5*x*, a full-featured CPU module conforming to the EBX 1.1 technical specification. It contains technical information about hardware requirements, interconnection, and software configuration.

Technical Support

Ampro technical support for this product is available from 8:00 AM to 5:00 PM, Pacific Time, Monday through Friday. When you call, please have the product's technical manual and the product available.

Table i lists contact information for Ampro technical support.

Table i. USA Technical Support Contact Information

Telephone	800-966-5200 (USA), or 408 360-0200
FAX	408 360-0226
Email	techsupport@ampro.com
Website	http://www.ampro.com
FTP	ftp://ftp.ampro.com
Surface Mail	Ampro Computers, Incorporated, 4757 Hellyer Avenue, San Jose, CA 95138, USA

Table ii. European Technical Support Contact Information

Telephone	011 31 10 292 7548
FAX	011 31 10 479 6887
Email	ge@pc104.nl
Website	www.pc104.nl
Surface Mail	Ampro European Logistics Center (AELC), Groene Tuin 267, 3078 KG Rotterdam, The Netherlands

Chapter 1

Introduction

General Description

The Little Board/P5*x* is a high integration, high-performance Pentium-based PC/AT-compatible system that conforms to the EBX V.1.1 specification. This rugged and high quality single-board system contains all the component subsystems of a PC/AT PCI motherboard plus the equivalent of up to six expansion boards. The Little Board/P5*x* is designed to meet the size, power consumption, temperature range, quality, and reliability demands of embedded system applications.

Key functions on the Little Board/P5*x* include:

- High-speed Pentium CPU
- 64-bit wide 3.3V DRAM – up to 256M bytes
- 512K synchronous secondary cache
- Embedded-PC BIOS in Flash EPROM
- Four buffered serial ports (with RS-232, RS-485, TTL options)
- Two universal serial bus (USB) ports
- Infrared (IrDA) port
- Multi-mode IEEE-1284 parallel port
- Floppy controller

- Dual PCI-bus EIDE/UltraDMA drive controllers
- Flat-panel/CRT display controller
- Adaptec UltraSCSI controller (Special Order)
- Built-in Adaptec SCSI BIOS
- Ethernet 100BaseT LAN interface,
- Compact Flash solid-state IDE drive support
- Standard PC keyboard and speaker interfaces

In addition, Ampro has made many improvements to the architecture and firmware of the traditional desktop PC to optimize it for embedded applications. Among the many embedded-PC enhancements that ensure fail-safe embedded system operation and application versatility are a watchdog timer, a powerfail NMI generator, serial console support, serial boot loader, batteryless boot, failsafe boot, accelerated boot, on-board high-density Compact Flash disk, and BIOS extensions for OEM boot customization.

System operation requires a single +5 Volt power source (and 3.3 Volts for low-voltage PCI expansion cards, if required) and offers "green PC" power-saving modes under support of Advanced Power Management (APM) BIOS functions.

Product Feature Summary

CPU/Motherboard

The Little Board/P5*x* has a fully PC-compatible motherboard architecture, with a Pentium low-voltage CPU. It supports all Socket 7 CPUs with up to 7.5A core current. As CPUs evolve, new versions may be offered. Contact your Ampro sales representative for current models.

For improved reliability in harsh thermal environments, the board implements a CPU thermal sensor and configurable thermal-management control logic in the BIOS.

The Pentium CPU has its standard on-chip cache memory (typically 16K). In addition, a 512K byte synchronous-burst secondary cache is provided to increase performance.

The board uses a single DIMM memory module for main DRAM memory, and supports from 16M bytes to 256M bytes in a 64-bit configuration. Both EDO and SDRAM 3.3V DRAM types are supported. (5V DRAMS, ECC, and DRAM parity are not supported.)

The module has a full complement of standard PCI PC/AT architectural features, including DMA channels, interrupt controllers, real-time clock, and timer counters.

Enhanced Embedded-PC BIOS

One of the most valuable features of the Little Board/P5*x* is its enhanced embedded-PC BIOS, which includes an extensive set of functions that meet the unique requirements of embedded-system applications. These enhancements include:

- **Compact Flash support**. You can use a solid-state Compact Flash memory module in place of a rotating media drive (see *Compact Flash Disk*, below).

- **Watchdog timer.** The WDT monitors the boot process and can be integrated into application programs using function calls provided in the BIOS.

- **Fast boot operation.** Normal or accelerated POST.

- **Fail-safe boot support.** Intelligently retries boot devices (configured in the BIOS) until a successful boot.

- **Battery-free boot support.** Saves system Setup information in non-volatile EEPROM. The board can use this information should the RTC battery fail.

- **Serial console option.** Lets you use a serial device, such as an ASCII serial terminal, as console.

- **Serial loader option.** Supports loading boot code from an external serial source.

- **EEPROM access function.** 256 bits of serial EEPROM storage are available to the user, useful for serialization, copy protection, security, etc.

- **OEM customization hooks.** The module can execute custom code prior to system boot via ROM extensions; allows sophisticated system customization without BIOS modification

Modular PC/104-*Plus* Expansion Bus

The Little Board/P5*x* provides a PC/104-*Plus* expansion bus for additional system functions. This bus offers compact, self-stacking, modular expandability. The PC/104-*Plus* expansion bus is an extension of the PC/104 bus. The PC/104 bus is defined in the IEEE P996.1 Standard for Compact Embedded PC Modules. It is an embedded system version of the signal set provided on a desktop PC's ISA bus. The PC/104-*Plus* bus includes this signal set, and in addition, signals implementing a PCI bus, available on an additional 120-pin PCI bus connector.

The growing list of PC/104 and PC/104-*Plu*s modules available from Ampro and hundreds of other PC/104 vendors includes such functions as communications interfaces, video frame grabbers, field bus interfaces, digital signal processors (DSPs), data acquisition and control functions, and many specialized interfaces and controllers. In addition, custom application-specific logic boards can also

be stacked directly on top of the Little Board/P5*x* using its PC/104-*Plus* expansion bus interface as a rugged and reliable interconnect.

The Little Board/P5*x* module's on-board EIDE, video interfaces, and optional SCSI interface are internally connected to its PCI bus. In addition, you can attach PCI peripherals to the board's stackable PCI bus expansion connector in much the same way PC/104 modules are stacked on the PC/104 connectors. The PCI expansion connector consists of 4 rows of 30 pins (120-pin header), and carries all of the appropriate PCI signals to accommodate up to 4 PCI add-on modules. The bus operates at clock speeds up to 33 MHz.

Compact Flash Disk

The Compact Flash interface allows you to substitute solid-state Flash memory for a conventional rotating-media drive. Any DOS-based application, including the operating system, utilities, drivers, and application programs, can easily be run from the Compact Flash device without modification

The Compact Flash disk is a solid-state disk system that emulates an IDE drive. It uses standard Compact Flash disk media, similar to a PCMCIA memory card, but smaller. Insert the Compact Flash disk media in the on-board Compact Flash socket, and use it in much the same way you would use a removable-media hard drive. The Compact Flash drive is architecturally equivalent to an IDE drive in your system. When installed, it becomes one of the two IDE drives supported by the primary EIDE disk controller. It can be configured as either an IDE master or slave drive.

Serial Ports

The Little Board/P5*x* provides four PC-compatible RS-232C serial ports, implemented using 16C550-type UARTs. These UARTs are equipped with 16-byte FIFO buffers to improve throughput.

Serial 1 through Serial 4 are configured for RS-232 operation and are compliant with standard PC serial port specifications. The ports' RS-232 level shifters incorporate built-in voltage pumps to generate RS-232 voltage levels from the system +5V supply.

You can optionally configure Serial 1 for RS-485 operation. In addition, Serial 2 and Serial 4 provide connections for TTL-level serial signals.

Parallel Port

An enhanced bi-directional parallel port interface conforms to the IEEE-1284 standard. It provides features attractive to embedded system designers, including increased speed, an internal FIFO buffer, and DMA transfer capability.

Floppy Interface

An on-board floppy disk interface provides access to standard floppy drives. The interface supports up to two floppy drives, 5.25 inch or 3.5 inch, in any combination. All standard floppy drive types, from 360K 5.25 inch to 1.44M 3.5 inch are supported.

PCI-Bus EIDE Interfaces

On-board PCI EIDE/Ultra DMA/33 interfaces provide high-speed hard disk, IDE CD-ROM drive, and other IDE device access. The interfaces support up to four IDE devices (via primary and secondary drive interfaces). The interfaces are fully compliant with the AS/NSIS ATA Rev. 3.0

specification and the ATAPI Specification. The Ampro Extended BIOS supports hard drives greater than 528M bytes through Logical Block Addressing (LBA).

The Compact Flash interface is implemented as an IDE drive. If it is installed, it takes the position of one of the drives of the primary IDE interface (settable as a master or slave drive).

PCI UltraSCSI Interface

An PCI UltraSCSI controller subsystem is available by special order. The SCSI components are not assembled on standard versions of the Little Board/P5*x*. The portions of this manual that document SCSI circuitry, software, connectors, jumpers, and hardware are relavant only on special order versions of the Little Board/P5*x* that contain the SCSI subsystem.

The SCSI interface is implemented using the high speed Adaptec AIC 7860 SCSI controller attached to the on-board PCI bus. SCSI bus termination is implemented with active terminators. Data rates of up to 20 megabytes/second are achievable. An Adaptec SCSI BIOS is included in the on-board Flash memory device. The SCSI interface is compatible with current SCSI standards and is ASPI-compatible.

PCI Flat-Panel/CRT Display Controller

A powerful and flexible PCI video display controller supports both flat panels and CRTs, and offers full software compatibility with all popular PC video standards (VGA, Super VGA, and VESA). All standard resolutions up to 1600 x 1200 pixels and up to 16.7 million colors are supported. Refer to Chapter 4 for detailed video specifications. 2M bytes of SDRAM video memory are standard. The display controller features:

- **High-speed PCI Architecture.** The video controller provides an optimized PCI-bus path between the CPU and SDRAM video memory.

- **Graphical User Interface (GUI) Accelerator.** The Chips and Technologies HiQVideo™ Multimedia Accelerator dramatically boosts the performance of Windows® and many graphics-intensive applications.

- **Full IBM VGA compatibility.** VESA DPMS and DCC standards supported.

- **TV Video Display.** Integrated composite NTSC/PAL support with flicker reduction circuitry. Simultaneous TV and Flat-panel display is supported.

- **Color Flat-Panel Support.** Up to 16.7 million colors can be displayed on color TFT LCD flat panels and color STN LCD panels. Uses the Chips and Technologies TMED™ algorithm to optimize low-cost STN panel displays for 256 gray shades and 16.7M colors.

- **Display Centering and Stretching.** A variety of automatic display centering and stretching techniques can be employed when running lower resolution software on a higher resolution display. Supports 16:9 aspect-ratio panels.

- **Automatic Power Sequencing Controls.** The video controller provides the signals to safely sequence the power and data signals to LCD flat panels.

- **Low-Power Modes.** Advanced Power Management (APM) features are implemented in the power control logic.

- **ZV Port Support.** The standard Chips and Technologies ZV input port is supported.

- **Standard Panel Support in the ROM BIOS.** The on-board video BIOS supports up to 16 of the most popular flat-panel displays, selectable from Setup.

- **Optional hardware modules may be installed.** These include an optional NTSC/PAL module to allow direct connection of NTSC or PAL video inputs, an optional module supporting either PanelLink or LVDS adapter modules, an optional module to convert 3.3V signals to 5.0V signals to support 5 Volt LCD Panels, and an adjustable LCD bias power supply to supply Vee for LCD panels.

100 MB/s Ethernet LAN Interface

The Ethernet subsystem is based on the Am79C972 PCnet™ Fast+ Enhanced 10/100 PCI Ethernet Controller. It fully supports IEEE 802.3 Ethernet standards — 10BaseT and 100BaseT. The Am79C972 supports an MII (Media Independent Interface) 10/100 Mb/s network port. For maximum performance, the Ethernet controller uses the PCI bus for system-side data transfers. Features of this Ethernet controller include:

- On-board DMA (programmable)
- Support for full-duplex operation
- Auto-negotiable data rate (10/100 Mb/s)
- Supports PC97, PC98, and Net PC standards

Enhanced Reliability

Reliability is especially important in embedded computer systems. Ampro, specializing in embedded system computers and peripherals, knows that embedded systems must be able to run reliably in rugged, hostile, and mission-critical environments without operator intervention. Over the years, Ampro has evolved system designs and a comprehensive testing program to ensure a reliable and stable system for harsh and demanding applications. These include:

ISO 9001 Manufacturing. Ampro is a certified ISO 9001 vendor.

Regulatory testing. Knowing that many embedded systems must qualify under EMC emissions and suscepibility testing, Ampro designs boards with careful attention to EMI issues. Boards are tested in standard enclosures to ensure that they can pass such emissions tests. Tests include European Union Directives EN55022 and EN55011 (for EMC), EN61000-4-2 (for ESD), ENV50140 (for RF Susceptibility), and EN61000-4-4 (for EFT). Conducted Emissions testing is also performed at US voltages per FCC Part 15, Subpart J (the European Union Directives are otherwise compatible with Part 15 testing).

Wide-range temperature testing. Ampro Engineering qualifies all of its designs by extensive thermal and voltage margin testing.

Voltage Reduction Technology (VRT) CPU for greater high temperature tolerance. The board uses the latest low-voltage CPU technology to extend its temperature range and reduce cooling requirements. In addition, this module utilizes active thermal monitoring features to reduce the CPU temperature.

Shock and Vibration Testing. Boards intended for use in harsh environments are tested for shock and vibration durability to MIL-STD 202F, Method 213-I, Condition A (three 50G shocks in each axis) and MIL-STD 202F, Method 214A, Table 214-I, Condition D (11.95B random vibration,

100 Hz to 1000 Hz). (Contact your Ampro sales representative to obtain *Shock and Random Vibration Test Report for the Little Board/P5x CPU* for details.)

Software

The vast array of commercial and public-domain software for the IBM PC and PC/AT is usable in Little Board/P5*x*-based systems. You can use the most popular software development tools (editors, compilers, debuggers, etc.) for developing code for your application. With this software and the standard Ampro-supplied utilities and drivers, you can quickly tailor a system to your needs.

Use the board's Setup function for all system configuration. Setup information is stored in both the battery-backed CMOS RAM-portion of the real-time clock, and in a configuration EEPROM. Setup information is retained in the EEPROM even if the real-time clock battery loses power, ensuring reliable start-up.

Setup can be invoked by pressing the DEL key during the Power-On Self Test (POST). The contents of the EEPROM can be written and read from the DOS command line using a utility program, SETCMOS.EXE, available on the Little Board/P5*x* Utilities diskette.

Designing Little Board Systems

The Little Board/5P*x* CPU affords a great deal of flexibility in system design. You can build a system using only the Little Board, serial or parallel devices for input/output, and a solid-state disk drive.

On-board MiniModule Expansion

The simplest way to expand a Little Board system is with self-stacking Ampro MiniModules. MiniModules are available for a wide variety of functions. You can stack the MiniModules on the Little Board and avoid the need for bus cables, card cages, and backplanes.

When installed on the PC/104 expansion bus headers, expansion modules fit within the Little Board/P5*x*'s outline dimensions. Most Ampro MiniModule products have stackthrough connectors compatible with the PC/104 specification. You can stack several modules on the Little Board/P5*x*. Each additional module increases the thickness of the package by ~0.66 inches (~15 mm). Thus, a 3-module system fits within the outline of the Little Board and within a 2.4-inch vertical space. Figure 1– 1 shows an example of how PC/104 modules stack on the Little Board/P5*x*.
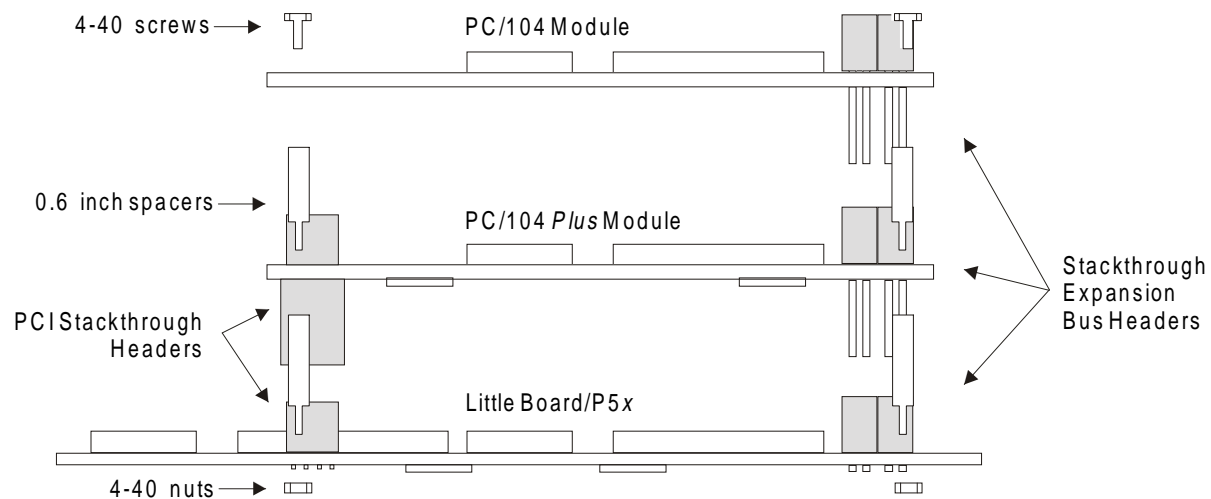
Figure 1– 1. Stacking PC/104 Modules on the Little Board/P5x

Using Standard PC and AT Bus Cards

Ampro offers several options that allow you to add conventional 8-bit and 16-bit ISA expansion cards to the Little Board/P5*x* system. Contact Ampro for further information about optional bus expansion products.

Little Board Development Platform And Quick Start Kit

Whatever your Little Board application, there will always be a need for an engineering development cycle. To help developers quickly assemble an embedded system, Ampro offers the Little Board Development Platform. It includes a power supply, 3.5 inch 1.44M floppy disk drive, IDE hard drive, speaker, I/O connectors, a backplane for ISA and PCI expansion cards, an I/O development board (described below), and mounting studs for the Little Board.

The Development Platform provides a "known good" environment for your development work. You can install the Little Board/P5*x*, MiniModules, or conventional expansion boards, keyboard, monitor, and I/O devices to quickly create a platform for your hardware and software engineering needs. Often, Development Platforms are used in repair and support facilities as well, and on the production floor for system test. Contact your Ampro sales representative for more information.

The Quick Start Kit includes cables, documentation, and software needed to develop an application with the Little Board. Unlike the Development Platform, you must supply the disk drives and power supply. Technical drawings for the cables provided in the Quick Start Kit are included in Appendix B.

There are other kits available from Ampro to aid in the development of your application. A Cable Kit that includes only the Little Board/P5*x* cable set is available. The latching clips that fit on the shrouded connectors on the Little Board to secure the cable connectors are available in another kit. The Literature Set that includes the Technical Manuals and Software is also available seperately.

Little Board/P5*x* Utility I/O Development Board

To facilitate I/O connections to the Little Board/P5*x* utility connectors, Ampro provides the Little Board/P5*x* Utility I/O Development Board. It is included in the Development Platform Kit and the Quick Start Kit.

The I/O Development Board provides connections for the USB ports, speaker, keyboard, front panel switches, external power supply connections, and so forth.

Figure 1– 2 is an illustration of the I/O Development board showing the connectors and switches
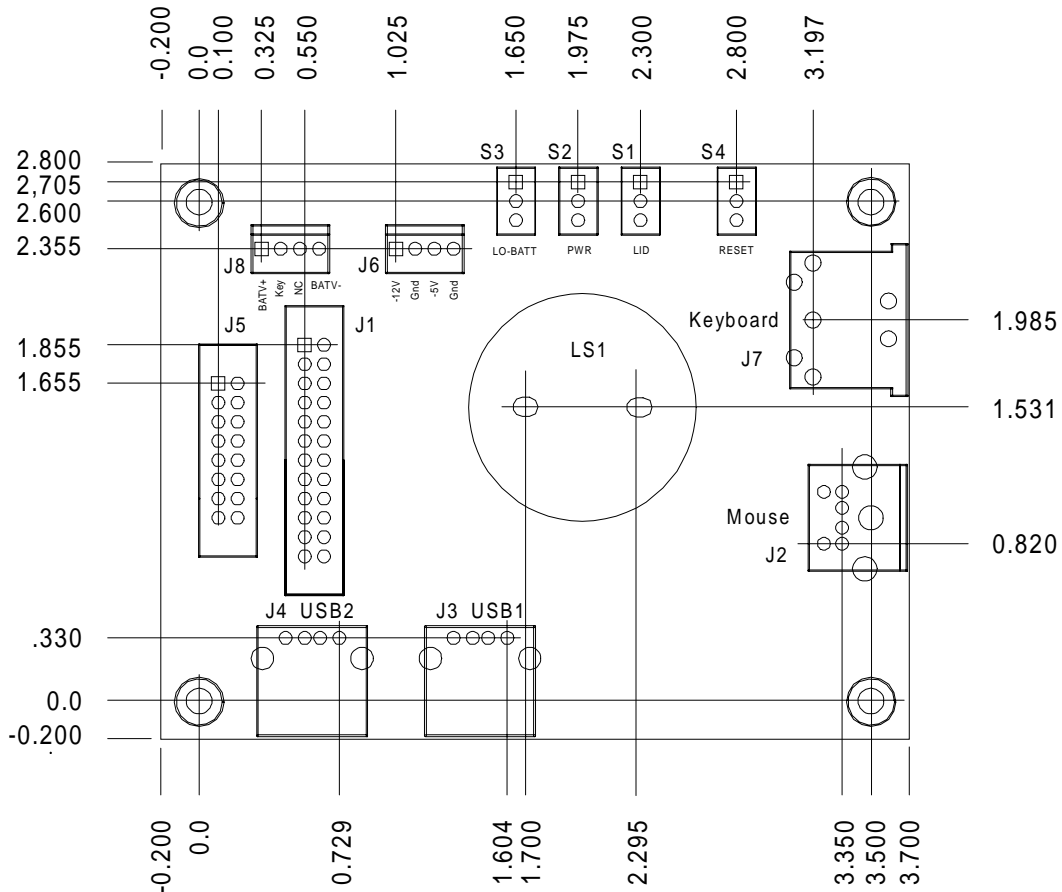
that are provided.

Figure 1– 2. I/O Development Board

Table 1– 1 summarizes the connectors available on the I/O Development Board.

Connector	Name	Description
J5	Utility 1	Connect to LB/P5*x* Utility 1 (J16)
J2	Mouse	Plug in PS/2 Mouse
J3	USB 1	Standard USB connector for USB 1
J4	USB 2	Standard USB connector for USB 2
J1	Utility 2	Connect to LB/P5*x* Utility 2 (J24)
J6	Power	Provides connections for -12V and -5V
J7	Keyboard	Plug in a standard PS/2 Keyboard
J8		Reserved - do not use

Table 1– 1. I/O Development Board Connector Summary

Connector Descriptions

The following sections describe the use of each connector on the I/O Development Board.

J5 — Utility 1

J5, the Utility 1 connector connects to the Little Board/P5*x* Utility 1 connector (J16). It provides connections to an on-board speaker, keyboard connector, reset switch, a connector for external -5V and -12V power supplies, and a power LED.

If you have the Ampro Quick Start Kit, connect a ribbon cable between J5 on the I/O Development Board and J16 on the Little Board.

If you install the Little Board on the Little Board Development Platform, it is not necessary to connect Utility 1 signals to the I/O Development Board. The Utility 1 features are already provided on the Development Platform.

J2 — Mouse

If you connect J1 to J24 on the Little Board, you can use J2 to connect a PS/2 mouse.

J3, J4 — USB

Connectors J3 and J4 provide connection to USB ports 1 and 2 respectively. These are standard shielded Type A connectors, the kind typically found on a host or hub. For details about the USB ports, refer to the Little Board/P5*x* Technical Manual. To use the USB ports, you must connect a cable from the I/O board's J1 connector to the Little Board's J24 connector.

J1 — Utilty 2

The Utility 2 connector (J1) connects to the Little Board/P5*x* Utility 2 connector at J24. It provides connections to the Universal Serial Bus (USB) ports (J3, J4), infrared interface (IrDA), and power management switches (S1, S2, and S3).

J6 — Power

If you connect J5 on the I/O board to J16 on the Little Board, you can use J6 to connect -5V and -12V power supplies to the Little Board. Table 1– 2 shows J6 wiring.

J6 Pin	Signal
1	-12 Volts
3	-5 Volts
2, 4	Ground

Table 1– 2. J6 Power Wiring

J7 — Keyboard

If you connect J5 on the I/O board to J16 on the Little Board, you can use J7 to connect a PS/2 keyboard. J7 is a standard 5-pin DIN connector.

Switch Descriptions (S1 – S4)

There are four switches on the I/O Development Board. They are identified by silkscreen designations S1, S2, S3, and S4. Table 1– 3 describes each switch function.

Switch	Name	Description
S1*	Lid	Power management input: causes an SMI to simulate a laptop lid closure.
S2*	Pwr	Power management input (push-button switch): when pushed for 6 seconds, it powers down the board. When pressed again, the board powers up.
S3*	Lo-Pwr	Power management input: causes an SMI to simulate a low-battery condition.
S4	Reset	Standard Reset signal to the Little Board
* For information about implementing S1, S2, and S3 functionality, contact Ampro Technical Support.		

Table 1– 3. I/O Development Board Switches

Figure 1– 3 is a block diagram of the Little Board/P5*x* architecture.
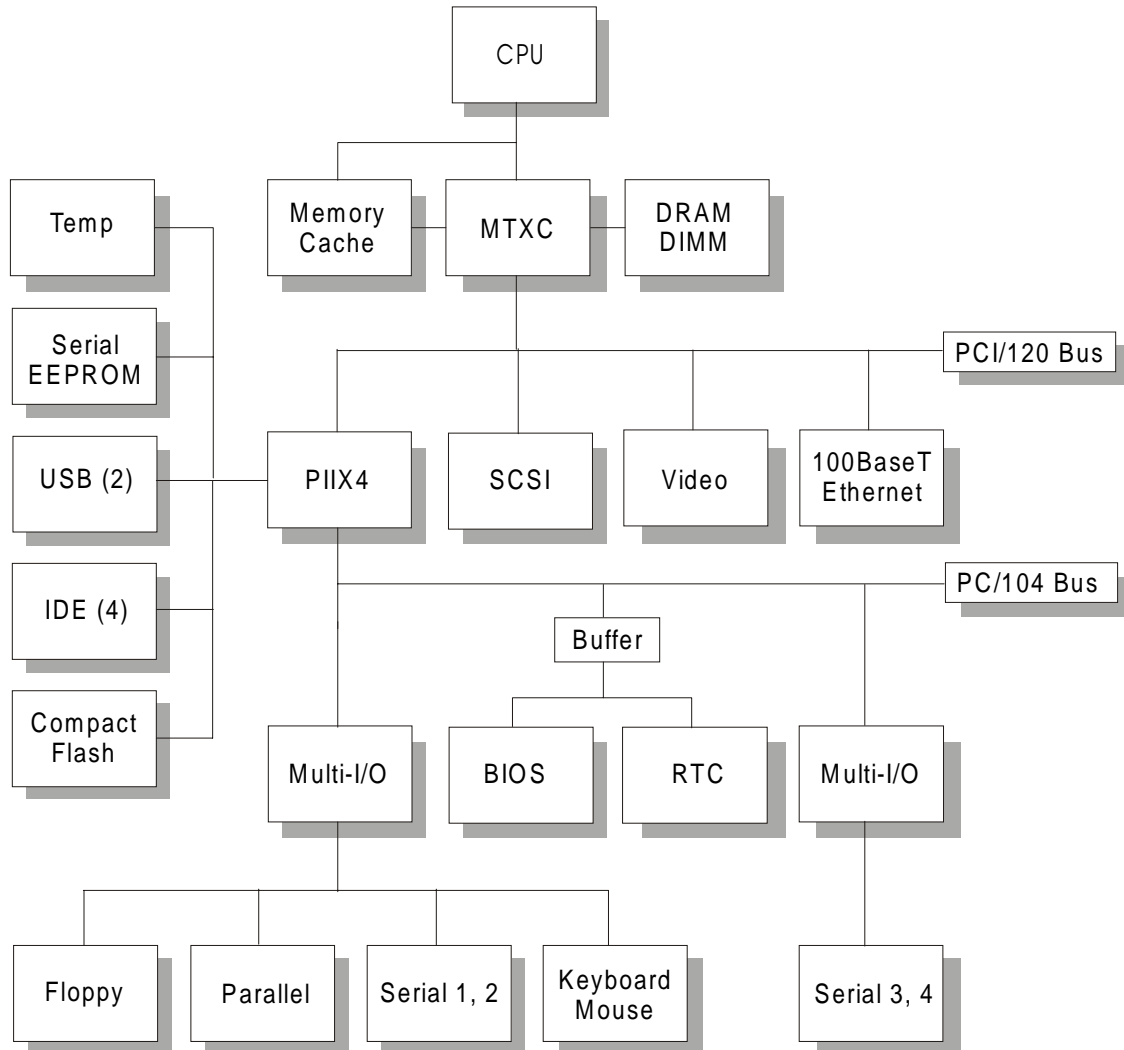
Figure 1– 3. System Block Diagram

Chapter 2

Product Reference

Overview

This chapter contains the technical information you will need to install and configure the Little Board/P5*x*. The information is presented in the following order:

Mounting Dimensions

Figure 2–1 shows the Little Board/P5*x* mounting dimensions.
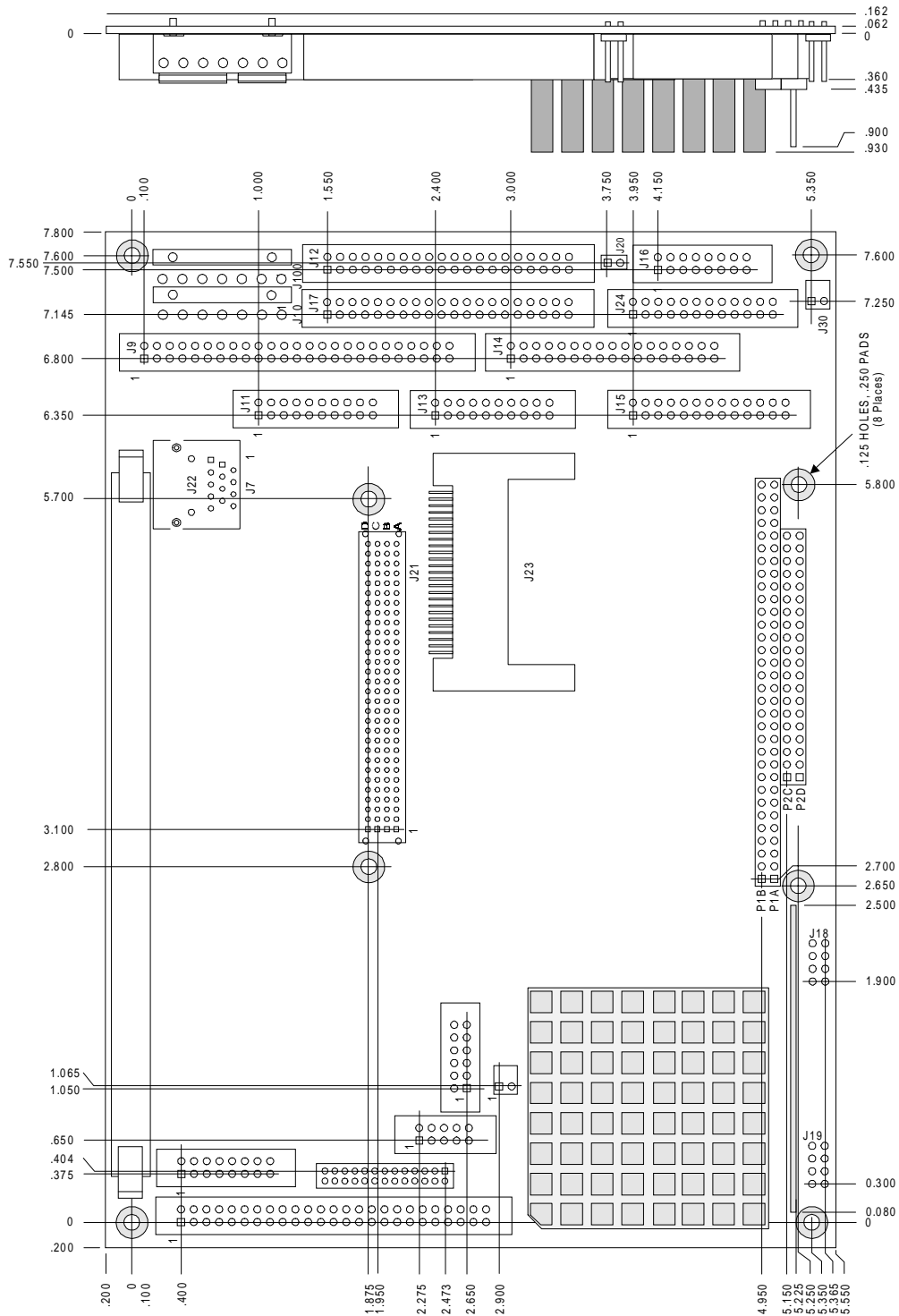
Figure 2– 1. Mounting Dimensions

Connector Summary

Refer to Figure 2– 1 and Figure 2– 2 for the locations of the connectors (P1, P2, J3 – J21) and configuration jumpers (W1 – W12). Table 2– 1 summarizes the use of the I/O connectors.

Each interface is described in its own section, showing connector pinouts, signal definitions, required mating connectors, and configuration jumper options.

Many of the connectors have a key pin removed. This allows you to block the corresponding cable connector socket to help prevent improper assembly. Table 2– 1 indicates which pins are key pins.

Table 2– 1. Connector Summary

Connector	Function	Size	Key Pin
P1 A/B	PC/104 Expansion Bus	64-Pin	B10
P2 C/D	PC/104 Expansion Bus	40-pin	C19
J3	Flat Panel Video	50-pin	None
J4	Vee Bias Supply Connector	12-pin	3, 10
J5	CRT Video	10-pin	None
J6	Video ZOOM	26-pin	None
J7	Ethernet Twisted Pair	RJ-45	Mechanical Key**
J9	SCSI Interface	50-pin	25
J10 (J100)	Power, +5V, +12V, +3.3V (J100 Alternate Connector)	7-pin Molex	Mechanical Key**
J11	Serial 1 and Serial 2	20-pin	None
J12	IDE1 Interface	40-pin	20
J13	Serial 3 and Serial 4	20-pin	None
J14	Floppy Interface	34-pin	6
J15	Parallel Port	26-pin	26
J16	Utility 1	16-pin	None
J17	IDE2 Interface	40-pin	20
J18, J19	CPU Power Supply (Factory)	12-, 8-pin	Mechanical Key**
J20	COM1 RS-485	2-pin	
J21	PCI Bus	120-pin	A1/D30*
J22	Ethernet Option	6-pin	None
J23	Compact Flash	50-pin	Mechanical Key**
J24	Utility 2	24-pin	None
J25	Flat Panel Video Extension	16-pin	None
J28	Fan Power	2-pin	None
J30	Support signals for External Power Management (Option)	2-pin	None
*A1 and D30 keys are used to key the PCI connector for 5V or 3.3V respectively.			
**Connector provides keying mechanism.			

Most I/O connectors are shrouded dual-row male headers for use with flat ribbon (IDC) female connectors and ribbon cable. Ampro recommends that you use "center-bump polarized" connectors to prevent accidentally installing cables backwards. Use non-strain-relief connectors to stay within the vertical height envelope shown in Figure 2– 1.

If you use the recommended mating connectors, you can install retaining clips to secure a cable to its connector. (The connector heights of some brands do not allow the use of retaining clips.) Retaining clips are especially useful in high-vibration environments.

You can also design a PC board assembly, made with female connectors in the same relative positions as the Little Board's connectors, to eliminate cables, meet packaging requirements, add EMI filtering, or customize your installation in other ways. Precise dimensions for locating connectors are provided in Figure 2– 1.

The ISA portion of the PC/104-*Plus* expansion bus appears on connector J1 (A, B, C, D). You can expand the system with on-board MiniModule products or other PC/104-compliant expansion modules. These modules stack directly on the connectors, or use conventional or custom expansion hardware, including solutions available from Ampro.

The PCI portion of the PC/104-*Plus* expansion bus appears on connector J21. It uses a 2 mm. 4-row connector called out in the PC/104-*Plus* draft specification. Like the J1 connectors, J21 has both male and female connections, allowing for "stackthrough" assembly.

If you plan to use the on-board video controller with a flat-panel LCD screen requiring a Vee bias voltage supply, you can install Ampro's optional LCD Bias Supply board on connector J4. This board can be jumpered to supply positive or negative Vee from ±15V to ±35V (adjustable). (Only certain LCD panels require an external Vee supply.)
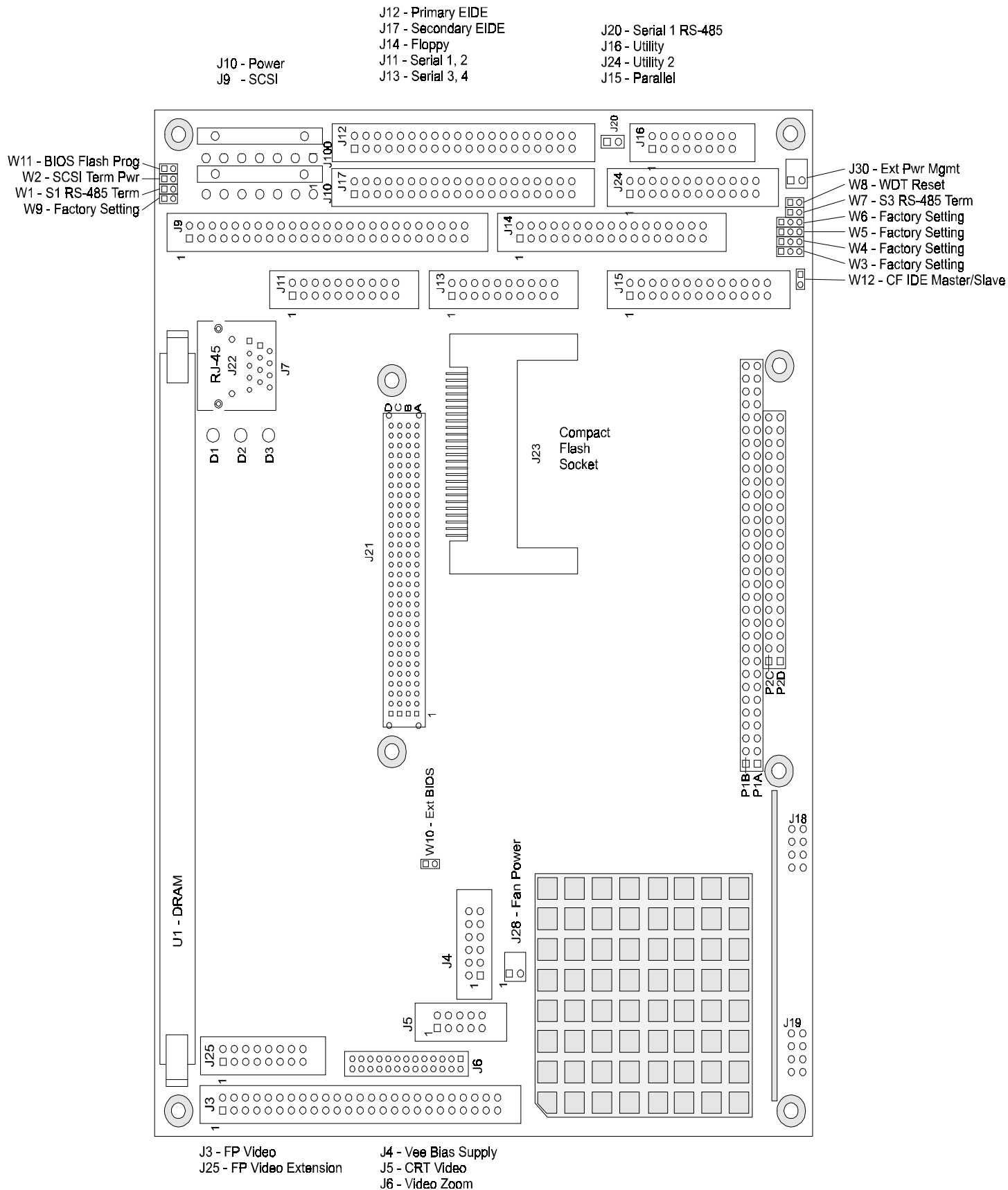
Figure 2– 2. Connector and Jumper Locations

J12 - Primary EIDE
J17 - Secondary EIDE
J14 - Floppy
J11 - Serial 1, 2
J13 - Serial 3, 4

J20 - Serial 1 RS-485
J16 - Utility
J24 - Utility 2
J15 - Parallel

J10 - Power
J9 - SCSI

W11 - BIOS Flash Prog
W2 - SCSI Term Pwr
W1 - S1 RS-485 Term
W9 - Factory Setting

J30 - Ext Pwr Mgmt
W8 - WDT Reset
W7 - S3 RS-485 Term
W6 - Factory Setting
W5 - Factory Setting
W4 - Factory Setting
W3 - Factory Setting
W12 - CF IDE Master/Slave

J3 - FP Video
J25 - FP Video Extension

J4 - Vee Bias Supply
J5 - CRT Video
J6 - Video Zoom

Jumper Summary

Ampro installs option jumpers in default positions so that in most cases the Little Board/P5*x* requires no special jumpering for standard AT operation. You can connect the power and peripherals and operate it immediately.

Jumper-pin arrays are designated W1, W2, and so forth. Jumper pins are spaced 2 mm apart. A square solder pad identifies pin 1 of each jumper array. Table 2– 2 is a summary of jumper use. Factory settings are shown in the Default column. Some jumpers are set at the factory to configure options that are not user-settable. These are indicated in the table. Do not change these settings.

Table 2– 2. Configuration Jumper Summary

Jumper Group	Function	Default
W1	Serial 1 RS-485 100 Ohm Termination ON=Terminated, OFF=Unterminated	OFF
W2	SCSI Termination Power ON Connects Termination Power to SCSI Bus	OFF
W3, W4, W5	Bus/CPU Speed Setting (Factory settings - do not change)	As Req'd.
W6	CPU Voltage (Factory setting - do not change) 1/2=3.3V 2/3=2.5V	As Req'd
W7	Serial 3 RS-485 100 Ohm Termination (this is a factory option. May not be implemented on your board) ON=Terminated, OFF=Unterminated	OFF
W8	Watchdog timer reset enable ON=Enabled, OFF=Disabled	OFF
W9	System Bus Frequency Selection (Factory option - do not change) ON=60 MHz, OFF=66 MHz	OFF
W10	External BIOS Board Enable/Cable Connection ON=Normal, OFF=External Cable	ON
W11	BIOS Flash EPROM Programming Power ON=Programming enabled OFF= Programming disabled	ON
W12	Compact Flash IDE Master/Slave ON=Master, OFF=Slave	ON

DC Power

The power connector J10 is a 7-pin polarized connector. Refer to Table 2– 3 for power connections and Table 2– 4 for mating connector information.

Caution

Be sure the power plug is wired correctly before applying power to the board! See Table 2– 3.

Table 2– 3. Power Connector (J10)

Pin	Signal Name	Function
1, 7	+5VDC	+5VDC ±5% input
2, 3, 6	Ground	Ground return
4	+12VDC	+12VDC ±5% input
5	+3.3VDC	+3.3V ±5% input (Only required for some PCI expansion boards)

Table 2– 4. J10 Mating Connector

Connector Type	Mating Connector
DISCRETE WIRE	MOLEX HOUSING 09-50-0073 Pins 08-52-0071

Power Requirements

The Little Board/P5*x* requires only +5VDC (±5%) for operation. The voltage required for the RS-232 ports is generated on-board from the +5VDC supply. An on-board +5V to +12V converter supplies power for programming the BIOS Flash EPROM. An on-board low-voltage power supply circuit provides power to low-voltage CPUs and certain other on-board components. An optional Vee power supply can be attached to supply Vee power to an LCD flat panel.

The exact power requirement of the Little Board/P5*x* system depends on several factors, including the installed memory devices, SCSI bus termination, CPU speed, the peripheral connections, and which, if any, MiniModule products or other expansion boards are attached. For example, the keyboard draws its power from the board, and there can be some loading from the serial, parallel, and other peripheral ports. Consult the specifications in Chapter 3 for the basic power requirements of your model.

Other Voltages

There may be a requirement for an external +12 volt supply, depending on what peripherals you connect to the Little Board system. For instance, +12V is required for most flat-panel backlight power supplies. You can connect a +12V supply to the Little Board module through the power

connector, J10. This will supply +12V to the ISA and PCI portions of the PC/104 expansion busses. Similarly, you can connect -12V and -5V to J16, the Utility Connector, to supply those voltages to both expansion busses. Pinouts for the Utility Connector are provided in Table 2- 45.

If a PCI expansion card requiring 3.3V is installed, that voltage can be connected to J10-5 to supply power to J21, the PCI bus interface connector.

Switching Power Supplies

If you use a switching power supply, be sure it regulates properly with the load your system draws. Some switching power supplies do not regulate properly unless they are loaded to some minimum value. If this is the case with your supply, consult the manufacturer about additional loading, or use another supply or another type of power source (such as a linear supply, batteries, etc.). The minimum power for the Little Board/P5*x* appears in the power specifications in Chapter 1.

Powerfail NMI

The Little Board/P5*x* includes a circuit that can sense a power failure. If the +5V power supply falls below ~4.7 V, the powerfail logic produces a non-maskable interrupt (NMI).

When an NMI occurs, the BIOS detects the NMI and displays the message "Power Fail NMI" on the console. At this point you have two options via the keyboard. You can mask the NMI and continue (the PC architecture provides a mask bit for the non-maskable interrupt), or reboot the system.

If you want your system to respond to the NMI, you can provide an NMI handler in your application, and patch the NMI interrupt vector address to point to your routine.

Backup Battery

Real-Time Clock Battery

The real-time clock backup battery on the Little Board/P5*x* should last 10 years under normal usage.

Cooling Requirements

The Pentium CPU, DRAM module, video controller, and core logic chips draw most of the power and generate most of the heat. The board is designed to support various speed versions of the Pentium from 133 MHz to 266 MHz with 66 MHz clocks. Since CPU speeds offered by manufacturers are continuing to increase, contact your Ampro sales representative for the currently available speeds.

A heat sink or fan assembly is provided for the CPU. The fan gets its +5V power from J28. J28 power can be controlled by a CPU thermal sensor, as described below.

Table 2– 5 shows the maximum ambient temperature for a CPU case temperature of 70 °C at various airflow values for various models of the Little Board/P5x. (Values for the 133, 166, and 266 MHz CPUs are given for an 85 °C CPU case temperature.) These numbers are based on typical power consumption.

Table 2– 5. Airflow vs. Maximum Ambient Temperature

Processor Speed	Still Air (°C)	200 LFM (°C)	400 LFM (°C)	Fan/Heatsink (°C)
200 MMX	15.3	41.5	55.4	59.1
233 MMX	10.8	39.2	54.2	58.2
133 VRT	55.0	69.4	77.0	79.0
166 Tillamook	63.3	73.2	79.2	80.7
266 Tillamook	51.3	67.5	76.0	78.3
Thermal Resistance of a Typical .65" Heat Sink and Fan/Heatsink Combination	7.5	3.9	2.0	1.5

Thermal Sensor

A thermal sensor is attached to the board under the Pentium CPU. It senses when the CPU temperature exceeds its upper temperature threshold. Running the CPU at a temperature higher than this can damage the CPU chip and should be avoided.

When triggered, the temperature sensor signals the BIOS to reduce the CPU clock speed. This speed reduction remains in effect until the processor has cooled to the lower sensor limit.

Fan Switch

Power to the CPU cooling fan can be turned on or off under control of the board's thermal management logic. To take advantage of the automatic fan switch, connect the fan to J28. Figure 2–3 illustrates how to connect the fan to J28. The pinout of J28 is shown in Table 2– 6. The fan can be turned on all of the time or controlled by the thermal sensor. This selection can be made in the BIOS Setup screen.
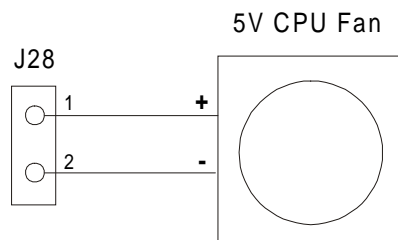
Figure 2– 3. Connecting a CPU Fan to J28

Table 2– 6. Fan Power Connector (J28)

J28 Pin	Function
1	+5V Power
2	Switched Ground

System Memory

The module supports a single standard 64-bit DIMM position (168-pin) for the 64-bit data path to the Pentium processor. Both EDO and SDRAM memory types are supported. Buffered DRAM is not supported. You can install from 16M bytes to 256M bytes, depending on your memory needs.

The ROM BIOS automatically detects the size of the installed memory module and configures the system accordingly at boot time. (No jumpering or manual configuration is required.) The amount of memory the BIOS measured can be displayed by running Setup.

You can use EDO DRAMs or SDRAMS with access times of 60 nS or less.

Memory parity and error correction (ECC) are not supported by the chip set used on the Little Board/P5x.

DRAM memory is allocated in the system as shown in Table 2– 7.

Table 2– 7. System Memory Map

Memory Address	Function
FE0000h - FFFFFFh	Duplicates BIOS at 0E0000-0FFFFFh.
100000h - FDFFFFh	Extended memory
0E0000h - 0FFFFFh	128K ROM BIOS
0D0000h - 0DFFFFh	BIOS extension option, if enabled. Otherwise, free.
0CB000h - 0CFFFFh	USB
0C0000h - 0CAFFFh	Video BIOS (44K)
0A0000h - 0BFFFFh	Normally contains video RAM, as follows: CGA Video: B8000-BFFFFh Monochrome: B0000-B7FFFh EGA and VGA video: A0000-AFFFFh
000000h - 09FFFFh	Lower 640K DRAM

ROM BIOS

The standard BIOS is installed in a 256K byte Flash device at the factory. The top 128K bytes of the Flash device is reserved for the system BIOS, located at 000E0000h – 000FFFFFFh and mirrored at the top of the memory address space. The remaining 128K bytes are mapped only to the top of memory.

A utility program, PGM5X.COM, can be used to program the on-board Flash device. It can be used to update the system BIOS, video BIOS, SCSI BIOS, or user area. The utility is included on the utility diskette that accompanies the Ampro Development Platform. The diskette includes documentation about how to use the program.

Shadowing

To improve system performance, the contents of the ROM BIOS and video BIOS are copied into DRAM for execution ("shadowed"), where they are accessed as 64-bit wide data. Shadowing a BIOS ROM substantially enhances system performance, especially when an application or operating system repeatedly accesses the BIOS. Shadowing for both the ROM BIOS and the video BIOS is built into the Ampro Extended BIOS. There is no user setting.

BIOS Recovery

If the BIOS Flash device somehow becomes corrupted, the Little Board/P5x may not boot. In this case, the BIOS will have to be reprogrammed. A disk with an image of the current BIOS along with the Utility PGM5X.COM may be used to restore the BIOS image.   Before this can be done, the Little Board/P5x needs to be Booted and running DOS.

Ampro provides a BIOS Extension Board that can be used to temporarily supply a working BIOS. Contact Ampro for information on the BIOS Extention Board (ACC-EBB-Q-72).

The BIOS Extension Board is a MiniModule that has an on-board BIOS that can replace the one in the on-board BIOS Flash device. This BIOS is contained in a socketed DIP memory device. Once the BIOS Extension Board is installed, the Little Board/P5x can be booted using this replacement BIOS. Then, by using the PGM5X.COM utility, the Flash device can be repaired, and working firmware programmed into it once again.

To recover a BIOS using the BIOS Extension Board:

- Install a Jumper on W11 if there is not one already there.
- Remove the shunt on W10.
- Plug the BIOS Extension Board into the PC/104 connectors on the CPU.
- Plug the two-wire cable into J1 on the BIOS Extension Board and plug the other end into W10 of the CPU.
- Power the system up. The CPU should boot. If it does not, the Little Board/P5x should be returned to Ampro for servicing.
- Once the system has booted, remove the cable from W10 on the CPU.
- Replace the shunt on W10 of the CPU.
- Use PGM5X.COM to write a new copy of the BIOS or firmware to the Flash device.
- Remove W11 if it is desired to write protect the BIOS.

The Little Board/P5x should function normally after this procedure.

Interrupt and DMA Channel Usage

The PC architecture provides several interrupt and DMA control signals. When you expand the system through the ISA portion of the PC/104-*Plus* bus with MiniModule products or plug-in cards that require either interrupt or DMA support, you must select which interrupt or DMA channel to use. Typically this involves switches or jumpers on the expansion module. In most cases, these are not shared resources. It is important that you configure the new module to use an interrupt or

DMA channel not already in use. For your convenience, Table 2– 8 and Table 2– 9 provide a summary of the normal interrupt and DMA channel assignments on the Little Board/P5x.

The PCI bus uses four interrupts (INTA*, INTB*, INTC*, and INTD*). These interrupts are mapped to any of the available ISA interrupts by the BIOS. If an expansion card has multiple functions, then more interrupts may be required. You can set the priority in which interrupts are assigned on Setup 6 — PCI Configuration Setup.

Table 2– 8. Interrupt Channel Assignments

Interrupt	Function
IRQ0	ROM BIOS clock tick function, from Timer 0
IRQ1	Keyboard interrupt
IRQ2	Cascade input for IRQ8-15
IRQ3	Serial 2, Serial 4 (shared)
IRQ4	Serial 1, Serial 3 (shared)
IRQ5	PCI
IRQ6	Floppy controller
IRQ7	Parallel port (option)
IRQ8	Reserved for battery-backed clock alarm
IRQ9	PCI
IRQ10	PCI
IRQ11	PCI
IRQ12	PS/2 Mouse
IRQ13	Reserved for coprocessor
IRQ14	Primary IDE hard disk controller
IRQ15	Secondary IDE hard disk controller
Note: IRQs for the Ethernet, Video, and SCSI interfaces are automatically assigned by the BIOS plug and play logic.	
PCI Interrupts assigned during initialization cannot be used by non-PCI devices.	

Table 2– 9. DMA Channel Assignments

Channel	Function
0	Available for 8-bit transfers
1	Available for 8-bit transfers
2	Floppy controller
3	Available for 8-bit transfers
4	Cascade for channels 0-3
5	Available for 16-bit transfers
6	Available for 16-bit transfers
7	Available for 16-bit transfers

Battery-Backed Clock

An AT-compatible battery-backed real-time clock (with CMOS RAM) is standard on the Little Board/P5*x*. A 3.0 volt Lithium battery soldered to the board powers the clock. Battery drain for the clock is less than 0.4 uA. This battery will support the clock for more than 10 years of normal usage.

The factory initializes the real-time clock and various parameters in the configuration memory for a standard configuration. The factory sets the date and time, but it may not be set for your time zone. Use Setup to change these values as needed.

The contents of the configuration memory are also stored in an on-board EEPROM. The ROM BIOS reads the EEPROM to get configuration information if the CMOS RAM data is lost. This means that the board will function if the battery fails. Note that without a battery, the real-time clock date and time will not be correct.

Serial Ports

The Little Board/P5x provides four standard RS-232C serial ports, Serial 1 and Serial 2 at J11, and Serial 3 and Serial 4 at J13.

All ports support software selectable standard baud rates up to 115.2K bits/second, 5-8 data bits, and 1, 1.5, or 2 stop bits. Note that the IEEE RS-232C specification limits the serial port to 19.2K bits/second on cables up to 50 feet in length.

I/O Addresses and Interrupt Assignments

The serial ports appear at the standard port addresses as shown in Table 2– 10. Each serial port can be independently disabled using the Setup function, freeing its I/O addresses for use by other devices installed on the PC/104 and PCI expansion buses.

Table 2– 10 also shows the IRQs assigned to each serial port. Note that these interrupts are shared resources via serial interrupt protocol. (They do not have PC/104-type interrupt sharing circuits, as defined in the PC/104 specification.)

Table 2– 10. Serial Port I/O Addresses and Interrupts

Port	I/O Address	Interrupt
Serial 1	3F8h - 3FFh	4
Serial 2	2F8h - 2FFh	3
Serial 3	3E8h - 3EFh	3, 4, 5, 7, 9, 10, 11, 12
Serial 4	2E8h - 2EFh	3, 4, 5, 7, 9, 10, 11, 12

When a serial port is disabled, its I/O addresses and IRQ are available to other peripherals installed on the PC/104 expansion bus. You can disable any of the serial ports using Setup.

ROM-BIOS Installation of the Serial Ports

Normally, the ROM BIOS supports Serial 1 as the DOS COM1 device, Serial 2 as the DOS COM2 device, and so on. If you disable a serial port, and there is no substitute serial port in the system, then the ROM-BIOS assigns the COMn designations in sequence as it finds the serial ports, starting from the primary serial port and searching to the last one, Serial 4. Thus, for example, if Serial 1 and Serial 3 are disabled, the ROM-BIOS assigns COM1 to Serial 2 and COM2 to Serial 4.

Serial Port Connectors (J11, J13)

Serial 1 and Serial 2 appear on connector J11; Serial 3 and Serial 4 appear on connector J13. Table 2– 11 gives the connector pinout and signal definitions for J11 and J13. Both connectors are wired the same.

In addition, the table indicates the pins to which each signal must be wired for compatibility with DB25 and DB9 connectors. The serial port pinout is arranged so that you can use a flat ribbon cable between the header and a standard DB9 connector. Split a 20-wire ribbon cable into two 10-wire

sections, each one going to a DB9 connector. Normally PC serial ports use male DB connectors.
Table 2– 12 shows the manufacturer's part number for mating connectors.

Table 2– 11. Serial Port Connectors (J11, J13)

Ports	Pin	Signal Name	Function	In/Out	DB25 Pin	DB9 Pin
Serial 1 (J11) or Serial 3 (J13)	1	DCD	Data Carrier Detect	IN	8	1
	2	DSR	Data Set Ready	IN	6	6
	3	RXD	Receive Data	IN	3	2
	4	RTS	Request To Send	OUT	4	7
	5	TXD	Transmit Data	OUT	2	3
	6	CTS	Clear to Send	IN	5	8
	7	DTR	Data Terminal Ready	OUT	20	4
	8	RI	Ring Indicator	IN	22	9
	9	GND	Signal Ground	-	7	5
	10	N/A	No Connection	-	-	-
Serial 2 (J11) or Serial 4 (J13)	11	DCD*	Data Carrier Detect*	IN	8	1
	12	DSR	Data Set Ready	IN	6	6
	13	RXD	Receive Data	IN	3	2
	14	RTS	Request To Send	OUT	4	7
	15	TXD	Transmit Data	OUT	2	3
	16	CTS	Clear to Send	IN	5	8
	17	DTR	Data Terminal Ready	OUT	20	4
	18	RI	Ring Indicator	IN	22	9
	19	GND	Signal Ground	-	7	5
	20	TXT	TxD at TTL level	-	-	-

Table 2– 12. J11 and J13 Mating Connector

Connector Type	Mating Connector
RIBBON	3M 3421-7600
	Latching Clip 3505-8020
DISCRETE WIRE	MOLEX HOUSING 22-55-2202
	PIN 16-02-0103

RS-485 Option

You can configure Serial 1 to operate as a two-wire RS-485 port. Use of the RS-485 option offers a low cost, easy-to-use communications and networking multi-drop interface that is suited to a wide variety of embedded applications requiring low-to-medium-speed data transfer between two or more systems.

Note

When you configure Serial 1 for RS-485, you cannot use the port for RS-232.

Serial 1's RS-485 interface appears on J20, a two-pin connector. The pinout for J20 is shown in Table 2– 13. Table 2– 14 shows a compatible mating connector to J20.

Table 2– 13. Serial 1 RS-485 Connector (J20)

J20 Pin	Signal
1	-I/O
2	+I/O

Table 2– 14. J20 Mating Connector

Connector Type	Mating Connector
Discrete Wire (Locking Connector)	MOLEX Housing 22-01-2027 Pin 08-55-0102

The RS-485 interface specification requires that both ends of the twisted-pair cable be terminated with 100 ohm resistors. You can terminate the RS-485 interface on J20 with a resistor provided on the LittleBoard/P5*x*. To terminate the line, install a jumper on W1, as shown in Table 2– 15.

Table 2– 15. RS-485 Termination

W1	Result
On	Connects a 100 ohm termination resistor between J20-1 and J20-2.
Off	No termination

Serial TTL Option

Serial 2 and Serial 4 can be configured for TTL operation. Of the serial ports' output signals, just the transmit (TxD) is supported for TTL. All of the serial ports' input signals are supported by virtue of the fact that the inputs of the RS-232C buffers used on the Little Board/P5*x* can function as TTL inputs.

The TxD signal for Serial 2 appears on J11-20. The TxD signal for Serial 4 appears on J13-20. The other serial port signals appear in J11 and J13 as shown in Table 2– 11.

Ampro Custom Serial Features

The Ampro extended BIOS provides custom serial port features useful in embedded applications.

■ The *serial console* feature enables you to operate the Little Board/P5*x* from a standard ASCII terminal, replacing the standard keyboard and display devices. See *Serial Console Features*, below, for a description of the serial console capabilities.

■ The *serial boot* facility enables the Little Board/P5*x* to boot from code downloaded through a serial port in a manner similar to booting from a local hard disk or from a network.

■ The *serial download* feature permits updating the OEM Flash memory device over a serial port.

Refer to Ampro Application Note AAN-9403 for a complete description of these features. Refer to the Ampro Common Utilities manual for descriptions of SERLOAD and SERPROG, utility programs used to support serial booting and serial downloading.

Serial Console Features

You can connect a device, such as an ASCII video terminal or PC running a video terminal emulation program, to either serial port to act as your system console.

To use the serial console features, connect a serial console device to Serial 1 or Serial 2. Use Setup to enable the serial console feature.

When enabled, the serial console is set up for:

■ 9600 baud
■ No parity
■ 8 bits
■ One stop bit

To use an ASCII terminal as the console device for your system, set the serial baud rate, parity, data length, and stop bits of the terminal to match the serial console settings.

For proper display of Setup and POST messages from the BIOS, you must use an IEEE-compatible terminal or terminal emulation program that implements the standard ASCII cursor commands. The required commands and their hexadecimal codes are listed in Table 2– 16.

Table 2– 16. Required Cursor Commands

Hex	Command
08	Backspace
0A	Line Feed
0B	Vertical Tab
0C	Non-destructive Space
0D	Carriage Return

Note

Some programs that emulate an ASCII terminal do not properly
support the basic ASCII command functions shown in Table 2– 16.
Ampro provides a suitable PC terminal emulator program, TVTERM,
on the Common Utilities diskette.

After booting this system, the keyboard and screen of the serial terminal become the system
console. Note that the programs you execute via the serial terminal must use ROM BIOS video
functions (rather than direct screen addressing) for their display I/O.

Note

DOS programs that write directly to video RAM will not display
properly on a serial console device.

Using a Standard PC Keyboard

If you have both a serial terminal and a standard keyboard attached to your system at the same
time, both keyboards will function.

Using Arrow Keys During Setup

During Setup, the serial console arrow keys and function keys must be simulated.

The **arrow keys** are simulated with the substitute keystrokes shown in Table 2- 17.

Table 2– 17. Arrow Key Substitutions

Function	Substitute Keys
Up	^ or Ctrl e
Down	v or Ctrl x
Right	> or Ctrl d
Left	< or Ctrl s
PgUp	Ctrl r
PgDn	Ctrl c

To simulate the function keys, enter two keystrokes, an "F" followed by the function key number.
Thus, function key F3 is simulated with the literal "F3" typed on the keyboard. (Don't type the
quotes). F10 is simulated with "F0".

Note that these keystroke simulations are only valid during Setup, not during normal operation.

COM Port Table

When the system boots under DOS, the serial ports are initialized to 9600 baud (typical). To
preserve the selected console port parameters stored in Setup, the Ampro ROM BIOS deletes the
selected console port from the internal COM port table, normally used by DOS to locate the serial

ports. With the port deleted from the COM port table, DOS cannot change its parameters. Because it is not listed in the BIOS COM port table, it is not assigned a COMn designation (COM1, COM2, etc.).

Universal Serial Bus (USB) Ports

The Universal Serial Bus connects USB devices with a USB host, in this case, the Little Board/P5*x*. The USB physical interconnect is a tiered star topology, or tree, consisting of hubs and USB devices. Each USB segment is a point-to-point connection between hubs or between hubs and USB devices. The entire tree can support up to 127 USB devices. The USB interface standard is intended for keyboards, mice, modems, digitizer pads, and other low- to medium-speed peripherals.

Each USB interface is implemented as a two-wire differential pair for data, a power wire, a ground wire, and a shield wire. The USB port signals appear on J24, the Utility2 connector, as shown in Table 2– 18.

Table 2– 18. USB Port Pinout on Utility2 Connector

J24 Pin	Signal Name	Function
15	USBPWR1	USB1 +5 Volt Power
17	USBP-1	USB1 Data-
19	USBP+1	USB1 Data+
21	USBGND1	Ground
23	SHIELD1	Cable Shield for USB1
16	USBPWR2	USB2 +5 Volt Power
18	USBP-2	USB2 Data-
20	USBP+2	USB2 Data+
22	USBGND2	Ground
24	SHIELD2	Cable Shield for USB2

The bus can run at 12 Mbits/second or 1.5 Mbits/second, depending on a pull-up on the peripheral device. A 1.5 KOhm pull-up on the +data line sets the speed to 12 Mbits/second. A 1.5 KOhm pull-up on the -data line sets the speed to 1.5 Mbits/second.

The power to the peripheral device is current limited with a self-resetting fuse.

Infrared (IrDA) Interface

The Little Board/P5*x* infrared interface provides for a two-way wireless communications port using infrared as a transmission medium. The Little Board/P5*x* IrDA interface supports both SIR (Serial Infrared) and FIR (Fast Infrared) standards . The SIR standard allows serial communication at baud rates up to 115K Baud. The FIR standard allows data rates up to 4 Mbits/second.

Requirements for an IrDA interface

On the Little Board/P5*x*, the IrDA physical link hardware consists of an IR transmit encoder and IR receiver decoder. To implement an IrDA port, the OEM must supply an IR transducer, which consists of the output driver and IR emitter for transmitting, and the receiver IR detector. Particular IR transducers may require additional external components.

The IrDA port uses the second serial port to drive its internal encoder/decoder. When using the IrDA interface, you cannot use serial 2 as an RS-232 port.

IrDA Connector (Part of J24)

The IrDA port pinout is listed in Table 2– 19.

Table 2– 19. IrDA Interface Pinout

J24 Pin	Signal Name	Function
4	IRMODE / IRRXB	Fast IR Receive/Mode Output:
5	IRTX	IR Transmit
6	IRRXA	IR Receive (SIR)

There are two popular implementations of Fast IR. One uses a separate receive line capable of receiving at the higher data rate (up to 4 Mbytes/second). The other is implemented with a mode control line. When the IR port is set for high speed, the mode output line (FIR/M, J24-4) is high. This switches the external transceiver to high speed mode.

Multi-Mode Parallel Port

The Little Board/P5*x* incorporates a multi-mode parallel port. This port supports four modes of operation:

■ Standard PC/AT printer port (output only)

■ PS/2-compatible bi-directional parallel port (SPP)

■ Enhanced Parallel Port (EPP)

■ Extended Capabilities Port (ECP)

This section lists the pinout of the parallel port connector and describes how to configure it for its I/O port and interrupt assignments, how to assign a DMA channel to the port when operating in ECP mode. And programming information, including how to use the port for bi-directional I/O.

I/O Addresses and Interrupts

The parallel port functions are controlled by eight I/O ports and their associated register and control functionality. The Little Board/P5*x* parallel port is assigned to the primary parallel port address normally assigned to LPT1 and cannot be changed. You may disable the port in Setup to free the hardware resources for other peripherals.

The parallel port can be configured to generate an interrupt request upon a variety of conditions, depending on the mode the port is in. Assignment of an interrupt to the parallel port is optional, and its use depends on software requirements and which mode of operation you are using. IRQ 7 is the default parallel port IRQ assignment.

Table 2– 20 lists the parallel port addresses and IRQs.

Table 2– 20. Parallel Printer I/O Addresses and Interrupt

Selection	I/O Address	Interrupt
Primary	378h - 37Fh	7
Secondary	278h - 27Fh	5
Secondary	3BCh - 3BFh	7
Disable	None	None

ROM-BIOS Installation of Parallel Ports

Normally, the BIOS assigns the name LPT1 to the primary parallel port, and LPT2 to the secondary parallel port (if present), and so on. However, the BIOS scans the standard addresses for parallel ports and if it only finds a secondary port, it assigns LPT1 to that one. Therefore, if the Little Board's parallel port is enabled, it will be assigned LPT1 by the BIOS. If it is disabled and there is another parallel port in your system, that port will be assigned LPT1 by the BIOS.

The ROM-BIOS scans I/O addresses for parallel ports in the following order: 3BCh, 378h, 278h.

DMA Channels

In ECP enhancement mode, the parallel port can send and receive data under control of an on-board DMA controller. DMA channels operate with a request/acknowledge hardware handshake protocol between an internal DMA controller and the parallel port logic. On the Little Board/P5x, select a DMA channel in Setup. You can configure the parallel port to use either DMA channel 1 or DMA channel 3.

If you will not be using DMA with the parallel port, leave it disabled. This makes the DMA channel available to other peripherals installed on the expansion buses.

Parallel Port Connector (J15)

The parallel port appears on J15. Its pinout on J15 is arranged so that a 26-pin ribbon cable attached to J15 can be directly connected to a 25-pin DB-25 connector to match the PC standard pinout. Table 2– 21 gives the connector pinout and signal definitions for the parallel port.

In addition, the table indicates the pins to which each signal must be wired for compatibility with a standard DB25 connector. Normally the PC parallel port uses a female "DB" connector.

Table 2– 21. Parallel Port Connections (J15)

J15 Pin	Signal Name	Function	In/Out	DB25 Pin
1	STB*	Output Data Strobe	Out	1
3	PD 0	LSB Of Printer Data	I/O	2
5	PD 1	Printer Data 1	I/O	3
7	PD 2	Printer Data 2	I/O	4
9	PD 3	Printer Data 3	I/O	5
11	PD 4	Printer Data 4	I/O	6
13	PD 5	Printer Data 5	I/O	7
15	PD 6	Printer Data 6	I/O	8
17	PD 7	MSB Of Printer Data	I/O	9
19	ACK*	Character Accepted	In	10
21	BUSY	Cannot Receive Data	In	11
23	PE	Out of Paper	In	12
25	SLCT	Printer Selected	In	13
2	AUTOFD*	Autofeed	Out	14
4	ERROR	Printer Error	In	15
6	INIT*	Initialize Printer	Out	16
8	SELIN*	Selects Printer	Out	17
26	KEY	Key Pin	N/A	

Note

For maximum reliability, keep the cable between the board and the device it drives to 10 feet or less in length.

IEEE-1284-compliant Cables

Using the parallel port for high-speed data transfer in ECP/EPP modes requires special cabling for maximum reliability.

Some of the parameters for a compliant IEEE-1284 cable assembly include:

• All signals are twisted pair with a signal and ground return

• Each signal and ground return should have a characteristic unbalanced impedance of 62 +/- 6 ohms within a frequency band of 4 to 16 MHz

• The wire-to-wire crosstalk should be no greater than 10%

Please refer to the IEEE-1284 standard for the complete list of requirements for a compliant cable assembly, including recommended connectors

Latch-Up Protection

The parallel port incorporates chip protection circuitry on some inputs, designed to minimize the possibility of CMOS "latch up" due to a printer or other peripheral being powered up while the Little Board/P5*x* is turned off.

Parallel Port Registers

The low-level software interface to the parallel port consists of eight addressable registers. The address map of these registers is shown in Table 2– 22.

Table 2– 22. Parallel Port Register Map

Register Name	Address
Data Port	Base address
Status Port	Base address + 1
Control Port	Base address + 2
EPP Address Port	Base address + 3
EPP Data Port 0	Base address + 4
EPP Data Port 1	Base address + 5
EPP Data Port 2	Base address + 6
EPP Data Port 3	Base address + 7
Note: EPP registers are only accessible when in EPP mode	

Standard and Bi-Directional Operation

You can use the parallel port as a standard output-only printer port or as a PS/2-compatible bi-directional data port with up to 12 output lines and 17 input lines. The bi-directional mode can be very valuable in custom applications. For example, you might use it to control an LCD display, scan keyboards, sense switches, or interface with optically isolated I/O modules. All data and interface control signals are TTL-compatible.

Set the parallel port's default mode using Setup.

Using the Parallel Port in Bi-Directional Mode

To use the port as a bi-directional data or digital control port you must set the default mode to bi-directional in Setup or put it in bi-directional mode with a BIOS call. The following code example shows how to set the parallel port mode to bi-directional.

```
;-------------------------------------------------------------
; Code to set the parallel port mode to bi-directional
;-------------------------------------------------------------
MOV    AH,0CDh            ; AMPRO command
MOV    AL,0Ch             ; AMPRO function
MOV    BX,01h             ; Extended mode (use 00 to set output-only mode)
INT    13h
```

Within bi-directional mode, the port can be in its input state or output state. The code shown above leaves the port in its input state. An IN instruction of I/O address 378h reads the current state of the data lines.

To change the port between input and output states, write a 1 to bit five of the control register to set the port to its input state; or a 0 to set it to its output state. Here is a code sample for dynamically changing the port direction (after it is in Extended Mode).

```
;-------------------------------------------------------------
; Code to change the parallel port direction to input
;-------------------------------------------------------------
MOV    DX,37A
IN AL,DX
OR AL,20h                                  ;set bit 5 (input)
OUT    DX,AL
;
;-------------------------------------------------------------
; Code to change the parallel port direction to output
;-------------------------------------------------------------
MOV    DX,37Ah
IN AL,DX
AND    AL,0DFh               ;clear bit 5
OUT    DX,AL
```

Using the Control Lines for Additional I/O

Besides the eight data lines, you can use the four control lines (STB*, AUTOFD*, INIT*, and SELIN*) as general purpose output lines. Similarly, you can use the five status lines (ERROR*, SLCT, PE, ACK*, and BUSY) as general purpose input lines.

You can read the four control lines and use them as input lines. These lines have open collector drivers with 4.7K ohm pull-ups. To use a control line as an input line, you must first write to its corresponding bit in the control register. If the line is inverting (*), write a 0, otherwise write a 1. This will cause the line to float (pulled up by the 4.7K ohm resistors). When a line floats, you can use it as an input.

Enabling the Parallel Port Interrupt

Bit 4 in the Control Register enables the parallel port interrupt. If this bit is high 1, then a rising edge on the ACK* (IRQ) line will produce an interrupt on the parallel port interrupt, IRQ7.

Table 2– 23 lists the parallel port register bits.

Table 2– 23. Parallel Port Register Bits

Register	Bit	Signal Name or Function	In/Out	Active High/Low	J5 Pin	DB25F Pin
DATA (378h)	0	PD 0	I/O	High	6	2
	1	PD 1	I/O	High	10	3
	2	PD 2	I/O	High	14	4
	3	PD 3	I/O	High	18	5
	4	PD 4	I/O	High	22	6
	5	PD 5	I/O	High	26	7
	6	PD 6	I/O	High	30	8
	7	PD 7	I/O	High	34	9
STATUS (379h)	0	TMOUT	In	---	---	---
	1	0	---	---	---	---
	2	0	---	---	---	---
	3	ERROR*	In	Low	8	15
	4	SLCT	In	High	50	13
	5	PE	In	High	46	12
	6	ACK* (IRQ)	In	Low	38	10
	7	BUSY	In	High	42	11
CONTROL (37Ah)	0	STB*	Out*	Low	2	1
	1	AUTOFD*	Out*	Low	4	14
	2	INIT*	Out*	High	12	16
	3	SELIN*	Out*	High	16	17
	4	IRQE	---	High	---	---
	5	PCD	---	High	---	---
	6	1	---	---	---	---
	7	1	---	---	---	---
* Can also be used as input (see text).						

Parallel port register bit definitions (Table 2– 24):

Table 2– 24. Standard and PS/2 Mode Register Bit Definitions

Signal Name	Full Name	Description
TMOUT	Time-out	Valid only in EPP mode , this signal goes true after a 10 μS time-out has occurred on the EPP bus. This bit is cleared by reset.
ERR*	Error	Reflects the status of the -ERROR input. 0 means an error has occurred.
SLCT	Printer selected status	Reflects the status of the SLCT input. 1 means a printer is on-line.
PE	Paper end	Reflects the status of the PE input. 1 indicates paper end.
ACK*	Acknowledge	Reflects the status of the ACK input. 0 indicates a printer received a character..
BUSY*	Busy	Reflects the complement of the BUSY input. 0 indicates a printer is busy.
STB*	Strobe	This bit is inverted and output to the -STROBE pin.
AUTOFD	Auto feed	This bit is inverted and output to the -AUTOFD pin.
INIT*	Initiate output	This bit is output to the -INIT pin.
SELIN*	Printer select input	This bit is inverted and output to the pin. It selects a printer.
IRQE	Interrupt request enable	When set to 1, interrupts are enabled. An interrupt is generated by the positive-going -ACK input.
PCD	Parallel control direction	When set to 1, port is in input mode. In printer mode, the printer is always in output mode regardless of the state of this bit.
PD0-PD7	Parallel Data Bits	

Floppy Disk Interface

The on-board floppy disk controller and ROM BIOS support one or two floppy disk drives in any of the standard DOS formats shown in Table 2– 25.

Table 2– 25. Supported Floppy Formats

Capacity	Drive Size	Tracks	Data Rate
360K	5-1/4 inch	40	250 KHz
1.2M	5-1/4 inch	80	500 KHz
720K	3-1/2 inch	80	250 KHz
1.44M	3-1/2 inch	80	500 KHz

Floppy Drive Considerations

Nearly any type of soft-sectored, single or double-sided, 40 or 80 track, 5-1/4 inch or 3-1/2 inch floppy disk drive is usable with this interface. Using higher quality drives improves system reliability. Here are some considerations about the selection, configuration, and connection of floppy drives to the Little Board/P5x.

■ **Drive Interface**— The drives must be compatible with the board's floppy disk connector signal interface, as described below. Ampro recommends any standard PC-or AT-compatible 5-1/4 inch or 3-1/2 inch floppy drive.

■ **Drive Quality**— Use high quality, DC servo, direct drive motor floppy disk drives.

■ **Drive Select Jumpering**— Both drives must be jumpered to the second drive select.

■ **Floppy Cable**— For systems with two drives, use a floppy cable with conductors 10-16 twisted between the two drives. This is standard practice for PC-compatible systems.

■ **Drive Termination**— Resistive terminations should be installed only on the drive connected to the last interface cable connector (farthest from the board). Near-end cable termination is provided on the Little Board/P5*x*.

■ **Head Load Jumpering**— When using drives with a Head Load option, jumper the drive for head load with motor on rather than head load with drive select. This is the default for PC-compatible drives.

■ **Drive Mounting**— If you mount a floppy drive very close to the Little Board or another source of EMI, you may need to place a thin metal shield between the disk drive and the device to reduce the possibility of electromagnetic interference.

Floppy Interface Configuration

The floppy interface is configured using Setup to set the number and type of floppy drives connected to the system. Refer to the Setup section starting on page 2–62 for details.

If you don't use the floppy interface, disable it in Setup. This frees the floppy's I/O addresses, IRQ6, and DMA channel 2 for use by other peripherals installed on the PC/104 bus.

Floppy Interface Connector (J14)

Table 2– 26 shows the pinout and signal definitions of the floppy disk interface connector, J14. The pinout of J14 meets the AT standard for floppy drive cables. Table 2– 27 shows the manufacturer's part numbers for mating connectors.

Table 2– 26. Floppy Disk Interface Connector (J14)

Pin	Signal Name	Function	In/Out
2	RPM/RWC*	Speed/Precomp	OUT
4	N/A	(Not used)	N/A
6	N/A	Key pin	N/A
8	IDX*	Index Pulse	IN
10	MO1*	Motor On 1	OUT
12	DS2*	Drive Select 2	OUT
14	DS1*	Drive Select 1	OUT
16	MO2*	Motor On 2	OUT
18	DIRC*	Direction Select	OUT
20	STEP*	Step	OUT
22	WD*	Write Data	OUT
24	WE*	Write Enable	OUT
26	TRKO*	Track 0	IN
28	WP*	Write Protect	IN
30	RDD*	Read Data	IN
32	HS*	Head Select	OUT
34	DCHG*	Disk Change	IN
1-33	(all odd)	Signal grounds	N/A

Table 2– 27. J14 Mating Connector

Connector Type	Mating Connector
RIBBON	3M 3414-7600
DISCRETE WIRE	MOLEX HOUSING 22-55-2342 PN 16-02-0103

EIDE Hard Disk Interface

The Little Board/P5*x* provides an interface for up to four Integrated Device Electronics (IDE) peripheral devices, such as hard disk drives and CD-ROM drives.

- The *primary* IDE interface appears at connector J12, a 40-pin, dual-row connector.
- The *secondary* IDE interface appears at connector J17, also a 40-pin, dual-row connector.

Table 2– 28 shows the interface signals and pin outs for the IDE interface connectors. Table 2– 29 shows manufacturer's part numbers for mating connectors.

Note

For maximum reliability, keep IDE drive cables less than 18 inches long.

Table 2– 28. IDE Interface Connectors (J12, J17)

Pin J12, J17	Signal Name	Function	In/Out
1	HOST RESET*	Reset signal from host	OUT
2	GND	Ground	OUT
3	HOST D7	Data bit 7	I/O
4	HOST D8	Data bit 8	I/O
5	HOST D6	Data bit 6	I/O
6	HOST D9	Data bit 9	I/O
7	HOST D5	Data bit 5	I/O
8	HOST D10	Data bit 10	I/O
9	HOST D4	Data bit 4	I/O
10	HOST D11	Data bit 11	I/O
11	HOST D3	Data bit 3	I/O
12	HOST D12	Data bit 12	I/O
13	HOST D2	Data bit 2	I/O
14	HOST D13	Data bit 13	I/O
15	HOST D1	Data bit 1	I/O
16	HOST D14	Data bit 14	I/O
17	HOST D0	Data bit 0	I/O
18	HOST D15	Data bit 15	I/O
19	GND	Ground	OUT
20	KEY	Keyed pin	N/C
21	DRQ0	DMA Request 0	OUT
22	GND	Ground	OUT
23	HOST IOW*	Write strobe	OUT
24	GND	Ground	OUT
25	HOST IOR*	Read strobe	OUT
26	GND	Ground	OUT
27	IDERDY	I/O Channel Ready	OUT
28	RSVD	Reserved	N/C
29	DACK0*	DMA Acknowledge 0	IN

Table 2– 28 (cont.). IDE Interface Connectors (J12, J17)

Pin	Signal Name	Function	In/Out
30	GND	Ground	OUT
31	HOST IRQ14	Drive interrupt request	IN
32	IDE16	IOCS16	OUT
33	HOST A1	Drive address 1	OUT
34	RSVD	Reserved	N/C
35	HOST A0	Drive address 0	OUT
36	HOST A2	Drive address 2	OUT
37	HOST CS0*	Chip select	OUT
38	HOST CS1*	Chip select	OUT
39	RSVD	Reserved	N/C
40	GND	Ground	OUT

Table 2– 29. J12, J17 Mating Connectors

Connector Type	Mating Connector
RIBBON, 40 wire	3M 3417-7600 Latching Clip 3505-8040
DISCRETE WIRE	MOLEX HOUSING 22-55-2402 PIN 16-02-0103

IDE Interface Configuration

Use Setup to specify your IDE hard disk drive types. Refer to the Setup section beginning on page 2–62 for details.

If you do not find a drive type whose displayed parameters match the drive you are using, use drive type USER. It allows you to manually enter the drive's parameters. The drive manufacturer provides the drive parameters— check the drive's documentation for the proper values to enter.

If you are using a newer IDE drive, use drive type AUTO. It automatically configures the drive type parameters from information provided by the drive itself.

Compact Flash Solid-State Disk

The Little Board/P5*x* connector J23 supports a Compact Flash device, a solid-state IDE hard-disk emulator. It acts as a removable hard-disk drive. You can format, read, and write the Compact Flash device much as you would a standard IDE drive.

Enabling the Drive

The Compact Flash interface emulates an IDE drive to the operating system. Note that the Compact Flash interface takes up one of the positions of the primary IDE drive controller. If you use the Compact Flash interface, you can only add one additional hard drive to the primary IDE controller.

Master/Slave Setting

The Compact Flash interface can be configured to emulate a master or slave IDE device in the system.

- To configure the drive as *master*, install a jumper on W12.
- To configure the drive as *slave*, remove the jumper on W12.

Note that an IDE drive attached to the primary IDE controller must have the opposite setting.

Solid-State Disk Preparation

To prepare Compact Flash device for use in the system, insert the device in connector J23. Boot the system and prepare the drive just as you would a new IDE drive. That is, use the DOS FDISK utility to set up one or more partitions, and then use the DOS FORMAT utility to format the drive.

A Compact Flash device, properly formatted and programmed, can be used as a boot drive. To do so, you must configure the drive to be master by installing a jumper on W12. First FDISK the device as a primary DOS partition, then format the drive using the /S option to include the DOS operating system.

UltraSCSI INTERFACE

The Little Board/P5*x* features an optional PCI Small Computer System Interface (UltraSCSI) controller.   This subsystem is available by special order. It is not assembled on the standard versions of the Little Board P5*x*. The SCSI port uses a 50-pin male header connector (J9) to interface with peripherals. This connector provides an 8-bit path to the peripheral device, standard for most peripherals. The controller subsystem is internally connected to the PCI expansion bus. Table 2– 30 shows the pinout and signal definitions of the SCSI interface. Refer to your SCSI device documentation or the ANSI X3.131 SCSI specification for detailed information on the SCSI signal functions.

Note

> For maximum reliability, keep the SCSI cable as short as possible for data transfer rates above 10 MB/s.

UltraSCSI Connector

Table 2– 30 shows the pinout of the SCSI interface connector, J9. Table 2– 31 shows manufacturer's part numbers for mating connectors.

Table 2– 30. SCSI Interface Connector (J9)

Pin	Signal	Function	Pin	Signal	Function
2	DB0*	Data Bit 0 (LSB)	4	DB1*	Data Bit 1
6	DB2*	Data Bit 2	8	DB3*	Data Bit 3
10	DB4*	Data Bit 4	12	DB5*	Data Bit 5
14	DB6*	Data Bit 6	16	DB7*	Data Bit 7
18	DBP*	Data Bit Parity	26	TERM PWR	Termination +5V DC
32	ATN*	Attention	34	GROUND	Signal Ground
36	BSY*	Busy	38	ACK*	Transfer Acknowledge
40	RST*	Reset	42	MSG*	Message
44	SEL*	Select	46	C/D*	Control/Data
48	REQ*	Transfer Request	50	I/O*	Data Direction
25	N/A	Key Pin			
1-49(odd), 20,22,24,28,30			Ground		

Table 2– 31. J9 Mating Connectors

Connector Type	Mating Connector
RIBBON	3M 3425-7600 Latching Clip 3505-8050
DISCRETE WIRE	MOLEX HOUSING 22-55-2502 PIN 16-02-0103

SCSI Interface Configuration

Enable or disable the SCSI interface using Setup. Refer to the Setup description beginning on page 2–62.

Interrupt Request Assignment

The SCSI interface is a PCI peripheral and is assigned to a PCI interrupt using the plug-and-play logic in the BIOS. No user setup is required

Active Terminators

The SCSI interface uses "active terminators" for the SCSI bus. Active terminators draw less current than 330/220 ohm terminators (standard for non-UltraSCSI interfaces), are less susceptible to noise, and are required for the high data transfer rates of UltraSCSI. Termination is controlled by the SCSI BIOS. There is no user setting.

Only the SCSI devices on each end of the SCSI bus should be terminated.

External Termination Power Option

You can power external SCSI terminations from the Little Board/P5*x*. A jumper option, W2, connects power (+5V) to the SCSI bus TERMPWR signal (J9, pin 26). The board includes a Schottky protection diode to prevent damage to the board by current flowing *from* the SCSI bus and a self-resetting fuse to prevent damage to the board should the output become shorted. The fuse resets automatically when the short is removed.

SCSI ID

Every SCSI device must be configured for a specific SCSI bus ID, between 0 and 7. The default ID for the SCSI controller is 7 and should not be used by peripherals you attached to the SCSI bus. Set disk drive and other SCSI target device IDs to 0 – 6. The SCSI BIOS automatically detects SCSI devices on the bus and logs them in at boot time.

Flat Panel/CRT Video Controller

The Little Board/P5*x* provides an integrated high-performance super-VGA video controller. The video controller supports both CRT and flat panel displays. The standard video controller supports only 3.3V video panels. (You can order an adapter to convert the 3.3V signals to 5V for 5V panels.)

There are five connectors associated with the video display. These connectors are summarized in Table 2– 32. Complete hardware details about each connector and the features they support are provided in sections that follow.

Table 2– 32. Video Connector Summary

Name	Connector	Pins/Type	Description
Flat Panel	J3	50-pin Shrouded .100 Header	Provides connections for a broad array of standard flat panel displays. Intended for a standard 50-wire ribbon cable.
	J25	16-pin Shrouded .100 Header	Provides additional connections for flat-panel video data.
LCD Bias Supply Option	J4	12-pin .100 Header	Ampro provides a small add-on board that can supply the Vee voltage for the most common LCD flat panel displays. The board mounts to this connector. For details about the Vee Supply Option, refer to its section, below.
CRT	J5	10-pin Shrouded .100 Header	Provides connections for a CRT display. To connect to a standard CRT cable, use a short "transition cable" to a DB-15 connector. The pinout for a transition cable is provided below.
ZV Port	J6	26-pin 2mm Header	Provides connections for external video overlay signals.

Connecting a Flat Panel (J3)

Signals for a wide range of flat-panel displays, both color and gray-scale, appear on connectors J3 and J25. Although flat panels of a similar type use similar sets of signals from the video controller, they do not share a standardized interface connector pin configuration. Note, also, that the names of panel control signals vary from manufacturer to manufacturer. Read the description of each signal carefully to determine how each signal is to be used for the display you choose. Refer to the panel manufacturer's technical literature to determine how to wire a cable for the panel you choose for your application.

In many applications, the power management functions control the LCD display, for example, in portable equipment. Furthermore, power and signals must be sequenced in time when the system is energized to prevent damage to the display. The Little Board/P5*x* video controller provides power and signal conditioning to meet these requirements.

Table 2– 33 lists the signals available on connector J3. Table 2– 34 shows compatible mating connectors to J3.

Table 2– 33. Flat Panel Video Connector (J3)

Pin	Signal Name	Description
2, 34, 37	+3.3V	Panel power
3	+12V	+12 Volt supply (from J10)
5	ShfClk	Shift Clock. Pixel clock for flat panel data.
7	M DE	M signal for panel AC drive control. Sometimes called ACDCLK or AC Drive. May also be configured to be -BLANK or as Display Enable (DE) for TFT panels.
9	LP	Latch Pulse. Sometimes called Load Clock, Line Load, or Input Data Latch. It's the flat panel equivalent of HSYNC.
10	FLM	First Line Marker. Also called Frame Sync or Scan Start-up. Flat panel equivalent to VSYNC.
12–31	FP0-FP19	Flat panel video data 0 through 19 (in order).
32, 33	+5V	+5 Volt supply from Little Board/P5*x*
35	ENABLK	Enable backlight. Power control for panel backlight. Active high.
36	EBKL*	Enable backlight. Power control for panel backlight. Active low.
38	ENAVEE	Enable Vee, active high. Power sequencing control for panel bias voltage. This signal is sent to the optional Vee supply board to control Vee output.
39	ENAVDD	Enable Vdd. Power sequencing control for panel driver electronics Vdd. Active high. This signal is used to switch VDVP (pin 44).
41	FP20	Video data 20
42	FP21	Video data 21
43	FP22	Video data 22
44	VDDP	Switched V_LCD supply to panel
45	FP23	Video data 23
46	VEE	Switched Vee supply to panel (from LCD Bias Supply option board or your own switched supply).
47	ECONT	External contrast adjustment voltage. This is an input to the flat panel to control the panel contrast ratio. The Ampro LCD Bias Supply option board provides this signal and a means of attaching an external contrast adjustment pot.
50	+12SAFE	Switched +12V supply to backlight power converter.
1, 4, 6, 8, 11, 40, 48, 49	Ground	Ground

Table 2– 34. J3 Mating Connectors

Connector Type	Mating Connector
RIBBON	3M 4325-7600
DISCRETE WIRE	MOLEX HOUSING 55-22-2502 PIN 16-02-0103

The flat-panel video controller supports LCD panels that require up to 36 data bits. J3 supplies the lower 24 data bits (FP0 - FP23), and connector J25 has the additional 12 bits. Table 2– 35 lists the signals available on connector J25, and Table 2– 36 shows J25 mating connectors.

Table 2– 35. Flat Panel Extension Video Connector (J25)

Pin	Signal Name	Description
3 - 14	FP24 - FP35	Video data 24 - 35
1,2,15,16	Ground	

Table 2– 36. J25 Mating Connectors

Connector Type	Mating Connector
RIBBON	3M 3452-7600 Latching Clip 3505-8016
DISCRETE WIRE	MOLEX Housing 22-55-2162 Pin 16-02-0103

Power Sequencing

Some LCD flat-panel displays can be damaged when its various voltages and data signals are applied at power up. This can result in damage to the panel or reduction of its operational life. The on-board video controller provides switched power lines that apply power and data signals in the proper sequence, controlled by the video BIOS. The board also provides the control signals, in case you need to provide your own switched power supply lines in your embedded system.

The Little Board/P5*x* supports automatic sequencing of Vdd (VDDP) and +12V (+12SAFE, for an external backlight power inverter). The Ampro LCD Bias Supply board (described below) supports automatic power sequencing of Vee, controlled by ENAVEE.

If you want to manage your own supplies, you must enable the power using the special enable signals provided on connector J3, ENAVEE, ENAVDD, and ENABKL.

Advanced Power Management

The same signals that support power sequencing are also used to provide the power management feature. In "panel off mode" both the CRT and flat-panel interfaces are turned off, but the VGA subsystem (registers and display memory) remain powered. In "standby mode", the CRT and flat-panel interfaces are turned off, and in addition, the VGA subsystem is turned off. The screen DRAM is placed in a low-power mode in which only the DRAM is refreshed.

BIOS Support of Standard Flat Panels

The Little Board/P5*x* supports flat-panel BIOS settings for up to 16 popular LCD panels. You select which flat-panel BIOS settings to use in Setup. For details about configuring the video controller, refer to the description of the Integrated Peripherals Setup on page 2–62. For the current list of supported LCD panels, look at the Ampro Website at www.ampro.com.

If you plan to use an unsupported panel, you must modify the standard BIOS to support the panel. Ampro can provide a BIOS modification kit you can use to do this. The new video BIOS is then loaded into the on-board Flash device.

To install the new video BIOS code in the on-board OEM Flash memory device:

- Install jumper W11 to write-enable the Flash device.
- Install your new video BIOS code in the on-board Flash device using a utility called PGM5X.COM, supplied by Ampro on the utility disk that comes with the Little Board/P5*x* Development Platform.
- Remove W11 to write-protect the on-board Flash device.

PGM5X is a DOS utility designed to write to the on-board Flash device. (The on-board Flash device contains the system's BIOS, the video BIOS, the SCSI BIOS.) Instructions for this utility are provided on the utility diskette. Contact your Ampro sales representative or Ampro Technical Support for information about the Little Board/P5*x* Flat-Panel BIOS Modification Kit.

The LCD Bias Supply Option (J4)

The LCD Bias Supply Option is a small circuit board that supplies Vee power to an LCD display. The board converts the +5V from the Little Board/P5*x* to the Vee voltage (between 15V and 35V, negative or positive) required by some LCD panels, and makes this voltage available on the flat-panel connector J3. It uses the signal, ENAVEE, to apply Vee power to the panel in the proper sequence with other signals. In addition, the board provides a contrast control as well as a way of providing an external contrast control.

The Ampro LCD Bias Supply option mounts parallel to the Little Board/P5*x*, connected to the board via a 12-pin connector, J4. You secure the board to the Little Board/P5*x* using a 0.6 inch standoff. Table 2– 37 shows the connector pinout for J4, with a description of each signal. Note that some of its output signals also appear on the flat panel connector, J3.

Table 2– 37. LCD Bias Supply Option Connector (J4)

J4 Pin	J3 Pin	Description
1		Ground
2		+5V to the Vee Supply Option board
4		Ground
6	38	Enable Vee — TTL control signal, driven by the VGA controller chip
8		Ground
11	46	Vee Output, to panel
12	47	Contrast adjustment — analog control signal

Selecting Vee Polarity

Most LCD displays require a Vee supply of between 15V and 35V. Some panels need a negative supply, and some a positive supply. The LCD Bias Supply Option provides a jumper for selecting the Vee output polarity. To select the polarity for the panel you will be using, set the jumper on W1 (on the LCD Bias Supply board, not on the Little Board/P5*x*) as follows:

■   Negative Vee   W1-1/2
■   Positive Vee   W1-2/3

Note

Incorrect Vee polarity or voltage can damage an LCD panel. Set the polarity and voltage on the Vee supply before connecting the LCD panel.

Attaching an External Contrast Control

Vee controls the contrast of the LCD display. (Do not confuse this with a backlight, which illuminates the screen using one or more fluorescent tubes. Backlights generally require a high voltage AC supply.)

An on-board control (R1) on the LCD Bias Supply board allows you to set the precise Vee voltage for the contrast you require. However, you may want to provide a more accessible Vee control so that a user can set the display contrast to accommodate various ambient lighting conditions. The board provides a jumper and control signal to allow the attachment of a remote potentiometer.

To use the contrast potentiometer on the LCD Bias Supply board, install a jumper on W2 on the LCD Bias Supply board.

To use an external potentiometer, remove the jumper from W2, and connect a circuit as shown in Figure 2– 4 between J3-47 and ground.
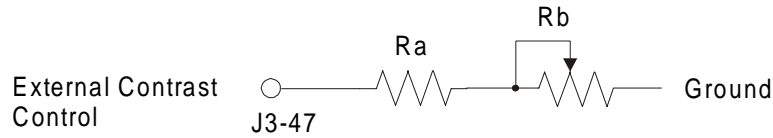

Figure 2– 4. External Contrast Adjustment for LCD panels

Select Ra and Rb to provide the appropriate voltage range adjustment for the LCD panel you are using. Consult your panel's technical literature for the range of voltages you need to supply for the contrast adjustment. Use the following formulae to calculate the resistor values (in K Ohms).

$$Ra = \frac{270}{(Vee\ max/1.5) - 1} - 12 \qquad\qquad Rb = \frac{270}{(Vee\ min/1.5) - 1} - 12 - Ra$$

Example:

Suppose the following values are shown in the panel's data sheet:

Vee Max = 24 V

Vee min = 20 V

Calculate the required resistor values as follows:

Ra = (270 / ((24 / 1.5) - 1)) -12

Ra = 6K Ω

Rb = (270 / ((20 / 1.5) - 1)) -12 - 6

Rb = 3.9K Ω

In this example, you would use 6K Ω for Ra and a 3.9K Ω potentiometer for Rb.

Connecting a CRT (J5)

Analog video signals from the video controller appear on a 10-pin dual-row header, J5. These signals are compatible with the standard video monitors commonly used with desktop PCs. Specifications for compatible monitors are provided in *Chapter 3, Technical Specifications*.

Normally, signals from J5 are connected to a standard DB-15 video connector by a "transition cable," made from a ribbon cable connectors and a short length of 10-wire ribbon cable. A transition cable can connect the video signals to a bulkhead-mounted DB-15 connector, allowing any standard CRT to be easily connected using a standard monitor video cable.

+5V power, protected by fuse F3, can supply power to an external device, such as an NTSC Video adapter module.

Table 2– 38 gives the signal pinout of J5 and pin connections for a DB-15 connector. Table 2– 39 shows J5 mating connectors.

Table 2– 38. CRT Interface Connector (J5)

Pin	Signal Name	DB-15
1	Red	1
2	Ground	6
3	Green	2
4	Ground	7
5	Blue	3
6	Ground	8
7	Horizontal Sync.	13
8	Ground	10
9	Vertical Sync.	14
10	+5V Power	-

Table 2– 39. J5 Mating Connectors

Connector Type	Mating Connector
RIBBON	3M 3473-7600 Latching Clip 3505-8010
DISCRETE WIRE	MOLEX HOUSING 22-55-2102 PIN 16-02-0103

ZV Port Interface (J6)

This section describes the ZV port interface (J6). The ZV port is a PCMCIA standard for video input. The ZV port can be used to receive video data in either RGB or YUV format. The input data can be scaled, positioned, and can overlay the Little Board/P5*x*'s VGA data stream. It can use color keying for non-rectangular windowing, or X-Y window keying.

For further information about the ZV port and its uses, read application notes for the 69000 video controller, available at the Intel Website, **http://www.intel.com**.

J6 is a high density connector with 2mm pitch pins. Table 2– 40 lists the signals and pin numbers for J6 and Table 2– 41 lists a compatible mating connector.

Table 2– 40. ZV Port Connector (J6)

J6 Pin	Name	Function
1 - 16	VP0 - VP15	Video Data Inputs
18	VREF	Vertical Reference Input
20	HREF	Horizontal Reference Input
22	RSVD	Reserved
24	PCCK	PC
26	PCLK	Video Clock Output (DCLK or DCLK/2)
17, 19, 21,23, 25	Ground	

Table 2– 41. J6 Mating Connector

Mating Connector
Discrete Wire:
Molex Housing   51110-2650 Molex Pin   50394-8051

Disabling the Video Controller

The video controller can be disabled in Setup. There are no jumpers to change.

Ethernet Network Interface

This section describes the hardware of the Ethernet interface and discusses relevant software considerations.

Hardware Description

The Ethernet subsystem is based on the AMD Am79C972 PCnet™ Fast+ Enhanced 10/100 PCI Ethernet Controller coupled with a Level 1, Inc. LXT970a dual-speed fast Ethernet transceiver. The Ethernet controller fully supports IEEE 802.3 Ethernet standards, and supports standard 10BaseT and 100BaseT via a standard RJ-45 connector.

The Ethernet controller interfaces to the PCI portion of the bus. Features of this controller include:

- Speed auto-negotiation (complies with IEEE802.3u standard)
- Full-duplex operation at 10 Mb/s and 100 Mb/s
- Low-power energy modes

Ethernet RJ-45 Interface Connector (J7)

Connector J7 is a standard RJ-45 jack for connecting directly to an Ethernet network using category 5 UTP/STP cabling.

Table 2– 42 lists the signals and pin numbers of the Ethernet connector, J7:

Table 2– 42. Ethernet RJ-45 Connector (J4)

J7 Pin	Function
1	TX +
2	TX -
3	RX +
6	RX -
4, 5, 7, 8	Signal Common

Ethernet Interface Software

Manufacturer's Ethernet ID

Each manufacturer of Ethernet network adapters and interfaces is assigned a unique manufacturer's ID by the IEEE Standards Office. A network address consists of 48 bits. The upper 24 bits are the manufacturer's ID and the lower 24 bits are the board's unique ID.

For developers who are creating network applications, knowing the manufacturer's ID for network adapters attached to the network may or may not be important.

Ampro's 24-bit manufacturer's ID for Ethernet controllers is displayed in hex as follows:

```
00 40 53
```

Network Operating Systems

The Ethernet interface is typically connected in a network controlled by a network operating system. The network operating system may be part of the computer's operating system or be provided separately. For example, Windows® NT provides the network operating system as part of computer's operating system. Novell's NetWare™ provides a separate, add-on network operating system for DOS and Windows. The network operating system provides file server and network services to the distributed systems connected to the network. Each node on the network must have a compatible network operating system installed as well.

Modern network architectures are based on the OSI model, which defines layers of software between the network hardware, the network operating system, and the applications that use the network services. The actual Ethernet cable and the Little Board/P5*x* hardware interface are at the bottom level. A driver program at the next level handles communication between the hardware and the operating system, masking any unique differences in the hardware from the layers above it, including the network operating systems.

Network OS Drivers

The Little Board/P5*x* Ethernet subsystem uses AMD PCnet-family drivers, available from AMD. The driver is the only unique software you need to use the Little Board/P5*x*. The supported network operating systems provide the other software layers normally provided in the OSI model. These include:

- AHSM ODI Drivers (DOS, OS/2, Server)
- CHSM ODI Driver for NetWare 5.0
- NDIS 2.0.1 Drivers (DOS version 6.x, OS/2 version 3.x and 4.x)
- NDIS 3.x MAC Drivers (for WFW 3.11; NT versions 3.5, 3.51, 4.0; Win95)
- NDIS 3.x Miniport Drivers (for Windows 95 and Windows NT 3.51)
- NDIS 4.x Driver (for Windows NT 4.0 and Windows 95 OSR 2)
- Novell UnixWare Drivers (for v1.1 and 2.0)

There are also drivers for various flavors of UNIX and for other operating systems. AMD also supplies diagnostic software for testing your Ethernet setup.

For the most up-to-date drivers and utility software, please refer to the AMD PCnet family driver web page. The AMD URL is:

http://www.amd.com/

Ethernet Setup

This section describes how to configure and connect the Ethernet LAN interface.

There are no jumpers to set on the Ethernet interface, and no hardware configuration, other than connecting the network cable to an appropriate connector.

Software configuration of the Ethernet interface includes the following steps:

- In Setup, enable the Ethernet interface.

■ If you plan to boot from the network (that is, if you plan to use the Little Board/P5*x* as a diskless peripheral or workstation), set up an Ethernet boot PROM. See the section, "Setting up a Boot PROM", below, for details.

■ Install the proper driver for the network operating system you will be running. Follow AMD's instructions for installing your PCnet driver.

Setting up a Boot PROM

Boot PROM code enables the Little Board/P5*x* system to boot from an Ethernet network server instead of a local hard disk or floppy. Boot PROM code can be installed in the OEM Flash memory on Little Board/P5*x*, or in an external byte-wide memory socket on a MiniModule or other system board.

If you plan to boot from the network, you must provide a boot PROM program compatible with your network operating system. (You can download AMD PCnet boot PROM code from AMD's Website.)

You install the boot PROM code in the on-board OEM Flash memory device. Briefly, these are the steps you take:

■ Install jumper W11 to write-enable the Flash device.
■ Program your boot PROM code into the Flash device using a utility called PGM5X.COM, supplied by Ampro on the utility disk that comes with the Little Board/P5*x* Development Platform.
■ Remove jumper W11 to write-protect the Flash device.

PGM5X is a DOS utility designed to write to the on-board Flash device. (The on-board Flash device contains the system's BIOS, the video BIOS, the SCSI BIOS.) Instructions for this utility are provided on the utility diskette.

Ethernet Indicator LEDs

Three LED indicator lamps are provided on the board to indicate the status of the Ethernet interface. You can use these LEDs as simple trouble-shooting aids when connecting to an Ethernet segment.

Table 2– 43 shows the meaning of each LED.

Table 2– 43. Ethernet Diagnostic LEDs

Color	Designation	Function
Yellow	D1	Receive (RX)
Red	D2	Transmit (TX)
Green	D3	Link

Watchdog Timer

The purpose of a watchdog timer function is to restart the system should some mishap occur. Possible problems include: a failure to boot properly; the application software losing control; temporary power supply problems including spikes, surges, or interference; the failure of an interface device; unexpected conditions on the bus; or other hardware or software malfunctions. The watchdog timer helps assure proper start-up after an interruption.

The Little Board/P5*x* ROM-BIOS supports the board's watchdog timer function in two ways:

■ There is an initial watchdog timer setting, specified using SETUP, which determines whether the watchdog timer will be used to monitor the system boot, and if so, how long the time-out is (30, 60, or 90 seconds).

■ There is a standard ROM-BIOS function which may be used by application software to start and stop the watchdog timer function.

The initial time-out should be set (using SETUP) to be long enough to guarantee that the system can boot and pass control to the application. Then, the application must periodically retrigger the timer by reading I/O Port 201h so that the time-out does not occur. If the time-out does occur, the system will respond in a manner determined by how the watchdog timer jumper, W8, is set (see Chapter 2).

The following simple assembly language routine illustrates how to control the watchdog timer using the Ampro ROM-BIOS function that has been provided for this purpose:

```
;------------------------------------------------------------
; Watchdog timer control program
;------------------------------------------------------------
MOV   AH,0C3h           ; Watchdog Timer BIOS function
MOV   AL,nn             ; Use "00" to disable, "01" to enable
                        ; timer.
MOV   BX,mm             ; Selects time, in seconds
                        ;(00-FFh; 1-255 seconds)
INT   15h
```

Ampro provides a simple DOS program that can be used from the command line or in a batch program to manage the watchdog timer. It is called WATCHDOG, and is described in the Ampro Common Utilities manual.

Utility Connectors (J16, J24)

Seven functions appear on Utility 1, a 16-pin connector at J16. These are:

- Auxiliary power connections
- Power indicator LED
- PC speaker
- Push-button reset switch
- Keyboard interface
- External back-up battery

Table 2– 44 shows the pinout and signal definitions of the Utility Connector. Since there are connections for diverse features on this single connector, you would usually choose a discrete-wire connector rather than a ribbon cable connector, though this is not a requirement. Table 2– 45 shows manufacturer's part numbers for both types of mating connectors.

Table 2– 44. Utility Connector (J16)

Pin	Signal Name	Function
1	-12V power	Connect external -12V supply here for distribution to expansion cards needing this voltage.
2	Ground	Ground return
3	-5V power	Connect external -5V supply here for distribution to expansion cards needing this voltage.
4	Ground	Ground return
5	LED Anode	LED current source (+5V through 330 ohms)
6	RSVD	No connection
7	Speaker +	PC audio signal output
8	Ground	Ground
9	Reset	To one side of manual reset button.
10	N/C	Reserved
11	Kbd Data	Keyboard serial data
12	Kbd Clk	Keyboard clock
13	Ground	Keyboard ground
14	Kbd Power	Keyboard +5V power
15	+ Bat	+ Battery *
16	Ground	- Battery *
* An external battery is not required.		

Table 2– 45. J16 Mating Connector

Connector Type	Mating Connector
RIBBON	3M 3452-7600 Latching Clip 3505-8016
DISCRETE WIRE	MOLEX Housing 22-55-2162 Pin 16-02-0103

LED Connection

To connect an external LED power-on indication lamp, connect the LED anode to J16-5 and the cathode to ground. J16-5 provides +5V through a 300 ohm resistor.

Speaker Connections

The board supplies about 100 mW for a speaker on J16-7. Connect the other side of the speaker to ground (J16-8). A transistor amplifier buffers the speaker signal. Use a small general purpose 2 or 3 inch permanent magnet speaker with an 8 ohm voice coil. Refer to Chapter 3, Section 3.14 for an explanation of the PC speaker circuit architecture.

Push-button Reset Connection

J16-9 provides a connection for an external normally-open momentary switch to manually reset the system. Connect the other side of the switch to ground. The reset signal is "de-bounced" on the board.

Keyboard Connection

You can connect an AT (not PC) keyboard to the keyboard port. J16-11 through J16-14 provide this function. Normally, AT keyboards include a cable that terminates in a male 5-pin DIN plug for connection to an AT (or a 6-pin miniature DIN plug for PS-2). Table 2– 46 gives the keyboard connector pinout and signal definitions, and includes corresponding pin numbers for DIN keyboard connectors.

Table 2– 46 Keyboard Connector (J16)

J16 Pin	Signal Name	DIN-5 Pins	DIN-6 Pins
12	Keyboard Clock	1	5
11	Keyboard Data	2	1
13	Ground	4	3
14	Keyboard power	5	4

Utility 2 Connector (J24)

Utility 2, a 24-pin connector at J24 provides the following connections:

- LIDSW – Simulates the lid switch on a laptop
- PWRBT – Turns off all but minimum power
- BATLOW – Simulates a low battery
- IrDA Interface – Infra-red serial interface signals
- PS/2 Mouse Port
- Universal Serial Bus (USB) Interfaces

The signals on the Utility 2 connector are shown in Table 2– 47. Table 2– 48 shows compatible mating connectors.

Table 2– 47. Utility2 Connector (J24)

Pin	Signal Name	Function	Pin	Signal Name	Function
1	LIDSW	Lid Switch Input	2	PWRBT-	Power Button Input
3	BATLOW-	Battery Low Input	4	IRMODE	IrDA Mode
5	IRTX	IrDA Transmit	6	IRRX	IrDA Receive
7	Ground		8	Vcc	
9	MDATA	PS/2 Mouse Data	10	MCLK	PS/2 Mouse Clock
11	Ground		12	Vcc	
13	SMBCLK	Serial Bus Clock	14	SMBDATA	Serial Bus Data
15	USBPWR1	USB1 +5V Power	16	USBPWR2	USB2 +5V Power
17	USBP-1	USB1 Data -	18	USBP-2	USB2 Data -
19	USBP+1	USB1 Data +	20	USBP+2	USB2 Data +
21	USBGND1	USB1 Ground	22	USBGND2	USB2 Ground
23	SHIELD1	Cable Shield for USB1	24	SHIELD2	Cable Shield for USB2

Table 2– 48. J24 Mating Connector

Connector Type	Mating Connector
RIBBON	3M 3626-7600 Latching Clip 3505-8024
DISCRETE WIRE	MOLEX HOUSING 22-55-2242 PIN 16-02-0103

PC/104-*Plus* EXPANSION BUS

The PC/104-*Plus* expansion bus appears on three header connectors, P1, P2, and J21. P1 is a 64-pin female dual-row header. P2 is a 40-pin female dual-row header, and J21 is a 120-pin 2mm female quad-row header (4 x 30). The PC-bus subset of the PC/104-*Plus* expansion bus connects to P1. The AT expansion bus signals connect to P2. The layout of signals on P1 and P2 is compliant with the PC/104 bus specification, and make up the ISA bus portion of the PC/104-*Plus* bus. An implementation of the PCI bus appears on J21.

PC/104-compatible expansion modules can be installed on the Little Board/P5x expansion bus. The buffered output signals to the expansion bus are standard TTL level signals. All inputs to the Little Board/P5x operate at TTL levels and present a typical CMOS load to the expansion bus.

On-board MiniModule Expansion

You can install one or more Ampro MiniModule products or other PC/104 modules on the Little Board/P5x expansion connectors. When installed on P1 and P2, the expansion modules fit within the Little Board/P5x's outline dimensions. Most Ampro MiniModule products have stackthrough connectors compatible with the PC/104 specification. You can stack several modules on the Little Board/P5*x* headers. Each additional module increases the thickness of the package by 0.66 inches (15 mm). See Figure 2– 5.
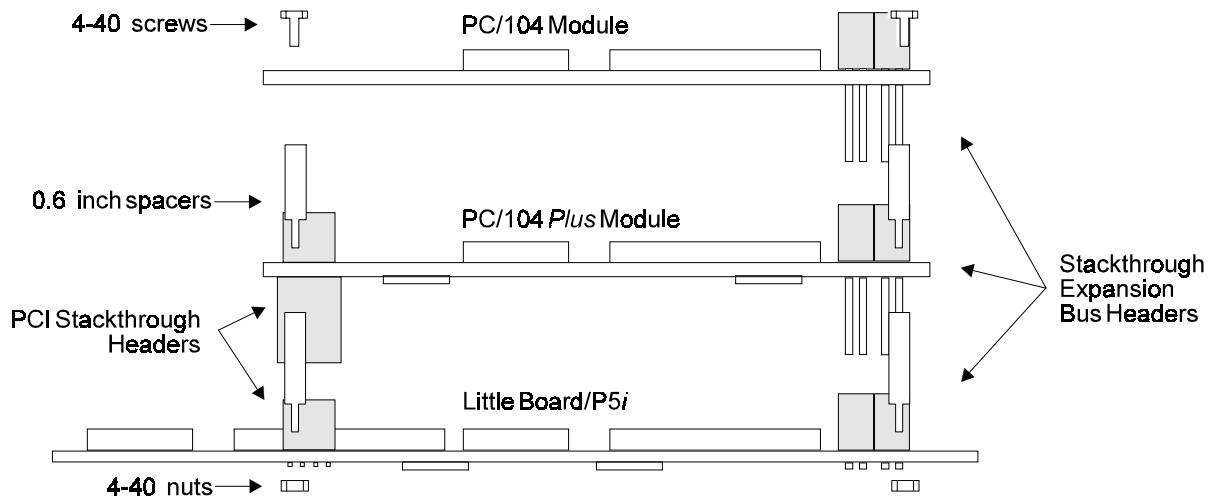

Figure 2– 5. Stacking PC/104 Modules on the Little Board/P5x

Using Standard PC and AT Bus Cards

Ampro offers several options that allow you to add conventional 8-bit and 16-bit ISA expansion cards to the Little Board/P5*x* system. Contact Ampro for further information about optional bus expansion products.

Expansion Bus Connector Pinouts

Table 2– 49 through Table 2– 53 show the pinout and signal functions on the PC/104 *-Plus-* compatible expansion bus connectors. These include P1, P2, and J21.

The Little Board/P5x does not generate ±12VDC, 3.3V, or -5VDC for the expansion bus. If devices on the bus require these voltages, -12V and -5V can be supplied to the bus connector from the Utility 1 connector (J16). +12V can be supplied through J10-4. If a PCI peripheral board requires 3.3V, you can attach this voltage to J10-5.

You do not need to add a +12V supply to program the on-board Flash device that stores the ROM BIOS, video BIOS, SCSI BIOS, and optional Ethernet boot PROM code. An on-board supply provides the programming voltage. This supply, however, does not provide power to the expansion bus. Most Ampro expansion products provide on-board DC-to-DC converters to convert the +5V supply to other voltages they require.

The expansion bus pin numbers for P1 and P2, shown in the following tables, correspond to the scheme normally used on ISA expansion bus card sockets. Rather than numerical designations (1, 2, 3) they have alpha-numeric designations (A1, A2…, B1, B2…, etc.). Similarly, the rows of J21 are designated A, B, C, and D.

Table 2– 49. PC/104 Expansion Bus Connector, P1 (A1-A32)

Pin	Signal Name	Function	In/Out
A1	IOCHCK*	bus NMI input	IN
A2	SD7	Data bit 7	I/O
A3	SD6	Data bit 6	I/O
A4	SD5	Data bit 5	I/O
A5	SD4	Data bit 4	I/O
A6	SD3	Data bit 3	I/O
A7	SD2	Data bit 2	I/O
A8	SD1	Data bit 1	I/O
A9	SD0	Data bit 0	I/O
A10	IOCHRDY	Processor Ready Ctrl	IN
A11	AEN	Address Enable	I/O
A12	SA19	Address bit 19	I/O
A13	SA18	Address bit 18	I/O
A14	SA17	Address bit 17	I/O
A15	SA16	Address bit 16	I/O
A16	SA15	Address bit 15	I/O
A17	SA14	Address bit 14	I/O
A18	SA13	Address bit 13	I/O
A19	SA12	Address bit 12	I/O
A20	SA11	Address bit 11	I/O
A21	SA10	Address bit 10	I/O
A22	SA9	Address bit 9	I/O
A23	SA8	Address bit 8	I/O
A24	SA7	Address bit 7	I/O
A25	SA6	Address bit 6	I/O
A26	SA5	Address bit 5	I/O
A27	SA4	Address bit 4	I/O
A28	SA3	Address bit 3	I/O
A29	SA2	Address bit 2	I/O
A30	SA1	Address bit 1	I/O
A31	SA0	Address bit 0	I/O
A32	GND	Ground	N/A

Table 2– 50. PC/104 Expansion Bus Connector, P1 (B1-B32)

Pin	Signal Name	Function	In/Out
B1	GND	Ground	N/A
B2	RESETDRV	System reset signal	OUT
B3	+5V	+5 Volt power	N/A
B4	IRQ9	Interrupt request 9	IN
B5	-5V	To J16-3	N/A
B6	DRQ2	DMA request 2	IN
B7	-12V	To J16-1	N/A
B8	ZWS*	Zero wait state	IN
B9	+12V	To J10-1	N/A
B10	N/A	Keyed pin	N/A
B11	SMEMW*	Mem Write(lwr 1MB)	I/O
B12	SMEMR*	Mem Read(lwr 1MB)	I/O
B13	IOW	I/O Write	I/O
B14	IOR	I/O Read	I/O
B15	DACK3*	DMA Acknowledge 3	OUT
B16	DRQ3	DMA Request 3	IN
B17	DACK1*	DMA Acknowledge 1	OUT
B18	DRQ1	DMA Request 1	IN
B19	REFRESH*	Memory Refresh	I/O
B20	SYSCLK	Sys Clock	OUT
B21	IRQ7	Interrupt Request 7	IN
B22	IRQ6	Interrupt Request 6	IN
B23	IRQ5	Interrupt Request 5	IN
B24	IRQ4	Interrupt Request 4	IN
B25	IRQ3	Interrupt Request 3	IN
B26	DACK2*	DMA Acknowledge 2	OUT
B27	TC	DMA Terminal Count	OUT
B28	BALE	Address latch enable	OUT
B29	+5V	+5V power	N/A
B30	OSC	14.3 MHz clock	OUT
B31	GND	Ground	N/A
B32	GND	Ground	N/A

Table 2– 51. PC/104 Expansion Bus Connector, P2 (C0-C19)

Pin	Signal Name	Function	In/Out
C0	GND	Ground	N/A
C1	SBHE	Bus High Enable	I/O
C2	LA23	Address bit 23	I/O
C3	LA22	Address bit 22	I/O
C4	LA21	Address bit 21	I/O
C5	LA20	Address bit 20	I/O
C6	LA19	Address bit 19	I/O
C7	LA18	Address bit 18	I/O
C8	LA17	Address bit 17	I/O
C9	MEMR*	Memory Read	I/O
C10	MEMW*	Memory Write	I/O
C11	SD8	Data Bit 8	I/O
C12	SD9	Data Bit 9	I/O
C13	SD10	Data Bit 10	I/O
C14	SD11	Data Bit 11	I/O
C15	SD12	Data Bit 12	I/O
C16	SD13	Data Bit 13	I/O
C17	SD14	Data Bit 14	I/O
C18	SD15	Data Bit 15	I/O
C19	Key	Key Pin	N/A

Table 2– 52. PC/104 Expansion Bus Connector, P2 (D0-D19)

Pin	Signal Name	Function	In/Out
D0	GND	Ground	N/A
D1	MEMCS16*	16-bit Mem Access	IN
D2	IOCS16*	16-bit I/O Access	IN
D3	IRQ10	Interrupt Request 10	IN
D4	IRQ11	Interrupt Request 11	IN
D5	IRQ12	Interrupt Request 12	IN
D6	IRQ15	Interrupt Request 15	IN
D7	IRQ14	Interrupt Request 14	IN
D8	DACK0*	DMA Acknowledge 0	OUT
D9	DRQ0	DMA Request 0	IN
D10	DACK5*	DMA Acknowledge 5	OUT
D11	DRQ5	DMA Request 5	IN
D12	DACK6*	DMA Acknowledge 6	OUT
D13	DRQ6	DMA Request 6	IN
D14	DACK7*	DMA Acknowledge 7	OUT
D15	DRQ7	DMA Request 7	IN
D16	+5V	+5 Volt Power	N/A
D17	MASTER*	Bus Master Assert	IN
D18	GND	Ground	N/A
D19	GND	Ground	N/A

Table 2– 53. PC/104-Plus Expansion Bus Connector, P21 (A1-D30)

Pin	A	B	C	D
1	GND/5.0V KEY[4]	Reserved	+5	AD00
2	VI/O (+5V)	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0*	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O (+5V)	AD10	M66EN[1]
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1*	AD15	+3.3V
9	SERR*	GND	SB0*	PAR
10	GND	PERR*	+3.3V	SDONE
11	STOP*	+3.3V	LOCK*	GND
12	+3.3V	TRDY*	GND	DEVSEL*
13	FRAME*	GND	IRDY*	+3.3V
14	GND	AD16	+3.3V	C/BE2*
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3*	VI/O (+5V)	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0*	GND	REQ1*	VI/O
24	GND	REQ2*	+5V	GNT0*
25	GNT1*	VI/O (+5V)	GNT2*	GND
26	+5V	CLK0	GND	CLK1F
27	CLK2	+5V	CLK3	GND
28	GND	INTD*	+5V	RST*
29	+12V	INTA*	INTB*	INTC*
30	-12V	Reserved	Reserved	GND/3.3V KEY[4]

PCI Bus (P21) Notes

1. **Signal M66EN is grounded on the motherboard (Ground = 33MHz bus speed).**

2. The shaded cells in the table denote unsupported signals.

3. The KEY pins are to guarantee proper module installation. Pin-A1 will be removed and the female side plugged for 5.0V I/O signals and Pin-D30 will be modified in the same manner for 3.3V I/O. Both pins will be removed for 3.3/5.0 operation.

Setup

Many options provided on the Little Board/P5*x* are controlled by the Setup function. The parameters are displayed on several screens, selected from a main menu screen. To configure the board, you modify the fields in these screens and save the results in the on-board *configuration memory*.

The configuration memory consists of portions of the CMOS RAM in the battery-backed real-time clock chip and an Ampro-unique configuration EEPROM. To enhance embedded-system reliability, the contents of the EEPROM mirror the contents of the CMOS memory. The EEPROM retains your configuration information even if the clock's backup battery fails.

The Setup information is retrieved from configuration memory when the board is powered up or when it is rebooted with a CTL-ALT-DEL key combination. Changes made to the Setup parameters (with the exception of the real-time clock time and date settings) do not take effect until the system is rebooted.

The Setup program is located in the ROM BIOS. To access Setup, press DEL while the computer is in the Power On Self Test (POST), just prior to booting. This is called *hot key* access. The screen will display a message indicating when entering DEL will access Setup.

Some Setup fields, for example, the amount of DRAM memory installed on the board, are read-only fields, intended for informational purposes only.

Setup Help

You can access help information for many of the Setup options by pressing F1. The information is displayed in a popup window. Some help screens list all the available option settings, while others display additional information.

Table 2– 54 summarizes the choices found on each Setup page.

Table 2– 54. Functions on Each Setup Page

Page	Menu Name	Functions
1	Main Menu	Select various Setup screens Load Setup defaults Save and/or Exit Setup
2	Standard CMOS Setup	Set date and time Enter IDE hard disk parameters Set type and number of floppy disks Set default video state Configure BIOS error handling Displays amount of installed DRAM memory

Table 2– 54 (cont.). Functions on Each Setup Page

Page	Menu Name	Functions
3	BIOS Features Setup	Enable/disable virus warning message Enable/disable internal CPU cache Enable/disable external cache Enable/disable quick POST Select boot sequence Additional floppy parameters Set NumLock default state Set initial system speed Configure keyboard typematic rates Enable/disable PCI/VGA palette snoop Select VGA video IRQ Set watchdog timer parameters Enable/disable system status messages Select OS for DRAM > 64MB Enable/disable shadowing of memory areas Enable/disable serial console Enable/disable boot loader
4	Chipset Features Setup	Configure memory timing (not recommended) Enable/disable cache options
5	Power Management Setup	Set power management level Set power management options Set power management timers Select power management events
6	PCI Configuration Setup	IRQ configuration IDE interrupt configuration
7	Integrated Peripherals Setup	Set IDE mode Enable/disable/configure IDE interfaces Enable/disable support for USB keyboard Enable/disable floppy disk controller Enable/disable/configure serial ports Configure for IrDA support Enable/disable/configure parallel port Configure video mode, select flat panel type Enable/disable Ethernet interface Enable/disable Ultra SCSI interface

Setup 1 — Main Menu

The first Setup page contains a menu for accessing several Setup screens, plus several additional parameters. Figure 2– 6 shows Setup page 1. Sections following the figure describe each option.

```
                        CMOS SETUP UTILITY
                     Ampro Computers, Inc.

STANDARD CMOS SETUP               INTEGRATED PERIPHERALS
BIOS FEATURES SETUP               LOAD SETUP DEFAULTS
CHIPSET FEATURES SETUP            SAVE & EXIT SETUP
POWER MANAGEMENT SETUP            EXIT WITHOUT SAVING
PCI CONFIGURATION SETUP



        ESC : Quit  ↑↓→←    : Select Item
        F1  : Help  (Shift)F2 : Change Color


      Help messages for each feature line appear here
```

Figure 2– 6. Setup 1 — Main Menu

The main menu screen allows the selection of other optional setup screens.

- **STANDARD CMOS SETUP** – allows the setup of time, date, hard and floppy disk, video and POST halt conditions.
- **BIOS FEATURES SETUP** – selects BIOS features including Virus Warning, caching, POST speed, boot sequence, floppy features, A20 options, memory parity, keyboard typematic selection, security, PCI/VGA palette snoop, shadowing, and onboard SCSI.
- **CHIPSET FEATURES SETUP** – allows the modification of CHIPSET function including configuration, AT bus clock, DRAM timing, SRAM timing, refresh, ISA bus timing, memory allocation at 15M, CPU pipelining, IDE controller, IDE buffering, secondary IDE, IDE modes, and onboard FDC, serial, and parallel port.
- **POWER MANAGEMENT SETUP** – selects the power management features and their implementation.
- **PCI CONFIGURATION SETUP** – configures the PCI interrupt and other PCI unique features.
- I**NTEGRATED PERIPHERALS** – configures the onboard peripheral device such as serial, parallel and other devices.
- **LOAD SETUP DEFAULTS** – initializes all CMOS settings to a predefined default state.
- **SAVE & EXIT SETUP** – option prompts to save CMOS information and exits.
- **EXIT WITHOUT SAVING** – exits setup without writing setup information.

Setup 2 — Standard CMOS Setup

Use Setup 2 to set the date and time, configure your hard and floppy disks, and report system memory. Figure 2– 7 shows what can be configured on Setup 2, and the sections that follow describe each parameter.

```
                     STANDARD CMOS Setup
                   Ampro Computers, Inc.

Date (mm:dd:yyyy) : Wed, Feb 23, 1998
Time (hh:mm:ss)   :  8 : 17 : 25

HARD DISK            TYPE  SIZE   CYLS HEAD PRECOMP LANDZ SECTOR MODE
Primary Master   : Auto    0       0    0      0      0       0 AUTO
Primary Slave    : Auto    0       0    0      0      0       0 AUTO
Secondary Master : Auto    0       0    0      0      0       0 AUTO
Secondary Slave  : Auto    0       0    0      0      0       0 AUTO

Drive A       : 1.44M, 3.5 in.        Base Memory:         640K
Drive B       : None                  Extended Memory: 31744K
Video         : EGA/VGA               Other Memory:        384K
Halt On       : All Errors            Total Memory:      32768K

ESC : Quit:          ↑ ↓ → ← : Select Item        PU/PD/+/- : Modify
F1  : Help           (Shift)F2 : Change Color
```

Figure 2– 7. Setup 2 — Standard CMOS Setup

This Setup screen allows you to configure the following parameters:

- **DATE** and **TIME** — requires the numeric entry of *mm:dd:yyyy*. (Note full 4 digit year.) Day of the week and calendar month are displayed. Time and date entries take effect as soon as they are entered.

- **HARD DISK** — set the parameters for the drives connected to the IDE interface. (No parameters are displayed for an auto-detected HD.) When Auto TYPE is used, the MODE should also be AUTO. When using any modern IDE drive larger than 512MB, AUTO is the best choice. See "IDE Hard Disk Drives" below for more information.

- **FLOPPY DISK** — select the type of floppy drive(s) connected to the floppy drive interface. See *Floppy Drives* below for more information.

- **VIDEO** — select the initial video mode. See "Video" below for more information.

- **HALT ON** — select the Power On Self Test (POST) response to errors. See "Error Halt" below for more information.

- **Base Memory, Extended Memory, Other Memory** — displays the amount of memory detected by the BIOS. Other Memory reports memory used for ROM shadowing the system BIOS, video BIOS, SCSI BIOS, and any other system extensions. It is not available for general OEM use. See "DRAM Memory" below for more information.

EIDE Hard Disk Drives

The module supports up to two hard disk drives connected to the IDE interface. Only hard disk drives are directly supported in the system's ROM BIOS. IDE CD-ROM drives and other IDE-interfaced peripherals are configured by software or drivers supplied separately.

Physical drives can have one or more logical partitions. You can install up to eight logical drives using drive partitions.

To configure the system for the IDE hard drives in your system, set the drive parameters with Setup, as outlined here:

■ **Drive Types** — the configuration memory contains a default list of parameters that specify the physical format of each drive. Each *type* specifies the total number of cylinders, number of heads, cylinder to begin precompensation, landing zone cylinder number, and the number of sectors per cylinder. The drive manufacturer supplies these parameters. The list contains "legacy values", standard for PCs — a number of older (smaller) drives are defined.

Drive type **USER** lets you enter drive parameters manually. If no built-in drive type matches your drive, select drive type USER and enter the drive parameters in the fields provided.

Drive type **AUTO** selects **Autoconfigure**. Autoconfigure queries the drive for its parameters. Most modern drives will respond to the query, allowing the BIOS to set the drive parameter values automatically. This option also provides Logical Block Addressing (LBA) capability, which is used to support drives larger than 512M bytes.

Note

> LBA uses a translation scheme to convert physical heads, sectors and cylinders to logical block numbers. Due to differences in the translation schemes used by different system BIOSes, LBA-compatible drives that have been formatted on Ampro systems may not function properly in other systems that support LBA mode. However, due to the intelligent translation algorithm in the Ampro BIOS, drives formatted in other systems are likely to be usable on the Little Board/P5*x* CPU. Note that this only applies to IDE drives that support LBA mode. Consult the technical literature for the drive you select to find out if it supports LBA mode.

Drive Selection

Besides specifying the physical characteristics of each IDE drive, you must also specify whether a drive is a *master* or *slave* drive. The first drive in a system is always configured as a master drive. A second drive would be a slave drive. Each manufacturer may use a different scheme to handle the master and slave relationship, so drives from different manufacturers may not be compatible. Be sure to test drive compatibility in systems with two IDE drives.

Drives default to master from the factory, so if you only have one IDE drive in a system it is generally already set up properly.

Once you have set the system's configuration memory, the IDE drive(s) can be formatted and otherwise prepared normally. Refer to your operating system and disk drive documentation for specific procedures and requirements.

Floppy Drives

The ROM BIOS supports all of the popular DOS-compatible floppy disk formats. This includes all the 5-1/4 inch and 3-1/2 inch floppy formats — 360K, 720K, 1.2M, and 1.44M.

Drive Parameter Setup

Enter the number and type of floppy drives in the system. If the drives connected to the system do not match the parameters in the configuration memory, POST displays an error message. To eliminate the error message, set the drive parameters to match your floppy drives.

Video

Specify the initial video mode. Select **Mono**, **CGA40, CGA80**, or **EGA/VGA**. If your video display card is VGA, super VGA, or any other high resolution standard, specify **EGA/VGA** no matter how it is configured to come up.

Error Halt

Select which kinds of errors will halt the Power-On Self Test (POST). If you plan to use the module without a keyboard, be sure to set this option to *not* halt on keyboard error.

DRAM Memory

The ROM BIOS automatically detects the amount of memory during POST and stores the result when you save the configuration values when exiting Setup. This Setup page displays the amount of memory found in the system.

Setup 3 — BIOS Features Setup

Use Setup 3 to set a variety of BIOS feature options. Figure 2– 8 shows what can be configured on Setup 3, and the sections that follow describe each parameter.

```
                        BIOS FEATURES Setup
                       Ampro Computers, Inc.

Virus Warning              : Disabled   Video BIOS Shadow      : Enabled
CPU Internal Cache         : Enabled
External Cache             : Disabled   Serial Console         : Disabled
Quick Power On Self Test   : Disabled   Serial Boot Loader     : Disabled
Boot Sequence              : A,C        OEM Flash (S0)         : Disabled
Swap Floppy Drive          : Disabled
Boot Up Floppy Seek        : Enabled
Boot Up NumLock Status     : Off
Typematic Rate Setting     : Enabled
Typematic Rate (chars/Sec) : 6
Typematic Delay (Msec)     : 250
PCI/VGA Palette Snoop:      : Disabled
Assign IRQ for VGA         : Disabled
Watchdog Timer             : Disabled
Show System Status at Boot : Enabled
OS2 Select for DRAM > 64MB : Non-OS2
                                        ESC:Quit          ↑ ↓ → ← :Select Item
                                        F1 :Help          PU/PD/+/-:Modify
                                        F5 :Old Values  (Shift)F2 :Color
                                        F6 :Load BIOS Defaults
                                        F7 :Load Setup Defaults
```

Figure 2– 8. Setup 3 — BIOS Features Setup

This Setup screen allows you to configure the following parameters:

■ **Virus Warning** — monitors for writes to the hard disk boot sector. If a write is detected, the BIOS will display the following warning message, beep the speaker, and wait for user confirmation.

<div align="center">

!!! WARNING !!!
Disk Boot sector is to be modified
type "Y" to accept, any key to abort
Award Software, Inc.

</div>

■ **CPU Internal Cache** — enable or disable the CPU internal cache.

■ **Quick Power On Self Test** — when enabled, the POST will skip some non-essential tests (such as repetitive memory tests) in order to shorten the POST time.

■ **Boot Sequence** — determines the order in which drives should be searched by the disk operating system. Options are **[A, C]**, **[C, A]**, **[A, SCSI]**, **[SCSI, A]**, **[CD, A, C]**, **[C only]**, and **[SCSI only]**. ("C" refers to an IDE drive, and "CD" refers to an IDE CD-ROM drive.)

■ **Swap Floppy Drive** — If two floppy drives are connected to the system, drive A becomes drive B and vice-versa.

■ **Boot Up Floppy Seek** — during POST, the BIOS performs a seek test to determine if the drive is 40 or 80 tracks (360K drives have 40 tracks, other drives have 80 tracks).

- **Boot Up NumLock Status** — sets the default state of the keyboard's numeric keypad. **On** sets the keypad to numbers, **Off** sets the keypad to arrows.
- **Typematic Rate Setting** — enable or disable the typematic function (automatic keyboard key repeat).
- **Typematic Rate (chars/S)** — set the typematic rate. This is the rate at which a held-down key is repeated.
- **Typematic Delay (mS)** — set the time a key must be pressed before typematic repeating begins.
- **PCI/VGA Palette Snoop** — enables PCI- or ISA-based graphics adapters which are not VGA-compatible to monitor writes to the VGA palette registers so they may update their own palette registers accordingly. Note that when PCI/VGA Palette Snoop is enabled, graphic screens may be distorted when booting Windows 95.
- **Assign IRQ for PCI VGA** — Enables auto assignment of VGA IRQ.
- **Watchdog Timer** — sets the timeout delay period for the watchdog timer, or disables it.
- **Show System Status at Boot** — when enabled (the default), some messages about detected hardware features are displayed on the console during the Power-On Self Test.
- **OS Select for DRAM > 64MB** — if you are running OS/2, set to **OS/2**. Otherwise set to **Non-OS/2**. This parameter limits reporting memory above 64 MB, as some operating systems fail when more than 64 MB is reported. Some versions of OS/2 have this problem.
- **Video BIOS Shadow** — The on-board video and SCSI BIOS always run from shadow RAM. PCI devices with on-board ROM are always shadowed. These are not affected by this setting.
- **Serial Console** — enables or disables use of a serial console connected to a serial port. When used as a serial console, the serial port does not appear in the BIOS COM port table. This means that it will not be COM1, COM2, etc. Select the serial port and its BAUD rate, such as **Serial 1@2400**, **Serial 2@9600**, and so forth. Other communication parameters are fixed at 8-bit words, 1 start bit, 1 stop bit, and no parity. Default setup of the serial console port is **Disabled**.
- **Serial Boot Loader** — enables or disables the serial boot loader function. When you enable the boot loader, select either **COM1 or COM2**. Other communication parameters are fixed at 9600 BAUD, 8-bit words, 1 start bit, 1 stop bit, and no parity.

Serial Console Operation During Setup

When Setup is being run using the serial console interface, keyboard arrow keys and function keys must be simulated. The following simulations are used for these keys:

Arrow Keys — arrow keys may be entered as shown on the screen. Use the following substitutes for the arrow keys. Note that there are both standard keys and control key sequences for each command:

^, Ctrl-e	Up arrow	**>, Ctrl-d**	Right arrow
v, Ctrl-x	Down arrow	**<, Ctrl-s**	Left arrow
Ctrl-r	Page up	**Ctrl-c**	Page down

Note that these keys simulate the arrow keys only during Setup, not during normal computer operation.

Function Keys — function keys (F1, F2, etc.) are entered with two keystrokes. The first entry is "F", followed by the number. F10 is simulated by typing "F" and then "0".

The WordStar diamond keys are also implemented identical to the MS-DOS editor.

- Ctrl-e = cursor up
- Ctrl-x = cursor down
- Ctrl-d = cursor right
- Ctrl-s = cursor left
- Ctrl-r = page up
- Ctrl-c = page down.

Note that these keystrokes simulate the function keys only during Setup, not during normal computer operation.

Setup 4 — Chipset Features Setup

Setup 4 — Chipset Features Setup controls internal chipset features. ***The OEM or end user should never change many of these items, as they specify internal parameters that have been chosen to support the existing motherboard design.*** Change these parameters only if directed to by Ampro Technical Support. Figure 2– 9 shows what can be configured on Setup 4. The items that can be changed by the OEM are listed below.

```
                         Chipset Features Setup
                         Ampro Computers, Inc.

Auto Configuration       : Enabled    Turn on CPU Fan        : 40°C/104°F
DRAM Timing              : 70ns       Current CPU Temperature : 68°C/154°F
DRAM Leadoff Timing      : 10/6/4
DRAM Read Bursts (EDO/FP) : x333/x444
DRAM Write Burst Timing  : x333
Fast EDO Lead Off        : Disable
Refresh RAS# Assertion   : 5 Clocks
Fast RAS To CAS Delay    : 3
DRAM Page Idle Timer     : 2 Clocks
DRAM Enhanced Paging     : Enabled
Fast MA to RAS# Delay    : 2 Clocks
SDRAM (CAS Lat/RAS-to-CAS) : 3/3
SDRAM Speculative Read   : Disabled
System BIOS Cacheable    : Disabled
Video BIOS Cacheable     : Disabled
8-bit I/O Recovery Time  : 1
16-Bit I/O Recovery Time : 2
Memory Hole At 15M-16M   : Disabled
PCI 2.1 Compliance       : Disabled   ESC:Quit  ↑ ↓ → ←   : Select Item
                                      F1 :Help  PU/PD/+/-  : Modify
                                      F5 :Old Values  (Shift)F2:Color
                                      F6 :Load BIOS Defaults
                                      F7 :Load Setup Defaults
```

Figure 2– 9. Setup 4 — Chipset Features Setup

This Setup screen allows you to configure the following parameters:

- **Auto Configuration** — if enabled, the DRAM timing selection of 70 nS or 60 nS automatically configures the following five RAM timing parameters. If disabled, these parameters must be configured manually. This option should be left in its default state. Contact Ampro Technical Support or your Ampro Sales Representative for advice if you have unique requirements that require changing these parameters.
- **System and Video BIOS Cacheable** — these options allow BIOS code to be cached in the CPU.
- **8- and 16-Bit I/O Recovery Time** — these options allow additional delays to be inserted between PCI-initiated I/O transactions to the ISA bus. Options are 1 to 8 clocks, or NA, for now additional delays.
- **Memory Hole at 15M-61M** — certain peripheral adapters may require memory in the 15M-16M address range for expansion ROM use. The memory hole option creates a 1 MB memory hole below the 16 M boundary for this purpose.

■ **PCI 2.1 Compliance** — this parameter controls the timing of certain PCI bus transactions. Select Enabled only if all PCI devices in the system are known to be compliant with Version 2.1 of the PCI specification.

■ **Turn on CPU Fan** — The fan interface is controlled by an external temperature monitor physically located below the CPU. "Current CPU Temperature:" displays a calculated value. The temperature difference between the monitor and the CPU was measured at 5°C.

Setup 5 — Power Management Setup

The Little Board/P5*x* CPU BIOS incorporates power management features compliant with Advanced Power Management (APM) BIOS Interface Specification Revision 1.1, created by Intel and Microsoft. Setup 5 — Power Management Setup allows you to configure your system to most effectively save energy while operating at the speed and response level you need in your application. Figure 2– 10 shows what can be configured on Setup 5. A description of each option is listed below.

Note

When features of the APM BIOS are enabled, some reduced power states are entered automatically. Reduced power states alter the performance of the system, usually slowing or halting the CPU. Use the power management functions with care when using the Little Board in applications that require guaranteed maximum response times.

```
                      POWER MANAGEMENT Setup
                      Ampro Computers, Inc.

Power Management     : Max-Saving    ** Reload Global Timer Events **
PM Control by APM    : Yes           IRQ[3-7,9-15],NMI     : Enabled
Video Off Option     : V/H SYNC+Blank Primary IDE 0        : Disabled
CPU Thermal Mgmt.    : Disable       Primary IDE 1         : Disabled
Modem Use IRQ        : 3             Secondary IDE 0       : Disabled
Doze Mode            : 1 Min         Secondary IDE 1       : Disabled
Standby Mode         : 1 Min         Floppy Disk           : Disabled
Suspend Mode         : 1 Min         Serial Port           : Enabled
HDD Power Down       : 1 Min         Parallel Port         : Disabled
Throttle Duty Cycle  : 62.5%         Thermal Duty Cycle    : Disabled
ZZ Active in Suspend : Disabled
Soft-Off by PWR-BTTN : Instant-Off
Resume By Ring       : Enabled
Resume By Alarm      : Disabled
IRQ 8 Break Suspend  :Disabled

                                    ESC:Quit  ↑ ↓ → ← : Select Item
                                    F1 :Help PU/PD/+/- : Modify
                                    F5 :Old Values   (Shift)F2:Color
                                    F6 :Load BIOS Defaults
                                    F7 :Load Setup Defaults
```

Figure 2– 10. Setup 5 — Power Management Setup

This Setup screen allows you to configure the following parameters:

- **Power Management** — sets the type or degree of power savings and is directly related to the power management modes defined by the APM specification. Settings are **Disable** (default), **Min. Savings**, **Max. Savings**, and **User Defined**. The difference between Min and Max Savings is the time delay period between modes.
- **PM Control by APM** — when enabled, it allows operating systems with power management support to control the modes required for safe operation of shutdown occurrences.

■ **Video Off Option** — sets the conditions under which the BIOS powers down the video (assuming your video interface supports power management). Select the **DPMS** option only if your monitor supports the VESA Display Power Management Signaling standard. **H/H SyNC+Blank** turns off the horizontal and vertical sync signals and blanks the video buffer. **Blank Screen** only blanks the video buffer.

■ **Thermal Duty Cycle** — CPU temperature may be controlled by an optional fan. When enabled the CPU performance will be limited by the stop clock interface at the percentage indicated when the CPU Fan is running.

The power management timers are only configurable if the **Power Management** option is set to **User Defined**. Each timer sets the amount of idle time before the system enters the specified power-saving mode. These modes are:

■ **Doze Mode** — when enabled and after a set time of system inactivity, the CPU clock speed is reduced. Other devices remain active.

■ **Standby Mode** — when enabled and after a set time of system inactivity, the CPU clock speed is reduced, and the disk drives and video monitor are shut down. Other devices remain active.

■ **Suspend Mode** — when enabled and after a set time of system inactivity, all activities except DRAM refresh are shut down.

■ **HDD Power Down** — when enabled and after a set time of system inactivity, the hard disk drives are shut down. All other devices remain active.

■ **Throttle Duty Cycle** — selects a percentage of time the CPU runs in Doze Mode.

■ **ZZ Active In Suspend** — controls L2 Cache Sleep signal during Suspend Mode. When enabled, the ZZ signal will be asserted under certain conditions when entering clock control mode. NOTE: The L2 cache can not be snooped with the ZZ signal asserted. It must be disabled in Level 2 power states such as Stop Grant.

■ **VGA Active Monitor** — when enabled, any video activity restarts the Standby Mode timer.

■ **Soft-Off by PWR-BUTTN** — Enables PWR-BUTTN input. A 4 second signal from this input will cause a power-down of all on-board systems.

■ **Resume by Ring** — Ring Detect on Serial Port 1 will cause an exit from any active power management mode.

■ **Resume by Alarm** — RTC Alarm will cause power management mode exit.

■ **IRQ 8 Break Suspend** — RTC Interrupt will cause power management mode exit.

■ **Reload Global Timer Events** — any of the Reload Global Timer Events will cause the Standby Mode timer to be restarted when the event is detected.

Setup 6 — PCI Configuration Setup

The Little Board/P5*x* CPU BIOS incorporates automatic PCI IRQ configuration for peripherals. You can, however, override the automatic features and specify PCI IRQ settings with SETUP 6. Figure 2– 11 shows what can be configured on SETUP 6. A description of each option is listed below.

```
┌──────────────────────────────────────────────────────────────────────┐
│                    PCI CONFIGURATION SETUP                             │
│                     Ampro Computers, Inc.                             │
├──────────────────────────────────┬───────────────────────────────────┤
│ 1st Available IRQ      :9         │                                   │
│ 2nd Available IRQ      :11        │                                   │
│ 3rd Available IRQ      :5         │                                   │
│ 4th Available IRQ      :10        │                                   │
│ PCI IDE IRQ Map To     :ISA       │                                   │
│                                   │                                   │
│                                   │                                   │
│                                   ├───────────────────────────────────┤
│                                   │ ESC:Quit        ↑ ↓ → ← : Select Item │
│                                   │ F1 :Help        PU/PD/+/- : Modify │
│                                   │ F5 :Old Values  (Shift)F2:Color    │
│                                   │ F6 :Load BIOS Defaults             │
│                                   │ F7 :Load Setup Defaults            │
└──────────────────────────────────┴───────────────────────────────────┘
```

Figure 2– 11. SETUP 6 — PCI Configuration Setup

This Setup screen allows you to configure the following parameters:

- **Nth Available IRQ** — selects the order in which ISA IRQ channels can be assigned to PCI devices.
- **PCI IDE Options** — these options must be left in their default state.

Setup 7 — Integrated Peripherals Setup

The peripheral interfaces integrated on the Little Board/P5x can be configured on Setup 7 — Integrated Peripherals Setup (Figure 2– 12). You can configure the IDE port, USB port, floppy controller, IrDA port, serial ports, and parallel port from this screen.

```
                    INTEGRATED PERIPHERALS SETUP
                       Ampro Computers, Inc.

IDE HDD Block Mode         : Enabled    Onboard Parallel Port     : 378/IRQ7
IDE Primary Master PIO     : Auto       Parallel Port Mode        : ECP+EPP1.9
IDE Primary Slave PIO      : Auto       ECP Mode use DMA          : 3
IDE Primary Master UDMA    : Auto       Onboard Serial Port 3     : Enabled
IDE Primary Slave UDMA     : Auto       Onboard Serial Port 4     : Enabled
IDE Secondary Master PIO   : Auto       Serial Port 4 use IRQ     : IRQ3
IDE Secondary Slave PIO    : Auto
IDE Secondary Master UDMA  : Auto       On-Board VGA Display      : CRT/FP
IDE Secondary Slave UDMA   : Auto       VGA Flat Panel Type       : 1
On-Chip Primary PCI IDE    : Enabled    Flat Panel Video          : Normal
ON-Chip Secondary PCI IDE  : Enabled    Onboard PCI Ethernet      : Disabled
                                        Onboard Ultra SCSI        : Enabled
USB Keyboard Support       : Disabled

Onboard FDC Controller     : Enabled    ESC:Quit        ↑ ↓ → ← : Select Item
Onboard Serial Port 1      : Enabled    F1 :Help          PU/PD/+/-: Modify
Onboard Serial Port 2      : Enabled    F5 :Old Values    (Shift)F2:Color
UART2 Mode                 : Standard   F6 :Load BIOS Defaults
                                        F7 :Load Setup Defaults
```

Figure 2– 12. SETUP 6 — PCI Configuration Setup

- **IDE HDD Block Mode** — when enabled, this allows your hard drive system to use a mode where the interface transfers large blocks of data instead of the normal small blocks. **Enabled** is the default state, and works for newer hard drives. Disable this feature if your drive does not support block mode transfers.

- **IDE Primary/Secondary Master/Slave PIO Mode** — sets the PIO mode for devices attached to the IDE interface. **Auto** (default) lets the BIOS automatically determine what mode is fastest for each device. **Mode 1** through **Mode 4** forces the BIOS to use the specified mode, and overrides the MODE setting on the Standard CMOS Setup Screen, Setup 2.

- **IDE Primary/Secondary Master/Slave UDMA** — enable or disable support for Ultra DMA/33 mode on the selected IDE device. When set to "AUTO", Ultra DMA/33 will be used if it is supported by the connected IDE drive.

- **On-Chip Primary/Secondary PCI IDE** — enable or disable the primary or secondary IDE controller.

- **USB Keyboard Support** — allows a USB keyboard to be used as the system keyboard. Disabling this option only removes support for USB keyboards. The USB interface is still available for other devices.

- **Onboard FDC Controller** — enables or disables the on-board floppy disk controller.

- **Onboard UART *n*** — configures each serial port's address and interrupt. Available choices for the I/O addresses are 3F8, 2F8, 3E8, and 2E8. Available IRQ choices are IRQ3 and IRQ4. If you select Auto, the BIOS makes the choices for you. You may also disable either port.

- **UART2 Mode** — configures the second serial port to be a standard serial port or for one of the IrDA modes. Enabling one of the IrDA modes provides access to the IR configuration parameters. Available IrDA modes are HPSIR (standard IrDA), ASKIR (amplitude shift keyed infrared), fast IR, or TTL.

- **Onboard Parallel Port** — set the parallel port address and IRQ assignments. Available addresses are 378, 278, or 3BC. Available IRQ assignments are IRQ 7 and IRQ5. You may also disable the port.

- **Parallel Port Mode** — set the parallel port mode.

- **ECP Mode Use DMA** — selects a DMA channel to use with the ECP mode of the parallel port. This selection only applies if the parallel port is configured for ECP or ECP/EPP modes.

- **Onboard VGA Display** — selects either CRT, flat panel (FP), or both. In CRT/FP mode the CRT may not display correctly depending on the Flat Panel selected and the scan capabilities of the CRT monitor. On-board VGA display default is CRT/FP.

- **VGA Flat Panel Type** — There is support for 16 VGA Flat Panel Types, numbered 1 to 16. Contact Technical Support for a list of supported panels.

- **Flat Panel Video** — select either normal video or reversed video.

- **Onboard PCI Ethernet** — enable or disable the on-board Ethernet controller.

- **Onboard Ultra SCSI** — enable or disable the on-board Ultra SCSI controller.

Chapter 3

Technical Specifications

Little Board/P5*x* SPECIFICATIONS

The following section provides technical specifications for the Little Board/P5*x*.

CPU/Motherboard

- CPU: Pentium processor
- System RAM:
    - DIMM module, utilizing 3.3V EDO, or SDRAM memory chips
    - Supports from 16M bytes to 256M bytes total RAM
    - Requires 60 Ns or faster DRAMS, without parity
- 512K level-two cache, synchronous-burst
- Shadow RAM support provides fast system BIOS and video BIOS execution
- 15 interrupt channels (8259-equivalent)
- 7 DMA channels (8237-equivalent)
- 3 programmable counter/timers (8254-equivalent)
- Standard PC/AT keyboard port
- Standard PC speaker port with .1 watt output drive
- Battery-backed real-time clock and CMOS RAM:
    - Up to 10 year battery life
    - Supports battery-free operation
- Ampro Extended BIOS

Embedded-PC System Enhancements

- Compact Flash Socket:
    - Usable with standard Compact Flash modules
    - Equivalent to an IDE drive
- OEM Flash Memory (available with 1M byte Flash BIOS option)
    - 768K OEM Flash memory is available for OEM use
- 4K-bit configuration EEPROM:
    - Stores system Setup parameters
    - Supports battery-free boot capability

- – 512 bits available for OEM use
- ■ Watchdog Timer
  - – Selectable Timeout: 30 seconds / 60 seconds / 90 seconds / Disabled
  - – Timeout triggers hardware reset
- ■ Powerfail NMI triggers when +5 Volt power drops below +4.7 Volts.

On-board Peripherals

This section describes standard peripherals found on every Little Board/P5x.

- ■ Four buffered serial ports with full handshaking
  - – Implemented with 16550-equivalent controllers with built-in 16-byte FIFO buffers
  - – On-board generation of RS-232C signal levels
  - – Serial 1 supports either RS-232C or RS-485
  - – Logged as COM1, COM2, COM3, and COM4 by DOS
  - – Serial 1/Serial 3 and Serial2/Serial4 share interrupts (IRQs)
- ■ Multi-mode Parallel Port
  - – Superset of standard LPT printer port
  - – Bi-directional data lines
  - – IEEE-1284 (EPP/ECP) compliant
  - – Standard hardware supports all four IEEE-1284 protocol modes
  - – Internal 16-byte FIFO buffer
  - – DMA option for data transfers
- ■ Floppy Disk Controller
  - – Supports one or two drives
  - – Reliable digital phase-locked loop circuit
  - – BIOS supports all standard PC/AT formats: 360K, 1.2M, 720K, and 1.44M
- ■ PCI EIDE Disk Controllers
  - – PCI bus implementation of Extended IDE (EIDE) hard disk controllers (2)
  - – Supports up to four hard disk drives.
  - – Fast ATA-capable interface supports high-speed PIO modes
  - – BIOS supports drives larger than 528 M bytes through Logical Block Addressing (LBA)
  - – Supports Compact Flash interface
- ■ PCI UltraSCSI Interface
  - – ANSI X3.131-compliant
  - – Uses the Adaptec AIC 7860 controller
  - – Synchronous or asynchronous data transfer

- – Supports UltraSCSI data transfers at up to 20 MB/sec

- – On-board active terminators for low current drain

- – Built-in Adaptec SCSI-BIOS

- – Compatible with standard SCSI driver products that are ASPI-compatible

■ PCI Flat Panel/CRT Video Controller

- – Supports CRT, LCD, and video (NTSC, PAL) displays

- – Uses state-of-the-art Chips and Technologies HiQVideo™ Multimedia Accelerator chips

- – On-board display RAM: 2M bytes SDRAM standard, 4M bytes by special order.

- – Video modes, resolutions, and memory requirements: See video tables starting on page 3–6.

- – Supports interlaced or non-interlaced displays in up to 1600 x 1200 resolution modes

- – Supports 24-bit True Color at 800 x 600 VGA resolution

- – GUI accelerator for enhanced performance

- – Video BIOS supports VESA DPMS and DDC; supports all standard super VGA modes. See video tables starting on page 3–6.

- – Software programmable flat-panel interface. Flat panel video BIOS contained in an on-board Flash EPROM device for easy customization

- – Standard model supports 3.3V flat panels; support for 5V flat panels with external adapter.

- – Supports Chips and Technologies Zoom Video Port

- – Optional LCD Bias Supply. Circuit board plugs on to connector on the Little Board/P5*x*

  - – Supplies 15 V < Vee < 35 V DC, positive or negative polarity, at 30 mA (Max)

  - – Voltage level (LCD contrast control) adjustable with an on-board or external potentiometer

  - – Sequences LCD power supplies to protect display

  - – Implements Advanced Power Management (APM) functions

■ Ethernet LAN Interface

- – Complies with IEEE 802.3 (ANSI 8802-3) MII

- – Controller: Am79C972 PCnet™ FAST+ Enhanced 10/100 Mbps Ethernet controller

- – Topology: Ethernet bus, using CSMA/CD

- – Plug and Play compatible

- – 10/100BaseT via an on-board RJ-45 connector

- – Data rate: automatic arbitration for 10/100 Mbit operation

- – 32-bit PCI host interface for fast operation, up to 33 MHz PCI clock frequency (PCI specification revision 2.1)

- – High-performance bus mastering capability

- – Boot ROM image can be installed in system using a Flash programming utility (provided)

Support Software

- Ampro embedded PC-BIOS features:
    - Watchdog timer (WDT) support
    - Fast boot options
    - Fail-safe boot logic
    - Battery-free boot
    - Serial console option
    - Serial loader option
    - EEPROM access functions
    - Advanced Power Management (APM) support
    - Large hard disk Logical Block Addressing (LBA) support

    See the Ampro Embedded-PC BIOS data sheet for additional details about these features.

- Software Utilities included:
    - Watchdog timer support
    - Serial access and development support
    - SCSI support, including ASPI manager
    - Display controller support
    - Ethernet controller support

Mechanical and Environmental Specifications

- 8.0 x 5.75 x 1.2* inches (146 x 203 x 30 mm). Refer to Figure 1–2 for mounting dimensions.
- Power requirements (typical, with 16M byte DRAM, measured at 5V ± 5%)

    Power requirements can vary, depending on the installed CPU and type of system DRAM installed. Table 3– 1 shows some examples of power requirements for various configurations.

Table 3– 1. Power Requirements

CPU Speed	DOS Prompt EDO DRAM Amps / Watts	Maximum EDO DRAM Amps / Watts	DOS Prompt SDRAM Amps / Watts	Maximum SDRAM Amps / Watts
166MHz Tillamook	1.963 /9.815	2.105 / 10.525	2.080 / 10.401	2.173 / 10.864
266MHz Tillamook	2.242 / 11.204	2.352 / 11.759	2.346 / 11.728	2.370 / 11.852
All measurements performed with 16MB Memory				

■ Operating environment:
  – Standard: 0° to 60° C (with adequate airflow); 0° to 70° C (with VRT processor); Extended temperature range can be tested by special order

  – 5 to 95% relative humidity (non-condensing)

■ Storage temperature: -55° to +85° C

■ Weight: 11.6 oz. (329 gm), no DRAM installed

■ Shock and Vibration

– Tested to MIL-STD 202F, Method 213B, Table 213-I, Condition A (three 50G shocks in each axis) and MIL-STD 202F, Method 214A, Table 214-I, Condition D (11.95B random vibration, 100 Hz to 1000 Hz for 5 minutes per axis).

■ ISA portion of the PC/104-Plus expansion bus

  – Female, non-stackthrough, 16-bit bus connectors, for expansion via PC/104 modules

  – Four mounting holes

■ PCI portion of the PC/104-Plus expansion bus:

  – 4 x 30 (120-pin) 2 mm. pitch non-stackthrough connector.

  – Electrical specifications equivalent to the PCI Local Bus Specification Rev. 2.1.

Note

Contact Ampro regarding custom configurations and special order options.

Flat Panel Displays

The Little Board/P5x display controller supports all flat panel display technologies including plasma, electroluminescent (EL), and LCD. LCD panel types include single panel-single drive (SS), and dual panel-dual drive (DD) configurations.

Note

> Panel technology is changing rapidly. Flat panel support in the Little Board/P5x ROM BIOS will change from time to time to maintain compatibility with current panel technology.

Table 3– 2. Flat Panel Controller Display Capabilities

Resolution	CRT Colors	Mono LCD Gray Scales	DD STN LCD Colors	9-bit TFT LCD Color	Video Memory	Simul-taneous Display?
320 x 200	256/256K	61/61	256/226,981	256/185,193	512K	Yes
640 x 480	16/256K	16/61	16/226,981	16/185,193	512K	Yes
640 x 480	256/256K	61/61	256/226,981	256/185,193	512K	Yes
800 x 600	16/256K	16/61	16/226,981	16/185,193	512K	Requires 1M
800 x 600	256/256K	61/61	256/226,981	256/185,193	512K	Requires 1M
1024 x 768	16/256K	16/61	16/226,981	16/185,193	512K	Requires 1M
1024 x 768	256/256K	61/61	256/226,981	256/185,193	1M	Yes
NOTE: Availability of colors and palette capacity depends on internal settings controlled by the video BIOS. A customized version of the BIOS is required for some displays.						

Table 3– 3. Supported CRT Video Modes—Standard VGA

Mode	Display Mode	Colors	Text	Font	Pixels	Clock (MHz)	Horiz (KHz)	Vert (Hz)
0+, 1+	Text	16	40x25 40x25 40x25	9x16 8x14 8x8	360x400 320x350 320x200	28.322 25.175 25.175	31.5	70
2+, 3+	Text	16	80x25 80x25 80x25	9x16 8x14 8x8	720x400 640x350 640x200	28.322 25.175 25.175	31.5	70
4	Graphics	4	40x25	8x8	320x200	25.175	31.5	70
5	Graphics	4	40x25	8x8	320x200	25.175	31.5	70
6	Graphics	2	80x25	8x8	640x200	25.175	31.5	70
7+	Text	Mono	80x25 80x25 80x25	9x16 9x14 9x8	720x400 720x350 720x350	28.322	31.5	70
D	Planar	16	40x25	8x8	320x200	25.175	31.5	70

Table 3– 4. Supported CRT Video Modes—Standard VGA (Cont.)

Mode	Display Mode	Colors	Text	Font	Pixels	Clock (MHz)	Horiz (KHz)	Vert (Hz)
E	Planar	16	80x25	8x8	640x200	25.175	31.5	70
F	Planar	Mono	80x25	8x14	640x350	25.175	31.5	70
10	Planar	16	80x25	8x14	640x350	25.175	31.5	70
11	Planar	2	80x30	8x16	640x480	25.175	31.5	60
12	Planar	16	80x30	8x16	640x480	25.175	31.5	60
13	Packed Pixel	256	40x25	8x8	320x200	25.175	31.5	70

CRT Support for Standard Video Modes:

- PS/2 fixed frequency analog CRT monitor or equivalent. 31.5/35.5 KHz horizontal frequency.
- Multi-frequency CRT monitor. 37.5 KHz minimum horizontal frequency.
- Multi-frequency high-performance CRT monitor. 48.5 KHz minimum horizontal frequency.

Table 3– 5. Supported CRT Video Modes—Extended Resolution

Mode	Display Mode	Colors	Text	Font	Pixels	Clock (MHz)	Horiz (KHz)	Vert (Hz)	Mem.	CRT
20	4-bit Linear	16	80x30	8x16	640x480	25.175	31.5	60	512K	a, b, c
22	4-bit Linear	16	100x37	8x16	800x600	40.000	37.5	60	512K	b,c
24	4-bit Linear	16	128x48	8x16	1024x768	65.000	48.5	60	512K	c
24I						44.900	35.5	43	512K	b,c
30	8-bit Linear	256	80x30	8x16	640x480	25.175	31.5	60	512K	a,b,c
32	8-bit Linear	256	100x37	8x16	800x600	40.000	37.5	60	512K	b,c
34	8-bit Linear	256	128x48	8x16	1024x768	65.000	48.5	60	1M	c
34I						44.900	35.5	43	1M	b,c
40	15-bit Linear	32K	80x30	8x16	640x480	50.350	31.5	60	1M	a,b,c
41	16-bit Linear	64K	80x30	8x16	640x480	50.350	31.5	60	1M	a,b,c
50	24-bit Linear	16M	80x30	8x16	640x480	65.000	27.1	51.6	1M	b,c
60	Text	16	132x25	8x16	1056x400	40.000	30.5	68	256K	a,b,c
61	Text	16	132x50	8x16	1056x400	40.000	30.5	68	256K	a,b,c
6A,70	Planar	16	100x37	8x16	800x600	40.000	38.0	60	256K	b,c
72,75	Planar	16	128x48	8x16	1024x768	65.000	48.5	60	512K	c
72I,75I						44.900	35.5	43	512K	b,c
78	Packed Pixel	16	80x25	8x16	640x400	25.175	31.5	70	256K	a,b,c
79	Packed Pixel	256	80x30	8x16	640x480	25.175	31.5	60	512K	a,b,c
7C	Packed Pixel	256	100x37	8x16	800x600	40.000	37.5	60	512K	b,c
7E	Packed Pixel	256	128x48	8x16	1024x768	65.000	48.5	60	1M	c
7EI						44.900	35.5	43	1M	b,c

(The "I" in the **Mode #** column indicates "Interlaced.")

Table 3– 6. Supported CRT Video Modes—High Refresh

Mode	Display Mode	Colors	Text	Font	Pixels	Clock (MHz)	Horiz (KHz)	Vert (Hz)	Mem.	CRT
12	Planar	16	80x30	8x16	640x480	31.500	37.5	75	256K	b, c
30	8-bit Linear	256	80x30	8x16	640x480	31.500	37.5	75	256K	c
79	Packed Pixel	256	80x30	8x16	640x480	31.500	37.5	75	512K	c
6A,70	Planar	16	100x37	8x16	800x600	49.500	46.9	75	512K	c
32	8-bit Linear	256	100x37	8x16	800x600	49.500	46.9	75	1M	c
7C	Packed Pixel	256	100x37	8x16	800x600	49.500	46.9	75	1M	c

CRT Support for Extended Resolution Modes:

a   PS/2 fixed frequency analog CRT monitor or equivalent. 31.5/35.5 KHz horizontal frequency..

b   Multi-frequency CRT monitor. 37.5 KHz minimum horizontal frequency specification.

c   Multi-frequency high-performance CRT monitor. 48.5 KHz minimum horizontal.

Ampro Product Reliability Testing

Regulatory testing

Knowing that many embedded systems must qualify under EMC emissions and suscepibility testing, Ampro designs boards with careful attention to EMI issues. Boards are tested in standard enclosures to ensure that they can pass such emissions tests. Tests include European Union Directives EN55022 and EN55011 (for EMC), EN61000-4-2 (for ESD), ENV50140 (for RF Susceptibility), and EN61000-4-4 (for EFT). Conducted Emissions testing is also performed at US voltages per FCC Part 15, Subpart J (the European Union Directives are otherwise compatible with Part 15 testing).

Shock and Vibration Testing

Boards intended for use in harsh environments are tested for shock and vibration durability to MIL-STD 202F, Method 213-I, Condition A (three 50G shocks in each axis) and MIL-STD 202F, Method 214A, Table 214-I, Condition D (11.95B random vibration, 100 Hz to 1000 Hz). (Contact your Ampro sales representative to obtain *Shock and Random Vibration Test Report for the Little Board/P5x CPU* for details.)

ISO 9001 Manufacturing

Ampro is a certified ISO 9001 vendor.

Wide-range temperature testing

Ampro Engineering qualifies all of its designs by extensive thermal and voltage margin testing.

Appendix A

Contacts

To contact the PC/104 Consortium for a copy of the proposed PC/104-*Plus* specification:

> PC/104 Consortium
> 849 Independence Avenue, Suite B
> Mountain View, CA 94043
> Telephone: 415 903-8304
> FAX: 415 967-0995

EPP and ECP Operation

The board's parallel port is compliant with the IEEE-1284 Extended Capabilities Port Protocol and ISA Standard (Rev 1.09, January 7, 1993), developed by Microsoft. Contact IEEE Customer Service and request IEEE Std 1284 for information about EPP and ECP operation.

> IEEE Customer Service
> 445 Hoes Lane
> PO Box 1331
> Piscataway, NJ 08855-1331 USA
>
> Phone: (800) 678-IEEE (in the US and Canada)
>   (908) 981-0060 (outside the US and Canada)
> FAX: (908) 981-9667
> Telex: 833233
> Website: http://standards.IEEE.org

Appendix B

Cables

Cables included in the Quick Start Kit (LB3-P5X-K-00) and the Cable Kit (CBL-P5X-Q-01) are detailed in this section. These cables are intended for use during your application development, and are only shown here to aid you in the design of cables for your particular application.

NOTES - UNLESS OTHERWISE SPECIFIED:

1 ARROW REFERENCES PIN 1 INDEX ON CONNECTOR.

2 DO NOT USE STRAIN RELIEF ON CONNECTOR P1.

3 MARK CABLE WITH PART NUMBER AND
   CURRENT REVISION LEVEL.

4 INSTALL KEYING PLUG IN CONTACT 20
   OF ALL THREE CONNECTORS.

◯ = NOTE

◯ = ITEM

P1

P2

P3

15.6±.2

2.40±.10

REV	REVISIONS DESCRIPTION	DATE	APPROVED
A	ECO 0329		
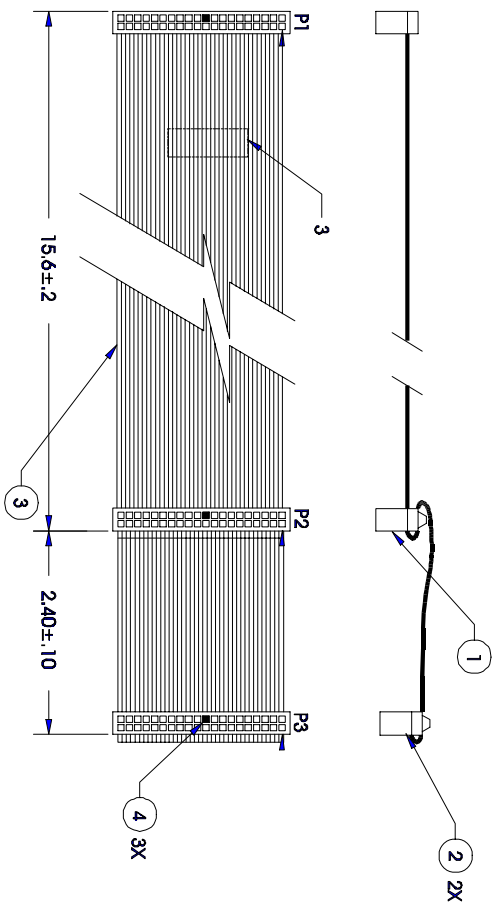
ITEM	QTY	DESCRIPTION	VENDOR ID
4	3	KEYING PLUG	3M #3435-0
3	A/R	CABLE FLAT RIBBON 40 COND	3M #3365/40
2	2	CONN HDR 40 POS FEM CE SR	3M #3417-7040
1	1	CONN HDR 40 POS FEM OE SR	3M #3417-6040

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
±   .XX ± .02   ±
             .XXX ± .010

MATERIAL

FINISH

DO NOT SCALE DRAWING

APPROVALS		DATE
DRAWN	IEC	1/25/90
CHECKED		
ENGR APPV.		
REL.		

SINGLE BOARD SYSTEMS

ASSY, CABLE
DUAL ATA DRIVE

SIZE	DWG. NO.	REV.
C	0800525	A

ACAD FILE: 0800525A

SCALE 1X   SHEET 1 OF 1

NOTES - UNLESS OTHERWISE SPECIFIED:

1 MARK CABLE WITH PART NUMBER AND CURRENT REVISION LEVEL.

2 CUT CONDUCTOR 10 NEAR THIS END.

3 POT THIS END WITH HOT GLUE OR EQUIVALENT TO STRAIN-RELIEVE WIRES.

◯ = NOTE

▢ = ITEM

17.00

P1

P2

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO 0577	4/5/91	C.M.H.
B	ECO 4205	10/27/95	R.E.C.
B	ECO 5160 (NEW PART NUMBER REV)		
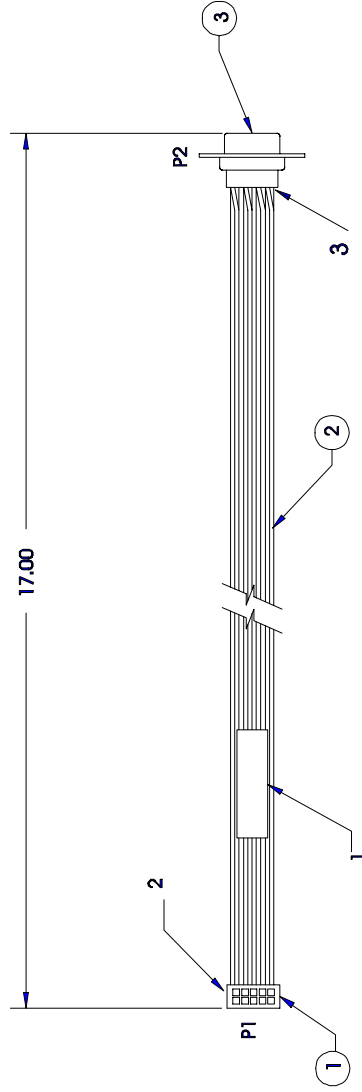
WIRE LIST

P1	P2
1	1
2	6
3	2
4	7
5	3
6	8
7	13
8	10.5
9	14
10	-

NUM	QTY	DESCRIPTION	MFG PART #
5	10	CONTACTS, FEMALE CRIMP, D-SUB	TEX TECH HD-C22S
4	A/R	WIRE, 28 AWG, STRANDED	SOLID ELECTRIC HD-EF-S15
3	1	FEMALE DB-15 - HIGH DENSITY	TEX TECH HDF-15 S7
2	1	RIBBON CABLE, 10 COND	3M 3365/10, BELDEN 9L28010 / SPECTRA STRIP 843-191-2801-010
1	1	FEMALE IDC CONNECTOR, 10 POS	BERG 71G02-310 / BURNDY FRB10BC-8P / SPECTRA STRIP 852-812-1022-134

AMPRO SINGLE BOARD SYSTEMS

ASSY, CABLE, DB15S VIDEO

DWG. NO.	0800595	REV. B
ACAD FILE: 0800595B	SHEET 1 OF 1	

| SIZE C | FSCM NO. | SCALE 1X |

APPROVALS

		DATE
DRAWN	IEC	4/6/90
CHECKED	M.B.	4/3/91
ENGR APPV.	C.M.H.	4/5/91

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS   DECIMALS   ANGLES
± /   .XX ± .02
            .XXX ± .010

CONTRACT NO.

MATERIAL

FINISH

DO NOT SCALE DRAWING

B-4

NOTES - UNLESS OTHERWISE SPECIFIED:

1. MARK CABLE WITH PART NUMBER AND CURRENT REVISION LEVEL.

2. ALL WIRES TO BE SURFACE IMPRINTED WITH UL RATING.

3. ALL SOLDER CONNECTIONS TO BE COVERED/PROTECTED WITH SHRINK TUBING (ITEM 5).

4. MARK CABLE WITH NAME "UTILITY."

△ = NOTE
◯ = ITEM

TOP VIEW
(WIRE SIDE)
P1

4.00

2.00

9.00

12.00

15.00

SEE DETAIL B

SEE DETAIL C

SEE DETAIL A

DETAIL C
P2
(WIRE SIDE)

DETAIL B
IS PIN 1 (CATHODE, LED+)
FLAT SIDE

DETAIL A
SHRINK TUBING
C ND NC

REVISIONS
REV | DESCRIPTION | DATE | APPROVED

APPLICATION
NEXT ASSY | USED ON

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX ± .01 - 0.00
.XXX ±

MATERIAL
FINISH

DO NOT SCALE DRAWING

DRAWN Ross Cox 5/17/95
CHECKED Casey Towers 5/31/95
APPROVALS DATE

AMD COMPUTERS INCORPORATED

ASSY, CABLE,
486i UTILITY

SIZE | FSCM NO. | DWG. NO.
D | | 0800805 | REV A

SCALE NONE | SHEET 1 OF 2

NOTES – UNLESS OTHERWISE SPECIFIED:

PARTS LIST

ITEM	VENDOR/PART NUMBER	QTY	DESCRIPTION
1 (P1)	AMP 102387-3 / MOLEX 22-55-3161	1	CONN, HOUSING, 10POS
2		10	TIE WRAP
3		1	LED, GREEN, T1 3/4
4	EATON PS1-11Q	1	PUSH BUTTON, SPST
	NKK MB2411E1W01-FA	1	NUT
	AMPRO 020202	1	LOCKWASHER
5		A/R	SHRINK TUBING
6	MOUSER 16DN100	1	JACK, DIN 5 PIN 180 DEG.
7	MOUSER 25SP016	1	SPEAKER, 15", 8 OHM, 1W
8	AMPRO 017001 / AMP 1-87756-6 / MOLEX 16-02-0069	8	TERMINAL, FEMALE CRIMP
9		A/R	WIRE 26AWG UL1061 BRN
10		A/R	WIRE 26AWG UL1061 RED
11		A/R	WIRE 26AWG UL1061 ORG
12		A/R	WIRE 26AWG UL1061 YEL
15		A/R	WIRE 26AWG UL1061 WHI/BRN
16		A/R	WIRE 26AWG UL1061 WHI/RED
18		A/R	WIRE 26AWG UL1061 WHI/YEL
19		A/R	WIRE 26AWG UL1061 WHI/GRN
20		A/R	WIRE 26AWG UL1061 GRN
21	BERG 65039-033	1	CONN, HOUSING, 4 POS, S/R
22	BERG 48116-000	3	TERMINAL, WIRE, CRIMP
23	MOLEX 50-57-9004	A/R	WIRE 26AWG UL1061 BLK
24	MOLEX 16-02-0109	A/R	WIRE 26AWG UL1061 VIO

WIRING LIST

ITEM	COLOR	LENGTH	FROM	TO
9	BRN	A/R	P1-2	GND SPEAKER
10	RED	A/R	P1-7	SPEAKER+
11	ORG	A/R	P1-8	SWITCH-C
12	YEL	A/R	P1-9	SWITCH-NO
11	ORG	A/R	P1-4	LED-
15	WHI/BRN	A/R	P1-12	P2-1
16	WHI/RED	A/R	P1-11	P2-2
18	WHI/YEL	A/R	P1-13	P2-4
19	WHI/GRN	A/R	P1-14	P2-5
20	GRN	A/R	P1-5	LED+
23	BLK	A/R	P1-16	P3-4
24	VIO	A/R	P1-15	P3-1

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS / DECIMALS .XX ± / .XXX ± / ANGLES ±

MATERIAL
FINISH

	DATE
DRAWN	
CHECKED	
ENGR APPV.	
REL	

APPROVALS

APPLICATION — NEXT ASSY / USED ON

DO NOT SCALE DRAWING

MPC COMPUTERS, INCORPORATED

ASSY, CABLE, LB/486i UTILITY

SIZE D / FSCM NO. / DWG. NO. 0800805 / REV A

SCALE / ACAD FILE: / SHEET 2 OF 2

NOTES: UNLESS OTHERWISE SPECIFIED .

1. CABLE TO BE MARKED WITH CURRENT PART NUMBER AND REVISION.
2. DIMENSION TOLERANCE IS ± 0.25".

△ = NOTE

◯ = ITEM

PIN 1

P1

RED STRIPE

P2

PIN 1

18.0
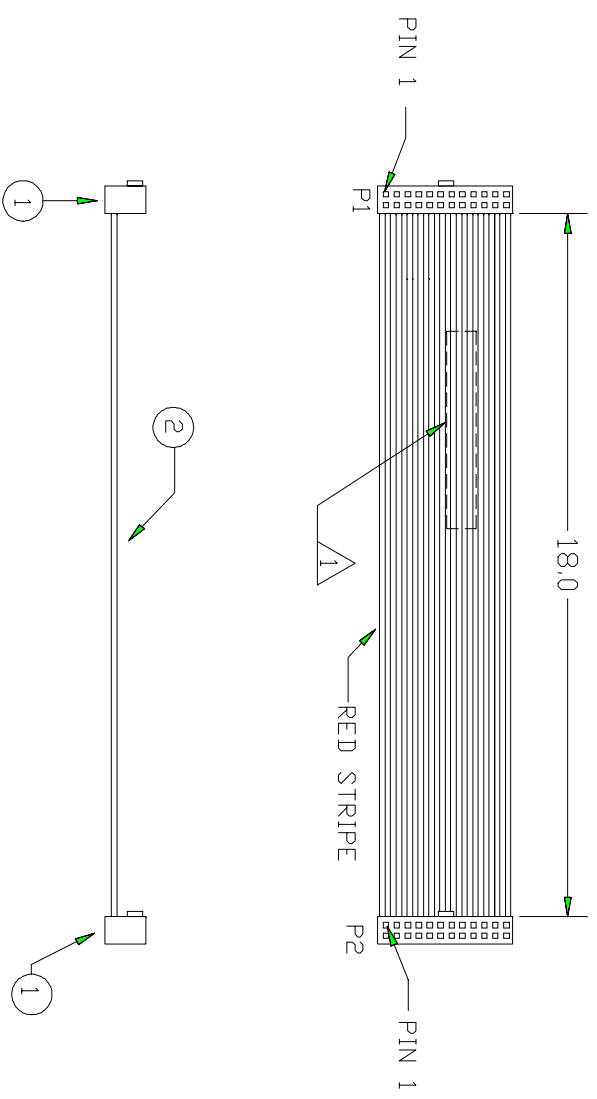
ITEM	QTY	DESCRIPTION	MFGR PN
2	A/R	CABLE,28AWG,24 COND	BELDEN 9L28024 (OR EQUIV)
1	2	CONN, 24 POS, IDC	3M 3626-6600 (OR EQUIV)

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
± .XX± ±
.XXX±

MATERIAL

FINISH

DO NOT SCALE DRAWING

APPROVALS | DATE
DRAWN ROSS COX | 4/27/98
CHECKED
ENGR APPROV
REL

NEXT ASSY | USED ON
APPLICATION

AMRO COMPUTERS, INC

CABLE, 24 POS, 18", IDC

SIZE B

DWG NO. 0801221

ACAD FILE 0801221A.DWG

REV A

SCALE | SHEET 1 OF 1

REVISIONS

REV	ECO	DESCRIPTION	DATE	APPROVED

NOTES – UNLESS OTHERWISE SPECIFIED:

1. ARROW REFERENCES CONTACT #1 INDEX ON CONNECTOR HOUSING.
2. DO NOT USE STRAIN RELIEF, THIS END ONLY.
3. ASSEMBLY TO BE STAMPED WITH AMPRO PART NUMBER AND CURRENT REVISION.
4. ASSEMBLY TO BE STAMPED WITH LABEL AS SHOWN.
5. INSTALL ITEM 3 ON P1-25.
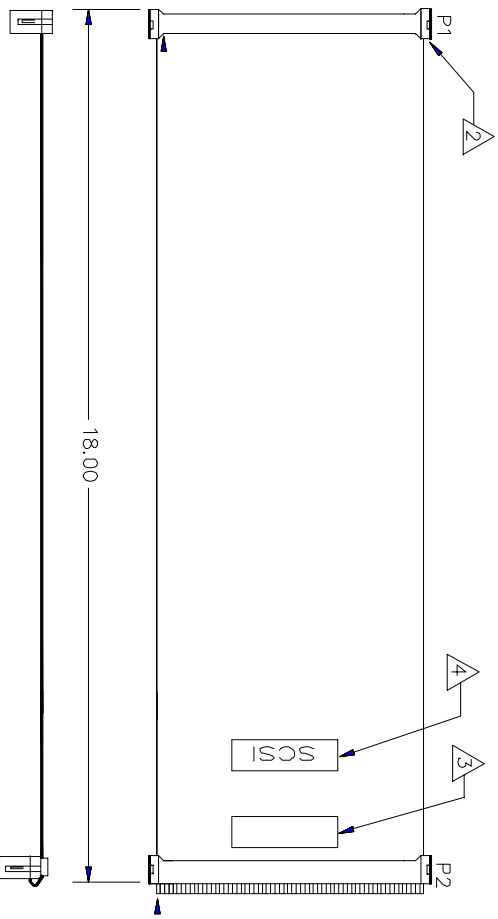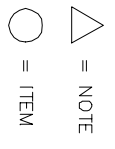
△ = NOTE
○ = ITEM

P1
PIN 1

P1
P2

SCSI

18.00

18.00

REV	DESCRIPTION	DATE	APPROVED
A	ECO 0548		
B	ECO 1012		
C	ECO 1075	12/20/90	L.E.P.

REVISIONS

NUM	QTY	DESCRIPTION		
3.	1	KEY PLUG	SAMTEC PK-01 SPECTRA STRIP #843-191-2801-050	
2.	18.00	CABLE, RIBBON, 50 COND., 28 AWG.	3M #3365/50	
1.	2	CONN, 50 POS, FEM, W/STRAIN RELIEF	T & B 609-5000M 3M 89150-0011	VENDOR ID

APPROVALS

DRAWN	L.D.T.	12/8/90
CHECKED		
ENGR APPV.	L.E.P.	12/20/90
R.L.		1/9/91

ASSY, CABLE, SCSI

SIZE C FSCM NO.
DWG. NO. 0800575
REV A
SCALE NONE ACAD FILE: A60311C SHEET 1 OF 1

DO NOT SCALE DRAWING

Index