F. VIAL

SUPER

Pentium™ System

P5VL-PCI
P54VL-PCI

USER'S MANUAL

Revision 1.21

Preface

About This Manual

This manual is written for system houses, PC technicians and knowledgeable PC end users. It provides information for the installation and use of the SUPER™ P54VL-PCI and SUPER™ P5VL-PCI motherboards, which support the 100/90 MHz (SUPER P54VL-PCI), and 66/60 MHz (SUPER P5VL-PCI), and 33 MHz (in Power-Saving mode when system is idle) Intel® Pentium™ processors.

The Intel Pentium processor will take personal computer systems to a new level of performance. The emergence of the PCI and VESA local bus will also have a significant impact on PCs. Memory and I/O components have also made significant strides in both performance and integration, enhancing the CPU's ability to move data quickly. Putting these all together creates the next generation of PC systems.

Manual Organization

Chapter 1, Introduction, describes the features, specifications and performance of the SUPER P54VL-PCI and SUPER P5VL-PCI system boards, provides detailed information about the chipset, cache memory, main memory system, and offers warranty information.

Refer to Chapter 2, Installation, for a list of the equipment needed for a system based on Pentium CPUs. This chapter provides you with the instructions for handling static-sensitive devices, checking and/or configuring the jumpers for manufacturing and selecting cache size. Read this chapter when you want to install or remove SIMM memory modules, cache memory, and to mount the system board in the chassis. Also refer to this chapter to connect the floppy and hard disk drives, as well as the cables for the power supply, reset cable, Keylock/Power LED, speaker, external battery, and keyboard.

Chapter 3, AMI BIOS, provides you with the setup requirements of the AMI BIOS, including instructions to change the standard setup, advanced setup, chipset setup, power management setup, and the password. AMI BIOS beep codes are listed in Appendix C. AMI BIOS error messages are listed in Appendixes D, E, and F.

If you encounter any problem, please see Chapter 4, Troubleshooting, which describes troubleshooting procedures for video, memory, and the setup configuration stored in memory. Instructions are also included on contacting a technical assistance support representative and returning merchandise for service.

Manual Conventions

This manual refers to pressing specific keys on the keyboard together using plus signs (+) between each key label. For example, <Ctrl>+<Alt>+<Esc> means press the Control, ALT, and Escape keys down together to achieve the desired result.

Keyboard keys listed without plus signs between the key labels should be pressed down sequentially. For example, <Esc> <F10> means to press the Escape key, release it, and then press the F10 key.

Special Symbols and Notations

The following is a list of the special symbols and notations used in this manual.

Symbol / Notation	Description
- (dash)	Used preceding a capitalized mnemonic or signal name to indicate an active low signal. Example: -DACK1
h	Used after a number to indicate that the number is a hexadecimal notation. Example: 1Fh

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Chapter 1
Introduction

1-1 Overview

SUPER™ P54VL-PCI and SUPER™ P5VL-PCI motherboards are high performance, function-enhanced computer system boards based on Intel® Pentium™ processors with Power-Saving (green) functions. Intel's new Pentium processors combine the performance traditionally associated with minicomputers and workstations with the flexibility and compatibility that characterize the personal computer platform. The Pentium processor is Intel's top-of-the-line generation of power for high-end server and desktop computers. The Pentium processor is the enabling technology for today's high-end and tomorrow's emerging applications. The Pentium processor is fully compatible with the entire range of Intel 486™ and Intel 386™ microprocessors.

Peripheral Component Interconnect (PCI) provides industry-leading performance and compatibility. The 32-bit, 33 MHz pathway to the CPU offers performance unmatched by other bus architectures. The PCI standard is clearly defined to ensure complete compatibility. A PCI add-on card available today will work in any PC-compliant system in the future — a competitive advantage that other local bus technologies can't offer.

The PCI local bus standard also provides a roadmap to the future. With provisions for 64-bit data paths and 3.3-volt CPUs, you can feel comfortable basing your solution on the PCI local bus. In addition to the security of a true standard, PCI add-on cards feature auto-configurability for easy integration. The user-friendly BIOS automatically allocates system resources for add-on cards and configures hard disk, memory, and other peripherals. No more hassles with settings, jumpers, or switches. Just plug in the card and go.

The motherboard's four 32-bit slots with industry standard PCI and two 32-bit slots with VESA® Bus Mastering and Buffer-enhanced design have a very high performance capability that provides an ideal system board solution for a wide range of demanding applications; such as networking multiuser environments, computer-aided design (CAD), computer-aided manufacturing (CAM), computer-aided engineering (CAE), database management, desktop publishing, image processing, and artificial intelligence. The motherboard's additional five ISA slots provide standard 16-bit compatibility for AT-type add-on card expansion.

These highly integrated system boards achieve the highest reliability and yet are small enough for all of its features to be supported in a 'Baby-AT' size. These features include: a Pentium central processing unit (CPU) with built-in 16 KB internal cache memory, 128/256/512 KB secondary cache memory, up to 128 MB of on-board memory, five 16-bit AT slots, four 32-bit PCI slots, two VESA Bus Master and Buffer-enhanced VL-Bus™ slots, and a built-in enhanced floating-point unit (FPU).

The motherboards support 'write-back' cache control for an Intel Pentium processor, with 'page' and 2-way 'page-interleave' memory control. The write-back technique removes most of the DRAM write penalty with 60ns (for 100 and 66 MHz) or 70ns (for 90 and 60 MHz) DRAM. When page-interleave mode is enabled, the performance of 2-way page-interleave is slightly higher than page mode interleave with one bank of memory.

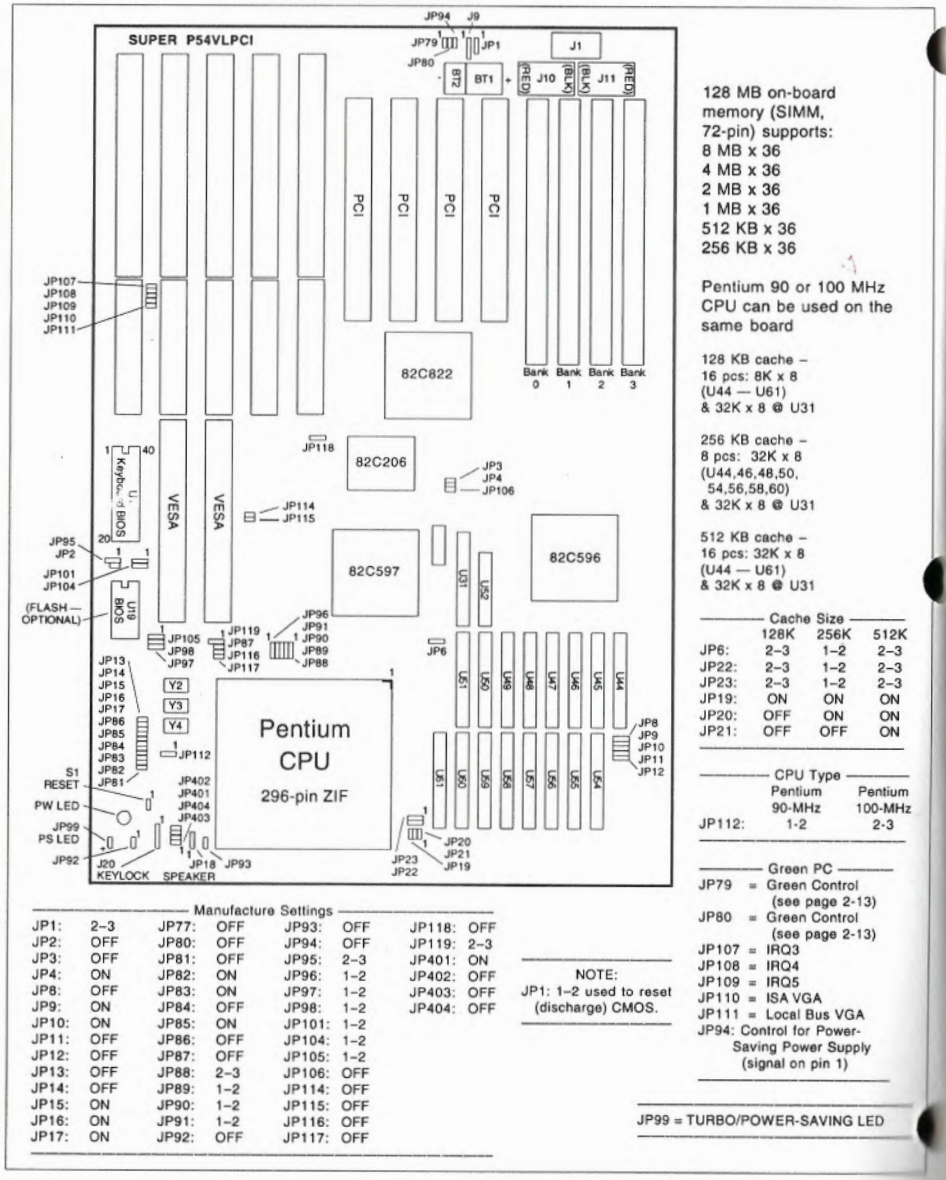
You can achieve both turbo and low speed operation using the system's software/BIOS keyboard function. Two non-cacheable regions are provided by the system. The system and video ROM BIOS can also be shadowed or cached to enhance performance.

For OS/2® optimization, the system supports Fast Reset. Two Fast Resets are provided: 1) Immediate Reset; and 2) 'Reset after HLT' which is used by some programs, after they issue the Reset command to the keyboard controller, to "steal" some time for their own use while waiting for the controller's slow response, and before the program's last HLT instruction arrives. This feature improves performance while maintaining compatibility.

The Pentium processor implements several enhancements to increase performance. The two instruction pipelines and the floating-point unit on the Pentium processor are capable of independent operation. Each pipeline issues frequently used instructions in a single clock. Together, the dual pipes can issue two integer instructions in one clock, or one floating-point instruction (under certain circumstances, two floating-point instructions) in one clock.

The Pentium processor includes separate code and data caches integrated on-chip to meet its performance goals. Each cache is 8 Kbytes in size with a 32-byte line size, and is 2-way set associative. The Pentium processor has increased the data bus to 64 bits to improve the data transfer rate. Burst read and burst write-back cycles are supported by the Pentium processor. In addition, bus cycle pipelining has been added to allow two bus cycles to be in progress simultaneously.

Figures 1-1 and 1-2 show the layout of the SUPER P54VL-PCI and SUPER P5VL-PCI motherboards. The architecture for these boards is illustrated in Figure 1-3.



128 MB on-board memory (SIMM, 72-pin) supports:
8 MB x 36
4 MB x 36
2 MB x 36
1 MB x 36
512 KB x 36
256 KB x 36

Pentium 90 or 100 MHz CPU can be used on the same board

128 KB cache –
16 pcs: 8K x 8
(U44 — U61)
& 32K x 8 @ U31

256 KB cache –
8 pcs: 32K x 8
(U44,46,48,50,
54,56,58,60)
& 32K x 8 @ U31

512 KB cache –
16 pcs: 32K x 8
(U44 — U61)
& 32K x 8 @ U31

Cache Size	128K	256K	512K
JP6:	2–3	1–2	2–3
JP22:	2–3	1–2	2–3
JP23:	2–3	1–2	2–3
JP19:	ON	ON	ON
JP20:	OFF	ON	ON
JP21:	OFF	OFF	ON

CPU Type	Pentium 90-MHz	Pentium 100-MHz
JP112:	1-2	2-3

Green PC
JP79 = Green Control (see page 2-13)
JP80 = Green Control (see page 2-13)
JP107 = IRQ3
JP108 = IRQ4
JP109 = IRQ5
JP110 = ISA VGA
JP111 = Local Bus VGA
JP94: Control for Power-Saving Power Supply (signal on pin 1)

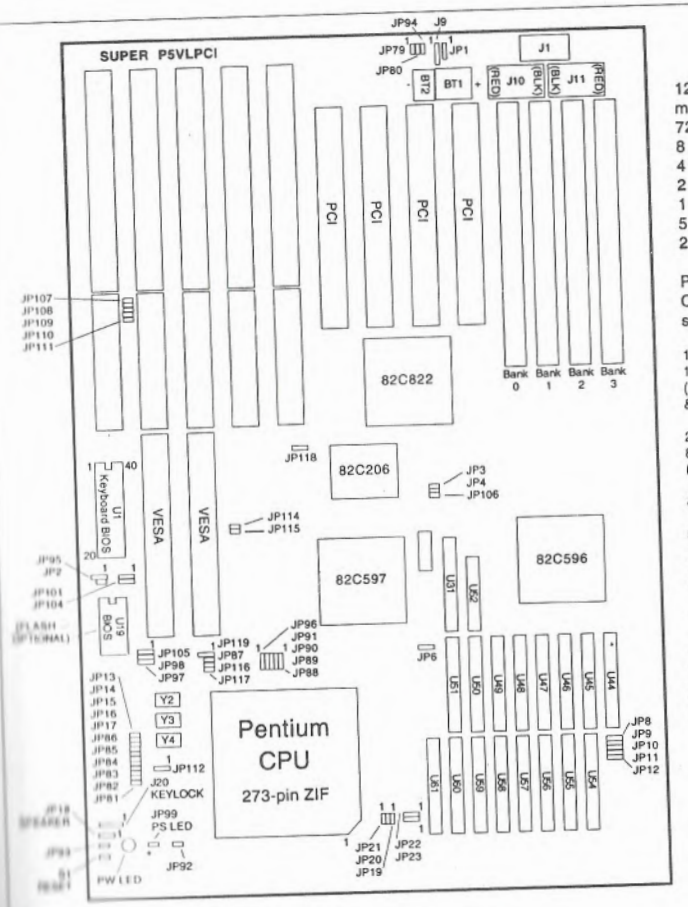
JP99 = TURBO/POWER-SAVING LED

Manufacture Settings

JP1:	2–3	JP77:	OFF	JP93:	OFF	JP118:	OFF
JP2:	OFF	JP80:	OFF	JP94:	OFF	JP119:	2–3
JP3:	OFF	JP81:	OFF	JP95:	2–3	JP401:	ON
JP4:	ON	JP82:	ON	JP96:	1–2	JP402:	OFF
JP8:	OFF	JP83:	ON	JP97:	1–2	JP403:	OFF
JP9:	ON	JP84:	OFF	JP98:	1–2	JP404:	OFF
JP10:	ON	JP85:	ON	JP101:	1–2		
JP11:	OFF	JP86:	OFF	JP104:	1–2		
JP12:	OFF	JP87:	OFF	JP105:	1–2		
JP13:	OFF	JP88:	2–3	JP106:	OFF		
JP14:	OFF	JP89:	1–2	JP114:	OFF		
JP15:	ON	JP90:	1–2	JP115:	OFF		
JP16:	ON	JP91:	1–2	JP116:	OFF		
JP17:	ON	JP92:	OFF	JP117:	OFF		

NOTE:
JP1: 1–2 used to reset (discharge) CMOS.

Figure 1-1. SUPER P54VL-PCI Motherboard Layout



128 MB on-board memory (SIMM, 72-pin) supports:
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4 MB x 36
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Pentium 60 or 66 MHz CPU can be used on the same board

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JP21:	OFF	OFF	ON

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Manufacture Settings

JP1:	2–3	JP77:	OFF	JP93:	OFF	JP118:	OFF
JP2:	OFF	JP80:	OFF	JP94:	OFF	JP119:	2–3
JP3:	OFF	JP81:	OFF	JP95:	2–3		
JP4:	ON	JP82:	ON	JP96:	2–3		
JP8:	OFF	JP83:	ON	JP97:	1–2		
JP9:	ON	JP84:	OFF	JP98:	1–2		
JP10:	ON	JP85:	ON	JP101:	1–2		
JP11:	OFF	JP86:	OFF	JP104:	1–2		
JP12:	OFF	JP87:	OFF	JP105:	1–2		
JP13:	OFF	JP88:	2–3	JP106:	OFF		
JP14:	OFF	JP89:	1–2	JP114:	OFF		
JP15:	ON	JP90:	1–2	JP115:	OFF		
JP16:	ON	JP91:	1–2	JP116:	OFF		
JP17:	ON	JP92:	OFF	JP117:	OFF		

NOTE:
JP1: 1–2 used to reset (discharge) CMOS.

Figure 1-2. SUPER P5VL-PCI Motherboard Layout

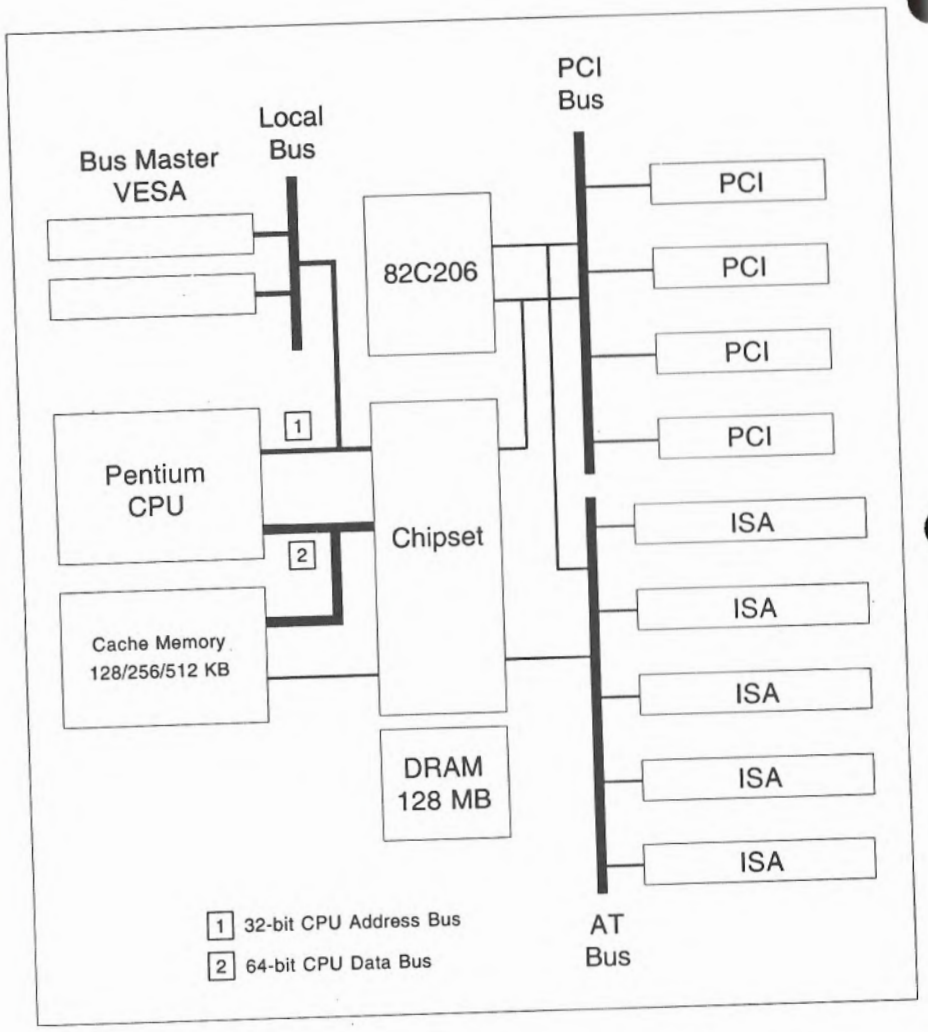


Figure 1-3. P5/54VL-PCI System Board Architecture

Features

The following list covers the general features of the SUPER P54VL-PCI and SUPER P5VL-PCI motherboards.

CPU

— SUPER P54VL-PCI —

- Intel 3.3-volt Pentium CPU with 64-bit data bus and 32-bit address bus
- 296-pin ZIF (Zero Insertion Force) socket 5

— SUPER P5VL-PCI —

- Intel 5-volt Pentium CPU with 64-bit data bus and 32-bit address bus
- 273-pin ZIF (Zero Insertion Force) socket 4

Math Coprocessor

- Enhanced on-chip, floating-point unit that incorporates sophisticated seven-stage pipelining and hardwired functions

Speed

— SUPER P54VL-PCI —

- Designed to work at 100/90 MHz (and low speed in Power-Saving mode when system is idle) on a Pentium-based computer

— SUPER P5VL-PCI —

- Designed to work at 66/60 MHz (and 33 MHz in Power-Saving mode when system is idle) on a Pentium-based computer

Cache

- 16 KB on-chip, 2-way set associative internal cache
- 64-bit wide data bus with write-back/write-through external cache that supports either 128 KB (8 KB x 8), 256 KB (32 KB x 8), or 512 KB (32 KB x 8) secondary cache

Memory

- 64-bit wide data bus with up to 128 MB of memory on the motherboard
- Page and 2-way Page-Interleave modes support 256 KB x 36, 512 KB x 36, 1 MB x 36, 2 MB x 36, 4 MB x 36, and 8 MB x 36 (60ns or 70ns, 72-pin) SIMMs for up to 128 MB of on-board memory

Multiple Power Savings

- *Green 1:* Smart and user-programmable System Auto Detect or Hardware switch Power-Saving function
- *Green 2:* When system is idle, a lower CPU clock boosts CPU cooling, thus extending system life cycle (Turbo Light will be off)
- *Green 3:* Power supply Power-Saving OUTLET function supports CRT and printer Power Saving

Turbo/Non-turbo Function

- BIOS turbo speed selectable by the keyboard (<Ctrl>+<Alt>+<Shift> and <+> or <->).

Bus

- Five 16-bit AT ISA slots
- Four PCI slots and two Bus Master, Buffer-enhanced, VESA VL-Bus slots; ideal for two Fast SCSI local bus cards and four Fast Network local bus cards in a file server system

BIOS

- AMI® BIOS with built-in setup
- Flash BIOS (optional) for better upgradeability in the future
- Fast Reset and Gate A20 to optimize OS/2

Shadowed/Cached BIOS

- Shadowed system/video BIOS
- Cached system/video BIOS

Software Compatibility

- 100% IBM® PC/AT® compatible
- DOS, OS/2, UNIX®, XENIX®, Novell®, Windows™, and Windows NT™

Testing

- 50°C, 48-hour, dynamic burn-in with system-level testing

Manufacturing and Support

- Made in U.S.A.
- Design-level Technical Support and Service in U.S.A.

1-2 Power Supply

As with all computer products, a stable power source is necessary for proper and reliable operation. It is even more important for high CPU clock rates like 100 and 90 MHz for the SUPER P54VL-PCI, and 66 and 60 MHz for the SUPER P5VL-PCI system boards.

Although most power supplies generally meet the specifications required by the CPU, some power supplies are not adequate. To obtain the highest system reliability, be certain that your power supply provides +5 VDC with a voltage range between +4.95 VDC (minimum) and +5.25 VDC (maximum).

It is highly recommended that you use a high quality power supply. Additionally, in areas where noisy power transmission is present, you may choose to install a line filter to separate noise from the computer. You can also install a power surge protector to help avoid problems caused by power surges.

1-3 Chipset Overview

The OPTi® chipset is comprised of four chips; the 82C597 SYSC controller, the 82C596 ATC controller, the 82C822 PCI bridge, and the 82C206 Integrated Peripherals Controller (IPC). The SYSC provides the control functions for the host CPU interface, the local bus interface, the L2 cache, and full 64-bit DRAM control. It also controls the data flow between the CPU bus, the 64-bit DRAM bus, the 32-bit local bus, and the 16/8-bit ISA bus. The ATC integrates the AT bus interface and the CD to MD bus buffers. The 82C206 IPC incorporates two DMA controllers, two interrupt controllers, one timer/counter, and the real-time clock offering single chip integration of all the peripherals attached to the PC/AT peripheral bus.

CPU Burst-Mode Control

The chipset fully supports the 64-bit wide data path for the Pentium burst-read and burst-write cycles. The 82C597 cache and 82C206 DRAM controllers insure that data is bursted into the CPU whenever the Pentium requests a burst line fill. The 82C597 contains separate burst counters to support DRAM and external cache burst cycles. The DRAM burst counter performs the cache read-miss line fill (DRAM to external cache) and the cache burst counter supports the Pentium burst line fill (external cache to the Pentium CPU). The burst order of the cache burst counter exactly matches the quad-word address sequencing expected by the Pentium CPU. The DRAM burst counter is used for cache read-miss cycles and dirty line fill write operations.

Cache Subsystem

The integrated cache controller, which uses a direct-mapped, bank-interleaved scheme, dramatically boosts the overall performance of the local memory subsystem by caching writes as well as reads (write-back mode). Cache memory can be configured as one or two banks, and sizes of 128 KB, 256 KB and 512 KB are supported. Provisions for two programmable, non-cacheable regions are provided. The cache controller operates in non-pipeline or pipeline mode with a fixed 32-byte line size (optimized to match a Pentium burst line fill) in order to simplify the motherboard design without increasing cost or degrading system performance. For Pentium systems, the secondary cache operates independently and in addition to the CPU's internal cache.

The 82C597 cache controller uses external TAG RAMs. The 82C597 has a built-in TAG comparator which improves system performance while reducing component count on the system board.

The cache controller features:

- 64-bit data bus with 32-byte CPU burst support
- 128 KB, 256 KB, 512 KB cache size
- Direct Mapped Adaptive write-back operation

- Optional write-through operation
- 32-byte secondary cache line size
- External TAG RAM, internal comparator
- 8-bit TAG with 1 dirty bit optional for write-back cache
- Uses standard SRAMs
- Two banks of 64-bit data RAMs supported for optimum cache performance

Cache Operation

The *cache hit/miss status* is generated by comparing the high-order address bits (for the memory cycle in progress) with the stored TAG bits from previous cache entries. When a match is detected, and the location is cacheable, a cache hit cycle takes place. If the comparator does not detect a match, or a non-cacheable location is accessed (based on the internal non-cacheable region registers), the current cycle is a cache miss. The TAG is invalidated automatically during memory reads when the cache is disabled; each memory read will write into the corresponding TAG location of a non-cacheable address (such as A0000 or B0000 of the video memory area).

A *cache hit/miss decision* is always made at the end of the first T2 for a non-pipeline cycle, and at the end of the first T2P for a pipeline cycle. Hence, the SRAM/DRAM read/write cycle will begin after the first T2 or T2P. The cacheable decision comes from the DRAM bank decodes, and the non-cache bits. There are bits to determine whether the shadow area is cached and has programmable non-cached regions. If the access is not within the DRAM area, it is non-cacheable.

The *'dirty bit'* is a mechanism for monitoring coherency between the cache system and DRAM. Each TAG entry has a corresponding dirty bit to indicate whether the data in the represented cache line has been modified since it was loaded from system memory. This allows the 82C597 to determine whether the data in memory is 'stale' and needs to be updated before a new memory location is allowed to overwrite the currently indexed cache entry.

Linefill cycle occurs for a cache read-miss cycle. It is a data read of the new address from the DRAM and a write to the cache. The TAG will also be updated with the new address.

Castout cycle occurs for a cache read-miss cycle, but only if the cache line that is being replaced is 'dirty.' So in this cycle the 'dirty' cache line is read from the cache and written to the DRAM. The address for this cycle is provided by the TAG RAMs.

Write-back cycle consists of doing a castout cycle and then a linefill cycle. The write-back cycle causes an entire cache line (32 bytes) to be written back to memory, followed by a line burst from the new memory location into the cache and to the CPU simultaneously. Normally, the performance advantage of completing fast writes to the cache outweigh the write-back, read-miss penalties which are incurred while operating the write-back scheme.

Cacheability and Write Protection

Only system DRAM is cacheable in both the primary or secondary cache, and these areas cannot be write protected. The shadow RAM areas will not be cached but can be write protected. Since the shadow RAM may get into the primary cache, which is a write-back cache, the write-protected area may be modified without updating the external memory.

SRAM Requirements

The 82C597 cache controller uses standard off-the-shelf SRAMs for both TAG and data.

The data RAMs are quad-word interleaved for the two-bank configurations, which requires 64-bit wide SRAMs. If a single bank of data RAMs are to be used, the cache controller will increase the burst wait state. The table below shows the data and TAG SRAM configurations.

Table 1-1. Data and TAG SRAM Configurations

	Data SRAMs		TAG SRAMs				
Cache Size	**Qty**	**Type**	**Qty**	**TAG address field**	**Qty**	**TAG dirty bit field**	**Cacheability**
128 Kbytes	16	8K x 8	1	32K x 8	1	16K x 1	32 MB
256 Kbytes	8	32K x 8	1	32K x 8	1	16K x 1	64 MB
512 Kbytes	16	32K x 8	1	32K x 8	1	16K x 1	128 MB

The DRAM Controller

This OPTi chipset uses *Page mode* technique for faster data access from the DRAMs. *Hidden refresh* is used to increase the CPU bandwidth by not having to put the CPU on hold every 15µs to refresh the DRAMs. The DRAM can be refreshed in the background while the CPU is accessing the internal cache and external cache. Page mode is always used in this chipset for CPU accesses both for bursts, and between bursts. Page mode is performed by keeping RAS active while reading or writing multiple words within a DRAM page, and by changing only the column address and toggling CAS with the new column address.

The DRAM controller is optimized for a cache-based system. The timing constraints to achieve optimum performance at 66 MHz are met without making the system design overly critical. All timing variations required at the different system speeds for a non-cache or a cache-based system are covered with five different timing modes that vary the wait states.

DRAM Block Programming

Each block has the following programming:

- *DRAM depth:* 256K, 1M, 4M
- *Single or Double Bank*
- *Starting Address:* A20–26. Must start on a block size boundary (i.e., a 256K deep single bank must start on a 1M boundary, a 256K deep double bank must start on a 2M boundary).

Because the blocks must be on a block size boundary, the largest blocks must be placed at the bottom of memory to avoid a hole in the memory map. The following table lists the addressing restrictions.

Table 1-2. DRAM Block Staffing Address

DRAM SIMM's Depth	Banks per Block	Size of Block	Address Bits Programmed	Placement Boundary Size
256K	Single	1M	A20–26	1M
256K	Double	2M	A21–26	2M
1M	Single	4M	A22–26	4M
1M	Double	8M	A23–26	8M
4M	Single	16M	A24–26	16M
4M	Double	32M	A25–26	32M

Shadow RAM

Since accesses to local DRAM are much faster than those to EPROM, the 82C597 provides shadow RAM capability. With this feature, code from slow devices like ROM and EPROM memories can be copied to local DRAM to speed up memory accesses. Accesses to the specified EPROM space are redirected to the corresponding DRAM location. Shadow RAM addresses range from C0000h to FFFFFh. 16K granularity is provided for the address range C0000h to EFFFFh, while the 64K range from F0000h to FFFFFh (location of system BIOS) can be shadowed as an entire segment.

The shadow RAM control is setup in the configuration registers. First, the ROM contents must be copied into the shadow RAM area. Next, the shadow RAM enable bit is set in the configuration register. For the system BIOS area, once the bit is set, the RAM area becomes read only. For the video and adapter BIOS area, the user can select read only or read/write by setting the write protect bit in index register 72h accordingly. Video BIOS at the C0000h–C8000h area can be shadowed and cached if bit 0 of register 74h is set to 1. System BIOS at F0000h–FFFFFh can also be shadowed and cached if bit 1 of register 7C is set to 1. If the adapter BIOS is not shadowed, the 82C597 can remap 256K of memory (A0000h–BFFFFh and D0000h–EFFFFh) to the top of system memory.

System ROM BIOS Cycles

The 82C597 supports both 8- and 16-bit EPROM cycles. If the system BIOS is 16 bits wide, ROMCS# should be connected to M16# through an open-collector gate indicating to the 82C597 that a 16-bit EPROM is responding. The system BIOS resides on the XD bus. The XD to SD data buffer is normally enabled (SDEN# active) except during I/O read cycles at addresses below 100h (byte-wide I/O), INTA cycles, and 8-bit ROM BIOS cycles.

ROMCS# is generated for both the E0000h–EFFFFh and F0000h–FFFFFh segments. If a combined video/system ROM BIOS is desired, these two segments should be used.

Fast Gate A20 and Reset Emulation

The 82C597 will intercept commands to ports 60h and 64h so that it can emulate the keyboard controller, allowing the generation of the fast Gate A20 and fast INIT signals. The decode sequence is software transparent and requires no BIOS modifications to function. The fast Gate A20 generation sequence involves writing "D1h" to port 64h, then writing data "02h" to port 60h. The fast CPU 'warm reset' function is

generated when a port 64h write cycle with data "FEh" is decoded. A write to port 64h with data "D0h" will enable the status of Gate A20 (bit 1 of port 60h) and the warm reset (bit 0 of port 60h) to be readable.

Special Cycles

The Pentium processor provides special bus cycles to indicate that certain instructions have been executed, or certain conditions have occurred internally. Special cycles such as SHUTDOWN and HALT cycles are covered by dedicated handling logic in the 82C597.

DRAM Bank Configurations

The DRAM decoding section was designed to be very versatile and to be able to use the 36-bit single or double bank type of SIMMs. Table 2-10 lists the various DRAM bank configurations.

1-4 Warranty, Technical Support, and Service

The manufacturer will repair or exchange any unit or parts free of charge due to manufacturing defects for one year (12 months) from the original invoice date of purchase.

Parts

Defective parts will be exchanged or repaired for one year (12 months) after the manufacturer's original invoice purchase date.

BIOS

The manufacturer will exchange the BIOS free of charge due to existing incompatibility issues for one year (12 months) after the manufacturer's original invoice purchase date.

Labor

Mail-in or carry-in service is available for one year (12 months) after the manufacturer's original invoice purchase date.

Returns

If you must return products for any reason, refer to Chapter 4 in this manual, "Returning Merchandise for Service."

Chapter 2
Installation

2-1 SUPER P54VL-PCI and SUPER P5VL-PCI System Components

The equipment listed in this section is required to build a high performance system based on the SUPER™ P54VL-PCI and SUPER™ P5VL-PCI motherboard. The minimum configuration for a standard system is listed below. To create the full enhanced configuration, add the enhanced system configuration equipment listed on the next page to the equipment listed below.

Standard System Configuration

- 230 watt (minimum) power supply
- Chassis (baby-AT, AT, portable/lunch box, or tower) with a speaker connected to a 4-pin connector, a push button switch with 2-pin connector for the reset function, and a keylock connected to a 5-pin connector (a 2-pin push button for hardware Turbo switch and Power-Saving is optional)
- SUPER P54VL-PCI or SUPER P5VL-PCI system board
- AT-compatible keyboard (84 or 101 style keyboard)
- 8 MB or 16 MB of system memory
- One 1.2 MB 5.25" and/or one 1.44 MB 3.5" floppy disk drive
- PCI/VESA VL-Bus IDE card with super I/O
- Use PCI/VESA VL-Bus Fast SCSI card and hard disk drive instead of PCI/VESA VL-Bus IDE card and hard disk drive
- PCI/VESA VL-Bus VGA card

Enhanced System Configuration

- Tape drive (for backups)
- Sound card
- Modem/FAX card
- CD-ROM drive
- Add SIMM modules for 32 MB, 64 MB, or 128 MB of system memory
- Use one or two PCI/VESA VL-Bus Fast SCSI cards
- Use up to four PCI, and one or two VESA VL-Bus Fast Network cards (for faster networking)

2-2 Static-Sensitive Devices

Static-sensitive electric discharge can damage electronic components. To prevent damage to your system board, it is important to handle it very carefully. The following measures are generally sufficient to protect your equipment from static discharge.

Precautions

- Use a grounded wrist strap designed for static discharge.
- Touch a grounded metal object before you remove the board from the anti-static bag.
- Handle the board by its edges only; do not touch its components, peripheral chips, memory modules, or gold contacts.
- When handling chips or modules, avoid touching their pins.
- Put the system board and peripherals back into their anti-static bags when not in use.
- Be sure your computer system's chassis allows excellent conductive contacts between its power supply, case, mounting fasteners, and the system board for grounding purposes.

Unpacking

The system board is shipped in anti-static packaging to avoid static damage. When unpacking the board, be sure the person handling the board is static-protected.

2-3 Configuring System Board Jumpers

Use the following settings to configure your system board. Refer to Figure 1-1 for an illustration of the jumpers.

Manufacturing Settings

Manufacturing jumpers are permanently fixed or preset in place on the system board. You cannot move them. These jumpers are labeled on the system board and are listed below as Manufacture Settings.

Manufacture Settings

JP1: 2–3, default; 1–2, discharge CMOS
JP2: OFF, default
JP3: OFF, default
JP4: ON, default
JP8: OFF, default
JP9: ON, default
JP10: ON, default
JP11: OFF, default
JP12: OFF, default
JP13: OFF, default
JP14: OFF, default
JP15: ON, default
JP16: ON, default
JP17: ON, default

Manufacture Settings (continued)

JP77: OFF, default
JP80: OFF, default
JP81: OFF, default
JP82: ON, default
JP83: ON, default
JP84: OFF, default
JP85: ON, default
JP86: OFF, default
JP87: OFF, default
JP88: 2–3 (P54VL-PCI), default; 1–2 (P5VL-PCI), default
JP89: 1–2 (P54VL-PCI), default; 1–2 (P5VL-PCI), default
JP90: 1–2 (P54VL-PCI), default; 1–2 (P5VL-PCI), default
JP91: 1–2 (P54VL-PCI), default; 1–2 (P5VL-PCI), default
JP92: OFF, default
JP93: OFF, default
JP94: OFF, default
JP95: 2–3, default
JP96: 1–2 (P54VL-PCI), default; 2–3 (P5VL-PCI), default
JP97: 1–2, default
JP98: 1–2, default
JP101: 1–2, default
JP104: 1–2, default
JP105: 1–2, default
JP106: OFF, default
JP114: OFF, default
JP115: OFF, default
JP116: OFF, default
JP117: OFF, default
JP118: OFF, default
JP119: 2–3, default
JP401: ON, default (P54VL-PCI only)
JP402: OFF, default (P54VL-PCI only)
JP403: OFF, default (P54VL-PCI only)
JP404: OFF, default (P54VL-PCI only)

Changing the CPU Speed

The SUPER P54VL-PCI and SUPER P5VL-PCI motherboards support the Intel Pentium 100/90 MHz (SUPER P54VL-PCI) and 66/60 MHz (SUPER P5VL-PCI) CPUs. To change the CPU speed, you must change the jumper shown in the following table.

Table 2-1. CPU Speed Jumper Selection

	Pentium 90/60 MHz	Pentium 100/66 MHz
JP112	1-2	2-3

On-Board Memory

There are no jumpers to configure the on-board memory (Banks 0, 1, 2, and 3). Two banks of memory totaling 2 MB are required for a minimum system configuration. These two banks of memory must contain two 72-pin SIMM modules. Refer to Table 2-10 for DRAM bank configurations.

Cache Size Selection

The SUPER P5/54VL-PCI motherboards support 128 KB (with 8K x 8 static RAM), 256 KB (with 32K x 8 static RAM), or 512 KB (with 32K x 8 static RAM) of secondary cache memory. For each cache size, six jumpers must be set as listed in Table 2-2.

Table 2-2. Cache Size Jumpers and Components

Jumpers / Components	Cache Size		
	128 KB	256 KB	512 KB
JP6	2–3	1–2	2–3
JP22	2–3	1–2	2–3
JP23	2–3	1–2	2–3
JP19	ON	ON	ON
JP20	OFF	ON	ON
JP21	OFF	OFF	ON
U31	32K x 8	32K x 8	32K x 8
Banks	16 chips of 8K x 8 (Banks 0 and 1) U44, 45, 46, 47, 48, 49, 50, 51, 54, 55, 56, 57, 58, 59, 60, 61	8 chips of 32K x 8 (Bank 0) U44, 46, 48, 50, 54, 56, 58, 60	16 chips of 32K x 8 (Banks 0 and 1) U44, 45, 46, 47, 48, 49, 50, 51, 54, 55, 56, 57, 58, 59, 60, 61

Green PC Function

The SUPER P54VL-PCI and SUPER P5VL-PCI motherboards support both manual (hardware switch) control and automatic system-detect, Power-Saving Green PC functions. Power-Saving functions consume less power and extend system life cycle because of less heat.

To manually control Power-Saving, connect the hardware Turbo switch (on most computer cases) to Turbo/Power-Saving switch connector JP92. When the Turbo switch is OFF (Turbo Light is on), the system will run at full speed (100 or 90 MHz for SUPER P54VL-PCI and 66 or 60 MHz for SUPER P5VL-PCI). When the Turbo switch is pushed ON, the system will run at low speed and consume less power—in this case Turbo means slower system speed and Power-Saving. (On traditional systems, the Turbo switch only slows the system speed, but *does not* consume less power.)

The automatic system-detect, Power-Saving function is a more powerful and smarter way to reduce power consumption. Automatic Power-Saving is enabled using the BIOS settings (refer to section 3-9 for more details). Four different automatic Power-Saving modes (device timeout options) can be set in the BIOS.

Device-1 Timeout: System board low speed (JP95)
Device-2 Timeout: Power supply outlet, power-off (JP94)
Device-3 Timeout: Peripheral Power-Saving control (JP79, JP80)
Device-4 Timeout: Reserved

These four options configure the amount of time a specified device can be idle before the system switches to a low power mode (sleep mode). At the end of a selected time period with no system activity, the system goes to low power mode until system activity occurs. Here "system activity" is defined as follows:

a. If jumpers JP107 through JP111 are all open, only keyboard activity is defined as system activity. Pressing any key on the keyboard will return the system from "sleep mode" back to full speed operation.

b. If jumper JP107 is closed, either keyboard activity or IRQ3 activity will return the system from sleep mode. IRQ3 is typically used by the mouse.
c. If jumper JP108 is closed, either keyboard activity or IRQ4 activity will return the system from sleep mode.
d. If jumper JP109 is closed, either keyboard activity or IRQ9 activity will return the system from sleep mode.
e. If jumper JP110 is closed, either keyboard activity or any video screen activity will return the system from sleep mode. Jumper JP110 is only used for ISA bus display cards.
f. If jumper JP111 is closed, either keyboard activity or any video screen activity will return the system from sleep mode. Jumper JP111 is only used for VESA VL-Bus display cards.

NOTE

Only one jumper at a time can be used at jumper block JP107 through JP111.

VESA VL-Bus Clock Optimization

With VESA bus clock frequencies as high as 33 MHz, a few VGA cards may not be compatible with some VESA bus motherboards. SUPER P5/54VL-PCI motherboards provide an optional jumper to adjust the VESA VL-Bus clock timing. This jumper option applies only to VESA slot J18 (the VESA slot next to the keyboard controller). If you use a VGA card, or any other VESA add-on card, that has timing problems in slot J18, try installing a jumper at JP87. Adding this jumper shifts the timing to VESA slot J18 by 1.5 nanoseconds.

2-4 Installing Cache Memory

Data RAM

As mentioned previously, the SUPER P5/54VL-PCI motherboard's write-back cache supports 128 KB, 256 KB, or 512 KB cache memory. Four full banks contain a total of sixteen chips of static RAM (SRAM). For the 128 KB cache, sixteen 8K x 8 SRAM chips are required. For the 256 KB cache, eight 32K x 8 SRAM chips are required. For the 512 KB cache, sixteen 32K x 8 SRAM chips are required. In any case, the SRAM chips are located in motherboard positions U44 through U61. See Table 2-2 for appropriate jumper settings.

TAG RAM

In all configurations of cache memory, you need to insert one chip of 32K x 8 SRAM at U31. See Table 2-2 for appropriate jumper settings.

2-5 Connecting Cables

After you have securely mounted the motherboard to the chassis, you are ready to connect the cables.

Power Supply Connectors

Attach power supply cables P58 (pins 1 through 6) and P59 (pins 7 through 12) to their matching connectors J10 and J11 respectively. Do not force the cables, but make sure they are fully seated. The two black wires on each power cable sit next to each other when correctly installed. See Table 2-3 for pin definitions.

Table 2-3. Power Supply Connector Pin Definitions

Connector Number	Pin Number	Function
J10	1	Power Good (Power on reset, TTL signal)
	2	+5 VDC
	3	+12 VDC
	4	-12 VDC
	5	Ground (Black wire to be connected)
	6	Ground (Black wire to be connected)
J11	7	Ground (Black wire to be connected)
	8	Ground (Black wire to be connected)
	9	-5 VDC
	10	+5 VDC
	11	+5 VDC
	12	+5 VDC

Reset Cable Connector

The reset cable connector S1 has two pins with no polarity. The connector attaches to the hardware Reset switch on the computer case.

Keylock/Power LED Cable Connector

The keylock/power LED cable connector J20 has five pins. See Table 2-4 for pin definitions. (NOTE: pins 1 and 3 are for LED power connection, pins 4 and 5 are for keyboard connection.)

Table 2-4. Keylock/Power LED Pin Definitions

Pin Number	Function	Definition
1	+	Red wire, LED power
2	Key	No connection
3	GND	Black wire
4		Keyboard inhibit
5	GND	Black wire

Speaker Cable Connector

The speaker cable connector JP18 has four pins. See Table 2-5 for pin definitions.

Table 2-5. Speaker Connector Pin Definitions

Pin Number	Function	Definition
1	+	Red wire, speaker data
2	Key	No connection
3	GND	Black wire
4	Vcc	+5 VDC

External Battery Cable Connector

The motherboard has an on-board battery and does not require an external battery. However, if the on-board battery fails, you can use the external battery connector J9 to connect an external battery. The external battery holder typically accommodates four AA-size batteries.

The external battery cable connector J9 has four pins. See Table 2-6 for pin definitions.

Table 2-6. External Battery Connector Pin Definitions

Pin Number	Function	Definition
1	+	Red wire
2	Key	No connection
3	GND	Black wire
4	GND	Black wire

Power-Saving Power Supplies with External Outlet

The motherboard supports a "Power-Saving" power supply with external outlet via control connector JP94. If a Power-Saving power supply is used, you must connect the appropriate control cable from JP94 to the power supply. The BIOS Green PC function then controls the power supply's external outlet by turning off power to peripheral devices after a user-defined timeout period. See Table 2-7 for pin definitions.

Table 2-7. Power-Saving Power Supply Connector Pin Definitions

Pin Number	Function
1	Power-Saving control signal
2	Ground

Power-Saving for Additional Peripherals

The BIOS Green PC function also controls additional peripherals through control connectors JP79 and JP80 by turning off the peripheral device after a user-defined timeout period. See Table 2-8 for pin definitions.

Table 2-8. Power-Saving Peripheral Connectors Pin Definitions

Pin Number	Function
1	Power-Saving control signal
2	Ground

Keyboard Connector

The keyboard connector J1 has five pins. See Table 2-9 for pin definitions.

Table 2-9. Keyboard Connector Pin Definitions

Pin Number	Function
1	Keyboard clock
2	Keyboard data
3	Spare
4	Ground
5	+5 VDC

Power-Saving Mode Light Connector

The Power-Saving Light connector JP99 has two pins. This connector attaches a Turbo Light cable to the front panel LED on the system chassis. When the system is in Normal/High Speed mode, the LED is on. When the system is in Power-Saving mode the LED is off.

2-6 Installing/Removing the SIMM Modules

The SUPER P5/54VL-PCI motherboards can accommodate a maximum of 128 MB (four banks) of on-board memory, using standard 72-pin SIMM memory modules. You can use any 256 KB x 36, 512 KB x 36, 1 MB x 36, 2 MB x 36, 4 MB x 36, or 8 MB x 36 Fast Page Mode SIMM modules. A 90- or 60-MHz system can use either 60ns or 70ns SIMM modules, while a 100- or 66-MHz system must use 60ns SIMM modules. The motherboards support any mixture of two banks of the six types of SIMMs, as long as both SIMM modules within two banks are of the same type. Table 2-10 lists the various DRAM bank configurations.

To optimize memory SIMMs, the motherboards have built-in support for Page and Page-Interleave modes. If Banks 0, 1, 2, and 3 are SIMMs of the same type, they can operate in 2-way Page-Interleave mode. In all other cases, each bank operates in Page mode only. The BIOS automatically configures memory size.

Refer to Figure 2-1 and the instructions below for installing or removing SIMM modules.

CAUTION

Exercise extreme care when installing or removing the SIMM modules to prevent any possible damages.

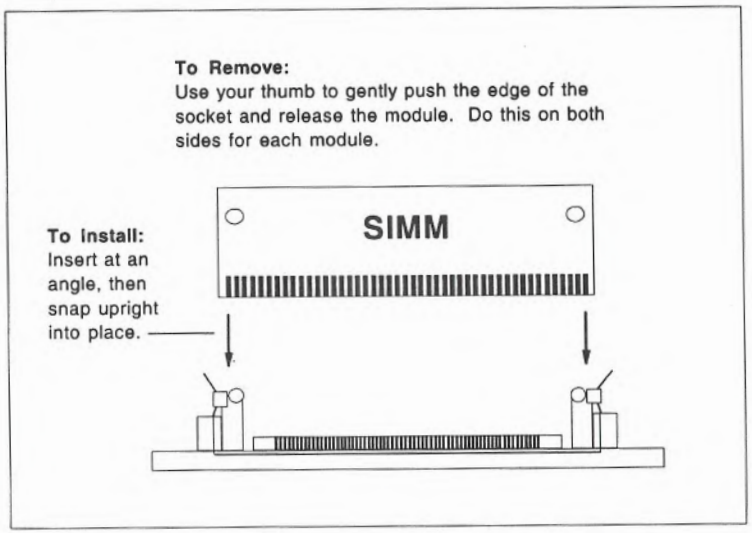


Figure 2-1. Installing/Removing a SIMM Memory Module

SIMM Module Installation

1. Insert SIMM modules in Bank 0 through Bank 3 as required for the desired system memory.
2. Insert each SIMM module into its socket at an angle away from the AT slots. The component side of the SIMM modules must face the AT slots.
3. Gently press the SIMM module in the direction of the AT slots until it snaps upright into place in the socket.

Removing SIMM Modules

1. Remove SIMM modules in correct descending order—from Bank 3 through Bank 0.
2. Gently push the edge of the sockets to the side to release the module. Remove one side of the SIMM module first, and then the other side, to prevent breaking the socket.

Table 2-10. DRAM Bank Configurations

Bank 0	Bank 1	Bank 2	Bank 3	Total
256K x 36	256K x 36	–	–	2M
512K x 36	512K x 36	–	–	4M
1M x 36	1M x 36	–	–	8M
2M x 36	2M x 36	–	–	16M
4M x 36	4M x 36	–	–	32M
8M x 36	8M x 36	–	–	64M
256K x 36	256K x 36	256K x 36	256K x 36	4M
256K x 36	256K x 36	512K x 36	512K x 36	6M
512K x 36	512K x 36	512K x 36	512K x 36	8M
256K x 36	256K x 36	1M x 36	1M x 36	10M
512K x 36	512K x 36	1M x 36	1M x 36	12M
1M x 36	1M x 36	1M x 36	1M x 36	16M
256K x 36	256K x 36	2M x 36	2M x 36	18M
512K x 36	512K x 36	2M x 36	2M x 36	20M
1M x 36	1M x 36	2M x 36	2M x 36	24M
2M x 36	2M x 36	2M x 36	2M x 36	32M
256K x 36	256K x 36	4M x 36	4M x 36	34M
512K x 36	512K x 36	4M x 36	4M x 36	36M
1M x 36	1M x 36	4M x 36	4M x 36	40M
2M x 36	2M x 36	4M x 36	4M x 36	48M
4M x 36	4M x 36	4M x 36	4M x 36	64M
256K x 36	256K x 36	8M x 36	8M x 36	66M
512K x 36	512K x 36	8M x 36	8M x 36	68M
1M x 36	1M x 36	8M x 36	8M x 36	72M
2M x 36	2M x 36	8M x 36	8M x 36	80M
4M x 36	4M x 36	8M x 36	8M x 36	96M
8M x 36	8M x 36	8M x 36	8M x 36	128M

Note: All SIMMs are the 72-pin (36-bit) type.

2-7 Mounting the Motherboard in the Chassis

The motherboard has ten standard mounting holes to fit all different types of chassis. Chassis may come with a variety of mounting fasteners, made of metal or plastic. Although a chassis may have both metal and plastic fasteners, metal fasteners are the most highly recommended because they ground the system board to the chassis. Therefore, use as many metal fasteners as possible for better grounding.

2-8 Connecting Floppy and Hard Disk Drives

Use the following information to connect the floppy and hard disk drive cables.

- The floppy disk drive cable has seven twisted wires. The hard disk drive cable has five wires.
- A red mark on a wire typically designates the location of pin 1.
- A single floppy disk drive ribbon cable has 34 wires and two connectors to provide for two floppy disk drives. The connector with twisted wires always connects to drive A, and the connector that does not have the twisted wires always connects to drive B.
- An IDE hard disk drive requires a data ribbon cable with 40 wires, and a SCSI hard disk drive requires a SCSI ribbon cable with 50 wires.
- A single IDE hard disk drive cable has two connectors to provide for two drives. To select an IDE disk drive as C, you would normally set the drive select jumper on the drive to DS1. To select an IDE disk drive as D, you would normally set the drive select jumper on the drive to DS2. Consult the documentation that came with your disk drive for details on actual jumper locations and settings.

- A single SCSI ribbon cable typically has three connectors to provide for two hard disk drives and the SCSI adapter. (Note: most SCSI hard drives are single-ended SCSI devices.) The SCSI ID is determined by jumpers or a switch on the SCSI device. The last internal (and external) SCSI device cabled to the SCSI adapter must be terminated.
- Some drives require a special controller card. Read your disk drive manual for details.

Chapter 3
AMI BIOS

3-1 Introduction

This chapter describes the WinBIOS for the OPTi® 82C596/597/822 chipset which is designed for an Intel Pentium-based 60/66/90/100 MHz computer system.

System BIOS

The BIOS is the basic input output system used in all IBM® PC, XT™, AT®, and PS/2® compatible computers. The WinBIOS is a high-quality example of a system BIOS.

Configuration Data

AT-compatible systems, also called ISA (Industry Standard Architecture) must have a place to store system information when the computer is turned off. The original IBM AT had 64 bytes of non-volatile memory storage in CMOS RAM. All AT-compatible systems have at least 64 bytes of CMOS RAM, which is usually part of the Real Time Clock. Many systems have 128 bytes of CMOS RAM.

How Data Is Configured

AMIBIOS provides a Setup utility in ROM that is accessed by pressing <Del> at the appropriate time during system boot. Setup configures data in CMOS RAM.

The AMIBIOS Setup utility included in the AMIBIOS for the OPTi 82C596/597 Chipset with 82C822 PCI bridge support can also be executed via a hot key.

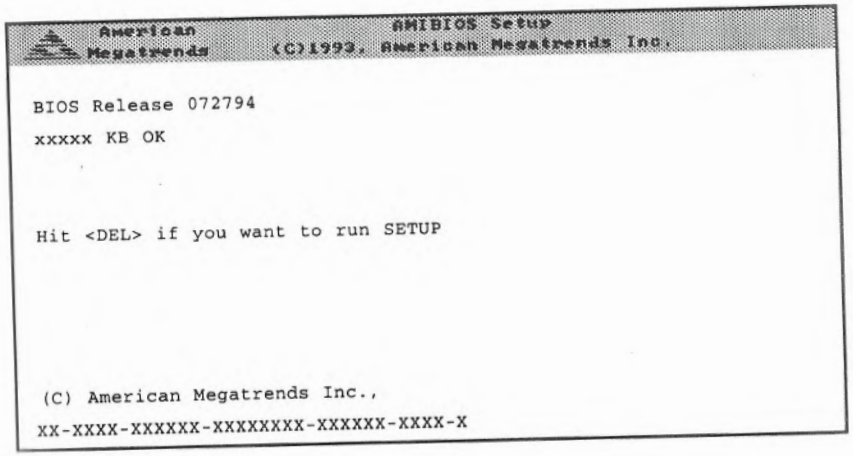
Types of AMIBIOS Setup

Types of Setup	Description
Standard Setup	Sets time, date, hard disk type, types of floppy drives, monitor type, and keyboard if installed. See pages 3-6 through 3-8.
Advanced Setup	Sets Typematic Rate and Delay, Above 1 MB Memory Test, Memory Test Tick Sound, Hit <Del> Message Display, System Boot Up Sequence, and many others. See pages 3-9 through 3-16.
Chipset Setup	Sets chipset-specific options and features. See pages 3-17 through 3-23.
Peripheral Setup	Controls I/O controller-related options.
Power Management Setup	Controls power conservation options. See page 3-24.

3-2 Running Setup

POST Memory Test

Normally, the only visible POST routine is the memory test. The screen that appears when the system is powered on is shown below.



An AMIBIOS Identification string is displayed at the left bottom corner of the screen, below the copyright message.

BIOS Configuration Summary Screen

AMIBIOS displays a screen that looks similar to the following when the POST routines complete successfully.

```
AMIBIOS System Configuration (C) 1985-1994 American Megatrends Inc.,

Main Processor        : P54C          Base Memory Size     : 640 KB
Numeric Coprocessor   : Built-In      Ext. Memory Size     : 7168 KB
Floppy Drive A:       : 1.2 MB, 5¼    Hard Disk C: Type    : SCSI
Floppy Drive B:       : 1.44 MB, 3½   Hard Disk D: Type    : SCSI
Display Type          : VGA/PGA/EGA   Serial Port(s)       : 3F8,2F8
ROM-BIOS Date         : 07/25/94      Parallel Port(s)     : 378

512KB CACHE MEMORY
```


AMIBIOS Setup Configuration

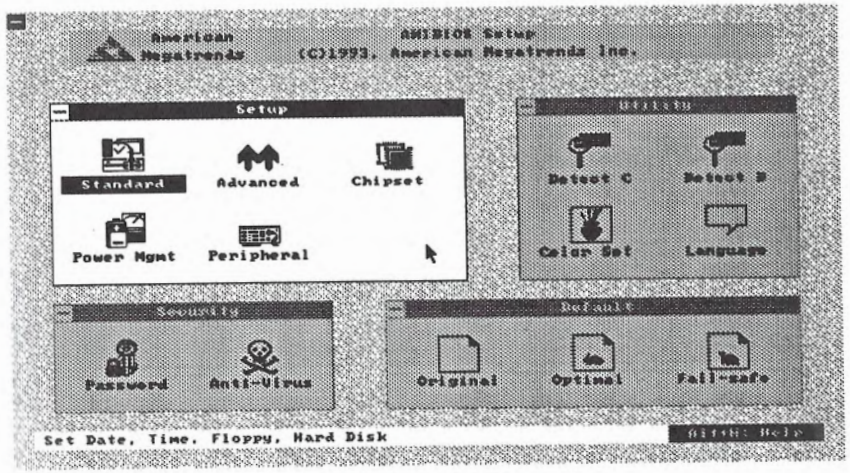
These settings determine the appearance of the WinBIOS Setup main menu, also shown below.

Setup options: Standard, Advanced, Chipset, and Power Mgmt all present. Peripheral absent.

Utility options: Detect C, Detect D, and Color Set all present. Language absent.

Security: Password and Anti-Virus present.

Default: Original, Optimal, and Fail-Safe all present.



The Windows coordinates (zero-based, x1, y1, x2, y2) for the four windows on the WinBIOS Setup main menu are:

Setup: 4, 5, 43, 14

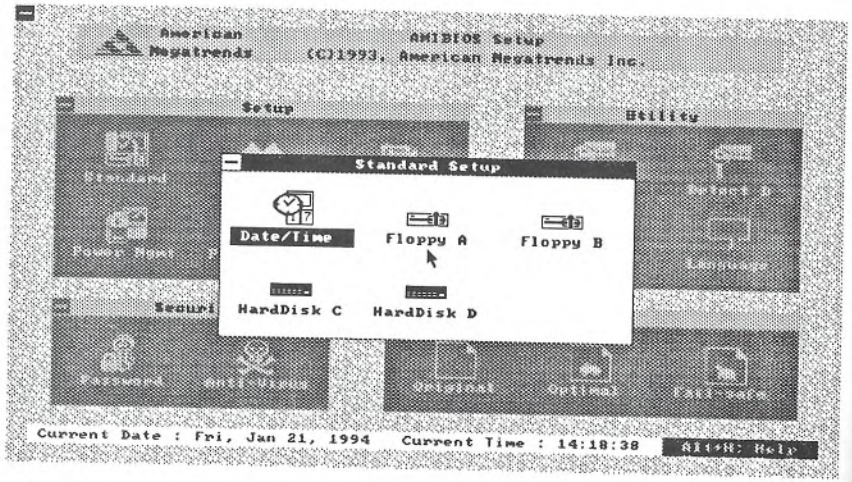
Utility: 49, 5, 75, 14

Security: 4, 16, 30, 21

Default: 36, 16, 75, 21

3-3 Standard Setup

The WinBIOS Setup options described in this section are selected by choosing the appropriate high-level icon from the Standard Setup screen. Standard Setup is selected from the Setup section on the WinBIOS Setup main menu (see the previous page). All displayed icons are described in this section, although the screen display is often all you need to understand how to set the option. The Standard Setup screen is shown below.



Date, Day, and Time Configuration

Select the Standard option. Select the *Date/Time* icon. The current values for each category are displayed. Enter new values through the keyboard.

Hard Disk C: Type
Hard Disk D: Type

Select one of these hard disk drive icons to configure the drive named in the option. A scrollable screen that lists all valid disk drive types is displayed. Select the correct type and press <Enter>. If the hard disk drive is an IDE drive, select *Detect C:* or *Detect D:* from the Utility section of the WinBIOS Setup main menu to have AMIBIOS automatically detect the IDE drive parameters and report them to this screen.

Entering Drive Parameters

You can also enter the hard disk drive parameters. The drive parameters are:

Parameter	Description
Type	The number for a drive with certain identification parameters.
Cylinders	The number of cylinders in the disk drive.
Heads	The number of heads.
Write Precompensation	The size of a sector gets progressively smaller as the track diameter diminishes. Yet each sector must still hold 512 bytes. Write precompensation circuitry on the hard disk compensates for the physical difference in sector size by boosting the write current for sectors on inner tracks. This parameter is the track number where write precompensation begins.
Landing Zone	This number is the cylinder location where the heads will normally park when the system is shut down.
Sectors	The number of sectors per track. MFM drives have 17 sectors per track. RLL drives have 26 sectors per track. ESDI drives have 34 sectors per track. SCSI and IDE drive may have even more sectors per track.
Capacity	The formatted capacity of the drive is (Number of heads) x (Number of cylinders) x (Number of sectors per track) x (512 bytes per sector)

Hard Disk Drive Types

Refer to Appendix B in this manual for a list of the various hard disk drive types.

Using Auto Detect Hard Disk (Only for IDE Drives)

If you select *Detect C:* or *Detect D:* from the Utility section of the WinBIOS Setup main menu, AMIBIOS automatically finds all IDE hard disk drive parameters. AMIBIOS places the hard disk drive parameters that it finds in the Drive C: Type or Drive D: Type fields in Standard Setup.

Floppy Drive A:
Floppy Drive B:

Move the cursor to these fields via ↑ and ↓ and select the floppy type. The settings are *360 KB 5¼ inch*, *1.2 MB 5¼ inch*, *720 KB 3½ inch*, *1.44 MB 3½ inch*, *2.88 MB 3½ inch* or *Not Installed.*

3-4 Advanced Setup

Default Settings

Every option in WinBIOS Setup contains three default settings: an Original default, a Fail-Safe default, and an Optimal default.

Optimal Default

The Optimal default settings provide optimum performance settings for all devices and system features.

Fail-Safe Default

The Fail-Safe default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance characteristics.

Advanced Setup Options

Typematic Rate (Chars/Sec)

This option sets the rate at which characters displayed on the screen repeat when a key is pressed and held down. The settings are *Disabled*, *15*, *20*, or *30* characters per second. The Optimal default setting is *30 cps*. The Fail-Safe default setting is *Disabled*.

System Keyboard

This option specifies if a keyboard is attached to the system. The settings are *Present* or *Absent*. The Optimal and Fail-Safe default settings are *Present*.

Primary Display

This option specifies the type of display adapter card installed in the system. The settings are *VGA/EGA*, *CGA40x25*, *CGA80x25*, *Monochrome*, or *Absent*. The Optimal and Fail-Safe default settings are *VGA/EGA*.

Mouse Support

When this option is set to *Enabled*, AMIBIOS supports a PS/2-type mouse. The settings are *Enabled* or *Disabled*. The Optimal default setting is *Enabled*. The Fail-Safe default setting is *Disabled*.

Above 1 MB Memory Test

When this option is set to *Enabled*, the AMIBIOS memory test is performed on all system memory. When this option is set to *Disabled*, the memory test is done only on the first 1 MB of system memory. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Disabled*.

Memory Test Tick Sound

This option enables (turns on) or disables (turns off) the ticking sound during the memory test. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Enabled*.

Parity Error Check

This option enables or disables parity error checking for system RAM. The settings are *Enabled* (all system RAM parity is checked) or *Disabled* (parity is checked only on the first 1 MB of system RAM). The Optimal default setting is *Enabled*. The Fail-Safe default setting is *Disabled*.

Hit "DEL" Message Display

Disabling this option prevents

```
Hit <DEL> if you want to run Setup
```

from appearing when the system boots. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Enabled*.

Extended BIOS RAM Area

This option specifies whether the top 1 KB of the system programming area beginning at 639K *(DOS 1K)* or address *0:300* in the system BIOS area in low memory will be used to store extended BIOS RAM information. The settings are *DOS 1K* or *0:300*. The Optimal and Fail-Safe default settings are *0:300*.

Wait for "F1" If Any Error

AMIBIOS POST runs system diagnostic tests that can generate a message followed by:

```
Press <F1> to continue
```

If this option is set to *Enabled*, AMIBIOS waits for the end user to press <F1> before continuing. If this option is set to *Disabled*, AMIBIOS continues the boot process without waiting for <F1> to be pressed. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Enabled*.

System Boot Up Num Lock

When this option is set to *On*, AMIBIOS turns off *Num Lock* when the system is powered on so the end user can use the arrow keys on both the numeric keypad and the keyboard. The settings are *On* or *Off*. The Optimal and Fail-Safe default settings are *On*.

Numeric Processor Test

Set this option to *Enabled* to permit AMIBIOS to test for the presence of a math coprocessor in the system. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Enabled*.

Floppy Drive Seek At Boot

When this option is set to *Enabled*, AMIBIOS performs a Seek command on floppy drive A: before booting the system. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Disabled*.

System Boot Up Sequence

This option sets the sequence of boot drives (either floppy drive A: or hard disk drive C:) that AMIBIOS attempts to boot from after AMIBIOS POST completes. The settings are *C:,A:* or *A:,C:*. The Optimal and Fail-Safe default settings are *A:,C:*.

System Boot Up CPU Speed

This option sets the speed of the CPU at system boot time. The settings are *High* or *Low*. The Optimal and Fail-Safe default settings are *High*.

External Cache

This option enables secondary (external) cache memory. If *Disabled* is chosen, secondary cache memory is disabled. The settings are *Disabled* or *Enabled*. The Optimal default setting is *Enabled*. The Fail-Safe default setting is *Disabled*.

Internal Cache

Set this option to *Enabled* to enable the cache memory on the CPU. The settings are *Enabled* or *Disabled*. The Optimal default setting is *Enabled*. The Fail-Safe default setting is *Disabled*.

Password Checking

This option enables the password check option every time the system boots or the end user runs WinBIOS Setup. If *Always* is chosen, a user password prompt appears every time the computer is turned on. If *Setup* is chosen, the password prompt appears if WinBIOS Setup is executed. The Optimal and Fail-Safe default settings are *Setup*.

Video Shadow C000,32K

When these options are set to *Enabled*, the video BIOS ROM area from C0000h–C7FFFh is copied (shadowed) from ROM to RAM for faster execution. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Enabled*.

Shadow C800,16K
Shadow CC00,16K
Shadow D000,16K
Shadow D400,16K
Shadow D800,16K
Shadow DC00,16K

These options enable shadowing of the contents of the ROM area beginning at the address named in the option title (for example, the **Shadow C800, 16K** option enables shadowing of the contents of ROM from C8000h–CBFFFh to RAM. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Disabled*.

IDE Multi-Block Transfer Mode

This option enables multiple sector reads and writes for IDE drives. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Disabled*.

IDE Drives Standby Timer

This option sets the length of a period of IDE drive inactivity. After this period expires, WinBIOS places the IDE drive in Standby mode. The settings are *Disabled*, *2 Min.*, *4 Min.*, or *8 Min.* The Optimal and Fail-Safe default settings are *Disabled*.

Primary IDE 32bit Mode
(32-Bit Mode for the Primary IDE Controller)

Set this option to *Enabled* to enable 32-bit data transfers to and from the IDE drives attached to the primary IDE controller (if the driver is loaded). The WinBIOS supports two IDE controllers. Each IDE controller can have up to two IDE drives attached to it. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Disabled*.

Primary IDE Master Drive LBA Mode
(Set LBA Mode for the first IDE drive attached to the Primary IDE Controller)

Set this option to *Enabled* to enable IDE LBA (Logical Block Address) Mode for the first IDE drive attached to the primary IDE controller. LBA Mode is an advanced method for accessing data on IDE drives. Data is accessed by block addresses rather than the traditional Cylinder-Head-Sector scheme. Data transfer rates can be much higher in LBA mode. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Disabled*.

Primary IDE Slave Drive LBA Mode
(Set LBA Mode for the second IDE drive attached to the Primary IDE Controller)

Set this option to *Enabled* to enable IDE LBA (Logical Block Address) Mode for the second IDE drive attached to the primary IDE controller. LBA Mode is an advanced method for accessing data on IDE drives. Data is accessed by block addresses rather than the traditional Cylinder-Head-Sector scheme. Data transfer rates can be much higher in LBA mode. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Disabled*.

Secondary IDE Cntrl Drives Installed

This option specifies the number of IDE drives controlled by the secondary IDE controller. The settings are *Disabled*, *Master*, or *Mst & Slv*. The Optimal and Fail-Safe default settings are *Disabled*.

Secondary IDE 32bit Mode
(32-Bit Mode for the Secondary IDE Controller)

Set this option to *Enabled* to enable 32-bit data transfers to and from the IDE drives attached to the secondary IDE controller. The WinBIOS supports two IDE controllers. Each IDE controller can have up to two IDE drives attached to it. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Disabled*.

Secondary IDE Master Drive LBA Mode
(Set LBA Mode for the first IDE drive attached to the Secondary IDE Controller)

Set this option to *Enabled* to enable IDE LBA (Logical Block Address) Mode for the first IDE drive attached to the secondary IDE controller. LBA Mode is an advanced method for accessing data on IDE drives. Data is accessed by block addresses rather than the traditional Cylinder-Head-Sector scheme. Data transfer rates can be much higher in LBA mode. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Disabled*.

Secondary IDE Slave Drive LBA Mode
(Set LBA Mode for the second IDE drive attached to the Secondary IDE Controller)

Set this option to *Enabled* to enable IDE LBA (Logical Block Address) Mode for the second IDE drive attached to the secondary IDE controller. LBA Mode is an advanced method for accessing data on IDE drives. Data is accessed by block addresses rather than the traditional Cylinder-Head-Sector scheme. Data transfer rates can be much higher in LBA mode. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Disabled*.

3-5 Chipset Setup

The WinBIOS Setup options described in this section are selected by choosing the appropriate high-level icon from the Chipset Setup screen. Chipset Setup is selected from the Setup section on the WinBIOS Setup main menu. All displayed icons are described in this section, although the screen display is often all you need to understand how to set the option.

Hidden Refresh

If this option is set to *Enabled*, system DRAM memory is refreshed without holding the CPU, improving system performance. This option must be enabled if 4 MB x 36 SIMMs are used in the system. The settings are *Enabled* or *Disabled*. The Optimal default setting is *Enabled*. The Fail-Safe default setting is *Enabled*.

DRAM Row Address Hold

This option specifies the length of time that the RAS (Row Address Strobe) hold segment of the system memory access cycle is prolonged. The settings are *2 CLK* or *3 CLK*. The Optimal and Fail-Safe default settings are *2 CLK*.

DRAM Read CAS Pulse Width

This option sets the length of time for the Read CAS (Column Address Strobe) signal pulse width. The settings are *2 CLK* or *3 CLK*. The Optimal and Fail-Safe default settings are *3 CLK*.

DRAM Write CAS Pulse Width

This option sets the length of time for the Write CAS pulse width. The settings are *2 CLK* or *3 CLK*. The Optimal and Fail-Safe default settings are *3 CLK*.

DRAM RAS Precharge

This option sets the length of time for the RAS precharge cycle. The settings are *6 CLK*, *3 CLK*, *4 CLK*, or *5 CLK*. The Optimal and Fail-Safe defaults are *5 CLK*.

External Cache Mode

The setting of this option determines the type of caching algorithm used in external (secondary) cache memory in the computer. The settings are *Wr-Back* or *Wr-Thru*. The Optimal default is *Wr-Back*. The Fail-Safe default is *Wr-Thru*.

External Cache CAS Precharge

This option sets the length of time for the CAS precharge cycle for SRAM-based L2 secondary cache memory. The settings are *1 CLK* or *2 CLK*. The Optimal and Fail-Safe default settings are *2 CLK*.

External Cache Read Burst Mode

This option sets the secondary cache memory read burst cycle. The settings are *3-2-2-2*, *3-3-3-3*, *4-3-3-3*, or *5-4-4-4*. The Optimal default is *4-3-3-3*. The Fail-Safe default is *5-4-4-4*.

External Cache Write Burst Mode

This option sets the secondary cache memory write burst cycle. The settings are *3-2-2-2*, *4-2-2-2*, *4-3-3-3*, or *5-3-3-3*. The Optimal and Fail-Safe defaults are *4-2-2-2*.

VL-Bus Master Wait State

This option specifies the number of wait states inserted before all VL-Bus bus mastering operations. The settings are *0 W/S* or *1 W/S*. The Optimal and Fail-Safe default settings are *1 W/S*.

VL-Bus Master Preemption

Set this option to Enabled to permit VL-Bus bus mastering devices to be preempted. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Disabled*.

DRAM Base Memory

This option specifies the amount of base DRAM system memory. The settings are *512 KB* or *640 KB*. The Optimal and Fail-Safe default settings are *640 KB*.

DRAM Region A Control Mode
DRAM Region B Control Mode

These options define how memory Region A and Region B are used. These regions must be located above 1 MB. The settings are *Disabled* (the contents of DRAM Region A or Region B cannot be read from or written to secondary cache memory), *Cached* or *Non-cached* (the contents of Region A or Region B can be read from or written to secondary cache memory but only via a write-through caching algorithm), or *Hole* (Region A or Region B become holes in memory where nothing can be stored). The Optimal and Fail-Safe defaults are *Disabled*.

DRAM Region A Size
DRAM Region B Size

These options define the size of the Region A and Region B memory areas. The settings are *256 KB*, *512 KB*, or *Disabled*. The Optimal and Fail-Safe defaults are *Disabled*.

DRAM Region A Base Address
DRAM Region B Base Address

These options set the base address (the beginning address) of the Region A and Region B memory areas. The base address must change in increments equal to the settings of the corresponding DRAM Region A/B Size option. If the DRAM Region A/B Size options are set to *Disabled*, the only choice for the base address for that block is *0 KB*. The Optimal and Fail-Safe defaults are *0 KB*. The base address must not be less than 1 MB if the respective DRAM Region A/B Control Mode is set to *Hole*.

Video Cacheable C000,32K

If this option is set to *Yes*, the contents of the video BIOS RAM area (C0000h–C7FFFh) can be read from or written to secondary cache memory, which improves system performance. But you must be certain that no program will write to the video BIOS area when this option is *Yes*. This option can be set to *Yes* only when Video BIOS shadowing is enabled in Advanced Setup. The settings are *Yes* or *No*. The Optimal and Fail-Safe defaults are *No*.

PCI IRQ

This option specifies the type of interrupts used by the onboard PCI. The settings are *Level* or *Edge*. The Optimal and Fail-Safe default settings are *Level*.

PCI VGA Palette Snooping

This option must be set to *Enabled* if any ISA adapter card installed in the system requires VGA palette snooping. The settings are *Enabled* or *Disabled*. The Optimal and Fail-Safe default settings are *Disabled*.

PCI Slot 1 Use ISA IRQ

This option specifies the type of IRQ (edge-triggered or level-triggered) and the ISA IRQ used by the PCI device in PCI slot 1. Level-triggered interrupts can be shared. The settings are *AUTO* (let WinBIOS automatically determine the IRQ and IRQ type), *5 Edge*, *9 Edge*, *10 Edge*, *11 Edge*, *12 Edge*, *14 Edge*, *15 Edge*, *5 Level*, *9 Level*, *10 Level*, *11 Level*, *12 Level*, *14 Level*, or *15 Level*. The Optimal and Fail-Safe default settings are *AUTO*.

PCI Slot 1 IRQ Connected To

This option specifies the PCI interrupt that the PCI device in PCI slot 1 is using. The settings are *INTA*, *INTB*, *INTC*, or *INTD*. The Optimal and Fail-Safe default settings are *INTA*.

PCI Slot 2 Use ISA IRQ

This option specifies the type of IRQ (edge-triggered or level-triggered) and the ISA IRQ used by the PCI device in PCI slot 2. Level-triggered interrupts can be shared. The settings are *AUTO* (let WinBIOS automatically determine the IRQ and IRQ type), *5 Edge*, *9 Edge*, *10 Edge*, *11 Edge*, *12 Edge*, *14 Edge*, *15 Edge*, *5 Level*, *9 Level*, *10 Level*, *11 Level*, *12 Level*, *14 Level*, or *15 Level*. The Optimal and Fail-Safe default settings are *AUTO*.

PCI Slot 2 IRQ Connected To

This option specifies the PCI interrupt that the PCI device in PCI slot 2 is using. The settings are *INTA*, *INTB*, *INTC*, or *INTD*. The Optimal and Fail-Safe default settings are *INTA*.

PCI Slot 3 Use ISA IRQ

This option specifies the type of IRQ (edge-triggered or level-triggered) and the ISA IRQ used by the PCI device in PCI slot 3. Level-triggered interrupts can be shared. The settings are *AUTO* (let WinBIOS automatically determine the IRQ and IRQ type), *5 Edge*, *9 Edge*, *10 Edge*, *11 Edge*, *12 Edge*, *14 Edge*, *15 Edge*, *5 Level*, *9 Level*, *10 Level*, *11 Level*, *12 Level*, *14 Level*, or *15 Level*. The Optimal and Fail-Safe default settings are *AUTO*.

PCI Slot 3 IRQ Connected To

This option specifies the PCI interrupt that the PCI device in PCI slot 3 is using. The settings are *INTA*, *INTB*, *INTC*, or *INTD*. The Optimal and Fail-Safe default settings are *INTA*.

PCI Slot 4 Use ISA IRQ

This option specifies the type of IRQ (edge-triggered or level-triggered) and the ISA IRQ used by the PCI device in PCI slot 4. Level-triggered interrupts can be shared. The settings are *AUTO* (let WinBIOS automatically determine the IRQ and IRQ type), *5 Edge*, *9 Edge*, *10 Edge*, *11 Edge*, *12 Edge*, *14 Edge*, *15 Edge*, *5 Level*, *9 Level*, *10 Level*, *11 Level*, *12 Level*, *14 Level*, or *15 Level*. The Optimal and Fail-Safe default settings are *AUTO*.

PCI Slot 4 IRQ Connected To

This option specifies the PCI interrupt that the PCI device in PCI slot 4 is using. The settings are *INTA*, *INTB*, *INTC*, or *INTD*. The Optimal and Fail-Safe default settings are *INTA*.

PCI IDE Card Present In

This option specifies which PCI expansion slot the onboard IDE controller is attached to. The settings are *Absent*, *Slot 1*, *Slot 2*, *Slot 3*, or *Slot 4*. The Optimal and Fail-Safe defaults are *Absent*.

PCI IDE IRQ Connected to

This option specifies the PCI interrupt that the IRQ used by the IDE on the PCI bus is connected to. The settings are *INTA*, *INTB*, *INTC*, or *INTD*. The Optimal and Fail-Safe default settings are *INTA*.

PCI IDE IRQ

This option specifies the type of interrupts used by the onboard PCI IDE controller. The settings are *Level* or *Edge*. The Optimal and Fail-Safe default settings are *Level*.

3-6 Power Management Setup

The options described in this section are selected by choosing the appropriate high-level icon from the Power Mgmt Setup screen. Power Mgmt Setup is selected from the Setup section on the WinBIOS Setup main menu. All displayed icons are described in this section, although the screen display is often all you need to understand how to set the option.

Power Management Setup Options

Most Power Management Setup options are specific to the individual system, but there are three options that appear in every AMIBIOS based on the 08/08/93 or later core AMIBIOS. These are the Device Timeout options.

Device-1 Timeout-CPU Low Speed
Device-2 Timeout-PW OUTLET
Device-3 Timeout-Peripheral Control
Device-4 Timeout-Reserved

These options configure the amount of time the specified device can be idle before AMIBIOS takes the device to a low power (or no power) consumption mode. These options are part of AMIBIOS Green PC support.

The character strings *Device 1, Device 2, etc,* should be replaced by the OEM names of the devices under Green PC power management. For example: System Board Timeout, Monitor Timeout, or Printer Timeout.

The settings for these options will vary, depending on the system architecture and the type of device. The BIOS Setup and Power-On defaults are *Disabled.*

Power-Saving Mode Timeout

When this option is set, the system goes to sleep at the end of the selected timeout period if no system activities (such as keyboard, mouse, or video screen activity) occur.

The settings are *Disabled, 1 min., 2 min., 3 min., 4 min., 5 min., 6 min., 7 min., 8 min., 9 min., 10 min.,* or *Reserved.* The BIOS Setup and Power-On default is *Disabled.*

Chapter 4
Troubleshooting

4-1 Troubleshooting Procedures

Use the following procedures to troubleshoot your system. If you have followed all of the procedures below and still need assistance, refer to the 'Technical Support Procedures' and/or 'Returning Merchandise for Service' section(s) in this chapter.

No Video

Use the following steps for troubleshooting your system configuration.

1. If you have no video, follow the flowchart in Figure 4-1.

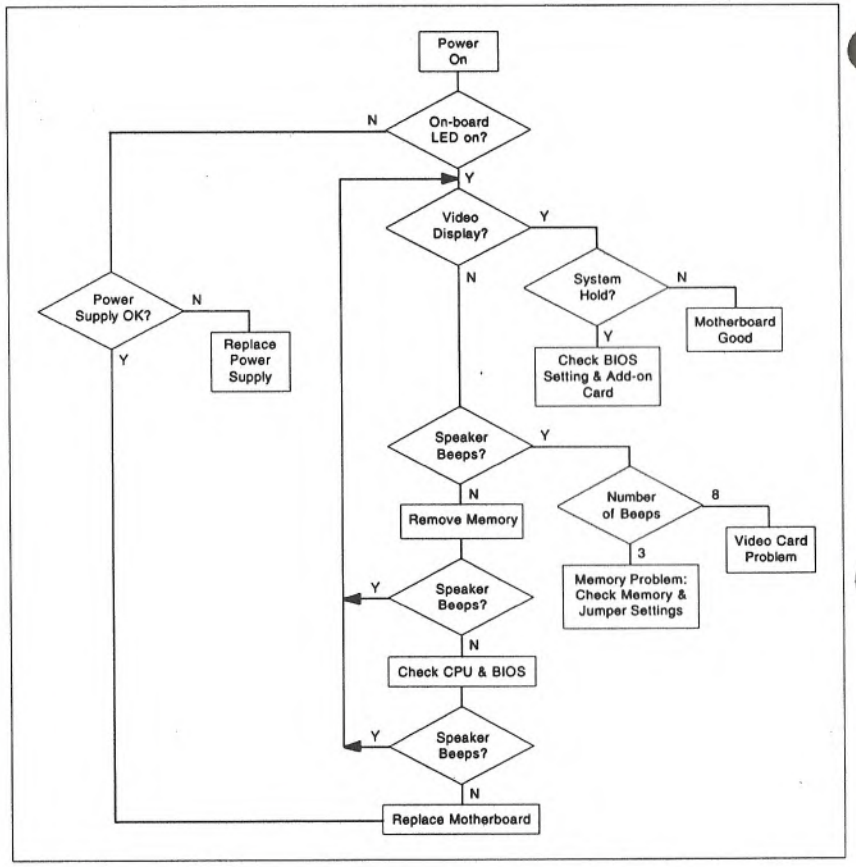


Figure 4-1. Troubleshooting Flowchart

2. Check for missing jumpers or improper installation of the ROM BIOS.
3. Make sure the video card and its jumper setting (as appropriate) match the monitor type.
4. Ensure that all peripheral cards are properly installed in their slots.
5. Check for incorrect cache memory jumper settings that may prevent the system from seeing memory.

6. Ensure that the I/O bus speed is running in the standard 8 MHz range.
7. Use the speaker to determine if any beep codes exist. Refer to Appendix C for details about beep codes.

NOTE

If you are a system integrator, VAR or OEM, a POST diagnostics card is recommended for port 80h codes. Refer to Appendix D.

Memory Error/Parity Error

If you encounter memory or parity errors, follow the procedures below.

1. Check to determine if SIMM modules are improperly installed.
2. Make sure that different types of SIMMs have not been installed in different banks (e.g., a mixture of 256 KB x 36 and 1 MB x 36 SIMMs in Bank 0 and Bank 1).
3. Determine if different speeds of SIMMs have been installed in the same or different banks, and the BIOS setup is configured for the fastest speed of RAM used. It is recommended to use the same RAM speed for SIMMs in different banks.
4. Check for bad SIMM modules or chips.
5. Ensure that cache memory jumpers are correctly set to enable the cache memory.

Losing the System's Setup Configuration

1. Ensure that you are using a high quality power supply. A poor quality power supply may cause the system to lose CMOS setup. Refer to Chapter 1 of this manual for details.
2. Determine if the rechargeable battery is bad. If it is, connect an external battery source of four AA-size batteries to connector J9.
3. If the above steps do not fix the Setup Configuration problem, contact your vendor for repair.

4-2 Technical Support Procedures

1. Go through the 'Troubleshooting Procedures' section in this chapter of the manual before calling Technical Support.
2. If you still cannot get the problem resolved, have the following information ready before you call for technical support:
   - System board serial number
   - CPU serial number
   - Invoice number and date
   - Purchased from
   - Salesperson's name
   - Product configuration

4-3 Returning Merchandise for Service

A receipt or copy of your invoice marked with the date of purchase is required before any warranty service will be rendered. You can obtain service by calling the manufacturer for a Returned Merchandise Authorization (RMA) number. The RMA number should be prominently displayed on the outside of the shipping carton, and mailed prepaid or hand-carried to the manufacturer. Shipping and handling charges will be applied for all orders that must be mailed when service is complete.

This warranty only covers normal consumer use and does not cover damages incurred in shipping or from failure due to the alternation, misuse, abuse, or improper maintenance of products.

During the warranty period, contact your distributor first for any product problems.

Appendix A
Technical Specifications

A-1 System Specifications

CPU

— SUPER P54VL-PCI —

- Intel 3.3-volt Pentium CPU with 64-bit data bus and 32-bit address bus
- 296-pin ZIF (Zero Insertion Force) socket 5

— SUPER P5VL-PCI —

- Intel 5-volt Pentium CPU with 64-bit data bus and 32-bit address bus
- 273-pin ZIF (Zero Insertion Force) socket 4

Math Coprocessor

- Enhanced on-chip, floating-point unit that incorporates sophisticated seven-stage pipelining and hardwired functions

Speed

— SUPER P54VL-PCI —

- Designed to work at 100/90 MHz (and low speed in Power-Saving mode when system is idle) on a Pentium-based computer

— SUPER P5VL-PCI —

- Designed to work at 66/60 MHz (and 33 MHz in Power-Saving mode when system is idle) on a Pentium-based computer

Cache

- 16 KB on-chip, 2-way set associative internal cache
- 64-bit wide data bus with write-back/write-through external cache that supports either 128 KB (8 KB x 8), 256 KB (32 KB x 8), or 512 KB (32 KB x 8) secondary cache

Memory

- 64-bit wide data bus with up to 128 MB of memory on the motherboard
- Page and 2-way Page-Interleave modes support 256 KB x 36, 512 KB x 36, 1 MB x 36, 2 MB x 36, 4 MB x 36, and 8 MB x 36 (60ns or 70ns, 72-pin) SIMMs for up to 128 MB of on-board memory

Multiple Power Savings

- *Green 1:* Smart and user-programmable System Auto Detect or Hardware switch Power-Saving function
- *Green 2:* When system is idle, a lower CPU clock boosts CPU cooling, thus extending system life cycle (Turbo Light will be off)
- *Green 3:* Power supply Power-Saving OUTLET function supports CRT and printer Power Saving

Turbo/Non-turbo Function

- BIOS turbo speed selectable by the keyboard (<Ctrl>+<Alt>+<Shift> and <+> or <->)

Bus

- Five 16-bit AT ISA slots
- Four PCI slots and two Bus Master, Buffer-enhanced, VESA VL-Bus slots; ideal for two Fast SCSI local bus cards and four Fast Network local bus cards in a file server system

BIOS

- AMI® BIOS with built-in setup
- Flash BIOS (optional) for better upgradeability in the future
- Fast Reset and Gate A20 to optimize OS/2®

Shadowed/Cached BIOS

- Shadowed system/video BIOS
- Cached system/video BIOS

Software Compatibility

- 100% IBM® PC/AT® compatible
- DOS, OS/2, UNIX®, XENIX®, Novell®, Windows™, and Windows NT™

Testing

- 50°C, 48-hour, dynamic burn-in with system-level testing

Manufacturing and Support

- Made in U.S.A.
- Design-level Technical Support and Service in U.S.A.

A-2 Memory Address Map

Table A-1. Memory Address Map

Address (Hex)	Size	Function
0000000–009FFFF	640 KB	System board memory
00A0000–00BFFFF	128 KB	Video RAM display buffer
00C0000–00DFFFF	128 KB	Reserved for add-on cards ROM BIOS (i.e., V/EGA)
00E0000–00EFFFF	64 KB	System ROM BIOS expansion
00F0000–00FFFFF	64 KB	System ROM BIOS
0100000–0FDFFFF	15232 KB	Extended memory
0FE0000–0FEFFFF	64 KB	Duplicates of System ROM BIOS expansion at 0E0000–0EFFFF
0FF0000–0FFFFFF	64 KB	Duplicates of System ROM BIOS at 0F0000–0FFFFF
1000000–3FFFFFF	48 MB	Extended memory
0000000–3FFFFFF	64 MB	Extended memory
0000000–7FFFFFF	128 MB	Total memory space addressable by SUPER P5/54VL-PCI System Board

A-3 I/O Address Map

The I/O address map for the system board is locations 00FFh, and for I/O it is 100h–3FFh.

Table A-2. I/O Address Map

Address	Function
000 – 01F	DMA Controller 1, 8237A-5
020 – 021	Interrupt Controller 1, 8259A, Master
022 – 023	Chip set Address
040 – 04F	Timer 1, 8254
050 – 05F	Timer 2, 8254
060 – 06F	8042 Keyboard/Controller
070 – 07F	Real Time Clock (RTC), Non-Maskable Interrupt (NMI) mask
080 – 09F	DMA Page Registers
0A0 – 0BF	Interrupt Controller 2, 8259A
0C0 – 0DF	DMA Controller 2, 8237A-5
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
1F8 – 0FF	Math Coprocessor
1F0 – 1F8	Fixed Disk
200 – 207	Game Ports
278 – 27F	Parallel Printer port 2 (PIO-2)
2F8 – 2FF	Serial Port 2 (SIO-2)
300 – 31F	Prototype Card/Streaming Tape Adapter
360 – 363	PC Network, Low Address
368 – 36B	PC Network, High Address
378 – 37F	Parallel Printer Port 1 (PIO-1)
380 – 38F	SDLC, Bisynchronous 2
3A0 – 3AF	Bisynchronous 1
3B0 – 3BF	Monochrome Display and Primer Adapter
3C0 – 3CF	EGA Adapter
3D0 – 3DF	Color/Graphics Monitor Adapter
3F0 – 3F7	Diskette Controller
3F8 – 3FF	Serial Port 1 (SIO-1)

A-4 I/O Expansion Slots

Input/output direction is determined from the system board's viewpoint. 'I' is input from the I/O bus to the system board. 'O' is output from the system board to the I/O bus.

Ground	GND	B1	A1	-I/O CH CK	I
O	RESET DRV	B2	A2	SD7	I/O
Power	+5 VDC	B3	A3	SD6	I/O
I	IRQ9	B4	A4	SD5	I/O
Power	-5 VDC	B5	A5	SD4	I/O
I	DRQ2	B6	A6	SD3	I/O
Power	-12 VDC	B7	A7	SD2	I/O
Ground	GND	B10	A10	-I/O CHRDY	I
O	-SMEMW	B11	A11	AEN	O
O	-SMEMR	B12	A12	SA19	I/O
I/O	-IOW	B13	A13	SA18	I/O
I/O	-IOR	B14	A14	SA17	I/O
O	-DACK3	B15	A15	SA16	I/O
I	DRQ3	B16	A16	SA15	I/O
O	-DACK1	B17	A17	SA14	I/O
I	DRQ1	B18	A18	SA13	I/O
I/O	-REFRESH	B19	A19	SA12	I/O
O	CLK	B20	A20	SA11	I/O
I	IRQ7	B21	A21	SA10	I/O
I	IRQ6	B22	A22	SA9	I/O
I	IRQ5	B23	A23	SA8	I/O
I	IRQ4	B24	A24	SA7	I/O
I	IRQ3	B25	A25	SA6	I/O
O	-DACK2	B26	A26	SA5	I/O
O	T/C	B27	A27	SA4	I/O
O	BALE	B28	A28	SA3	I/O
Power	+5 VDC	B29	A29	SA2	I/O
O	OSC	B30	A30	SA1	I/O
Ground	GND	B31	A31	SA0	I/O
I	-MEMCS16	D1	C1	-BHE	I/O
I	-I/OCS16	D2	C2	LA23	I/O
I	IRQ10	D3	C3	LA22	I/O
I	IRQ11	D4	C4	LA21	I/O
I	IRQ12	D5	C5	LA20	I/O
I	IRQ15	D6	C6	LA19	I/O
I	IRQ14	D7	C7	LA18	I/O
O	-DACK0	D8	C8	LA17	I/O
I	DRQ0	D9	C9	-MEMR	I/O
O	-DACK5	D10	C10	-MEMW	I/O
I	DRQ5	D11	C11	SD08	I/O
O	-DACK6	D12	C12	SD09	I/O
I	DRQ6	D13	C13	SD10	I/O
O	-DACK7	D14	C14	SD11	I/O
I	DRQ7	D15	C15	SD12	I/O
Power	+5 VDC	D16	C16	SD13	I/O
I	-MASTER	D17	C17	SD14	I/O
Ground	GND	D18	C18	SD15	I/O

A-5 82C206 Integrated Peripheral Controller (IPC)

Details for the Integrated Peripheral Controller (IPC) chip Direct Memory Address (DMA) channels, controller registers, page register addresses, interrupts, timers/counters, and CMOS RAM address map are given below.

Table A-3. DMA Channels

Channel	Function
0	Spare (8-bit, 64 KB block transfer)
1	SDLC (8-bit, 64 KB block transfer)
2	Floppy Disk (8-bit, 64 KB block transfer)
3	Spare (8-bit, 64 KB block transfer)
4	Cascade for DMA controller 1
5	Spare (16-bit, 128 KB block transfer)
6	Spare (16-bit, 128 KB block transfer)
7	Spare (16-bit, 128 KB block transfer)

Table A-4. DMA Controller Registers

Address (Hex)	Command Code
C0	CH-0 base and current address
C2	CH-0 base and current word count
C4	CH-1 base and current address
C6	CH-1 base and current word count
C8	CH-2 base and current address
CA	CH-2 base and current word count
CC	CH-3 base and current address
CE	CH-3 base and current word count
D0	Read Status Register/Write Command Register
D2	Write Request Register
D4	Write Single Mask Register Bit
D6	Write Mode Register
D8	Clear Byte Pointer Flip-Flop
DA	Read Temporary Register/Write Master Clear
DC	Clear Master Register
DE	Write All Mask Register Bits

Table A-5. Page Register Addresses

Page Register	I/O Address (Hex)
DMA Channel 0	87
DMA Channel 1	83
DMA Channel 2	81
DMA Channel 3	82
DMA Channel 5	8B
DMA Channel 6	89
DMA Channel 7	8A
Refresh	8F

Table A-6. Interrupt Controller

Level	Function
NMI	System memory parity error or I/O channel check
IRQ0	System timer 0 output
IRQ1	Keyboard output buffer full
IRQ2	Interrupt from controller 2 (levels 8-15)
IRQ3	Serial port 2
IRQ4	Serial port 1
IRQ5	Parallel port 2
IRQ6	Floppy disk controller
IRQ7	Parallel port 1
IRQ8	Real-time clock
IRQ9	Reserved
IRQ10	Reserved
IRQ11	Reserved
IRQ12	Reserved
IRQ13	Coprocessor interrupt
IRQ14	Hard disk controller
IRQ15	Reserved

Table A-7. Timers/Counters

Channel	Function	Status
0	System Timer	
	Gate 0:	Always Enabled
	Clock In 0:	1.19 MHz clock
	Clock Out 0:	IRQ0
1	Memory Refresh Request/Generator	
	Gate 1:	Always Enabled
	Clock In 1:	1.19 MHz clock
	Clock Out 1:	Refresh request cycle
2	Speaker Tone Generator	
	Gate 2:	Bit 0 of I/O port 61 H
	Clock In 2:	1.19 MHz
	Clock Out 2:	Audio frequency to speaker

Table A-8. CMOS RAM Address Map

Address (Hex)	Description		
00 – 0D*	Real-time clock:		
	Hex	Decimal	Function
	0	0	Seconds
	1	1	Second alarm
	2	2	Minutes
	3	3	Minute alarm
	4	4	Hours
	5	5	Hour alarm
	6	6	Day of week
	7	7	Date of month
	8	8	Month
	9	9	Year
	A	10	Status Register A
	B	11	Status Register B
	C	12	Status Register C
	D	13	Status Register D

* This byte is not included in the checksum calculation and is not part of the configuration record.

Table A-8. CMOS RAM Address Map (Continued)

Address (Hex)	Description
0E*	Diagnostic status byte
0F*	Shutdown status byte
10	Floppy disk drive type byte
11	Reserved
12	Fixed disk type byte, for drives C and D, types 1–14
13	Reserved
14	Equipment byte
15	Base memory, low byte
16	Base memory, high byte
17	Expansion memory, low byte
18	Expansion memory, high byte
19	Fixed disk C extended byte, for types 15–47
1A	Fixed disk D extended byte, for types 15–47
1B – 2D	Reserved
2E – 2F	CMOS RAM checksum, 2 bytes
30*	Expansion memory, low byte
31*	Expansion memory, high byte
32*	Date century byte
33*	Information flag byte set during power-up
34 – 3F	Reserved

* This byte is not included in the checksum calculation and is not part of the configuration record.

A-6 Keyboard Controller

The 8042 keyboard controller is a single chip microcomputer that interfaces between the system board and keyboard. It performs the following functions:

- Interacts with the system power-up initialization.

- Receives data from the keyboard, translates it into system scan codes, puts the scan codes in a data buffer, and then interrupts the system to receive the data or waits until the system polls the status register.
- Transmits system commands to the keyboard and reports the keyboard response to the system.
- Directs its I/0 ports to perform control functions for the system.

Status Register

The status register is an 8-bit Read-Only register, located at 64h.

Bit	Function	Status
7	Parity Error	
	0:	Odd parity
	1:	Even parity
6	Receive Time-Out	
	0:	No time-out
	1:	Time-out
5	Transmit Time-Out	
	0:	No time-out
	1:	Time-out
4	Inhibit Switch	
	0:	Keyboard is inhibited
	1:	Data is placed in the keyboard controller's output buffer
3	Command/Data	
	0:	If data port 60h is written
	1:	If command port 64h is written
2	System Flag	
	0:	Controller will set to 0 at power on test
	1:	Controller will set to 1 after self test
1	Input Buffer Full	
	0:	Input buffer empty
	1:	Input buffer full, will become 0 after read
0	Output Buffer Full	
	0:	Output buffer empty
	1:	Output buffer full, will become 0 after read

Input Buffer

I/O port 60h, Read-Only, 8-bit

Output Buffer

I/O port 60h or 64h, Write-Only, 8-bit

Write 60h: Data Write
Write 64h: Command Write

Keyboard I/O Ports

The keyboard controller has two I/O ports, one for input and the other for output. The bit definitions are as follows.

Input Port

Bit	Function	Status
7	Keyboard Inhibit Switch	
	0:	Keyboard inhibited
	1:	Keyboard not inhibited
6	Display type	
	0:	Color adapter
	1:	Monochrome adapter
5	Reserved	
4	RAM on system board	
	0:	Disable second 256 KB system RAM
	1:	Enable second 256 KB system RAM
3	Reserved	
2	Reserved	
1	Reserved	
0	Reserved	

Output Port

Bit	Function	Status
7	Keyboard data output	
6	Keyboard clock output	
5	Input buffer empty indicator	
	0:	Input buffer not empty
	1:	Input buffer empty
4	Output buffer full	
	0:	Output buffer not full
	1:	Output buffer full
3	Reserved	
2	Reserved	
1	Gate A20	
	0:	Gate A20 inhibited
	1:	Gate A20 not inhibited
0	System Reset	
	0:	System reset
	1:	System not reset

Appendix B
BIOS Hard Disk Drive Types

Table B-1. AMI BIOS Hard Disk Drive Types

Type	Cylinders	Heads	Write Precompensation	Landing Zone	Sectors	Size
1	306	4	128	305	17	10 MB
2	615	4	300	615	17	20 MB
3	615	6	300	615	17	31 MB
4	940	8	512	940	17	62 MB
5	940	6	512	940	17	47 MB
6	615	4	65535	615	17	20 MB
7	462	8	256	511	17	31 MB
8	733	5	65535	733	17	30 MB
9	900	15	65535	901	17	112 MB
10	820	3	65535	820	17	20 MB
11	855	5	65535	855	17	35 MB
12	855	7	65535	855	17	50 MB
13	306	8	128	319	17	20 MB
14	733	7	65535	733	17	43 MB
16	612	4	0	663	17	20 MB
17	977	5	300	977	17	41 MB
18	977	7	65535	977	17	57 MB
19	1024	7	512	1023	17	60 MB
20	733	5	300	732	17	30 MB
21	733	7	300	732	17	43 MB
22	733	5	300	733	17	30 MB
23	306	4	0	336	17	10 MB
24	925	7	0	925	17	54 MB
25	925	9	65535	925	17	69 MB
26	754	7	754	754	17	44 MB
27	754	11	65535	754	17	69 MB
28	699	7	256	699	17	41 MB
29	823	10	65535	823	17	68 MB
30	918	7	918	918	17	53 MB
31	1024	11	65535	1024	17	94 MB
32	1024	15	65535	1024	17	128 MB
33	1024	5	1024	1024	17	43 MB
34	612	2	128	612	17	10 MB
35	1024	9	65535	1024	17	77 MB
36	1024	8	512	1024	17	68 MB

Table B-1. AMI BIOS Hard Disk Drive Types (Continued)

Type	Cylinders	Heads	Write Precompensation	Landing Zone	Sectors	Size
37	615	8	128	615	17	41 MB
38	987	3	987	987	17	25 MB
39	987	7	987	987	17	57 MB
40	820	6	820	820	17	41 MB
41	977	5	977	977	17	41 MB
42	981	5	981	981	17	41 MB
43	830	7	512	831	17	48 MB
44	830	10	65535	830	17	69 MB
45	917	15	65535	918	17	114 MB
46	1224	15	65535	1223	17	152 MB
47	ENTER PARAMETERS PROVIDED WITH HARD DRIVE					

Appendix C
BIOS Error Beep Codes

During the POST (Power-On Self-Test) routines, which are performed each time the system is powered on, errors may occur.

Non-fatal errors are those which, in most cases, allow the system to continue the boot-up process. The error messages normally appear on the screen. See Appendix E for BIOS Error Messages.

Fatal errors are those which will not allow the system to continue the boot-up procedure. If a fatal error occurs, you should consult with your system manufacturer for possible repairs.

These fatal errors are usually communicated through a series of audible beeps. The numbers on the fatal error list below correspond to the number of beeps for the corresponding error. All errors listed, with the exception of #8, are fatal errors.

Beeps	Error message	Description
1	Refresh Failure	The memory refresh circuitry on the motherboard is faulty.
2	Parity Error	A parity error was detected in the base memory (the first 64 KB block) of the system.
3	Base 64 KB Memory Failure	A memory failure occurred within the first 64 KB of memory.
4	Timer Not Operational	A memory failure was detected in the first 64 KB of memory, or Timer 1 is not functioning.
5	Processor Error	The CPU on the system board generated an error.
6	8042 - Gate A20 Failure	The keyboard controller (8042) contains the Gate A20 switch which allows the CPU to operate in virtual mode. This error means that the BIOS cannot switch the CPU into protected mode.
7	Processor Exception Interrupt Error	The CPU on the motherboard generated an exception interrupt.
8	Display Memory Read/Write Error	The system video adapter is either missing or its memory is faulty. ***Please Note:*** This is not a fatal error.
9	ROM Checksum Error	The ROM checksum value does not match the value encoded in the BIOS.
10	CMOS Shutdown Register Read/Write Error	The shutdown register for CMOS memory has failed.
11	Cache memory bad - do not enable cache	The cache memory test failed. Cache memory is disabled. ***Do not press <Ctrl>+<Alt>+<Shift> and <+> to enable cache memory.***

Appendix D
AMI BIOS POST Diagnostic Error Messages

This section describes the power-on self-tests (POST) port 80 codes for the AMI BIOS.

Check Point	Description
01	Processor register test about to start, and NMI to be disabled.
02	NMI is Disabled. Power-on delay starting.
03	Power-on delay completed. Any initialization before keyboard BAT is in progress.
04	Any initialization before keyboard BAT is completed. Reading keyboard SYS bit to check soft reset/power-on.
05	Soft reset/power-on determined. Going to enable ROM (i.e., disable shadow RAM/cache, if any).
06	ROM is enabled. Calculating ROM BIOS checksum, and waiting for keyboard controller input buffer to be free.
07	ROM BIOS checksum passed, keyboard controller I/B free. Going to issue the BAT command to keyboard controller.
08	BAT command keyboard controller is issued. Going to verify the BAT command.
09	Keyboard controller BAT result verified. Keyboard command byte to be written next.
0A	Keyboard command byte code is issued. Going to write command byte data.

Check Point	Description
0B	Keyboard controller command byte is written. Going to issue pin-23, 24 blocking/unblocking command.
0C	Pin-23, 24 of keyboard controller is blocked/unblocked. NOP command of keyboard controller to be issued next.
0D	NOP command processing is done. CMOS shutdown register test to be done next.
0E	CMOS shutdown register R/W test passed. Going to calculate CMOS checksum, and update DIAG byte.
0F	CMOS checksum calculation is done, DIAG byte written. CMOS initialization to begin (if "INIT CMOS IN EVERY BOOT" is set).
10	CMOS initialization done (if any). CMOS status register about to initialize for Date and Time.
11	CMOS Status register initialized. Going to disable DMA and Interrupt controllers.
12	DMA controller #1, #2 and interrupt controller #1, #2 disabled. About to disable video display and initialize port-B.
13	Video display is disabled and port-B is initialized. Chip set initialize/auto memory detection about to begin.
14	Chip set initialization/auto memory detection over. 8254 timer test about to start.
15	CH-2 timer test halfway. 8254 CH-2 timer test to be completed.
16	CH-2 timer test over. 8254 CH-1 timer test to be completed.

Check Point	Description
17	CH-1 timer test over. 8254 CH-1 timer test to be completed.
18	CH-0 timer test over. About to start memory refresh.
19	Memory refresh started. Memory Refresh test to be done next.
1A	Memory Refresh line is toggling. Going to check 15 microsecond ON/OFF time.
1B	Memory Refresh period 30 microsecond test completed. Base 64 KB memory test about to start.
20	Base 64 KB memory test started. Address line test to be done next.
21	Address line test passed. Going to do toggle parity.
22	Toggle parity over. Going for sequential data R/W test.
23	Base 64 KB sequential data R/W test passed. Any setup before Interrupt vector initialize about to start.
24	Setup required before vector initialization completed. Interrupt vector initialization about to begin.
25	Interrupt vector initialization done. Going to read I/O port of 8042 for turbo switch (if any).
26	I/O port of 8042 is read. Going to initialize global data for turbo switch.
27	Global data initialization is over. Any initialization after interrupt vector to be done next.
28	Initialization after interrupt vector is completed. Going for monochrome mode setting.

Check Point	Description
29	Monochrome mode setting is done. Going for Color mode setting.
2A	Color mode setting is done. About to go for toggle parity before optional ROM test.
2B	Toggle parity over. About to give control for any setup required before optional video ROM check.
2C	Processing before video ROM control is done. About to look for optional video ROM and give control.
2D	Optional video ROM control is done. About to give control to do any processing after video ROM returns control.
2E	Return from processing after the video ROM control. If EGA/VGA not found, then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. About to do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. About to look for the alternate display retrace checking.
33	Video display checking over. Verification of display type with switch setting and actual card to begin.
34	Verification of display adapter done. Display mode to be set next.
35	Display mode set completed. BIOS ROM data area about to be checked.

Check Point	Description
36	BIOS ROM data area check over. Going to set cursor for power-on message.
37	Cursor setting for power on message ID complete. Going to display the power-on message.
38	Power-on message display complete. Going to read new cursor position.
39	New cursor position read and saved. Going to display the reference string.
3A	Reference string display is over. Going to display the "Hit <ESC>" message.
3B	"Hit <ESC>" message is displayed. Virtual mode memory test about to start.
40	Preparation for virtual mode test started. Going to verify from video memory.
41	Returned after verifying from display memory. Going to prepare the descriptor tables.
42	Descriptor tables prepared. Going to enter in virtual mode for memory test.
43	Entered in the virtual mode. Going to enable interrupts for diagnostics mode.
44	Interrupts enabled (if diagnostics switch is on). Going to initialize data to check memory remap at 0:0.
45	Data initialized. Going to check for memory remap at 0:0 and find the total system memory size.
46	Memory remap test done. Memory size calculation over. About to go for writing patterns to test memory.

Check Point	Description
47	Pattern to be tested written in extended memory. Going to write patterns in base 640 KB memory.
48	Patterns written in base memory. Going to find out amount of memory below 1 MB memory.
49	Amount of memory below 1 MB found and verified. Going to find out amount of memory above 1 MB memory.
4A	Amount of memory above 1 MB found and verified. Going for BIOS ROM data area check.
4B	BIOS ROM data area check over. Going to check <ESC> and to clear memory below 1 MB for soft reset.
4C	Memory below 1 MB cleared. (SOFT RESET.) Going to clear memory above it.
4D	Memory above 1 MB cleared. (SOFT RESET.) Going to save the memory size.
4E	Memory test started. (NO SOFT RESET.) About to display the first 64 KB memory test.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory test below 1 MB completed. Going to adjust memory size for relocation/shadow.
51	Memory size adjusted due to relocation/shadow. Memory test above 1 MB to follow.
52	Memory test above 1 MB completed. Going to prepare to go back to real mode.

Check Point	Description
53	CPU registers are saved including memory size. Going to enter into real mode.
54	Shutdown successful, CPU in real mode. Going to restore registers saved during preparation for shutdown.
55	Registers restored. Going to disable Gate A20 address line.
56	A20 address line disable successful. BIOS ROM data area about to be checked.
57	BIOS ROM data area check halfway. BIOS ROM data area check to be completed.
58	BIOS ROM data area check over. Going to clear "Hit <ESC>" message.
59	"Hit <ESC>" message cleared. "WAIT..." message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. About to verify from display memory.
61	Display memory verification over. About to go for DMA #1 base register test.
62	DMA #1 base register test passed. About to go for DMA #2 base register test.
63	DMA #2 base register test passed. About to go for BIOS ROM data area check.
64	BIOS ROM data area check halfway. BIOS ROM data area check to be completed.
65	BIOS ROM data area check over. About to program DMA unit 1 and 2.

Check Point	Description
66	DMA unit 1 and 2 programming over. About to initialize 8259 interrupt controller.
67	8259 initialization over. About to start keyboard test.
80	Keyboard test started. Clearing out buffer, checking for stuck key. About to issue keyboard reset command.
81	Keyboard reset error/stuck key found. About to issue keyboard controller interface test command.
82	Keyboard controller interface test over. About to write command byte and initialize circular buffer.
83	Command byte written. Global data initialize done. About to check for lock-key.
84	Lock-key checking over. About to check for memory size mismatch with CMOS.
85	Memory size check done. About to display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup completed. Going to CMOS setup program.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup completed. Going to display power-on screen message.
8A	First screen message displayed. About to display "WAIT..." message. Mouse check and initialization to be done next.

Check Point	Description
8B	"WAIT..." message displayed. Mouse check and initialization done. About to do Main and Video BIOS shadow.
8C	Main and Video BIOS shadow successful. Setup options programming after CMOS setup about to start.
8D	Setup options are programmed. Going for hard disk, floppy reset.
8E	Hard disk, floppy reset applied. About to go for floppy check.
8F	Floppy check returns that floppy is to be initialized. Floppy setup to follow.
90	Floppy setup is over. Test for hard disk presence to be done.
91	Hard disk presence test over. Hard disk setup to follow.
92	Hard disk setup complete. About to go for BIOS ROM data area check.
93	BIOS ROM data area check halfway. BIOS ROM data area check to be completed.
94	BIOS ROM data area check over. Going to set base and extended memory size.
95	Memory size adjusted due to mouse support, hard disk type-47. Going to verify from display memory.
96	Returned after verifying from display memory. Going to do any initialization before C800 optional ROM control.
97	Any initialization before C800 optional control is over. Optional ROM check and control will be done next.

Check Point	Description
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control.
99	Any initialization required after optional ROM test over. Going to set up timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test.
9C	Required initialization before coprocessor test is over. Going to initialize the coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after coprocessor test.
9E	Initialization after coprocessor test is completed. Going to check extended keyboard, keyboard ID and num-lock.
9F	Extended keyboard check, ID flag set, num-lock on/off is done. Keyboard ID command to be issued.
A0	Keyboard ID command is issued. Keyboard ID flag to be reset.
A1	Keyboard ID flag reset. Cache memory test to follow.
A2	Cache memory test over. Going to display any soft errors.
A3	Soft error display complete. Going to set the keyboard typematic rate.
A4	Keyboard typematic rate set. Going to program memory wait states.

Check Point	Description
A5	Memory wait states programming over. Screen to be cleared next.
A6	Screen cleared. Going to enable parity and NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
00	System configuration is displayed. Going to give control to INT 19h boot loader.

Appendix E
BIOS Non-Fatal Error Messages

If a non-fatal error occurs during the POST routines performed each time the system is powered on, the error message will appear on the screen in the following format:

```
ERROR Message Line 1
ERROR Message Line 2
Press <F1> to RESUME
```

Note the error message and press the <F1 > key to continue with the boot up sequence.

NOTE

If the "Wait for <F1> If Any Error" option in the Advanced CMOS Setup portion of the BIOS SETUP PROGRAM has been set to "disabled," the <FI> prompt will not appear on the third line.

For most of the error messages, there is no ERROR Message Line 2. Generally, for those messages containing a line 2 ERROR Message the text will be "RUN SETUP UTILITY." Pressing the <F1> key will invoke the BIOS SETUP PROGRAM.

A description of the error messages appears below.

1. **CH-2 Timer Error** — Most PC AT™ standard system boards include two timers. An error with timer #1 is a fatal error, explained in Appendix C. If an error occurs with timer #2, this error message appears.

2. **INTR #1 Error** — The interrupt channel #1 has failed the POST routine.

3. **INTR #2 Error** — The interrupt channel #2 has failed the POST routine.

4. **CMOS Battery State Low** — There is a battery in your system which is used for storing the CMOS values. This battery appears to be low in power and needs to be replaced.

5. **CMOS Checksum Failure** — After the CMOS values are saved, a checksum value is generated to provide for error checking. If the previous value is different from the value currently read, this error message appears. To correct this error, you should run BIOS SETUP Program.

6. **CMOS System Options Not Set** — The values stored in the CMOS are either corrupt or nonexistent. Run the BIOS SETUP Program to correct this error.

7. **CMOS Display Type Mismatch** — The type of video stored in CMOS does not match the type detected by the BIOS. Run the BIOS SETUP Program to correct this error.

8. **Display Switch Not Proper** — Some systems require that a video switch on the motherboard be set to either color or monochrome, depending upon the type of video you are using. To correct this situation, set the switch properly. (Remember to shut down the system first.)

9. **Keyboard is Locked...Unlocked It** — The keyboard lock on the system is engaged. The system must be unlocked to continue the boot-up procedure.

10. **Keyboard Error** — The BIOS has encountered a timing problem with the keyboard. Make sure you have an AMI keyboard BIOS installed in your system. You may also set the 'Keyboard' option in the BIOS SETUP Program, Standard CMOS Setup to "Not Installed," which will cause the BIOS to skip the keyboard POST routines.

11. **KB/Interface Error** — The BIOS has found an error with the keyboard connector on the system board.

12. **CMOS Memory Size Mismatch** — If the BIOS finds the amount of memory on your system board to be different from the amount stored in CMOS, this error message is generated. Run the BIOS SETUP Program to correct this error.

13. **FDD Controller Failure** — The BIOS is not able to communicate with the floppy disk drive controller. Check all appropriate connections after the system is powered off.

14. **HDD Controller Failure** — The BIOS is not able to communicate with the hard disk drive controller. Check all appropriate connections after the system is powered down.

15. **C: Drive Error** — The BIOS is not receiving any response from hard disk drive C. It may be necessary to run the Hard Disk Utility to correct this problem. Also, check the type of hard disk selected in the Standard CMOS Setup of the BIOS SETUP Program to see if the correct hard disk drive has been selected.

16. **D: Drive Error** — The same error has occurred with hard drive D. Follow the procedures in Error #15 to correct the situation.

17. **C: Drive Failure** — The BIOS cannot get any response from the hard disk drive C. It may be necessary to replace the hard disk.

18. **D: Drive Failure** — The same error as #17 has occurred with hard drive D.

19. **CMOS Time & Date Not Set** — Run the 'Standard CMOS Setup' of the BIOS SETUP Program to set the date and time of the CMOS.

20. **Cache Memory Bad, Do Not Enable Cache!** — The BIOS has found the cache memory of the motherboard to be defective. Consult your system manufacturer to repair this problem.

21. **8042 Gate A20 Error** — The Gate A20 portion of the keyboard controller (8042) has failed to operate correctly. The 8042 chip should be replaced.

22. **Address Line Short!** — An error has occurred in the address decoding circuitry of the motherboard.

23. **DMA #2 Error** — An error has occurred with the second DMA channel on the motherboard.

24. **DMA #1 Error** — An error has occurred with the first DMA channel on the motherboard.

25. **DMA Error** — An error has occurred with the DMA controller on the motherboard.

26. **No ROM BASIC** — This error occurred when a proper bootable sector cannot be found on either the floppy diskette drive A: or the hard disk drive C:. The BIOS will try at this point to run ROM Basic, and the error message will be generated when the BIOS does not find it.

27. **Diskette Boot Failure** — The diskette used to boot-up in floppy drive A is corrupt, which means you cannot use it to boot-up the system. Use another boot diskette and follow the instructions on the screen.

28. **Invalid Boot Diskette** — The BIOS can read the diskette in floppy drive A, but it cannot boot-up the system with it. Use another boot diskette and follow the instructions on the screen.

29. * **On Board Parity Error** — The BIOS has encountered a parity error with some memory installed on the system board. The message will appear as follows:

```
ON BOARD PARITY ERROR
ADDR (HEX) = (XXXX)
```

Where XXXX is the address (in hexadecimal) where the error has occurred. "On Board" means that it is part of the memory attached directly to the system board, as opposed to memory installed via an expansion card in an I/O bus slot.

30. * **Off Board Parity Error** — The BIOS has encountered a parity error with some memory installed in an I/O bus slot. The message will appear as follows:

```
OFF BOARD PARITY ERROR
ADDR (HEX) = (XXXX)
```

Where XXXX is the address (in hexadecimal) where the error has occurred. "Off Board" means that it is part of the memory installed via an expansion card in an I/O bus slot, as opposed to memory attached directly to the system board.

* Memory diagnostic software, such as AMIDIAG, can be used to find and correct memory problems.

31. * **Parity Error ????** — The BIOS has encountered a parity error with some memory in the system, but it is not able to determine the address of the error.

* Memory diagnostic software, such as AMIDIAG, can be used to find and correct memory problems.

Appendix F
Hard Disk Utility Error Messages

The following messages may appear during execution of the 'Hard Disk Utility' section of the AMI BIOS SETUP Program.

The first group of errors listed below may appear during the initialization process, before anything else happens.

1. **No Hard Disk Installed** — The program could not find a hard disk drive installed on the system. This message appears if there is no hard disk on the system and you have chosen to run the Hard Disk Utility.

2. **FATAL ERROR Bad Hard Disk** — The program is not getting a response from the hard disk, or the hard disk is not repairable. Check all cable and power connections to the hard disk.

3. **Hard Disk Controller Failure** — The program is getting an error response from the reset command sent to the hard disk controller. Check to see that the controller is seated properly in the bus slot.

4. **C: (D:) Hard Disk Failure** — The hard disk drive (C or D) is not responding to commands sent to it by the program. Check power and cable connections to the hard disk.

NOTE

The errors listed below may appear during operation.

5. **Undefined Error - Command Aborted** — An error condition has occurred which the program cannot identify.

6. **Address Mark Not Found** — The address mark (initial address) on the hard disk could not be found.

7. **Requested Sector Not Found** — The sector currently requested on the hard disk could not be found.

8. **Reset Failed** — The program issued a reset command to the hard disk, but this command did not properly reset the hard disk.

9. **Drive Parameter Activity Failed** — The program has sent a reset command to the controller, followed by the drive parameters. Using the parameters sent to it, the controller is not getting a response from the hard disk drive. Check to see if the drive type selected in the 'Standard CMOS Setup' is correct for the disk drive being used.

10. **Bad Sector Flag Detected** — The program has tried to perform an operation on a sector which has been flagged (i.e., marked as "bad").

11. **Bad ECC on Disk Read** — When the program attempts to write to the disk, it also calculates an ECC (Error Correction Code) value for the data being written. This ECC value is written to the drive and then read back. If the value read back is different from the one calculated, then, this error will occur.

12. **ECC Corrected Data Error** — The ECC value (explained above) read from the disk is not the same value which was written to the disk; therefore, the program assumes that the data is not correct. It, then, attempts to correct the data, but the ECC value is not corrected. In this situation, this message appears.

13. **Controller Has Failed** — The program has issued a diagnostic command to the controller, which has failed; therefore, the controller has failed as well.

14. **Seek Operation Failed** — The program has issued a seek command to the drive and this operation has failed. A seek operation is the act of finding a particular sector on the hard disk.

15. **Attachment Failed to Respond** — No response has been received from the hard disk drive. This message appears if an operation has already begun and the hard disk does not respond, when it has responded earlier.

16. **Drive Not Ready** — The program is trying to perform an operation on the hard disk drive, and it has waited beyond a preset specified time limit. This situation is known as "timeout."

17. **Write Fault on Selected Drive** — A 'Write Fault' has occurred during the write operation on the hard disk.

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