P5-PCI-VL

SYSTEM BOARD

Version 1 .O

USER'S *MANUAL*

P5-PCI-VL SYSTEM BOARD

Ver 1.0

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This manual contains information important for the successful installation and operation of the system board. Please read the information carefully and be sure that you understand it thoroughly before proceeding with installation.

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INTRODUCTION

The PS-PCI-VL supports both Intel Pentium 60/66 MM CPUs

Features:

* Cache controller:

    a. 16Kbytes of CPU internal cache memory

    b. Burst Mode Write-Back

    c. Secondary Cache from 0 to 256KB. 5l2KB, 1MB using SRAM (32 KB x 8.64KB x 8.128KB x 8 SRAMS respectively)

* 64-bit DRAM controller

    a. supports both Single Density and Double Density 72 pin SIMM modules

    b. Supports up to 128 MB of memory on board (using 256 KB x 32/36, 1MB x 32/36, 2 MB x 32/36,4 MB x 32/36, 8 MB x 32/36, 16 MB x 32/36 SIMM)

* AWARD PCI BIOS

* OPTi 82C596/597 and OPTi 82C822 surface-mounted chipset

* Three 32-bit PCI Local Bus slots

* Two 32-bit VESA Local Bus slots

* Four 16 bit ISA expansion slots

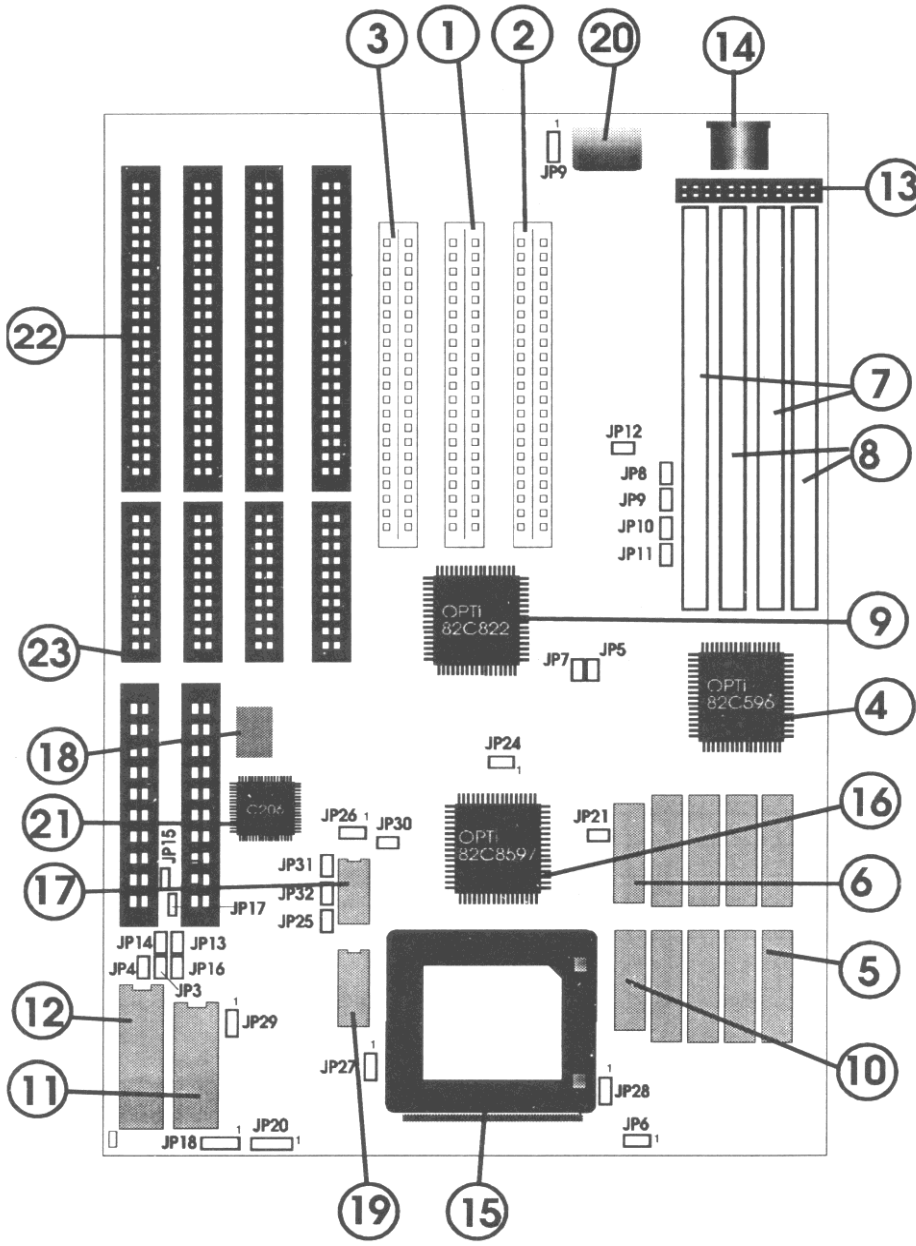
* Onboard Clock Generator facilitates CPU upgrades. Simply change jumpers to change CPU speed (no oscillators required).

A) Board Layout & Jumpers

This section provides an indication of the location of main system board components as well as a list of the jumpers on the motherboard

Number	Item
1	32-bit PCI Slots, slot #1
2	32-bit PCI Slots, slot #2
3	32-bit PCI Slots, slot #3
4	OPTi 82C596 Chip
5	SRAM Memory
6	TAG SRAM
7	SIMM Memory Bank 0
8	SIMM Memory Bank 1
9	OPTi 82C822 Chip
10	DIRTY SRAM
11	BIOS EPROM
12	Keyboard Controller
13	Power Connector
14	Keyboard Connector
15	Pentium ZIF Socket
16	OPTi 82C597 Chip
17	Clock Generator
18	Oscillator
19	PAL
20	Battery
21	82C206
22	16-bit ISA Slots
23	32-bit VESA Slot

Board Layout



Jumpers

The following list is a" overview of the system jumpers. More details on certain settings can be found in later sections.

POSITION	COMMENTS
JP6	Cache jumper
JP9	Always keep on
JP21	Cache jumper
JP25	Clock Frequency
JP26	Clock Frequency
JP27 1-2	For CPU fan
JP28 1-2	For system second fan
JP29	Flash BIOS Note: put jumper on only when reprogramming
JP30	Clock Frequency
JP31	Clock Frequency
JP32	Clock Frequency

Sl	Reset Connector
JP20	Keylock Connector
JPl8	Speaker connector

B) CPU Installation / Upgrade

The Central Processing Unit (CPU) is the brain of a computer. The CPU interprets and executes instructions and thereby controls the computer system. In micro-computers. the CPU is designed as a highly integrated chip called the micro-processor. The PS-PCI-VL incorporates only the best in micro-processor speed and technology. The following are CPUs and speeds available for the PS-PCI-VL.

PENTIUM™ - The P5-PCI-VL supports both **Pentium™** 60 and 66 MHZ. These processors use Pentium technology and include separate 16 KB code and data caches. Internally they may be clock doubled or tripled. A 273 pi" ZIP socket is included to house these processor.

For installation of a new CPU, or upgrade of a" existing CPU, observe the following **procedure** (ALWAYS "se a CSA approved grounding strap or other anti-static device):

1) Turn off the power.

2) Upgrading an existing CPU is easy with the ZIF (Zero Insertion Force) socket. Open the ZIF socket by moving the handle to the upright position, the old CPU is now free. Lift it straight out of the socket.

3) Align the new CPU with the socket (be sure all the pins on the CPU are aligned with the holes). One comer of the CPU is notched and marked with a round dot and you should align it with the pin one mark (white triangle on the board or alignment pins on the socket).

4) With the ZIF socket handle in the upright position set the CPU straight into the socket, it should drop in easily requiring no force. Make sore that all pins are folly inserted in the appropriate holes. Gently hold the CPU in place and push the handle to the closed position.

5) The P5-PCI-VL uses a clock generator to produce the system clock and simplifies processor upgrades. Set the jumpers to select the appropriate frequency, as outlined in the table on the following page.

CPU Clock Frequency

I. If AV9107-04 is mounted on the board, use the following table to set up the CPU speed.

Jumper	Frequency (MHz)		
	50	60	66
JP25	ON	OFF	ON
JP32	ON	OFF	ON
JP31	OFF	OFF	ON
JP30	ON	ON	OFF
JP26	2-3	1-2	2-3

II. If CH9007E is mounted on the board, use the following table to set up the CPU speed.

Jumper	Frequency (MHz)		
	50	60	66
JP25	OFF	OFF	OFF
JP32	ON	OFF	OFF
JP31	OFF	ON	ON
JP30	OFF	OFF	ON
JP26	2-3	2-3	2-3

C) Cache Installation / Upgrade

CACHE MEMORY In addition to the CPU internal cache, the PS-PCI-VL system board supports an optional, user-upgradeable, secondary cache of 0 KB, 256 KB, 512KB, 1MB. The increased speeds of microprocessors during the last few years have outpaced the development of DRAMS (DRAMS are used for system memory). Cache memory utilizes SRAM which is much faster than the DRAM used for system memory. Cache memory provides fast local storage for frequently accessed codes and data. Cache memory (SRAM) is used in tandem with main memory (DRAM) to enhance motherboard performance Frequently used codes and data are transferred from main memory and placed in cache memory (SRAM) thus allowing the system to function at a much higher rate of performance. System performance is improved by reducing bus cycles and increasing instruction throughput. The actual realized performance increase will depend on the particular applications used.

The P5-PCI-VL utilizes a Direct Map caching scheme with a Burst Mode Write-Back Cache controller. Direct Map is a common caching scheme whereby a segment of DRAM memory is directly reproduced in cache memory. Write-Back cache architecture is a scheme whereby the system will write modified data to the cache only. Main memory will NOT be updated until the system requires some new data that is NOT available in the cache. Standard Write-Through architecture is penalized during Writes because every time the system writes to cache it must also update the slower main memory. Therefore Write-Back is preferable to Write-Through.

The secondary cache utilizes SRAM (Static Random Access Memory) chips. There are a total of ten sockets for the secondary cache chips. Sockets U44. U48. U46, U50, U54, U56, U58, U60 comprise one bank. Socket U30 is the tag RAM and U52 is the Dirty RAM.

Tag RAM is used to store the address of the information that is in cache memory. The CPU looks at the tag RAM to see if the memory address for its required information is there. If the address is not found in the tag RAM, then the data is not in cache memory and the CPU must go to system memory for the data.

The Dirty RAM is used as a status indicator for true Write-Back cache. The system will poll the Ditty RAM when it needs to move new data into the cache. If it polls a set or ON status, then it will write the information out of the cache to main memory before loading new data. Otherwise OFF status indicates that the data in main memory is equivalent or just as current as that in cache and the system will directly load the new data that it requires.

For installation of cache memory, observe the following procedure (ALWAYS use a CSA approved grounding strap or other anti-static device):

1) Select the size of the cache desired and consult the following table to determine the size and quantity of chips required. The speed required will depend on the speed of the CPU. We recommend using top quality 15ns or faster SRAM.

SRAM REQUIREMENT

Total Cache	
256KB	32KB x 8 -15
512KB	64KB x 8 -15
1MB	128K x 8 15

TAG/DIRTY REQUIREMENT

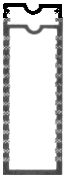
Use 32K x 8 15ns only

2) Turn off and unplug the system.

3) Set the appropriate jumpers according to the size of cache to be installed.

Jumper	256KB	512KB	1MB
JP6	OFF	OFF	ON
JP21	OFF	ON	ON

4) Insert the SRAM chips into the appropriate sockets. The notches in the chip must be aligned with the notches in the sockets. If 32K x 8-15ns using, place cache memory away from indent.



5) Update the BIOS settings using the advanced CMOS setup program. Enable the cache, select the proper Bunt rate and SRAM read and write wait states according to the instructions in the BIOS section. (Refer to the BIOS setup on page 17 for detail)

D) Memory Installation / Upgrade

Memory is used to hold information and programs while they are being accessed by the micro-processor. The P5-PCI-VL system board uses DRAM (Dynamic Random Access Memory) memory modules. The system board can support memory from 2MB to 128MB using various combinations of 256 KB x 32/36 (1 MB), 512 KB x 32/36 (2 MB), 1 MB x 32/36 (4 MB), 2 MB x 32/36 (8 MB), 4 MB x 32/36 (16 MB), 8 MB x 32/36 (32 MB), 16 MB x 32/36 (64 MB) SIMMs.

There are a total of four single/double density SIMM sockets on the system board. The DRAM controller supports both single density (~~one socket = one module = one bank~~) and double density (~~one socket = one module = 2 banks~~) SIMMs. Since the DRAM controller uses ~~64-bit~~ architecture, 2 pieces of 72 pin SIMM (32-bit) are required for one 64-bit bank. (Refer to layout on Pg. 6).

The following chart describes available memory configurations and the module type and quantity required for each configuration.

Total	Bank 0	Bank 1
2MB	256KB	-
4MB	512KB	-
8MB	1MB	-
16MB	2MB	-
32MB	4MB	-
64MB	8MB	-
4MB	256KB	256KB
6MB	256KB	512KB
8MB	512KB	512KB
10MB	256KB	1MB
12MB	512KB	1MB
16MB	1MB	1MB
18MB	256KB	2MB
20MB	512KB	2MB
24MB	1MB	2MB
32MB	2MB	2MB
34MB	256KB	4MB
36MB	512KB	4MB
40MB	1MB	4MB
48MB	2MB	4MB
64MB	4MB	4MB
66MB	256KB	8MB
68MB	512KB	8MB
72MB	1MB	8MB
80MB	2MB	8MB

Total	Bank 0/1	Bank 2/3
96MB	4MB	8MB
128MB	8MB	8MB

Double Density SIMM	Single Density SIMM
512KBx32/36=2MB	1 MB x 32/36 = 4 MB
2MBx32/36=8MB	4 MB x 32/36 = 16 MB
8 MB x 32/36 = 32 MB	16MBx32/36=64KB

Note: 32/36 32 stands for 32-bit (without parity)
36 stands for 36-bit (with parity)

SIMM INSTALLATION:

To install a SIMM, observe the following procedure(ALWAYS use a CSA approved grounding strap or other anti-static device):

1) Turn off and unplug the system.

2) Align the module with the socket so that pin 1 on the module is toward the keyboard connector and the edge connector is facing the socket.

3) Keep the module at a 70 degree angle to the board and carefully insert the edge connecter into the socket. Confirm that the SIMM is evenly seated in the socket.

4) Carefully push the module to a vertical position, until it clips into the metal latch on the socket assembly. The metal latch will hold the module fully in place. Double check that the module is properly installed.
NOTE: Excessive force will damage the SIMM sockets, and void the warranty.

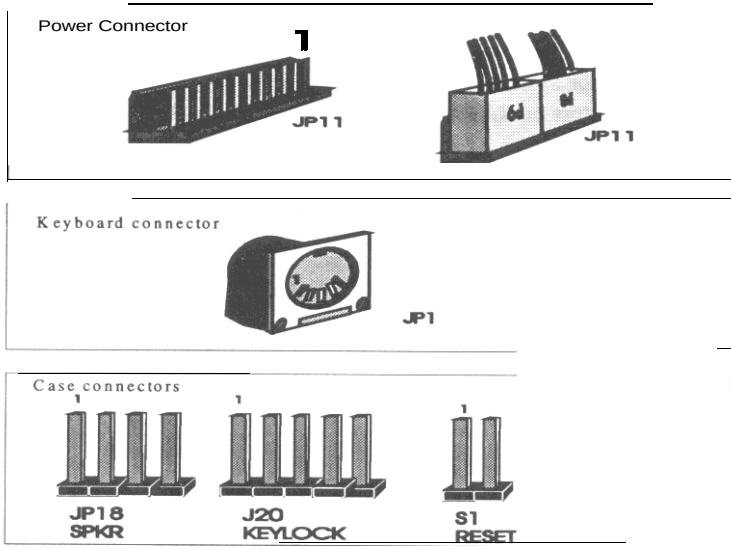
5) To remove a SIMM module, carefully pry the metal latch away from each end of the module. The module should flip forward and can be lifted out.
NOTE: Excessive force will damage the SIMM sockets, and void the warranty.

The system board will automatically recognize the memory. No jumper changes are necessary but you must save the changes using the advanced CMOS setup program. Simply to acknowledge and save the new configuration.

E) Connectors

After setting the jumpers, installing CPU, cache SRAM, and Memory DRAM, the next step is to install the system board in the case and make the proper case connections. There are five connectors on the P5-PCI-VL system board. Refer to the figure on the next Page.

Connectors	Pin	Description
Reset Switch S1	1	Ground
	2	Reset in
Power LED I Keylock J20	1	+5v
	2	NC
	3	Ground
	4	Keylock
	5	Ground
Speaker JP18	1	Data out
	2	NC
	3	Ground
	4	+5v
Power Connectors J10/J11	1	Power good
	2	+5v
	3	+12v
	4	-12v
	5	Ground
	6	Ground
	7	Ground
	8	Ground
	9	-5v
	IO	+5v
	11	+5v
	12	+5v
Keyboard Connectors ... J1	1	Keyboard clock
	2	Keyboard data
	3	NC
	4	Ground
	5	KBD power



It is imperative that the power connectors be secured in the proper configuration Failure to do so could cause damage to the board at power up.

F) CHIPSET FEATURES:

BUS ARCHITECTURE PS-PCI-VL has two 32-bit VESA Local Bus slots. four 16-bit ISA Bus slots, and three 32-bit PCI slots. The ISA bus offers an 8 or 16-bit data path and is normally run at 8 MHz. The Local Bus provides full 32-bit data path and operates at the same speed as the system speed. Local Bus peripheral devices can be bus-master or bus-slave. Local bus offers a significant performance advantage over the standard 8/16-bit ISA Bus. PC1 provides 33MHz transfer rate and burst transfer mode, and it gives high performance for the peripherals.

Note that many *VESA local* bus ***peripherals*** *run at a maximum of 33MHz.*

CHIPSET - For optimal control in interfacing or processing, the PS-PCI-VL system board features the OPTi 82C596/597/822 highly integrated chipset. This chipset minimizes the clutter and maximizes the integrity of the PS-PCI-VL system **board.**

The 82C596/597/822 controls the following functions:

(i) 82C596 (AT Controller ATC)

AT bus controller
Data bus controller
- Data bus buffer (HD <-> MD)
Data bus buffer control (LD/SD <-> MD)
Parity generation and detection circuitry
Keyboard controller chip select
-Local bus interface (ISA bus <--> local bus command translation)

The ATC contains the AT bus controller, the buffer interface between the HD and MD bus, the buffer control logic to steer the LD/SD <--> MD buses, parity generation and detection logic and ISA <-> local bus command translation circuitry.

(ii) 82C597 (System Controller -SYSC):

Pentium CPU interface
DRAM controller
- L2 cache controller
Ll cache control
Local bus interface
Reset generation
Arbitration logic
Data bus buffer control (MD –> HD, HD –> MD)
Extended DMA page register

Keyboard emulation of A20M# and CPU warm reset
Port B and Port 92h register

The SYSC provides the control functions for the host CPU interface, local bus interface, L2 cache and 64-bit DRAM control. It also provides the buffer control signals to steer the HD <-> MD bus. It interprets and translates cycles from the CPU, local bus master, ISA master and DMA to the host memory (DRAM/L2 cache), local bus slave, or ISA bus devices. The SYSC contains an extensive register set to provide maximum programmability for all DRAM, cache and system performance attributes.

(iii) 82C822 (PCIB)

-Fully compliant to the PC1 V.20 Specification
Provides central arbiter to arbitrate the bus requests between:
host CPU
PCI masters
DMA/lSA masters
Refresh
Offers programmable priority scheme for both the central arbiter and DMA channels:
Fixed
- Rotating
Fixed/Rotating combination
Burst mode PCI accesses to local memory support
Combine host CPU sequential writes into PCI burst write cycles

G) BIOS Setup

After the board has been properly upgraded, configured, and connected and all peripherals have been installed I/O controller, VGA card, floppy drives. hard drives etc.), then it is time to power up.

At power up, press DEL if you want to run setup utility.

After hitting the 'DEL' key, the BIOS setup program main menu will be displayed.

Choose the following options:

1) Standard CMOS Setup

Choose the 'Standard CMOS Setup' option from the main menu. Hit 'Return' key to clear the waning screen. Use the "Page Up" and "Page Down" and arrow keys to move around and make modifications to the information. The available options for configuration are:

a) Set the Time and Date

b) Set the hard disk parameters

If you have no hard disk, choose NONE,

- If you have one hard disk, configure Hard Disk C: for the correct type of the drive that you are using.

If you have two hard disks, both Hard Disk C: and D: must be configured.

Consult your dealer/supplier for the hard disk(s) type(s) or parameter(s).

c) Choose your floppy drive(s):

The available options are: 36OKB. 1.2KB. 72OKB. 1.44KB. 2.88KB. and not installed.

d) Set the display type

VGA/PGA/EGA, Color80X25, Monochrome. and not installed.

e) Set the error type:

Set this to ALL ERRORS

After you have selected the necessary options for your particular configuration, hit 'ESC' key to return to the main menu.

The information in the following two sections are to fine tune the system board's performance. Most of the options will be standard across all possible motherboard configurations.

2) BIOS Feature Setup

ROM PCI/ISA BIOS (2A5U1SA0)
BIOS FEATURES SETUP
AWARD SOFTWARE INC.

Virus Warning	Disabled
CPU Internal Cache	Enabled
External Cache	Enabled
Quick Power On Self Test	Disabled
Boot Sequence	A,C
Swap Floppy Drive	Disabled
Boot Up Floppy Seek	Enabled
Boot Up Numlock Status	On
Boot Up System Speed	High
IDE HDD Block Mode	Enabled
Gate A20 Option	Fast
Typematic Rate Setting	Disabled
Typematic Rate (Chars/Sec)	6
Typematic Delay (Msec)	250
Security Option	Setup

System BIOS Shadow	Enabled
Video BIOS Shadow	Enabled
C8000-CBFFF Shadow	Disabled
CC000-CFFFF Shadow	Disabled
D0000-D3FFF Shadow	Disabled
D4000-DFFF Shadow	Disabled
D8000-DBFFF Shadow	Disabled
DCCO-DFFFF Shadow	**Disabled**
E0000-E3FFF Shadow	**Disabled**

ESC	: Quit	↑↓→←	: Select Item
F1	: Help	PU/PD/+/-	: Modify
F5	: Old Value	(Shift)F2	: Color
F6	: Load BIOS Defaults		
F7	: Load Setup Defaults		

3) Chips.5 Feature Setup (For Pentium 60/66MHz and all different Cache size)

ROM PCI/ISA BlOS (2A5U1SAO)
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.

Auto Configuration	: Disabled
Row Address Hold in CLKs	:2
RAS Pulse Width in CLKs	:5
CAS Read Width in CLKs	:3
CAS Write Width in CLKs	:3
RAS Precharge in CLKs	:5
CAS Precharge in CLKs	:2
DRAM Post Write	:Enabled
CPU Address Pipelining	:Disabled
L1 Cache Write Policy	:Write Back
L2 Cache Write Policy	:Write Back
Cache Write Burst Mode	:4-2-2-2
Cache Read Burst Mode	:3-2-2-2
Video BIOS Cacheable	:Enabled
System BIOS Cacheable	:Enabled

Memory Hole at 512-640K	:Disable
Hidden Refresh	:Enabled
LGNT# Synchronous to LCK	:Disable

ESC	: Quit	↑↓→←	: Select Item
F1	: Help	PU/PD/+/-	: Modify
F5	: Old Value	(Shift)F2	: Color
F6	: Load BIOS Defaults		
F7	: Load Setup Defaults		

4) PCI Feature Setup

ROM PCI/ISA BIOS (2A5U1SA0)
PCI CONFUGURATION SETUP
AWARD SOFTWARE. INC.

*

Slot 1 Using INT# : A ** INTA# Connect IRQ : Disabled INTB# Connect IRQ : Disabled INTC# Connect IRQ : Disabled INTD# Connect IRQ : Disabled Slot 2 Using INT# : A INTA# Connect IRQ : Disabled INTB# Connect IRQ : Disabled INTC# Connect IRQ : Disabled INTD# Connect IRQ : Disabled Slot 3 Using INT# : A INTA# Connect IRQ : Disabled INTB# Connect IRQ : Disabled INTC# Connect IRQ : Disabled INTD# Connect IRQ : Disabled	Slot 4 Using INT# : A INTA# Connect IRQ : Disabled INTB# Connect IRQ : Disabled INTC# Connect IRQ : Disabled INTD# Connect IRQ : Disabled Assert LDEVO# For VL : Disable PCI Bus Clock : Async PCI/VGA Snooping : Auto ESC : Quit ↑↓→← : Select Item F1 : Help PU/PD/+/- : Modify F5 : Old Value (Shift)F2 : Color F6 : Load BIOS Defaults F7 : Load Setup Defaults

*For IRQ information, consult your PCI peripherial card manual

**Slot #4, not available.

Glossary

BIOS:(Basic Input Output System) Program usually contained in a ROM chip or flash device on the system board that is the interface between the system hardware and the operating system.

The ROM BIOS is a group of low level programs responsible for interfacing the computer to peripheral devices, such as disk drives, serial and parallel ports, keyboard, and video display. Low-level BIOS routines are common to all operating systems and are generally resident in ROM. Higher-level BIOS routines are specific to the particular operating system in use and are therefore generally stored on disk, and loaded only when the operating system is booted.

BIT: A binary digit that is the most reducible element of computer information. Eight bits make one byte.

BOOT or BOOTSTRAP: A small ROM-based program which is automatically loaded when the system is first powered up (or "booted"), in order to load and execute an operating system or other large program from disk. Also, the process of stating the computer, either by turning on the power, hitting the Reset switch or by pressing the CTRL + ALT + DEL keys simultaneously. The latter is known as a "warm boot".

BYTE: Smallest unit of storage required to hold a character of information in memory or on a disk.

BUS CLOCK: The speed at which data is transferred between the microprocessor and the I/O channel

CMOS: Acronym for Complimentary Metal Oxide Semiconductor. CMOS integrated circuitry uses very little electrical power. Hence CMOS RAM is ideal for storing system configuration information that cannot be stored permanently in ROM.

CONVENTIONAL MEMORY: System main memory from 0 to 640KB. Many programs run in this area.

CPU (CENTRAL PROCESSING UNIT): Also called the micro-processor. The "brain" of the computer, where program instructions and arithmetic operations are executed.

CPU CLOCK: The speed at which the microprocessor executes its instructions.

DOS (DISK OPERATING SYSTEM): Software that controls the activities performed by the computer. DOS sets up an environment under which application software can load and function. It is an interface between the system and application software.

DRAM (DYNAMIC RANDOM ACCESS MEMORY): A type of RAM that requires a refresh cycle to keep information valid. Main system memory uses DRAM.

EXPANSION SLOT: a connector on the system board into which an adapter card can be inserted.

EXTENDED MEMORY: memory beyond the 1MB limit that is accessed by programs such as Windows.

INTERFACE: The connection between the system board and a peripheral

INTERLEAVING: A technique for improving system performance by speeding up memory access. Successive memory locations are assigned to different memory banks. Then when the system requires the information it accesses both banks in less clock cycles and therefore, the system runs faster.

ISA: Industry Standard Architecture.

JUMPER: A patch cable, wire or other such device used to establish a circuit.

MEMORY: RAM and ROM are devices used to hold information and programs while they are being accessed by the system.

MICROPROCESSOR: Also known as the CPU. The "brain" of the system, which contains the circuitry used for calculation and communication with the rest of the system.

PAGE MODE: Special function in DRAM that saves cycle time by not n-loading the Row Address strobe bits.

PARITY BIT: An additional non-informational bit appended to a group of 8 bits to make the number of ones in the group of bits either even or odd. This is an elementary error correction mechanism. Example: During a subsequent read from a memory location, and using odd parity, the system will check the sum of ones. If the sum of ones is NOT still odd then system knows that the information at that location has been corrupted.

PCI: Peripheral Component Interface. At 33MHz, the synchronous PCI Local Bus transfers 32 bits of data at up to 132 MB/sec

PGA (Pin Grid Array): This refers to CPU, and other similar components, that are installed in sockets on the system board. PGA CPU have rows of pins sticking out underneath.

SHADOW RAM: Refers to the technique of copying BIOS routines from slower ROM chips to faster RAM, thereby increasing system performance.

VESA: Video Electronics Standard Association.

VL-BUS: VESA local bus. An architectural, timing. electrical and physical interface that allows high-speed peripheral device to interface, either directly or indirectly, to the local bus of the host CPU. The specification of VL-BUS is available from VESA.

WRITE BACK CACHE: Cache architecture in which wires of new information by the CPU to cache are NOT accompanied by writes to update system memory. The advantage over Write-Through cache is that the system does not have to wait for the slower main memory. However, main memory has not been updated, therefore a penalty will be incurred during read misses. A read miss occurs when the CPU can not find the information it requires in cache memory and must go to system memory for another block of information. However, before transfer of new information into the cache, the current content of the cache must be saved to system memory or the updated information in the cache will be lost.

WRITE THROUGH CACHE: Cache architecture in which writes by the CPU to system cache are accompanied by writes to update system DRAM memory as well. The penalty is that the system must wait for the slow system memory to receive and store the data. The advantage of this architecture is that during read misses no penalty is incurred as in Write Back cache.