P55-IT Layout

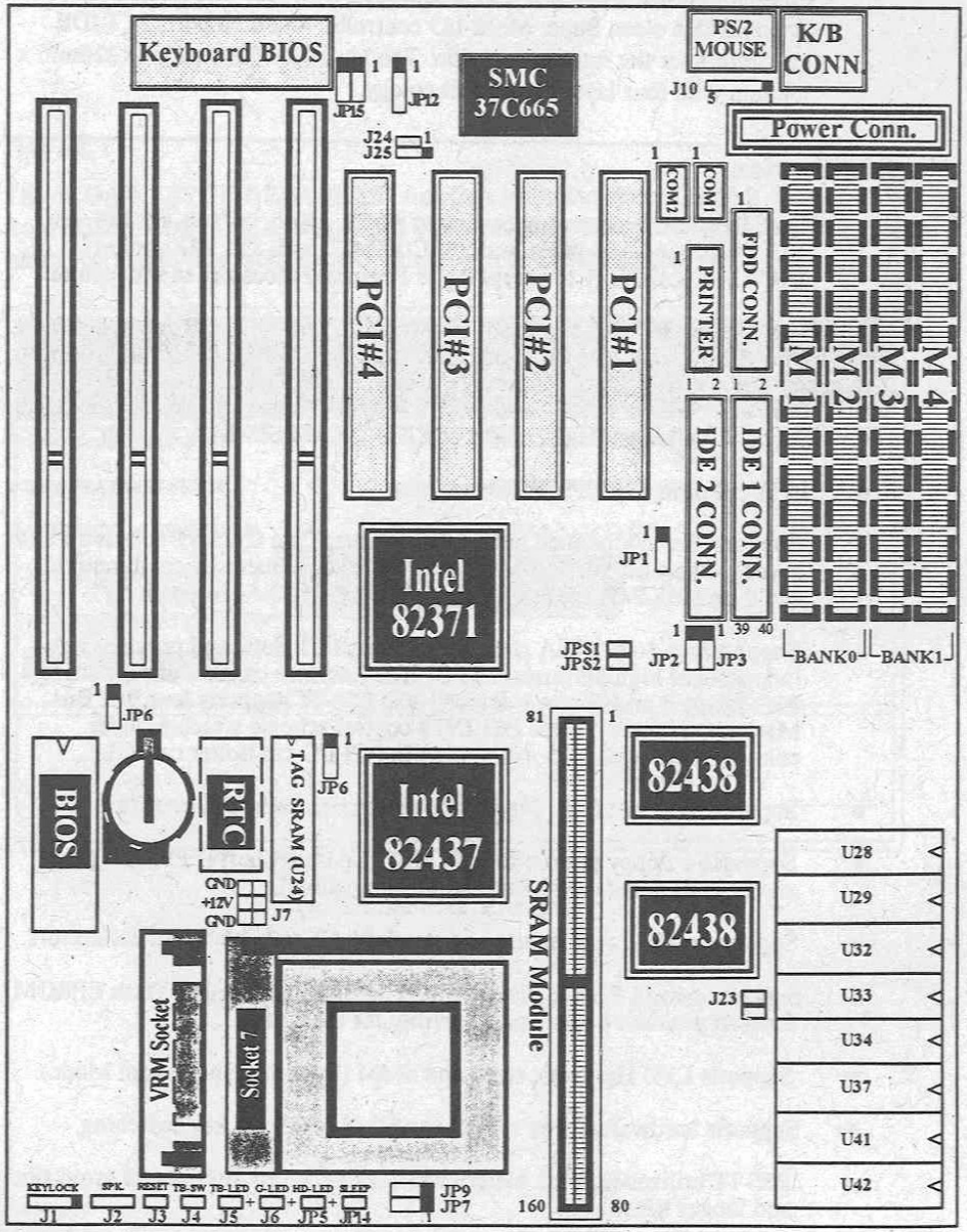


Figure 1-1

Chapter 2
Hardware design

2-1 Motherboard Layout

The P55-IT is designed with Intel Triton 82430FX PCIset chipset which is developed by INTEL Corporation to fully support Intel Pentium PCI/ISA system. The Intel "Triton" 82430FX PCIset chipset prpovides increased integration and improved performance designs. The "Triton" chipset provides an integrated IDE controller with two high performance IDE interfaces for up to four IDE devices (hard devices, CD-ROM device, etc). The SMC (STANDARD MICROSYSTEMS CORPORATION) FDC37C665GT Super I/O controller provides the standard PC I/O function: floppy interface (up to 2.88 MB), two 16 Byte FIFO serial ports and EPP/ECP capable parallel port. The **P55-IT** layout is shown in previous page (left page) for user's reference. **Care must be taken** when inserting memory modules, inserting Intel **P54C/P55C/P55CT** processor, inserting **VRM(Voltage Regulator Module)** or even plugging PCI card into associated slots to avoid damaging any circuits or sockets on board. A cooling fan is strongly recommended when installing P54C/P55C processor due to possible overheat.

The P55-IT supports minimum of 8MB of System Memory and maximum of 128MB while L2 Cache can be 256KB/512KB synchronous (The **COAST "Cache-On-A-STick"** solution) or asynchronous SRAM to increase system performance.(refer to **Page 2-5 Cache Memory Configuration** for the details.)

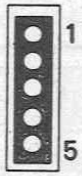
The P55-IT support standard Fast Page or EDO (Extended Data Out or Hyper Page Mode) DRAM. The EDO DRAM is designed to improve the DRAM read performance (When L2 Cache is asynchronous SRAM and not installed). **The P55-IT** provides four 72-pins SIMM sites for memory expansion. The socket support 1M x 32(4MB), 2M x 32(8MB), 4M x 32(16MB), and 8M x 32(32MB) single-sided or double-sided SIMM modules. The memory timing requires 70 nS Fast page devices or 60 nS EDO DRAM. Memory parity generation and checking is not supported. (DRAM Modules may be parity[x 36] or non-parity[x 32].

The P55-IT supports **Onboard two PCI IDE** connectors, and detects IDE harddisk type by BIOS utility automatic.

The P55-IT supports Award Plug & Play BIOS for the ISA and PCI cards. The BIOS can be located in Flash EPROM. The advantage of having Flash EPROM is much easier to replace BIOS code if necessary.

2-2 Connectors and Jumpers

This section describes all of the connectors and jumpers equipped in the motherboard. Please refer to **Figure 1-1** for actual location of each connector and jumper.

J1 

KeyLock - Keyboard lock switch & Power LED connector.
1.Power LED(+)
2.N/C
3.GND
4.Keylock
5.GND

J2 

Speaker - connect to the system's speaker for beeping.
1. Speaker
2. N/C
3. GND
4. GND

J3 

Reset - Close to restart system.

J4 

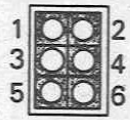
Turbo Switch : Open for slower speed while Close for higher speed. A BIOS hot key <CTRL><ALT><+> also brings system to a higher speed while<CTRL> <ALT><-> set system to a slower speed(When J4 is open.).

J5 

Turbo LED indicator - LED ON when higher speed is selected.

J6 

Power Saving LED indicator - LED ON when system is in any Saving mode.

J7 

The Power supply of the CPU cooling fan
1,2 GND
3,4 +12V
5,6 GND

JP5 

IDE LED indicator - LED ON when Onboard PCI IDE Harddisks activites.

JP1 

CPU Install : 1-2 for Intel Pentium P54C, P54CS CPU (Default).
2-3 for Intel Pentium P55C/P55CT CPU.

JP2 

Onboard IDE 1: 1-2 for Primary IDE 1 Interrupt IRQ14.
2-3 for None

JP3 

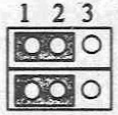
Onboard IDE 2 : 1-2 for Secondary IDE 2 Interrupt IRQ15.
2-3 for None

JP14 

Sleep/Resume switch : Close to enter sleep mode.
A keystrobe or mouse movement (mouse driver exists). The system will instantly "wake up".

J24 

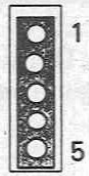
Onboard SMC's chip select :
Open: Normal operation.(Default)
Close: Disable the Onboard SMC chip.

JP15 

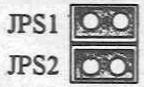
Keyboard Operation Clock Select :
1-2 The clock rate is depend on the system AT CLOCK (J25). (Default)
2-3 The clock rate is 12MHz.

JP6 

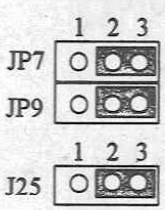
EPROM BIOS Select : 1-2 for 5V Flash EPROM (Default)
while 2-3 for 12V Flash EPROM.

J10 

PS/2 MOUSE CONNECTOR:
1.RED wire
2.BLUE wire
3.GREEN wire
4.NC
5.YELLOW wire

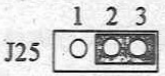


Clock chip is IMI SC484					
Clock/CPU Op.	JPS1	JPS2	JP7	JP9	J25
50/75 MHz	OPEN	OPEN	2-3	2-3	1-2
60/90 MHz	CLOSE	OPEN	2-3	2-3	2-3
66/100 MHz	CLOSE	CLOSE	2-3	2-3	2-3
60/120 MHz	CLOSE	OPEN	1-2	2-3	2-3
66/133 MHz	CLOSE	CLOSE	1-2	2-3	2-3
60/150 MHz	CLOSE	OPEN	1-2	1-2	2-3
66/166 MHz	CLOSE	CLOSE	1-2	1-2	2-3



* Clock is System Clock.

* CPU OP. is CPU operation at 75, 90, 100 MHz, etc.



System AT BUS CLOCK Select:

1-2 ATCLK is devided **PCICLK*** by 3.

2-3 ATCLK is devided **PCICLK*** by 4.(Default)

* **PCICLK** = System Clock / 2

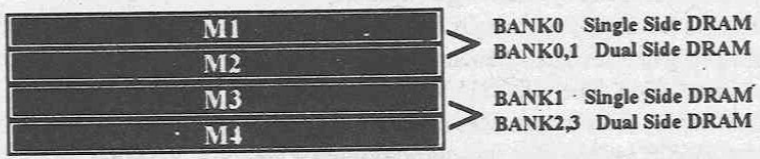
If system is operating at 66/100 MHz, than **PCICLK** is 33Mhz.

JP7	JP9	CLOCK Chip Frequency.
2-3	2-3	x (1.5) (Default)
1-2	2-3	x (2)
2-3	1-2	x (3)
1-2	1-2	x (2.5)

* The **JP7 and JP9** be used to setting the faster Pentium Processor in the feature.

2-3 System Memory Configuration

The P55-IT supports different type of settings for the system memory. There is no jumper nor connector needed for memory configuration. Following figures provides all possible memory cominations.



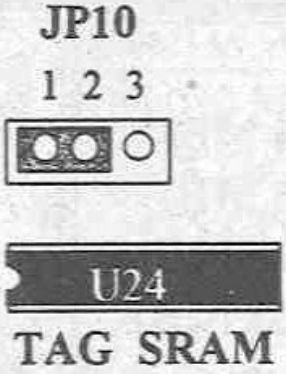
M1,M2(BANK 0)	M3,M4(BANK 1)	Total Size
1M x 32 (4 MB)	Empty	8MB
1M x 32 (4 MB)	1M x 32 (4 MB)	16MB
1M x 32 (4 MB)	2M x 32 (8 MB)	24MB
1M x 32 (4 MB)	4M x 32 (16 MB)	40MB
1M x 32 (4 MB)	8M x 32 (32 MB)	72MB
2M x 32 (8 MB)	Empty	16MB
2M x 32 (8 MB)	1M x 32 (4 MB)	24MB
2M x 32 (8 MB)	2M x 32 (8 MB)	32MB
2M x 32 (8 MB)	4M x 32 (16 MB)	48MB
2M x 32 (8 MB)	8M x 32 (32 MB)	80MB
4M x 32 (16 MB)	Empty	32MB
4M x 32 (16 MB)	1M x 32 (4 MB)	40MB
4M x 32 (16 MB)	2M x 32 (8 MB)	48MB
4M x 32 (16 MB)	4M x 32 (16 MB)	64MB
4M x 32 (16 MB)	8M x 32 (32 MB)	96MB
8M x 32 (32 MB)	Empty	64MB
8M x 32 (32 MB)	1M x 32 (4 MB)	72MB
8M x 32 (32 MB)	2M x 32 (8 MB)	80MB
8M x 32 (32 MB)	4M x 32 (16 MB)	96MB
8M x 32 (32 MB)	8M x 32 (32 MB)	128MB

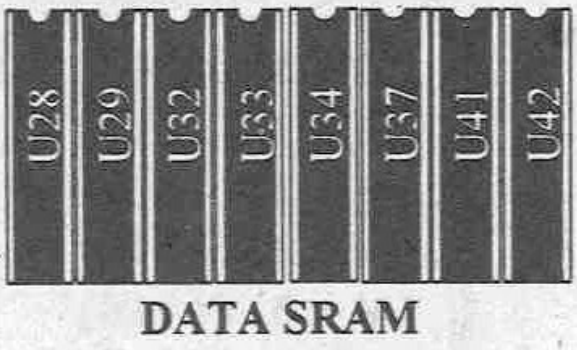
NOTE :

1. **P55-IT support both Fast Page DRAM or EDO DRAM SIMMs, but they cannot be mixed within the same memory bank.**
2. **SIMMs may be parrity(x 36) or non parity (x 32).**
3. **The 70nS Fast Page Mode or 60nS EDO DRAM is necessary.**
4. **"BANK' = 64 Bit = M1, M2 = M3, M4**

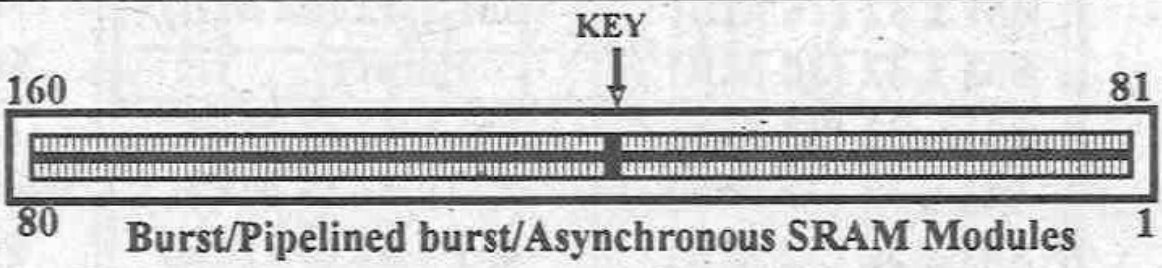
2-4 Cache Memory Configuration

The second level (L2) of cache is installed in the motherboard to increase the system performance. The **P55-IT** supports different type of combinations for the cache installation. The **COAST (Cache-On-A-STick. The cache modules has a TAG SRAM.)** solution provides Onboard flexibility, allowing Onboard to accommodate 256KB and 512KB asynchronous, burst and piplined burst SRAM modules. Jumper JP10 settings is used to Onboard's DIP asynchronous SRAM for differential such combinations. Please refer to following configurations for the details.





CACHE Size	TAG SRAM (U24)	Data SRAM Install	Jumper Setting JP10
256KB	8K8 x 1 or 16K8 x 1 or 32K8 x 1	32K8 x 8 U28,29,32,33 U34,37,41,42	1-2
512KB	16K8 x 1 or 32K8 x 1	64K8 x 8 U28,29,32,33 U34,37,41,42	2-3



Note: When you have a cache module to plug into a 160-pin daul readout connector. You must make sure that cache modules has a TAG SRAM(**Care must be taken** when you inserting the modules. If you can't sure whether that is a **COAST** solution modules or not. Please contact the modules supplier to avoid **burned-out and damaging** any modules circuits.) and take off the Onboard's DIP asynchronous DATA and TAG SRAM. The BIOS can auto-detect the type and size of the SRAM modules on display System Configurations before the system boots Operating System.