P54CVIP

SYSTEM BOARD

Version 1.1

USER'S MANUAL

P54CVIP SYSTEM BOARD

Ver 1.1

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A) Board Layout & Jumpers

This section provides an indication of the location of main system board components as well as a list of the jumpers on the motherboard .

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1	32-bit PCI Slots, slot #1
2	32-bit PCI Slots, slot #2
3	32-bit PCI Slots, slot #3
4	32-bit PCI Slots, slot #4
5	SRAM Memory
6	TAG SRAM
7	SIMM Memory Bank 0
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9	OPTi 82C822 Chip
10	DIRTY SRAM
11	BIOS EPROM
12	Keyboard Controller
13	Power Connector
14	Keyboard Connector
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16	OPTi 82C547 Chip
17	Clock Generator
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19	82C206
20	Battery
21	82C606
22	82C606
23	82C546
24	16-bit ISA Slots
25	32-bit VESA Slot
26	Heat Sink and regulator

Jumpers

The following list is an overview of the system jumpers. More details on certain settings can be found in later sections.

POSITION		COMMENTS
JP3	OFF	Fast VL-BUS Disable
	ON	Fast VL-BUS Enable
JP4	1-2	5V Flash Memory
	2-3	12V Flash Memory
		LCLK/5 LCLK/4 LCLK/3 LCLK/2
JP13		ON OFF ON OFF
JP14		ON ON OFF OFF
JP15	ON	Back to Back I/O Delay Fast
	OFF	More Delay Slow
JP18	ON	LDEV sample at End of Second T2
	OFF	LDEV sample at End of First T2
JP20	1-2	Always Invalidate L1 Cache
	2-3	Invalidate L1 Cache on Write Only
JP32	1-2	128MB DRAM on Board Running UNIX
	2-3	Memory Mapping I/O at Top of Memory
JP33		CPU BUS/Core Ratio
	1/2	ON
	2/3	OFF

Please set below jumpers as following position:
JP1=2-3, JP2=OFF, JP7=OFF, JP8=OFF, JP12=OFF, JP16=1-2,
JP17=ON, JP21=2-3, JP22,23,24,26=OFF, JP25=ON, JP27=OFF, JP31=1-2

S1	Reset Connector
J17	Keyboard
J18	External Battery

CPU Clock Frequency

I. If MK1432 is mounted on the board, use the following table to set up the CPU speed.

Jumper	Frequency (MHz)		
	75	90	100
JP5	1-2	1-2	1-2
JP6	OFF	OFF	ON
JP9	ON	OFF	OFF
JP10	OFF	OFF	OFF
JP11	2-3	2-3	2-3

II. If 9154A-42 is mounted on the board, use the following table to set up the CPU speed.

Jumper	Frequency (MHz)		
	75	90	100
JP5	1-2	1-2	1-2
JP6	OFF	ON	ON
JP9	OFF	ON	OFF
JP10	OFF	OFF	OFF
JP11	2-3	2-3	2-3

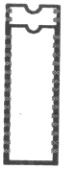
C) Cache Installation / Upgrade

CACHE MEMORY - In addition to the CPU internal cache, the P54CVIP system board supports an optional, user-upgradeable, secondary cache of 256 KB, 512KB. The increased speeds of microprocessors during the last few years have outpaced the development of DRAMs (DRAMs are used for system memory). Cache memory utilizes SRAM which is much faster than the DRAM used for system memory. Cache memory provides fast local storage for frequently accessed codes and data. Cache memory (SRAM) is used in tandem with main memory (DRAM) to enhance motherboard performance. Frequently used codes and data are transferred from main memory and placed in cache memory (SRAM) thus allowing the system to function at a much higher rate of performance. System performance is improved by reducing bus cycles and increasing instruction throughput. The actual realized performance increase will depend on the particular applications used.

The P54CVIP utilizes a Direct Map caching scheme with a Burst Mode Write-Back Cache controller. Direct Map is a common caching scheme whereby a segment of DRAM memory is directly reproduced in cache memory. Write_Back cache architecture is a scheme whereby the system will write modified data to the cache only. Main memory

4) Insert the SRAM chips into the appropriate sockets. The notches in the chip must be aligned with the notches in the sockets. If 32K x 8-15ns using, place cache memory away from indent.

5) Update the BIOS settings using the advanced CMOS setup program. Enable the cache, select the proper Burst rate and SRAM read and write wait states according to the instructions in the BIOS section. (Refer to the BIOS setup for detail)



D) Memory Installation / Upgrade

Memory is used to hold information and programs while they are being accessed by the micro-processor. The P54CVIP system board uses DRAM (Dynamic Random Access Memory) memory modules. The system board can support memory from 2MB to 128MB using various combinations of 256 KB x 32/36 (1 MB), 512 KB x 32/36 (2 MB), 1 MB x 32/36 (4 MB), 2 MB x 32/36 (8 MB), 4 MB x 32/36 (16 MB), 8 MB x 32/36 (32 MB), 16 MB x 32/36 (64 MB) SIMMs.

There are a total of four single/double density SIMM sockets on the system board. The DRAM controller supports both single density and double density SIMMs. Since the DRAM controller uses 64-bit architecture, 2 pieces of 72 pin SIMM (32-bit) are required for one 64-bit bank. (Refer to board layout picture).

The following chart describes available memory configurations and the module type and quantity required for each configuration.

Total	Socket 1	Socket 3	Soctet 2	Socket 4
2MB	256KB	-	256KB	-
4MB	512KB	-	512KB	-
8MB	1MB	-	1MB	-
16MB	2MB	-	2MB	-
32MB	4MB	-	4MB	-
64MB	8MB	-	8MB	-
4MB	256KB	256KB	256KB	256KB
6MB	256KB	512KB	256KB	512KB
8MB	512KB	512KB	512KB	512KB
10MB	256KB	1MB	256KB	1MB
12MB	512KB	1MB	512KB	1MB
16MB	1MB	1MB	1MB	1MB

The system board will automatically recognize the memory. No jumper changes are necessary but you must save the changes using the advanced CMOS setup program. Simply to acknowledge and save the new configuration.

E) Connectors

After setting the jumpers, installing CPU, cache SRAM, and Memory DRAM, the next step is to install the system board in the case and make the proper case connections. There are five connectors on the P54CVIP system board.

Connectors	Pin	Description
Reset Switch S1	1	Ground
	2	Reset in
Power LED / Keylock J17	1	+5V
	2	NC
	3	Ground
	4	Keylock
	5	Ground
Speaker J18	1	Data out
	2	NC
	3	Ground
	4	+5V
Power Connectors J3/J4	1	Power good
	2	+5V
	3	+12V
	4	-12V
	5	Ground
	6	Ground
	7	Ground
	8	Ground
	9	-5V
	10	+5V
	11	+5V
	12	+5V
Keyboard Connectors J1	1	Keyboard clock
	2	Keyboard data
	3	NC
	4	Ground
	5	KBD power

It is imperative that the power connectors be secured in the proper configuration. Failure to do so could cause damage to the board at power up.

- Arbitration logic
- Data bus buffer control (memory data to/from host data)
- Extended DMA page register
- Keyboard emulation of A20M# and CPU warm reset
- Port B and Port 92h register

(iii) 82C206 (IPC) Integrated Peripherals Controller

The 82C206 IPC provides two DMA controllers, two interrupt controllers, one timer/counter, and a real-time clock in an industry standard single-chip solution for the peripherals attached to the PC/AT peripheral bus.

- 84-pin PLCC or 100-pin PQFP
- Supports four DMA transfer modes
- Special Commands provided for ease of programming

(iv) 82C822 (PCIB)

- Fully compliant to the PCI V.20 Specification
- Provides central arbiter to arbitrate the bus requests between:
    - host CPU
    - PCI masters
    - DMA/ISA masters
    - Refresh
- Offers programmable priority scheme for both the central arbiter and DMA channels:
    - Fixed
    - Rotating
    - Fixed/Rotating combination
- Burst mode PCI accesses to local memory support
- Combine host CPU sequential writes into PCI burst write cycles

(v) 82C606

The 82C606A and 82C606B are two buffer/translation devices used to translate 3.3V signals to 5.0V signal levels in Python motherboard solutions.

-100-pin PQFP
- Mixed voltage to support 3.3V to 5.0V signal translation
- Two devices replace approxiamately eleven TTL devices

2) BIOS Feature Setup

ROM PCI/ISA BIOS (2A5UMSA0)
BIOS FEATURES SETUP
AWARD SOFTWARE, INC.

External Cache	: Enabled	Video BIOS Shadow	: Enabled
Boot Sequence	: A,C	C8000-CBFFF Shadow	: Disabled
		CC000-CFFFF Shadow	: Disabled
		D0000-D3FFF Shadow	: Disabled
		D4000-D7FFF Shadow	: Disabled
		D8000-DBFFF Shadow	: Disabled
		DC000-DFFFF Shadow	: Disabled
		E0000-EFFFF Shadow	: Disabled
IDE HDD Block Mode	: Disabled		
Security Option	: Setup		
		ESC : Quit	↑↓→← : Select Item
		F1 : Help	PU/PD/+/- : Modify
		F5 : Old Value	(Shift)F2 : Color
		F6 : Load BIOS Defaults	
		F7 : Load Setup Defaults	

3) Chipset Feature Setup

ROM PCI/ISA BIOS (2A5UMSA0)
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.

Auto Configuration	: Disabled	Memory Hole at 512-640K	:Disabled
Row Address Hold in CLKs	: 2	Hidden Refresh	:Enabled
RAS Pulse Width in CLKs	: 5	LGNT# Synchronous to LCK	:Disabled
CAS Read Width in CLKs	: 3		
CAS Write Width in CLKs	: 3		
RAS Precharge in CLKs	: 5		
CAS Precharge in CLKs	: 2		
DRAM Post Write	:Enabled		
CPU Address Pipelining	:Disabled		
L1 Cache Write Policy	:Write Back		
L2 Cache Write Policy	:Write Back		
Cache Write Burst Mode	:4-2-2-2		
Cache Read Burst Mode	:3-2-2-2	ESC : Quit	↑↓→← : Select Item
		F1 : Help	PU/PD/+/- : Modify
Video BIOS Cacheable	:Enabled	F5 : Old Value	(Shift)F2 : Color
System BIOS Cacheable	:Enabled	F6 : Load BIOS Defaults	
		F7 : Load Setup Defaults	

Troubleshooting

This section is intended as a general guide to solve configuration problems and to help pinpoint possible component failures. If after reading this section, an issue still can NOT be resolved, please contact your dealer.

AWARD BIOS performs various diagnostic tests at the time the system is powered up. Whenever an error is encountered during these tests, there will be either a few short beeps or an error message displayed on the monitor. If the error occurs before the display device is initialized, the system reports the error with several short beeps only.

If the error is fatal, the system halts after reporting the Fatal error. If the error is Non-fatal, the process continues after reporting the error.

Suggested courses of action are included in every section. Remember that these suggestions are guidelines only and are based on general experience. Also, ALWAYS power down and unplug the system before attempting any hardware changes.

Errors usually reported by BIOS

The following codes are reported by port 80 debug cards. If the system has a problem, a port 80 card will halt at the current attempted function. This information can be used to debug a problem system. Note that this is not recommended but only provided for reference.

Note: ISA POST coded are typically output to port address 80h.

POST (hex)	Name	Description
C0	Turn Off Chipset Cache	OEM Specific-Cache control
1	Processor Test 1	Processor Status Verification. Tests the following processor status flags carry zero, sign overflow. The BIOS will set each of these flags verify they are set, then turn each flag off and verify it is off.
3	Initialize Chips	Disable NMI, PIE, AIE, UEI, SQWV Disable video, parity checking DMA Reset math coprocessor Clear all page registers CMOS shutdown by byte Initialize timer 0, 1 and 2 Initialize DMA controllers 0 and 1 Initialize interrupt controllers 0 and 1

14	Test Timer Counter 2	Test 8254 Timer 0 Counter 2
15	Test 8259-Mask Bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines
16	Test 8259-2 Mask Bits	Verify 8259 Channel 2 masked interrupts by alternately turning off and on the interrupt lines
17	Test Stuck 8259's Interrupt Bits	Turn off interrupts then verify no interrupt mask register is on
18	Test 8259 Interrupt Functionality	Force an interrupt and verify the interrupt occurred
19	Test Stuck NMI Bits (Parity I/O Check	Verify NMI can be cleared
1A		Display CPU clock
20	Enable Slot 0	Initialize slot 0 (System Board)
21-2F	Enable Sits 1-15	Initialize slots 1 through 15
30	Size Base and Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB
31	Test Base and Extended Memory	Test base memory from 256K to 640K and extended memory above 1MB using various patterns
3C	Setup Enabled	
3D	Initialize & Install Mouse	Detect if mouse is present, initialize mouse, install interrupt vectors
3E	Setup Cache Controller	Initialize cache controller.
BF	Chipset Initialization	Program chipset registers with Setup values
40		Display virus protest disable or enable
41	Initialize Floppy Drive & Controller	Initialize floppy disk drive controller and any drives
42	Initialize Hard Drive & Controller	Initialize hard drive controller and nay drives
43	Detect & Initialize Serial/Parallel Ports	Initialize any serial and parallel ports (also game port)
45	Detect & Initialize Math Coprocessor	Initialize math coprocessor
4E	Manufacturing POST Loop or Display Messages	Reboot if Manufacturing POST Loop pin is set. Otherwise display any messages (i.e. any non-fatal errors that were detected during POST) and enter Setup
4F	Security Check	Ask password security (optional)

CMOS display type mismatch: indicates failure of display verification

Suggested Action: Check jumper for proper display setting and also check the CMOS setup for the proper display setting.

Error in Hard Disk Drive setup

Suggested Action: Run the standard CMOS setup and check that the parameters are correct for the installed hard drive(s). Also check all cable connections for proper orientation. Verify that the controller is properly seated in its expansion slot.

C:Drive error: indicates hard disk setup error

Suggested Action: Follow the procedure indicated for HDD controller failure.

C:Drive failure: indicates hard disk or hard disk controller failure.

Suggested Action: Follow the procedure indicated for HDD controller failure. Also try different cables.

OTHER PROBLEMS:

Power Supply Fan Stops Running - Turn off the power immediately and check to see if the system power has shorted to ground.

Power is on and the power supply is running but nothing happens: - check that the power supply is properly connected to the motherboard.

Diskette Error message: Try another diskette and check that the CMOS setting is correct.

Error Reading Fixed Disk: If all cables are properly connected and the CMOS is properly configured, then the indication is that the hard drive has failed.

No fixed disk present: This error indicates that the hard drive is improperly connected or configured.

DRIVE NOT READY ERROR
Insert BOOT Diskette in A:
Press any key when ready

The above message indicates the motherboard is unable to find a bootable disk (i.e. the motherboard is unable to load an operating system). Consult your operating system manual.

Non-system disk or disk error

Glossary

BIOS:(Basic Input Output System) Program usually contained in a ROM chip or flash device on the system board that is the interface between the system hardware and the operating system.

The ROM BIOS is a group of low level programs responsible for interfacing the computer to peripheral devices, such as disk drives, serial and parallel ports, keyboard, and video display. Low-level BIOS routines are common to all operating systems and are generally resident in ROM. Higher-level BIOS routines are specific to the particular operating system in use and are therefore generally stored on disk, and loaded only when the operating system is booted.

BIT: A binary digit that is the most reducible element of computer information. Eight bits make one byte.

BOOT or BOOTSTRAP: A small ROM-based program which is automatically loaded when the system is first powered up (or "booted"), in order to load and execute an operating system or other large program from disk. Also, the process of starting the computer, either by turning on the power, hitting the Reset switch or by pressing the CTRL + ALT + DEL keys simultaneously. The latter is known as a **"warm boot"**.

BYTE: Smallest unit of storage required to hold a character of information in memory or on a disk.

BUS CLOCK: The speed at which data is transferred between the microprocessor and the I/O channel

CMOS: Acronym for Complimentary Metal Oxide Semiconductor. CMOS integrated circuitry uses very little electrical power. Hence CMOS RAM is ideal for storing system configuration information that cannot be stored permanently in ROM.

CONVENTIONAL MEMORY: System main memory from 0 to 640KB. Many programs run in this area.

CPU (CENTRAL PROCESSING UNIT): Also called the micro-processor. The "brain" of the computer, where program instructions and arithmetic operations are executed.

CPU CLOCK: The speed at which the microprocessor executes its instructions.

DOS (DISK OPERATING SYSTEM): Software that controls the activities performed by the computer. DOS sets up an environment under which application software can load and function. It is an interface between the system and application software.

VL-BUS: VESA local bus. An architectural, timing, electrical and physical interface that allows high-speed peripheral device to interface, either directly or indirectly, to the local bus of the host CPU. The specification of VL-BUS is available from VESA.

WRITE BACK CACHE: Cache architecture in which wires of new information by the CPU to cache are NOT accompanied by writes to update system memory. The advantage over Write-Through cache is that the system does not have to wait for the slower main memory. However, main memory has not been updated, therefore a penalty will be incurred during read misses. A read miss occurs when the CPU can not find the information it requires in cache memory and must go to system memory for another block of information. However, before transfer of new information into the cache, the current content of the cache must be saved to system memory or the updated information in the cache will be lost.

WRITE THROUGH CACHE: Cache architecture in which writes by the CPU to system cache are accompanied by writes to update system DRAM memory as well. The penalty is that the system must wait for the slow system memory to receive and store the data. The advantage of this architecture is that during read misses no penalty is incurred as in Write Back cache.

DRAM (DYNAMIC RANDOM ACCESS MEMORY): A type of RAM that requires a refresh cycle to keep information valid. Main system memory uses DRAM.

EXPANSION SLOT: a connector on the system board into which an adapter card can be inserted.

EXTENDED MEMORY: memory beyond the 1MB limit that is accessed by programs such as Windows.

INTERFACE: The connection between the system board and a peripheral.

INTERLEAVING: A technique for improving system performance by speeding up memory access. Successive memory locations are assigned to different memory banks. Then when the system requires the information it accesses both banks in less clock cycles and therefore, the system runs faster.

ISA: Industry Standard Architecture.

JUMPER: A patch cable, wire or other such device used to establish a circuit.

MEMORY: RAM and ROM are devices used to hold information and programs while they are being accessed by the system.

MICROPROCESSOR: Also known as the CPU. The "brain" of the system, which contains the circuitry used for calculation and communication with the rest of the system.

PAGE MODE: Special function in DRAM that saves cycle time by not re-loading the Row Address strobe bits.

PARITY BIT: An additional non-informational bit appended to a group of 8 bits to make the number of ones in the group of bits either even or odd. This is an elementary error correction mechanism. Example: During a subsequent read from a memory location, and using odd parity, the system will check the sum of ones. If the sum of ones is NOT still odd then system knows that the information at that location has been corrupted.

PCI: Peripheral Component Interface. At 33MHz, the synchronous PCI Local Bus transfers 32 bits of data at up to 132 MB/Sec.

PGA (Pin Grid Array): This refers to CPU, and other similar components, that are installed in sockets on the system board. PGA CPU have rows of pins sticking out underneath.

SHADOW RAM: Refers to the technique of copying BIOS routines from slower ROM chips to faster RAM, thereby increasing system performance.

VESA: Video Electronics Standard Association.

Replace and press any key when ready

The above message indicates that the disk in drive A: is not bootable (i.e. it does NOT possess the operating system files). Consult your operating system manual.

DISKETTE BOOT FAILURE
Insert BOOT diskette in A:
Press any key when ready

The above message indicates that the disk in the drive is defective or not formatted.

Consult your operating system manual.

If problems persist, contact your dealer for technical support.

50	Write CMOS	Write all CMOS values back to RAM and clear screen
51	Pre-boot Enable	Enable parity checker Enable NMI. Enable cache before boot
52	Initialize Option ROMs	Initialize any option ROMs present from C8000h to EFFFFn. Note: When FSCAN option is enabled will initialize from C8000h to F7FFFn
53	Initialize Time Value	Initialize time value in 40h: BIOS area
60	Setup Virus Protect	Setup virus protect according to Setup
61	Set Boot Speed	Set system speed for boot
62	Setup NumLock	Setup Numlock status according to Setup
63	Boot Attempt	Set low stack Boot via INT 19b
B0	Spurious	If interrupt occurs in protected mode
B1	Unclaimed NMI	If unmasked NMI occurs, display Press F1 to disable NMI, F2 reboot
E1-EF	Setup Pages	E1-Page 1, E2-Page 2 etc
FF	Boot	

The preceding list is quite extensive. In most cases, running the setup program and configuring with the proper settings will resolve this issue. However, sometimes further action will be required:

Verify that all components, memory, CPU, cache, BIOS chips, etc. are properly installed and properly seated. If the problem persists, try another VGA adapter and try replacing the memory.

GENERAL DESCRIPTIONS:

CMOS battery state low: indicates failure of CMOS battery or failure in set and checksum tests

CMOS system options not set: indicates failure of CMOS battery, or failure in set and checksum tests.

Suggested Action: check and reconfigure the standard and advanced CMOS setups.

CMOS checksum failure: indicates CMOS battery low or a failure in the set and checksum tests

Suggested Action: Once again, run the BIOS setup program.
After changes, press F10 to save and exit.

4	Test Memory Refresh Toggle	RAM must be periodically refreshed in order to keep the memory from decaying. This function assures that the memory refresh function is working properly.
5	Black video. Initialize keyboard	Keyboard controller initialization.
7	Test CMOS Interface and Battery Status	Verifies CMOS is working correctly, detects bad battery.
BE	Chipset Default Initialization	Program chipset registers with power on BIOS defaults.
C1	Memory presence test	OEM Specific-Test to size on-board memory
C5	Early Shadow	OEM Specific-Early Shadow enable for fast boot
C6	Cache presence test	External cache size detection
8	Setup low memory	Early chip set initialization Memory presence test OEM chip set routines Clear low 64K of memory Test first 64K memory
9	Early Cache Initialization	Cyrix CPU initialization Cache initialization
A	Setup Interrupt Vector Table	Initialize first set interrupt vectors with SPURIOUS-INT_HDLR and initialize INT 00h-1fh according to INT_TBL
B	Test CMOS RAM Checksum	Test CMOS RAM checksum, if bad or insert key pressed load defaults
C	Initialize keyboard	Detect type of keyboard controller (optional) Set NUM LOCK status
D	Initialize Video Interface	Detect CPU clock Read CMOS location 14h to find out type of video in use Detect and initialize Video Adapter
E	Test Video Memory	Test video memory, write sign-on message to screen Setup shadow RAM - Enable shadow according to Setup
F	Test DMA Controller 0	BIOS checksum test Keyboard detect and initialization
10	Test DMA Controller	
11	Test DMA Page Registers	Test DMA Page Registers

4) PCI Feature Setup

ROM PCI/ISA BIOS (2A5UMSA0)
PCI CONFIGURATION SETUP
AWARD SOFTWARE, INC.

Slot 1 Using INT #	: Auto			
Slot 2 Using INT #	: Auto			
Slot 3 Using INT #	: Auto			
Slot 4 Using INT #	: Auto			
1st Available IRQ	: 9			
2nd Available IRQ	: 10			
3rd Available IRQ	: 11			
4th Available IRQ	: 12			
PCI IRQ Activated By	: Level			
PCI IDE IRQ Map To	: PCI-AUTO			
Primary IDE INT #	: A			
Secondary IDE INT #	: B			
Assert LDEVO# For VL	: Disable	ESC	: Quit	↑↓→← : Select Item
PCI Bus Clock	: Async	F1	: Help	PU/PD/+/- : Modify
PCI/VGA Snooping	: Auto	F5	: Old Value	(Shift)F2 : Color
		F6	: Load BIOS Defaults	
		F7	: Load Setup Defaults	

G) BIOS Setup

After the board has been properly upgraded, configured, and connected and all peripherals have been installed (I/O controller, VGA card, floppy drives, hard drives etc.), then it is time to power up.

At power up, press DEL if you want to run setup utility.

After hitting the 'DEL' key, the BIOS setup program main menu will be displayed.

Choose the following options:

1) Standard CMOS Setup

Choose the 'Standard CMOS Setup' option from the main menu. Hit 'Return' key to clear the warning screen. Use the "Page Up" and "Page Down" and arrow keys to move around and make modifications to the information. The available options for configuration are:

a) Set the Time and Date

b) Set the hard disk parameters
- If you have no hard disk, choose NONE.
- If you have one hard disk, configure Hard Disk C: for the correct type of the drive that you are using.
- If you have two hard disks, both Hard Disk C: and D: must be configured.

Consult your dealer/supplier for the hard disk(s) type(s) or parameter(s).

c) Choose your floppy drive(s):
The available options are: 360KB, 1.2KB, 720KB, 1.44KB, 2.88KB, and not installed.

d) Set the display type:
VGA/PGA/EGA, Color80X25, Monochrome, and not installed.

e) Set the error type:
Set this to ALL ERRORS

After you have selected the necessary options for your particular configuration, hit 'ESC' key to return to the main menu.

The information in the following two sections are to fine tune the system board's performance. Most of the options will be standard across all possible motherboard configurations.

F) CHIPSET FEATURES:

BUS ARCHITECTURE - P54CVIP has two 32-bit VESA Local Bus slots, five 16-bit ISA Bus slots, and four 32-bit PCI slots. The ISA bus offers an 8 or 16-bit data path and is normally run at 8 MHz. The Local Bus provides full 32-bit data path and operates at the same speed as the system speed. Local Bus peripheral devices can be bus-master or bus-slave. Local bus offers a significant performance advantage over the standard 8/16-bit ISA Bus. PCI provides 33MHz transfer rate and burst transfer mode, and it gives high performance for the peripherals.

Note that many VESA local bus peripherals run at a maximum of 33MHz.

CHIPSET - For optimal control in interfacing or processing, the P54CVIP system board features the OPTi 82C206/546/547/822 highly integrated chipset. This chipset minimizes the clutter and maximizes the integrity of the P54CVIP system board.

The 82C546/547/206/822 controls the following functions:

(i) 82C546 (AT Controller - ATC)

The 82C546 ATC integrates the AT bus interface and data buffers for transfers between the CPU data bus, local data bus and the DRAM data bus. It also provides the ISA to local bus command translation

- 208-pin PQFP
- Data bus buffer (host data to memory data)
- Data bus buffer control (ISA to memory)
- Parity generation and detection circuitry
- Keyboard controller chip select
- Local bus interface (ISA bus to Local bus command translation)

(ii) 82C547 (System Controller -SYSC):

The 82C547 SYSC provides the control functions for the host CPU interface, the 32-bit local bus interface, the 64-bit Level 2 (L2) cache and the 64-bit DRAM bus. The SYSC also controls the data flow between the CPU bus, the DRAM bus, the local bus, and the 8-16-bit ISA bus

- 160-pin PQFP
- Pentium CPU interface
- DRAM controller
- L2 cache controller
- L1 cache control
- Local bus interface
- Reset generation

18MB	256KB	2MB	256KB	2MB
20MB	512KB	2MB	512KB	2MB
24MB	1MB	2MB	1MB	2MB
32MB	2MB	2MB	2MB	2MB
34MB	256KB	4MB	256KB	4MB
36MB	512KB	4MB	512KB	4MB
40MB	1MB	4MB	1MB	4MB
48MB	2MB	4MB	2MB	4MB
64MB	4MB	4MB	4MB	4MB
66MB	256KB	8MB	256KB	8MB
68MB	512KB	8MB	512KB	8MB
72MB	1MB	8MB	1MB	8MB
80MB	2MB	8MB	2MB	8MB
96MB	4MB	8MB	4MB	8MB
128MB	8MB	8MB	8MB	8MB

Double Density SIMM
512 KB x 32/36 = 2MB
2 MB x 32/36 = 8 MB
8 MB x 32/36 = 32 MB

Single Density SIMM
1 MB x 32/36 = 4 MB
4 MB x 32/36 = 16 MB
16 MB x 32/36 = 64 KB

Note: 32/36 32 stands for 32-bit (without parity)
36 stands for 36-bit (with parity)

SIMM INSTALLATION:
To install a SIMM, observe the following procedure(**ALWAYS** use a CSA approved grounding strap or other anti-static device):

1) **Turn off and unplug the system.**

2) Align the module with the socket so that pin 1 on the module is toward the keyboard connector and the edge connector is facing the socket.

3) Keep the module at a 70 degree angle to the board and carefully insert the edge connector into the socket. Confirm that the SIMM is evenly seated in the socket.

4) Carefully push the module to a vertical position, until it clips into the metal latch on the socket assembly. The metal latch will hold the module firmly in place. Double check that the module is properly installed.
NOTE: Excessive force will damage the SIMM sockets, and void the warranty.

5) To remove a SIMM module, carefully pry the metal latch away from each end of the module. The module should flip forward and can be lifted out.
NOTE: Excessive force will damage the SIMM sockets, and void the warranty.

will NOT be updated until the system requires some new data that is NOT available in the cache. Standard Write-Through architecture is penalized during Writes because every time the system writes to cache it must also update the slower main memory. Therefore Write-Back is preferable to Write-Through.

The secondary cache utilizes SRAM (Static Random Access Memory) chips. There are a total of ten sockets for the secondary cache chips. Sockets U35, U37,U40, U42, U41, U43, U46, U47 comprise one bank. Socket U30 is the tag RAM and U31 is the Dirty RAM.

Tag RAM is used to store the address of the information that is in cache memory. The CPU looks at the tag RAM to see if the memory address for its required information is there. If the address is not found in the tag RAM, then the data is not in cache memory and the CPU must go to system memory for the data.

The Dirty RAM is used as a status indicator for true Write-Back cache. The system will poll the Dirty RAM when it needs to move new data into the cache. If it polls a set or ON status, then it will write the information out of the cache to main memory before loading new data. Otherwise OFF status indicates that the data in main memory is equivalent or just as current as that in cache and the system will directly load the new data that it requires.

For installation of cache memory, observe the following procedure (**ALWAYS** use a CSA approved grounding strap or other anti-static device):

1) Select the size of the cache desired and consult the following table to determine the size and quantity of chips required. The speed required will depend on the speed of the CPU. We recommend using top quality 15ns or faster SRAM.

SRAM REQUIREMENT

Total Cache	
256KB	32KB x 8 -15ns
512KB	64KB x 8 -15ns

TAG/DIRTY REQUIREMENT

2) **Turn off and unplug the system.**

3) Set the appropriate jumpers according to the size of cache to be installed.

Jumper	256KB	512KB
JP28	OFF	ON
JP29	ON	ON
JP30	ON	ON

B) CPU Installation / Upgrade

The Central Processing Unit (CPU) is the brain of a computer. The CPU interprets and executes instructions and thereby controls the computer system. In micro-computers, the CPU is designed as a highly integrated chip called the micro-processor. The P54CVIP incorporates only the best in micro-processor speed and technology. The following are CPUs and speeds available for the P54CVIP.

PENTIUM™ - The P54CVIP supports Pentium™ 75/90/100MHz. These processors use Pentium technology and include separate 16 KB code and data caches. Internally they may be clock doubled or tripled. A 320 pin ZIP socket is included to house these processor.

For installation of a new CPU, or upgrade of an existing CPU, observe the following procedure (**ALWAYS** use a CSA approved grounding strap or other anti-static device):

1) **Turn off the power.**

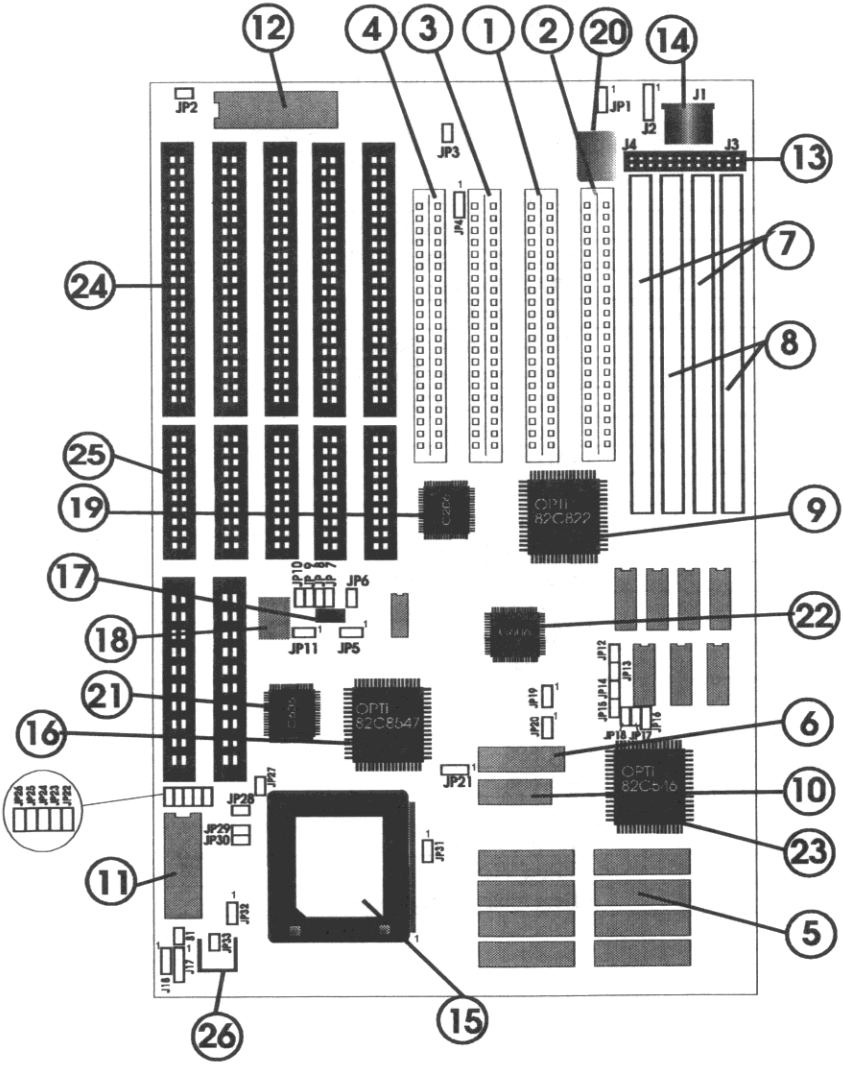
2) Upgrading an existing CPU is easy with the ZIF (Zero Insertion Force) socket. Open the ZIF socket by moving the handle to the upright position, the old CPU is now free. Lift it straight out of the socket.

3) Align the new CPU with the socket (be sure all the pins on the CPU are aligned with the holes). One corner of the CPU is notched and marked with a round dot and you should align it with the pin one mark (white triangle on the board or alignment pins on the socket).

4) With the ZIF socket handle in the upright position set the CPU straight into the socket, **it should drop in easily requiring no force**. Make sure that all pins are fully inserted in the appropriate holes. Gently hold the CPU in place and push the handle to the closed position.

5) The P54CVIP uses a clock generator to produce the system clock and simplifies processor upgrades. Set the jumpers to select the appropriate frequency, as outlined in the table on the following page.

Board Layout



INTRODUCTION

The P54CVIP supports both Intel Pentium 75/90/100MHz CPUs.

Features:

* Cache controller:

    a. L1 and L2 Write Back Policy

    b. L1 and L2 Burst Write and Burst Read 3-2-2-2 fast cycle

    c. Fast next address pipeline

    d. Secondary Cache 256KB and 512KB
    using SRAM (32 KB x 8, 64KB x 8 respectively)

* 64-bit DRAM controller

    a. supports both Single Density and Double Density 72 pin SIMM modules

    b. Supports up to 128 MB of memory on board (using 256 KB x 32/36, 1MB x 32/36, 2 MB x 32/36, 4 MB x 32/36, 8 MB x 32/36, 16 MB x 32/36 SIMM)

    c. Fast page access

    d. Hidden refresh

* AWARD PCI BIOS

* OPTi 82C206/546/547 and OPTi 82C822 surface-mounted chipset

* Four 32-bit PCI Local Bus slots

* Two 32-bit VESA Local Bus slots

* Five 16 bit ISA expansion slots

* Onboard Clock Generator facilitates CPU upgrades. Simply change jumpers to change CPU speed (no oscillators required).

* Flash BIOS for easy upgrade

Notice

Arvida Technology Inc. reserves the right to make changes or improvements in the product described in this manual at any time without notice.

This manual contains information important for the successful installation and operation of the system board. Please read the information carefully and be sure that you understand it thoroughly before proceeding with installation.

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