PAT48PG4

Version 1.2A

User's Manual

SPC 96079

94-LON-AQ-249

PAT48PG/PG4
System Board
User's Manual

NOTES

Contents

NOTES

Chapter 1 Specifications

Architecture

ISA (Industry Standard Architecture) with ***VL-Bus*** implementation
VL-Bus compliant

Main Processor

486SX, 486DX, 486DX2 or 486DX4

Processor Upgrades

A ZIF socket for a Pentium OverDrive processor

Cache Memory

8KB of on-chip cache memory
128KB or 256KB of write-back secondary cache memory

Main Memory

Up to **128MB** of on board main memory
Four 30-pin & Two 72-pin SIMM(Single In-Line Memory Module) sockets for *(256K; 512K, 1M, 2M,4M, 8M, 16M, 32M) x 36* or *(256K, 1M, 4M, 16M) x 9* modules

BIOS

Licensed BIOS

Clock/Calendar

Battery Backed Real Time Clock(146818 compatible) and 128 bytes of CMOS RAM
On board rechargeable battery

DMA Channels

Seven DMA channels(8237 compatible)

Interrupts

Sixteen levels of hardware interrupts(dual 8259 compatible)

System Timer

Three channels of programmable system timer (8254 compatible)

Expansion Slots

Seven ISA slots
Three VL-Bus slots(two master and one slave)

Connectors

Connectors for: power supply, keyboard, reset switch, Power LED, keylock, speaker, turbo switch, turbo LED, external battery and hard disk access LED

Physical Dimensions

4/5 Baby AT form factor

Power Requirement

+ 5V @ 2 AMPs (Normal Operation)
+ 5V @ 1 AMP (Power Saving Mode)

Chapter 2 Hardware Description

This chapter briefly describes each of the major features of the PAT48PG system board. The function block of the board is shown in *Figure 1*. The layout of the board is shown in *Figure 2* to show the locations of key components. The topics covered in this chapter are as follows:

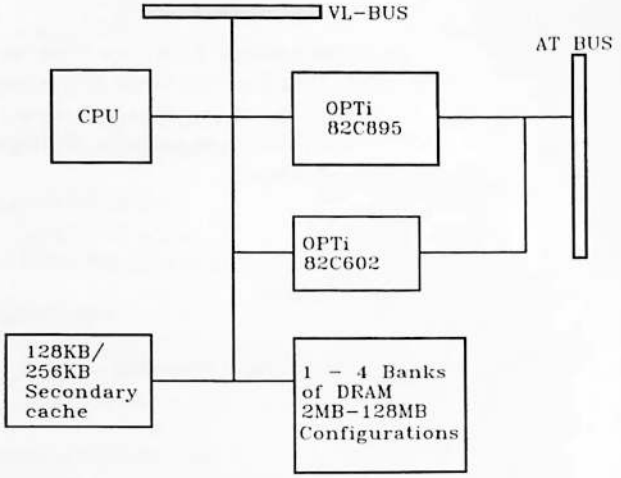


Figure 1: Function block of the PAT48PG

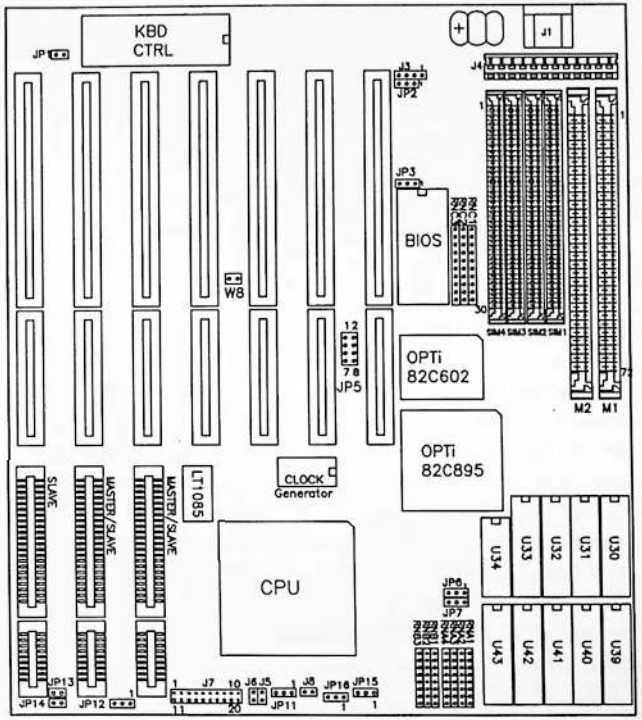


Figure 2: Layout and connector locations of the PAT48PG

2.1 PAT48PG Motherboard

The PAT48PG is designed by implementing a 486 processor and a highly integrated chipset, the **82C895/602**.

The 82C895 integrates a write-back cache controller, local DRAM controller, AT Bus and CPU interface logic. The 82C895 also incorporates the DMA controller, System Controller and System Timer. A 146818 RTC is implemented and provides the Clock/Calendar functions. The 82C602 provides buffer control logic.

2.2 486 Microprocesssor

The Central Processing Unit (CPU) of the PAT48PG motherboard is a 486 microprocessor. There are various models in the 486 family: 486SX, 486DX, 486DX2 and 486DX4.

The 486SX is the basic model in the 486 family. The 486DX, in additions to the features of the 486SX, provides on-chip 80387 compatible math coprocessor. The 486DX2 has a core frequency two times the bus frequency and provides twice the performance. The 486DX4 has the core frequency that is either two or three times the bus frequency and operates at 3.3V.

The socket on board also supports the OverDrive processor. The OverDrive is an upgrade processor for 486 family. It has Pentium equivalent core with 486 compatible pin-outs. It provides capability of a user to upgrade from a 486 to Pentium performance with a simple processor change.

2.3 Cache Controller and Cache Memory

The on-chip cache, 8KB in size, is a unified code and data cache. The cache is used for both instruction and data accesses and acts on physical addresses.

This cache is organized as 4-way set associative with a line size of 16 bytes. The on-chip cache memory is logically organized as 128 sets, each containing four lines.

For the Pentium OverDrive processor, the cache line size is 32 bytes.

For the secondary cache, the system controller, 82C895, supports 486 burst cycles. The PAT48PG can be configured with *128KB* or *256KB* of *write-back secondary cache memory*, greatly enhancing system performance in the event of on-chip cache miss cycles.

The system controller also provides *page mode* operations for main memory. The main memory also supports burst mode operations of the 486, further enhancing system performance.

2.4 I/O Port Address Map

The CPU of the PAT48PG communicates via I/O ports. There are a total of 1K port address space defined. The following tables list the I/O port addresses used in the PAT48PG and those assigned to other devices that can be used by I/O expansion cards.

Table 2: I/O port addresses of the devices on the PAT48PG

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0Ah0 - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor

Table 3: I/O port addresses of devices on the I/O slots

Address	Description
1F0h - 1F8h	Floppy Disk Controller
200h - 207h	Game Port
278h - 27Fh	Parallel Port #2(LPT2)
2F8h - 2FFh	Serial Port #2(COM1)
300h - 31Fh	Prototype Card
360h - 36Fh	Reserved
378h - 3FFh	Parallel Port #1(LPT1)
380h - 38Fh	SDLC #2
3A0h - 3AFh	SDLC #1
3B0h - 3BFh	MDA Video Card (including LPT0)
3C0h - 3CFh	Reserved
3D0h - 3DFh	CGA Video Card
3F0h - 3F7h	Hard Disk Controller
3F8h - 3FFh	Serial Port #1(COM1)

2.5 Memory Map

The PAT48PG has a maximum memory capacity of 128MB. The first megabyte is divided into four blocks with each block dedicated to a fixed function. The following table illustrates the memory map for the PAT48PG.

Table 4: Memory map of the PAT48PG

Memory	Address	Description
0KB	000000h - 09FFFFh	Conventional RAM
640KB	0A0000h - 0BFFFFh	128KB of Video RAM
768KB	0C0000h - 0EFFFFh	192KB of I/O Expansion ROM
960KB	0F0000h - 0FFFFFh	64KB of System BIOS ROM
1MB	100000h - 7FEFFFFh	127MB of User RAM
128MB	7FF0000h - 7FFFFFFh	Duplicated 64KB of System BIOS ROM at 0F0000h

2.6 BIOS

The PAT48PG contains a 27C512 EPROM that contains the system BIOS. The BIOS resides at the upper 64KB of address space in the first megabyte.

In protected mode, the BIOS is also mapped to the upper 64KB of the 128MB space and can be accessed at either location.

2.7 System Timer

The PAT48PG has three channels of timer/counter in the 82C802G chip, which is Intel 8254 compatible. The function of each channel is listed as follows:

Table 5: System timer of the PAT48PG

Channel	Function
0	**System Timer** - This timer generates the time base for the system timer. Its output is tied to IRQ0.
1	**Memory Refresh Request** - This timer is used to generate memory refresh requests. It triggers the memory refresh cycle.
2	**Tone Generator for Speaker** - This timer provides the speaker tone. Various sounds can be generated by programming the timer.

2.8 DMA Channels

The PAT48PG contains the equivalent of two 8237A DMA controllers in the 82C895.

The 82C895 provides the user with two DMA controllers, four channels of DMA*(DMA #1)* for 8-bit transfers, and three channels of DMA*(DMA #2)* for 16 bit transfers.(The first 16-bit DMA channel is used for cascading.)

Channel		Function
Controller #1	Controller #2	
0		DRQ0, Reserved
1		DRQ1, SDLC
2		DRQ2, Floppy Disk Controller
3		DRQ3, Reserved
	4	DRQ4, Cascade for DMA
	5	DRQ5, Reserved
	6	DRQ6, Reserved
	7	DRQ7, Reserved

2.9 Interrupt Controllers

The PAT48PG contains two Intel 8259A compatible interrupt controllers in the 82C895. Sixteen channels are partitioned into the cascaded controllers (INTC1, INTC2) with 8 inputs each. Of these 16 channels, three are connected internally to various devices, allowing 13 user definable channels of interrupt. Any or all of these interrupts can be masked.

Level	Function
NMI	RAM Parity Check
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ8	Real Time Clock
IRQ9	Software Redirected to Int 0Ah
IRQ10	Reserved
IRQ11	Reserved
IRQ12	Reserved
IRQ13	80287
IRQ14	Fixed Disk Controller
IRQ15	Reserved
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Parallel Port #2
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1

2.8 DMA Channels

The PAT48PG contains the equivalent of two 8237A DMA controllers in the 82C895.

The 82C895 provides the user with two DMA controllers, four channels of DMA*(DMA #1)* for 8-bit transfers, and three channels of DMA*(DMA #2)* for 16 bit transfers.(The first 16-bit DMA channel is used for cascading.)

Channel Controller #1	Channel Controller #2	Function
0		DRQ0, Reserved
1		DRQ1, SDLC
2		DRQ2, Floppy Disk Controller
3		DRQ3, Reserved
	4	DRQ4, Cascade for DMA
	5	DRQ5, Reserved
	6	DRQ6, Reserved
	7	DRQ7, Reserved

2.9 Interrupt Controllers

The PAT48PG contains two Intel 8259A compatible interrupt controllers in the 82C895. Sixteen channels are partitioned into the cascaded controllers (INTC1, INTC2) with 8 inputs each. Of these 16 channels, three are connected internally to various devices, allowing 13 user definable channels of interrupt. Any or all of these interrupts can be masked.

Level	Function
NMI	RAM Parity Check
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ8	Real Time Clock
IRQ9	Software Redirected to Int 0Ah
IRQ10	Reserved
IRQ11	Reserved
IRQ12	Reserved
IRQ13	80287
IRQ14	Fixed Disk Controller
IRQ15	Reserved
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Parallel Port #2
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1

2.10 Real Time Clock and CMOS RAM

The PAT48PG contains an MC146818 compatible Real Time Clock (RTC) and 128 bytes of CMOS RAM in the 82C206.

The CMOS RAM stores the system's configuration information entered via the Setup program. The RTC and the CMOS RAM are kept active by a battery when the system power is turned off.

Note

The Real Time Clock and the CMOS RAM are kept active by an on board rechargeable battery. The PAT48PG also provides an interface for an external battery.

Chapter 3 Configuring the PAT48PG

This chapter provides illustrated instruction on configuring the PAT48PG motherboard.

This chapter is divided into four major areas.

- **3.1 CPU Related Jumpers/Switches**
  - **3.1.1 Installing the CPU**
  - **3.1.2 Setting CPU Related Jumpers**
- **3.2 Main Memory Configurations/Installation**
  - **3.2.1 Installing Memory**
  - **3.2.2 Setting Memory Related Jumpers**
- **3.3 Cache Memory Configuration/Installation**
  - **3.3.1 Installing Cache Memory**
  - **3.3.2 Setting Cache Related Jumpers**
- **3.4 Miscellenous Jumpers/Switches**

3.1 CPU Related Jumpers and Switches

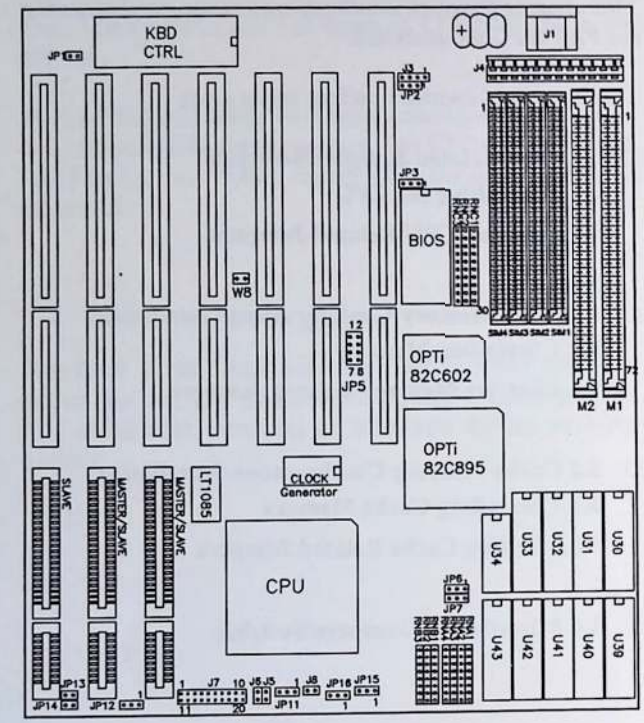


Figure 3: CPU related jumpers

3.1.1 Installing and/or Upgrading the CPU

To install a CPU, refer to the following figures. If there is a ZIF socket, lift the lever to its vertical position to install the CPU.

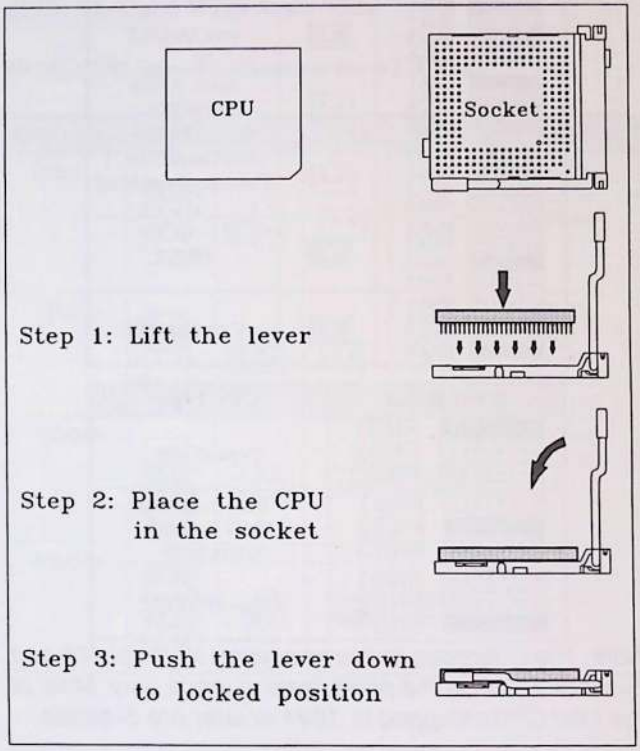


Figure 4: Installing the CPU

3.1.2 Setting CPU Related Jumpers

3.1.2a Setting CPU Type:RNA1 - RNA4 & RNB1 - RNB3, W8

RNA1 - RNA4	W8	CPU Type
RNA1 RNA2 RNA3 RNA4		486DX/DX2
RNA1 RNA2 RNA3 RNA4		Intel, AMD 486DX4 Cyrix 5x86
RNA1 RNA2 RNA3 RNA4		Over Drive/P24CT Pentium OverDrive
RNA1 RNA2 RNA3 RNA4		486SX
RNA1 RNA2 RNA3 RNA4		Cyrix 486DX

RNB1-RNB3	CPU Type
RNB1 RNB2 RNB3	Typical 486
RNB1 RNB2 RNB3	Intel S-series AMD Enhance Cyrix 5x86
RNB1 RNB2 RNB3	Cyrix 486 CPU

Note: The difference between a typng a typical 486 and S-series 486 is in the power saving mode only. Most of the Intel CPUs shipped in 1994 or later are S-series.

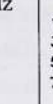
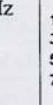
3.1.2b Setting CPU Frequeny Related Jumpers

JP12: Clock Frequency Selector

JP5: Clock Generator Frequency

JP13: VL Card Write Wait State

JP14: CPU Speed Indication for VL Cards

CPU Speed	JP5	JP12	JP13	JP14	CPU Models
25MHz					SX-25 DX2-50 P24T-63
33MHz					SX-33 DX-33 DX2-66 P24T-83 DX4-100
40MHz					DX-40 DX2-80 DX4-120
50MHz					DX-50

3.1.2c Intel & AMD CPU Internal Cache W.B Selection: JP15, JP16

	JP15	JP16
Intel, AMD Write Back		
Others		

3.2 Main Memory Installing

1.Memory cofiguration with RNC1 installed

Bank0 M1 (single)	Bank1 M2 (single)	Bank2 SIM1-4	Total Memory
256Kx36	256Kx36	-----	2M
1Mx36	-----	-----	4M
256Kx36	1Mx36	-----	5M
256Kx36	256Kx36	1Mx9	6M
1Mx36	1Mx36	-----	8M
1Mx36	-----	1Mx9	8M
4Mx36	-----	-----	16M
256Kx36	4Mx36	-----	17M
1Mx36	4Mx36	-----	20M
1Mx36	-----	4Mx9	20M
4Mx36	4Mx36	-----	32M
4Mx36	-----	4Mx9	32M
16Mx36	-----	-----	64M
16Mx36	16Mx36	-----	128M
16Mx36	-----	16Mx9	128M

2.Momory configurations with RNC2 installed

Bank0 SIM1-4	Bank1 M2 (single)	Bank2 M1 (single)	Total Memory
256Kx9	256Kx36	-----	2M
1Mx9	-----	-----	4M
256Kx9	1Mx36	-----	5M
256Kx9	256Kx36	1Mx36	6M
1Mx9	1Mx36	-----	8M
1Mx9	-----	1Mx36	8M
4Mx9	-----	-----	16M
256Kx9	4Mx36	-----	17M
1Mx9	4Mx36	-----	20M
1Mx9	-----	4Mx36	20M
4Mx9	4Mx36	-----	32M
4Mx9	-----	4Mx36	32M
16Mx9	-----	-----	64M
16Mx9	16Mx36	-----	128M
16Mx9	-----	16Mx36	128M

3.Memory configuations with RNC3 installed

M1 socket Bank0	Bank1	M2 scoket Bank2	Bank3	Total Memory
512Kx36		-----	-----	2M
1Mx36	-----	-----	-----	4M
512Kx36		512Kx36		4M
512Kx36		1Mx36	-----	6M
2Mx36		-----	-----	8M
1Mx36	-----	1Mx36	-----	8M
512Kx36		2Mx36		10M
1Mx36	-----	2Mx36		12M
4Mx36	-----	-----	-----	16M
2Mx36		2Mx36		16M
1Mx36	-----	4Mx36	-----	20M
8Mx36		-----	-----	32M
4Mx36	-----	4Mx36	-----	32M
16Mx36	-----	-----	-----	64M
8Mx36		8Mx36		64M
32Mx36		-----	-----	128M
16Mx36	-----	16Mx36	-----	128M

M1 socket Bank0Bank1		SIM1-4 Bank 2	Total Memory
512Kx36		1Mx9	6M
1Mx36	-----	1Mx9	8M
1Mx36	-----	4Mx9	20M
16Mx36	-----	16Mx9	128M

3.3 Installing Cache Memory

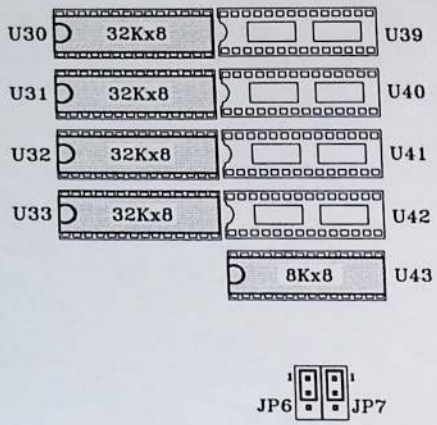


Figure 5: 128KB of cache memory

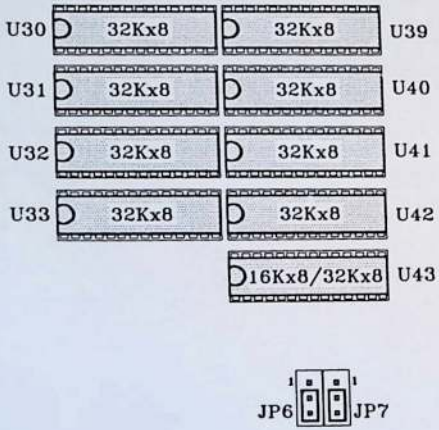


Figure 6: 256KB of cache memory

3.4 Miscellenous Jumpers

Video Adapter Selection Jumper: JP1

JP1	Function
	Color
	Monochrome

Battery Selection Jumper: JP2

JP2	Function
	Clear Contents of the CMOS RAM
	Use the on board memory
	Use an external battery connected to J3

BIOS ROM Type: JP3

The PAT48PG can accommodate a flash ROM or an EPROM. Use JP3 to select whether a flash ROM or an EPROM is being used in socket **U11.**

JP3	Function
	Flash ROM
	EPROM

Chapter 4 Installation

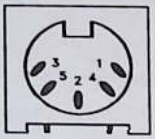
This chapter describes the interface that the PAT48PG provides for creating a working system. Refer to Figure 2 for the location of the connectors.

The following items are covered in this chapter.

- ☐ **4.1 Keyboard Connector: J1**
- ☐ **4.2 External Battery Connector: J3**
- ☐ **4.3 Power Supply Connector: J4**
- ☐ **4.4 Power Saving Switch and LED Connector: J5 & J8**
- ☐ **4.5 Speaker Connector: J7(Pins 1 - 4)**
- ☐ **4.6 Power LED and Keylock Connector: J7(Pins 11 - 15)**
- ☐ **4.7 Turbo Switch Connector: J7(Pins 7 & 17)**
- ☐ **4.8 Turbo LED Connector: J7(Pins 8 & 18)**
- ☐ **4.9 Reset Switch Connector: J7(Pins 9 & 19)**
- ☐ **4.10 Hard Disk Access LED Connector: J7(Pins 10 & 20) and J6**

4.1 Keyboard Connector: J1

The keyboard connector, **J1**, is a *5-pin DIN* connector for attaching an IBM AT or an IBM Enhanced 101-key compatible keyboard.



J1 Pin #	Description
1	Keyboard Clock
2	Keyboard Data
3	N.C.
4	Ground
5	Vcc

4.2 External Battery Connector: J3

This *4-pin* connector, **J3**, allows the user to connect an external battery to maintain the information stored in the CMOS RAM.

J3 Pin #	Description
1	Vcc
2	N. C.
3	Ground
4	Ground

4.3 Power Supply Connector: J4

When using an AT compatible power supply, plug both of the power supply connectors into J4.

Make sure the power supply connectors are connected in the right orientation. The power supply connectors are connected in the right orientation if the black wires of each power cable are *ADJACENT* to each other. That is, black wires of each connector should be aligned in the center of the power supply connector, J4, of the PAT48PG

The following table indicates the pin-out assignments of the power supply connector.

J4 Pin #	Description	Wire Color
1	Power Good	Orange
2	+5V	Red
3	+12V	Yellow
4	-12V	Blue
5	Ground	Black
6	Ground	Black
7	Ground	Black
8	Ground	Black
9	-5V	White
10	+5V	Red
11	+5V	Red
12	+5V	Red

4.4 Power Saving Switch and LED Connector: J8 & J5

J8, allows the user to attach a power saving switch located in the system's front panel. To switch the system into power saving mode, simply press switch and the LED connected to J5 will be on and the system will immediately go into power saving mode. *Orientation is not required when attaching the switch to J8.*

To return to normal mode, press switch again or type any key on the keyboard or move the mouse.

J5 Pin #	Description
1	Anode
2	Cathode

Note

The PAT48PG can be configured to go into power saving mode via the system setup program. Refer to the system setup screen for details.

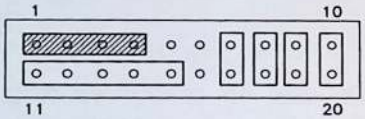
4.5 Speaker Connector: J7(Pins 1 - 4)

Pins 1 - 4 of the 20-pin connector, **J7**, provide an interface to a speaker for audio tone generation. A speaker with 8-Ohm or higher impedence is recommended.

Note

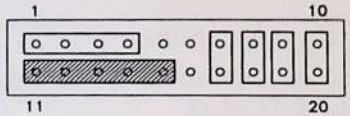
Orientation is not required when connecting a speaker to pins 1 - 4 of J7.

J8 Pin #	Description
1	Speaker Out
2	N.C.
3	Ground
4	+ 5V



4.6 Power LED and Keylock Connector: J7(Pins 11 - 15)

Pins 11 - 15 of the 20-pin connector, **J7**, allow the user to connect the power LED and keylock switch of the system's front panel. The power LED indicates the *ON/OFF* status of the system. The keylock switch, when *CLOSED*, will disable the keyboard function.



J7 Pin #	Description
11	Power LED
12	N.C.
13	Ground
14	Keylock
15	Ground

4.7 Turbo Switch Connector: J7(Pins 7 & 17)

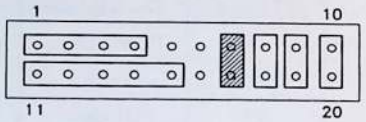
Pins 7 & 17 of the 20-pin connector, **J7**, allow the user to connect a turbo switch on the front panel of the system chassis.

A turbo switch is usually a push-on switch. When the switch is on, pins 7 & 17 are SHORTED and the system will be running at **FULL*(TURBO)*** speed.

To switch to **LOW*(NON-TURBO)*** speed, simply PRESS the switch. To return to turbo speed, press the switch again.

Note

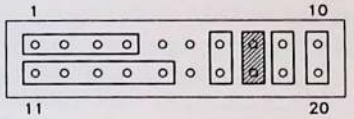
Orientation is not required when connecting a turbo switch to pins 7 & 17 of J7.



4.8 Turbo LED Connector: J7(Pins 8 & 18)

Pins 8 & 18 of the 20-pin connector, **J7**, provide the user with an interface for connecting a turbo LED indicator in the system's front panel.

This LED, when on, indicates the **TURBO**(*FULL*) speed mode of the PAT48PG system.



J7 Pin #	Description
8	Anode
18	Cathode

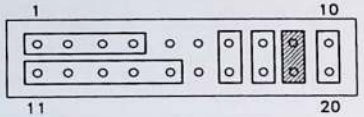
4.9 Reset Switch Connector: J7(Pins 9 & 19)

Pins 9 & 19 of the 20-pin connector, **J7**, provide an interface for a reset switch. The reset switch allows the user to reset the system without turning the power switch off and on.

To reset the PAT48PG based system, *SHORT* pins 9 and 19 of J7 by pressing the reset switch of the system chassis.

Note

Orientation is not required when connecting a reset switch pins 9 and 19 of J7.



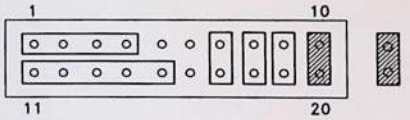
4.10 Hard Disk LED Connector: J7(Pins 10 & 20), J6

These connectors allow the user to connect the hard disk access LED on the system's front panel. The LED will be on whenever the system is accessing the hard drive.

Connect the 2-pin connector from the system chassis to *pins 10 & 20* of **J7**. Also, make a connection from **J6** to the hard disk controller's LED interface.

Note

You may also connect HDD LED on the system's front panel directly to the hard disk controller's LED interface without using these connectors.



Pin #	Description
J7(Pins 10 & 20)	LED In
J6	LED Out

NOTES