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October 9, 2000

NL810

External Product Specification

August 27, 1999

Revision 1.0

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Revision History

Revision	Date	Description
0.2	5/03/99	Prelim release for TAIS review
0.3	5/07/99	Video resolutions added from Intel data sheet
0.4	5/21/99	Formatting and pagination changes
0.9	7/22/99	Reformatting and cleanup
1.0	8/27/99	Production release

Preface

1. Hardware Feature Summary

The BCM NL810 is a Intel 810 chipset(Whitney), Pentium II based system for Q2 1999. NL810 is NLX form factor with Integrated Graphics Controller, LAN, and AC97 interface through NLX Riser connector.

Major system components include:

Processor:

Intel Socket 370 Mendocino and PIII Cppermine FC-PGA and PPGA family CPU with integrated 0K/128KB L2 Cache. 66/100/133MHz Front Side Bus Frequency.

System Memory:

2 x 168-pin DIMM sockets, supporting SDRAM PC-100 DIMMs with SPD.

Chip Set:

Intel 810 "Whitney"(GMCH/GMCH0, Graphics and Memory Controller Hub)
ICH/ICH0(I/O Controller Hub) , ICH with 6 REQ/GNT , ICH0 with 4 REQ/GNT pairs PCI.
Bus Master support.
FWH(FirmWare Hub)
Winbond LPC I/O W83627HF

LAN Interface:

Intel 82559 Fast Ethernet Multifunction PCI Controller with RJ45 connector interface with an integrated 10/100 Mbps physical layer device. Supports ACPI, WFM 2.0.

Integrated I/O Controller:

Winbond LPC I/O W83627HF, supporting two async serial ports (UARTs) with high speed 16550 and 16-byte FIFO. One Parallel port supports EPP, ECP and Centronics Bi-directional modes. PS/2 keyboard port (using, AMI keyboard controller), mouse port and game/MIDI port. W83627HF also includes system hardware monitor.

Soft power, Ultra DMA 66/33 and 2 USB support integrated in ICH/ICH0.

Infrared Interface:

One infrared port with IrDA v1.0 SIR protocol, SHARP ASKIR. When IrDA is enabled, only one UART channel will be supported.
Consumer IR is also supported.

Hard Disk:

Two-channel (four devices) IDE controller integrated in ICH, with PCI Bus Master support, true independent device timing, ultra DMA/66, and ultra DMA/33. IDE interface is available from the Riser connector.

Floppy Disk:

720K, 1.44MB and 2.88MB(3.5 inch format only) diskette drives support. Support LS120, IDE ZIP drive. Floppy interface is available from the Riser connector.

System BIOS:

2Mb, 4Mb or 8Mb with boot block flash ROM in FWH. (Default 4 MB.)
PC99 and PnP/ACPI compatible.
WfM 2.0 support (remote boot-up)

Power Management:

APM 1.2
ACPI 1.0
Instantly Available PC

NLX Riser Card Functions (Customer Specific):

Up to 5 x 32 bits PCI slots.
Up to 5 ISA slots.
Power, On/Off Control
2 Bus Master IDE Ports (Up to 4 IDE devices) that support Ultra ATA 66MB/sec & ATA 33MB/sec
1 Floppy Port (up to 2.88 MB)
2 Standard USB connectors (48 Mhz)
Front Panel Reset, Power LED
Fan Control, PC Speaker

2. System BIOS Feature Summary

Processor:

Intel Socket 370 Mendocino PPGA family CPU.

System Memory

2 x 168-pin DIMM sockets supporting SDRAM PC-100 DIMMs with SPD
Support Double-side DIMM modules
Support various combination of SDRAM up to 512MB
Support DIMM modules with various device widths (x8, x16, and x32).

Core Logic Chipset

INTEL 810 Whitney-GMCH/GMCH0 (Memory Controller Hub)
INTEL 810 Whitney –ICH/ICH0 (I/O Controller Hub)
INTEL 810 Whitney -FWH (FirmWare Hub)

LAN Interface

On board optional, Intel 82559 Fast Ethernet Multifunction PCI Controller with RJ45 connector interface with an integrated 10/100 Mbps physical layer device. Supports ACPI, WFM 2.0.

Super IO

Winbond W83627HF-AW: supporting Keyboard, PS/2 mouse, Serial, Parallel, IrDA and Floppy.
PS/2 keyboard and mouse support.
2 x Sync Serial port (UARTs) with high speed 16550 and 16-byte FIFO.
1 x Parallel port that supports EPP, ECP and Centronics Bi-directional modes.
1 x infrared port with IrDA V1.0 SIR protocol.
2 x USB ports that support both UHCI and OHCI protocols.

TAIS requires to support the following buttons and condition:

1. Power button: Push ON and Push and hold for 4 sec or more for OFF.
2. Sleep button: Push to go to sleep state/suspend.
3. Reset button: Push to reset the system.

Ultra DMA/33 and Ultra DMA/66
W83627HF-AW supports system Hardware Monitor.
ICH: supporting RTC, ACPI, USB and CMOS.

PS/2 Mouse and Keyboard Support

Supported from Winbond W83627HF-AW
Support Keyboard and Mouse port swap function.

Plug and Play

Supporting PnP BIOS Specification V1.0A

PCI 2.2

Supporting PCI 2.1 Specification and Delay Transaction.
Supporting PCI 2.2 Power Management Event (PME#, PCI slot pin#A19)
and Stand-By 3.3V voltage (3.3VAux, PCI slot pin#A14) signals.
SubSystem ID and SubVendor ID are required in PCI 2.2.

Power Management

Must meet APM Specification version 1.2.

ACPI

Supporting ACPI V1.0 and Instantly Available PC.
Support ACPI states: S0, S1, S3, S4, and S5.
Remote Wake up via modem & network.
Resume on modem ring(disabled now for TAIS but still required for other customers).

IDE Hard Disk Features

PCI Bus Master supported true independent device timing , Ultra DMA/66, and Ultra DMA/33.

Enhanced IDE Support

Hard disk support for 8GB and bigger.
Auto Detect and Auto Configuration.
Multisector and 32 bit Transfer.
LBA mode.
ZIP drive support including A: drive
LS-120 optical support.
Advanced PIO Modes 3 & 4.

CD-ROM Features

Support bootable CD in no emulation mode booting function.

System BIOS

2MB, 4MB or 8MB with boot block flash ROM in FWH.
WfM 2.0 support for Remote Boot-up.
PnP BIOS specification V1.0A

System States

Full-On
APM/Hardware Doze
Stand-by
Suspend to RAM

Device Power Management

Video Logic Power Down
HDD, FDD & FDC Power Down
Sound chip Power Down
Super I/O chip Power Down
Everything is powered down in S4

PCI Devices and Slots:

The NL810 supports up to five PCI slots and up to five ISA slots through the NLX Riser in addition to the Whitney (GMCH) Chipset

USB

The BIOS must contain the support for bootable USB devices such as Keyboards.
Full Bus Enumeration.
UHCI & OHCI support.
Hot insertion of USB devices.
Hub Device support.
Legacy Keyboard, FDD and mouse support.

Security Features

User password for access BIOS/System.
Two passwords required for CMOS.
Password protected resume from Suspend.
A unique Random Number Generator in FWH to enable enhanced platform security.
Register-based and hardware-based locking.
Remote Wake-up and Local Security (APM mode only)

* Password checking on Resume

The following behaviors are required upon system resume if the 'password on resume' is enabled and either supervisor and user password is set:

a. Local wakeup event (sleep button, KB/mouse movement): The system does not wakeup unless the correct password is entered.
b. Remote wakeup event (WOL): The system wakes up for remote activity, but the local KB/Mouse stay locked and monitor stay off. The local KB/Mouse stays locked until the correct password is entered.

DMI

Must meet DMTF BIOS specification V2.0

Jumper-Related Features:

GPIs:

Clear Password: accessible via ICH Function 0, **GPIO6**
1 = normal operation mode, 0 = clear password.

SLEEP Control: accessible via ICH Function 0, **GPIO8**
0 > 1 transition will toggle sleep mode.

GPOs:

Power LED: Use W83627HF-AW GP35. 1 = Normal; 0 = Suspend.
Fan Control: Use W83627HF-AW FANPWM1/2 to control.

PC98/PC99

Quiet Boot and **Quick Boot** are required.
Reporting Disabled Devices: Report the devnode as unconfigurable with possible resources.

DIMM Timing Parameters

Use flexible timing settings as provided in BIOS EDS.
INTEL SPD protocol supported for SDRAM

Clock Generator

IC-Works W195BH

Special System Feature

1. IrDA shares with UART channel #B.
2. Y2K Compliant.
3. Resume from PCI Power Management Event (PME)
4. Wired For Management (WfM) 2.0 support for Remote Boot-Up.
5. SMBIOS 2.3 Compliant.
6. SMBus support.
7. Auto Time Adjust for Daylight Saving and Leap Year
8. AMI AnyLanguage Support
9. Built in BIOS POST Diagnotics
10. Elonex Patent
    This option should be implemented in that the system BIOS Display Standby or Display Suspend request to the video BIOS is replaced with Display Off. There are only two states for the monitor; ON and OFF not the intermediate power saving states.

TAIS FAN BEHAVIOR REQUIREMENT

-TAIS requirement:
APM Mode
Standby--- CPU Fan=On, Chassis Fan=On
Suspend--- CPU Fan=Off, Chassis Fan=On

ACPI Mode
S1----------CPU Fan=Off, Chassis Fan=On
S3, S4, S5---- CPU Fan=Off, Chassis Fan=Off

TAIS NLX REQUIREMENT - FRONT PANEL POWER LED

-TAIS requirement:
ON state=Green, **SLEEP** state(S1,S3,S4,Standby,Suspend)=Amber, **OFF/S5** state=Off

-Implementation:
1. If PowerLED# signal = 1, then LED color = green
2. If PowerLED# signal = 0, then LED color = amber

-Note:
During S5, PowerLED# signal must be 1. This will cause the LED to be OFF since the power source for the Green LED is Vcc, which is off during S5. If PowerLED is at 0, the LED will be Amber since the power source for the Amber LED is 5v standby and that stays active during S5.

3. Product Configurations

21021 All features

- LPC I/O with hardware monitor (AMI keyboard controller code)

21022 For TAIS

Included

- Intel i810 chipset(GMCH0 and ICH)
- LPC I/O with hardware monitor (AMI keyboard controller code)
- Support for Suspend to RAM

NOT included

- ISA bridge
- DFP
- LAN

-AOL2 circuitry

Document Outline

Section 1: Introduction
Provides an overview of the NL810 motherboard showing functional blocks.

Section 2: Functional Architecture
Describes the way each functional block of the NL810 motherboard works. Summarizes major bus interface signal pin names and their meaning.

Section 3: Configuration
The NL810 configuration tables with considerations for all the different environments the hardware can be set to is given.

Section 4: Electrical and Mechanical Specifications
Specifies electrical and operational parameters, considerations and other hardware specifications.

References

The Following documents should be available for reference when using this document:

Referenced BCM Internal Documents

Several documents are required during the process of design, regulatory approvals, manufacturing and servicing the NL810 product family. The required documents are as follows:

- NL810 PWB Fabrication Drawing
- NL810 PWB Layout Artwork for each revision of PWB
- NL810 PWB Gerber Files
- NL810 Schematics for each revision of PWB & PWA
- NL810 Assembly Drawings and Process Instructions
- All production level ECOs
- Bill of Material (BOM) with Approved Vendor List (AVL)
- Option Control List (OCL)

Referenced External Documents

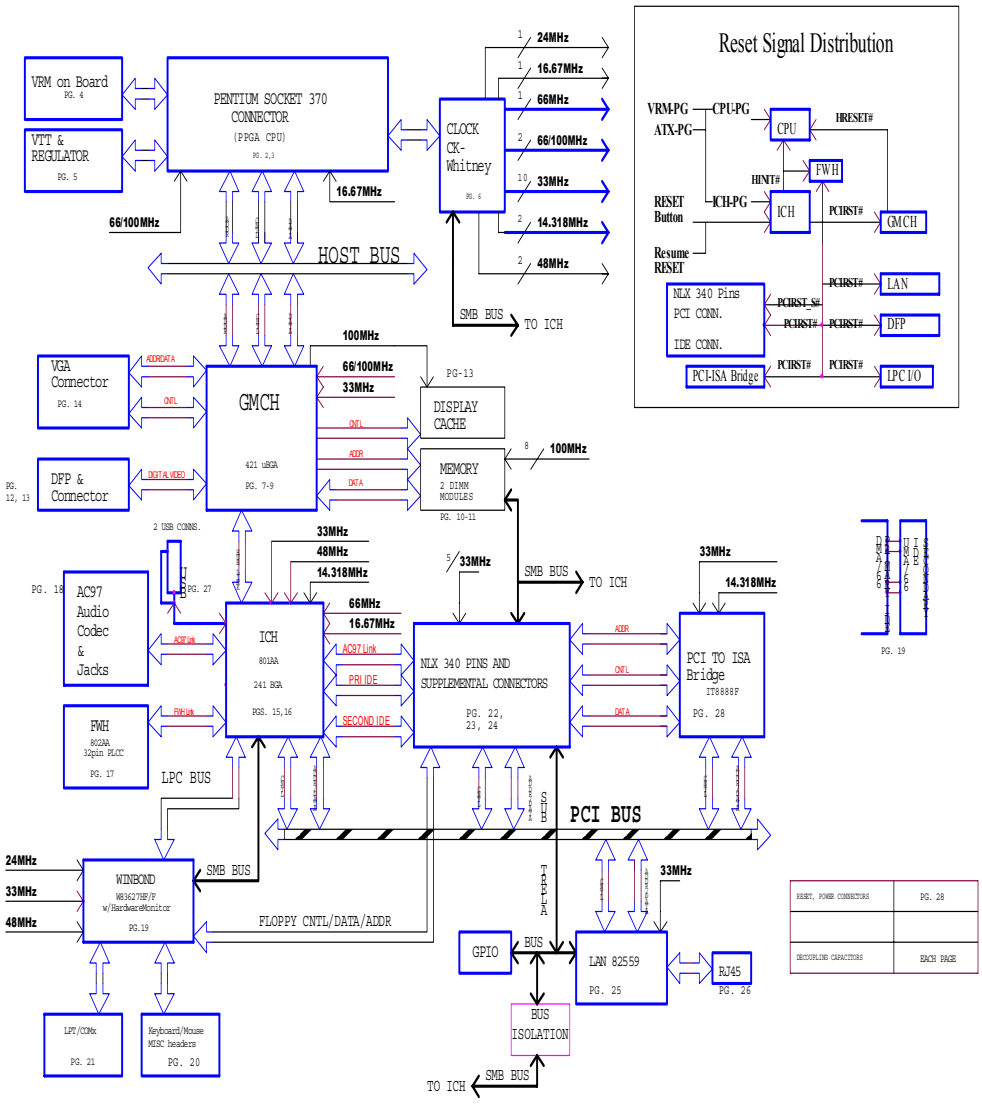
- PCI Local Bus Specification. Revision 2.2
- Advanced Configuration and Power Interface Specification. Revision 1.0
- Intel Celeron™ Processor User's Manual and Data Sheet
- Intel Graphics & Memory Controller Hub (GMCH) External Design Specification
- Intel I/O Controller Hub (ICH) External Design Specification
- Intel Firmware Hub (FWH) External Design Specification
- Winbond LPC I/O W83627HF & W83627F Data Sheet
- Intel 82559 LAN Controller External Design Specification
- NLX Motherboard Specification, Rev. 1.2
- Intel 810 Chipset: Intel 82810/82810-DC100 Graphics and Memory Controller Hub (GMCH) datasheet, April 1999, Order Number 290656-001

1

Introduction

This section provides an overview for the MicroATX Intel Celeron™ based PCI/ISA Printed Wiring Assembly (PWA) code-named "NL810". It describes functional blocks and their relationship. The following diagram shows the functional blocks of the NL810.

Figure 1-1. NL810 Motherboard Block Diagram



Overview

The NL810 is an implementation of BCM/BCM Advanced Research for a High-Volume NLX formfactor motherboard featuring these subsystems:

- Intel Celeron™ processor support through the Socket 370 connector
- Intel i810 chipset, "Whitney", (integrated graphics)
- PCI IDE Bus Master interface
- Integrated audio
- Embedded advanced I/O support (via LPC chip)
- USB (Universal Serial Bus)
- System Monitoring Hardware (via LPC chip)
- NLX form-factor motherboard

The targeted Operating Systems for the NL810 are: Windows 95, Windows 98 and Windows NT.

Processor Subsystem

The NL810 has provisions to support the Intel® Celeron™ Processors operating at either 66 or 100MHz Front Side Bus speed:

There are two (2) 168 pin DIMM sockets, supporting PC-100 DIMMs with SPD.

Cache Subsystem

The memory cache function for the Intel Celeron™ Processor is internal to the processor and no external cache is required.

Memory Subsystem

The NL810 DRAM controller supports a 64-bit memory data interface, optionally supporting 64-bit wide and 128-bit wide DIMM modules, without ECC/EC. The DRAM types supported are Synchronous DRAM (SDRAM). SDRAM is supported at 66 or 100 MHz.

The NL810 Main Memory interface provides two (2) 168-pin DIMM socket (DIMM0 and DIMM1) sites, allowing system memory from 8MB to 256MB of SDRAM.

The DIMM sockets support either single or double-sided **'Unbuffered DIMM'** modules. The installed DRAM type can be 8MB, 16MB, 32MB, 64MB or 128MB DIMMs. The DRAM Controller uses the JEDEC standard Serial Presence Detect (SPD) Mechanism to detect memory and array configurations, there is no jumper settings required for the memory size. Memory is automatically detected by the system BIOS.

Rules for Populating the DIMM memory array

- DIMM sockets can be populated in any order.
- The DRAM Timing register, which provides the DRAM speed grade control for the entire memory array, will be programmed to use the timings of the slowest DRAMs installed.

Data Integrity Subsystem

A data integrity feature included in the system is:

PCI Bus. The system implements parity generation/checking as defined by the PCI specification.

Graphics and Memory Controller Hub

The Graphics and Memory Controller Hub (GMCH) provides:

- Support for one processor
- 64-bit GTL+ based Host Bus Interface
- 32-bit Host Address support
- 64-bit System memory interface
- Integrated 2D & 3D graphics engine
- Integrated H/W motion compensation engine
- Integrated 230 MHz DAC
- Integrated digital video out port
- I/O Controller Hub interface (ICH)

I/O Controller Hub

The I/O Controller Hub (ICH) provides:

- PCI Rev 2.2 support
- Request/Grant pairs for PCI slots
- Power management support logic
- DMA contoller, Interrupt controller & timer functions
- Integrated IDE controller
- USB host interface for 2 USB ports
- System Management Bus (SMBus)
- AC'97 compliant link for audio and telephony CODECs
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support

Firmware Hub

The Firmware Hub (FWH) provides:

- Non-volatile memory for platform code and data
- A random number generator
- General Purpose Inputs (GPIs) for security/manageability features

The FWH component is part of the Intel 810 chipset and is available in 2Mb, 4Mb, and 8Mb capacities.

Embedded PCI Devices

PCI Bus Master IDE

ICH provides an integrated Bus Mastering IDE controller with two high performance IDE interfaces for up to four devices, such as Hard Drives and CD-ROM.

PCI Add-in Cards

High Performance PCI I/O cards can be used with the NL810 via the PCI connector slots on the NLX riser card. The ICH provides the PCI bus on the DR760 board and can support two on-board devices, the on-board LAN as well as the PCI to ISA bridge, and supports a maximum of 5 PCI slots via an NLX riser card.

Embedded Graphics Device

The GMCH provides integrated graphics capability. The GMCH is available in two configurations: one uses system memory for the display memory and the other (as a separate build configuration) works with an external display cache using industry standard SDRAMs. Display cache options are either 4MB or 0 MB.

Embedded I/O Subsystem

The Winbond LPC I/O W83627HF(or W83627F) represents the newest technology in functionality and integration for PC I/O. These two LPC I/O chips differ in that hardware monitor funtions are included as part of the W83627HF chip.
Some of the features of the LPC I/O are: Meets LPC Specification 1.0, 8042 keyboard controller. Infrared interface support for IrDA version 1.0, ASK-IR, and Consumer IR. Floppy disk interface (including 3-mode FDD). Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs. One EPP/ECP supported bi-directional parallel port. Game port. MIDI port. OnNow functions. Hardware monitor funtions (W83627HF only).

System Management Subsystem

The NL810 can support the System Monitor services using Winbond's W83627HF. The W83627HF is used to monitor Voltage, Temperature, Fan Speed and Open Case Intrusion as well as other system funtions.

Advanced Configuration and Power Interface "ACPI"

The NL810 supports the ACPI specification and its key elements. ACPI evolves the existing collection of power management BIOS code, APM APIs, PNP BIOS APIs, and so on into a well-specified power management and configuration mechanism. It provides support for an orderly transition from existing (legacy) hardware to ACPI hardware, and it allows for both mechanisms to exist in a single machine and be used as needed. ACPI evolves the existing motherboard configuration interfaces to support these advanced architectures in a more robust, and potentially more efficient manner.

Operating System directed Power Management (OSPM) provides a new appliance interface to customers. In particular, it provides for a sleep button. This sleep button is a "soft" button, which does not turn the machine physically off but signals the OS to go into a 'soft off' or sleeping state. ACPI defines two types of these "soft" buttons: one for putting the machine into sleep mode and one for putting the machine into 'soft off' mode.

This gives the OEM two different ways to implement machines: A one or a two-button(for TAIS) model. The button on the one-button model can be used as a power button or a sleep button as determined by user settings. The two-button model has an easily accessible sleep button and a separate power button. In either model, an override feature that forces the machine to turn off or to reset without OS consent is also needed to deal with various rare, but problematic, situations.

ACPI is neither a software nor a hardware specification, although it addresses both software and hardware and how they must behave. ACPI is actually an interface specification.

2

Functional Architecture

Processor Subsystem

The Intel Celeron™ Processor connects with the system through a 370-pin socket (PGA370) on the circuit board labelled PPGA The 370-pin configuration corresponds to a standard pinout that can accommodate Intel Celeron™ processors with CPU clock speed of upto 500MHz and 66 MHz Front Side Bus.

PGA 370 Socket Pinout

The 370-pin socket is provided to allow for easy configuration at the time of manufacture or as a field upgrade of the microprocessor.

Socket Type: Zero insertion force, female, 370 pin socket

Table 2.1 PGA 370 Pinout Description

Pin No.	Pin Name	Pin No.	Pin Name
A3	D29#	AC37	Reserved
A5	D28#	AD2	GND
A7	D43#	AD4	A31#
A9	D37#	AD6	$V_{REF\ 5}$
A11	D44#	AD32	$Vcc_{\ core}$
A13	D51#	AD34	GND
A15	D47#	AD36	$Vcc_{1\ 5}$
A17	D48#	AE1	A17#
A19	D57#	AE3	A22#
A21	D46#	AE5	Vcc_{core}
A23	D53#	AE33	A20M#
A25	D60#	AE35	IERR#
A27	D61#	AE37	FLUSH#
A29	Reserved	AF2	Vcc_{core}
A31	Reserved	AF4	Reserved
A33	Reserved	AF6	A25#
A35	PRDY#	AF32	GND
A37	GND	AF34	Vcc_{core}
AA1	A27#	AF36	GND
AA3	A30#	AG1	EDGCTRL
AA5	Vcc_{Core}	AG3	A19#
AA33	Reserved	AG5	GND
AA35	Reserved	AG33	INIT#
AA37	Vcc_{core}	AG35	STPCLK#
AB2	$Vcc_{\ core}$	AG37	IGNNE#
AB4	A24#	AH2	GND
AB6	A23#	AH4	Reserved
AB32	GND	AH6	A10#
AB34	Vcc_{core}	AH8	A5#
AB36	$Vcc_{\ cmos}$	AH10	A8#
AC1	Reserved	AH12	A4#
AC3	A20#	AH14	BNR#
AC5	GND	AH16	REQ1#
AC33	GND	AH18	REQ2#
AC35	FERR#	AH20	Reserved

Pin No.	Pin Name	Pin No.	Pin Name
AH22	RS1#	AK18	REQ0#
AH24	Vcc_{CORE}	AK20	LOCK#
AH26	RS0#	AK22	$VREF_7$
AH28	THERMTRIP#	AK24	Reserved
AH30	SLP#	AK26	PWRGOOD
AH32	Vcc_{CORE}	AK28	RS2#
AH34	GND	AK30	Reserved
AH36	Vcc_{CORE}	AK32	TMS
AJ1	A21#	AK34	Vcc_{CORE}
AJ3	GND	AK36	GND
AJ5	Vcc_{CORE}	AL1	GND
AJ7	GND	AL3	GND
AJ9	Vcc_{CORE}	AL5	A15#
AJ11	GND	AL7	A13#
AJ13	Vcc_{CORE}	AL9	A9#
AJ15	GND	AL11	Reserved
AJ17	Vcc_{CORE}	AL13	Reserved
AJ19	GND	AL15	A7#
AJ21	Vcc_{CORE}	AL17	REQ4#
AJ23	GND	AL19	REQ3#
AJ25	Vcc_{CORE}	AL21	Reserved
AJ17	GND	AL23	HITM#
AJ29	Vcc_{CORE}	AL25	HIT#
AJ31	GND	AL27	DBSY#
AJ33	BSEL	AL29	THERMDN
AJ35	SMI#	AL31	THERMDP
AJ37	VID3	AL33	TCK
AK2	Vcc_{CORE}	AL35	VID0
AK4	GND	AL37	VID2
AK6	A28#	AM2	GND
AK8	A3#	AM4	Vcc_{CORE}
AK10	A11#	AM6	GND
AK12	$VREF_6$	AM8	Vcc_{CORE}
AK14	A14#	AM10	GND
AK16	Reserved	AM12	Vcc_{CORE}

Pin No.	Pin Name	Pin No.	Pin Name
AM14	GND	B12	GND
AM16	Vcc_{CORE}	B14	Vcc_{CORE}
AM18	GND	B16	GND
AM20	Vcc_{CORE}	B18	Vcc_{CORE}
AM22	GND	B20	GND
AM24	Vcc_{CORE}	B22	Vcc_{CORE}
AM26	GND	B24	GND
AM28	Vcc_{CORE}	B26	Vcc_{CORE}
AM30	GND	B28	GND
AM32	Vcc_{CORE}	B30	Vcc_{CORE}
AM34	GND	B32	GND
AM36	VID1	B34	Vcc_{CORE}
AN3	GND	B36	Reserved
AN5	A12#	C1	D33#
AN7	A16#	C3	Vcc_{CORE}
AN9	A6#	C5	D31#
AN11	Reserved	C7	D34#
AN13	Reserved	C9	D36#
AN15	Reserved	C11	D45#
AN17	BPRI#	C13	D49#
AN19	DEFER#	C15	D40#
AN21	Reserved	C17	D59#
AN23	Reserved	C19	D55#
AN25	TRDY#	C21	D54#
AN27	DRDY#	C23	D58#
AN29	BR0#	C25	D50#
AN31	ADS#	C27	D56#
AN33	TRST#	C29	Reserved
AN35	TDI	C31	Reserved
AN37	TDO	C33	Reserved
B2	D35#	C35	BPM0#
B4	GND	C37	CPURES#
B6	Vcc_{CORE}	D2	GND
B8	GND	D4	GND
B10	Vcc_{CORE}	D6	Vcc_{CORE}

Pin No.	Pin Name	Pin No.	Pin Name
D8	D38#	F4	Vcc_{CORE}
D10	D39#	F6	D32#
D12	D42#	F8	D22#
D14	D41#	F10	Reserved
D16	D52#	F12	D27#
D18	GND	F14	Vcc_{CORE}
D20	Vcc_{CORE}	F16	D63#
D22	GND	F18	$VREF_1$
D24	Vcc_{CORE}	F20	GND
D26	GND	F22	Vcc_{CORE}
D28	Vcc_{CORE}	F24	GND
D30	GND	F26	Vcc_{CORE}
D32	Vcc_{CORE}	F28	GND
D34	GND	F30	Vcc_{CORE}
D36	Vcc_{CORE}	F32	GND
E1	D26#	F34	Vcc_{CORE}
E3	D25#	F36	GND
E5	Vcc_{CORE}	G1	D21#
E7	GND	G3	D23#
E9	Vcc_{CORE}	G5	GND
E11	GND	G33	BP2#
E13	Vcc_{CORE}	G35	Reserved
E15	GND	G37	Reserved
E17	Vcc_{CORE}	H2	GND
E19	GND	H4	D16#
E21	$VCORE_{DET}$	H6	D19#
E23	Reserved	H32	Vcc_{CORE}
E25	D62#	H34	GND
E27	RTTCTRL	H36	Vcc_{CORE}
E29	Reserved	J1	D7#
E31	Reserved	J3	D30#
E33	VREF0	J5	Vcc_{CORE}
E35	BPM1#	J33	PICCLK
E37	BP3#	J35	PICD0
F2	Vcc_{CORE}	J37	PREQ#

Pin No.	Pin Name	Pin No.	Pin Name
K2	Vcc_{CORE}	Q37	Reserved
K4	$VREF_2$	R2	Reserved
K6	D24#	R4	D17#
K32	Vcc_{CORE}	R6	$VREF_3$
K34	Vcc_{CORE}	R32	Vcc_{CORE}
K36	GND	R34	GND
L1	D13#	R36	Vcc_{CORE}
L3	D20#	S1	D8#
L5	GND	S3	D5#
L33	Reserved	S5	Vcc_{CORE}
L35	PICD1	S33	Reserved
L37	LINT1/NMI	S35	SLEWCTRL
M2	GND	S37	Reserved
M4	D11#	T2	Vcc_{CORE}
M6	D3#	T4	D1#
M32	Vcc_{CORE}	T6	D6#
M34	GND	T32	GND
M36	LINT0/INTR	T34	Vcc_{CORE}
N1	D2#	T36	GND
N3	D14#	U1	D4#
N5	Vcc_{CORE}	U3	D15#
N33	Reserved	U5	GND
N35	Reserved	U33	PLL2
N37	Reserved	U35	Reserved
P2	Vcc_{CORE}	U37	Reserved
P4	D18#	V2	GND
P6	D9#	V4	Reserved
P32	GND	V6	V REF 1
P34	Vcc_{CORE}	V32	Vcc_{CORE}
P36	GND	V34	GND
Q1	D12#	V36	Vcc_{CORE}
Q3	D10#	W1	D0#
Q5	GND	W3	Reserved
Q33	Reserved	W5	Vcc_{CORE}
Q35	Reserved	W33	PLL1

Pin No.	Pin Name	Pin No.	Pin Name
W35	Reserved	Y5	GND
W37	BCLK	Y33	GND
X2	Reserved	Y35	Vcc_{CORE}
X4	RESET#	Y37	GND
X6	Reserved	Z2	GND
X32	GND	Z4	A29#
X34	Vcc_{CORE}	Z6	A18#
X36	GND	Z32	Vcc_{CORE}
Y1	Reserved	Z34	GND
Y3	A26#	Z36	$Vcc_{2\ 5}$

Processor Upgrade

The Intel Celeron™ processor maybe removed and replaced to accommodate supported higher speed processors. Changes to the VCORE (Core Voltage Selection) are automatically adjusted.

Processor Heat Sink

The NL810 M/B provides 12V power for the cooling fan through a 3-pin header with Fan-On control and Fan Speed detection.

Memory Subsystem

DRAM Subsystem

The NL810 has two 64-bit (168-pin) DIMM sockets (DIMM0 and DIMM1) allowing system memory from 8 MB to 512MB of main DRAM, using two 256MB at 128bit technology. There are no jumpers settings required for the memory size, which is automatically detected by the system BIOS.

The DIMMs are rated 100 MHz SDRAM (Synchronous DRAM). DIMM modules must be 'Unbuffered' and operate at 3.3V. All the allowable memory size configurations are described on table 2.1 (Refer to Table 3.6 in the "Configuration" section for the different combinations and sizes of DIMMs).

Table 2.2. DRAM memory configurations in Megabytes.

8	16	24	32	40	48
64	72	80	96	128	136
144	176	192	256		

DRAM (DIMM) Sockets

Connection to the main system DRAM can be done via two (2) DIMM connectors on the system PWA.

Reference: DIMM0, DIMM1
Connector Type: female, 168 pin DIMM, in-line connector

Table 2.3. DRAM DIMM Pinout Description

Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	/OE2	86	DQ32	128	DU
3	DQ1	45	/RAS2	87	DQ33	129	/RAS3
4	DQ2	46	/CAS2	88	DQ34	130	/CAS6
5	DQ3	47	/CAS3	89	DQ35	131	/CAS7
6	Vcc	48	/WE2	90	Vcc	132	DU
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	DU	104	DQ47	146	DU
21	NC	63	NC	105	NC	147	NC
22	NC	64	Vss	106	NC	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	/WE0	69	DQ24	111	DU	153	DQ56
28	/CAS0	70	DQ25	112	/CAS4	154	DQ57
29	/CAS1	71	DQ26	113	/CAS5	155	DQ58
30	/RAS0	72	DQ27	114	/RAS1	156	DQ59
31	/OE0	73	Vcc	115	DU	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	A11	164	NC
39	A12	81	NC	123	A13	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	DU	167	SA2
42	DU	84	Vcc	126	DU	168	Vcc

Note: DU = Don't Use, NC = Not Connected

System BIOS

The system and video BIOS are stored in a 4M-bit Firmware Hub (FWH). The system BIOS is always shadowed and cached.

L2 Cache Subsystem

The Intel Socket 370 Celeron™ PPGA CPU has an integrated 0KB/128KB L2 cache. There is no L2 memory cache external to the CPU.

Graphics/Video Subsystem

The Graphics and Memory Controller Hub (GMCH) includes a highly integrated graphics accelerator. Its architecture consists of dedicated multi-media engines executing in parallel to deliver high performance 3D, 2D and motion compensation video capabilities. The 3D and 2D engines are managed by a 3D/2D pipeline preprocessor allowing a sustained flow of graphics to be rendered and displayed. The deeply pipelined 3D accelerator engine provides 3D graphics quality and performance via per-pixel3D rendering and parallel data paths which allow each pipeline stage to simultaneously operate on different primitives or portions of the same primitive. The GMCH graphics accelerator engine supports perspective-correct texture mapping, bilinear and anisotropic Mip-Mapping, Gouraud shading, blending, fogging, and Z-buffering. A rich set of 3D instructions permit these features to be independently enabled or disabled.

The GMCH with DDM+ supports a Display Cache (DC). Textures and display buffer can be located in the system memory and the display cache can be used for back and Z-buffers, bitmaps, etc. In addition, the GMCH supports a memory interface that will allow all graphics rendering to take place in system memory, thus eliminating the need for the display cache.

The GMCH integrated accelerator's 2D capabilities include BLT and arithmetic STRBLT engines, a hardware cursor and an extensive set of 2D registers and instructions. The high performance 64-bit BitBLT engine provides hardware acceleration for many common Windows operations.

In addition to its 2D/3D capabilities, the GMCH integrated graphics accelerator also supports full MPEG-2 motion compensation for software-assisted DVD video playback, a VESA DDC2B compiant display interface and a digital video out port which supports (via a plug-in adaptor card) NTSC and PAL broadcast standards.

Video Modes

The GMCH supports a wide range of resolutions, color depths, and refresh rates via a programmable dot clock that has a maximum frequency of 230 MHz.

Table 2.9 Partial list of Display Modes Supported

Resolution	Bits Per Pixel (frequency in Hz)		
	8-bit Indexed	16-bit	24-bit
320x200	70	70	70
320x240	70	70	70
352x480	70	70	70
352x576	70	70	70
400x300	70	70	70
512x384	70	70	70
640x400	70	70	70
640x480	60,70,72,75,85	60,70,72,75,85	60,70,75,85
720x480	75,85	75,85	75,85
720x576	60,75,85	60,75,85	60,75,85
800x600	60,70,72,75,85	60,70,72,75,85	60,70,75,85
1024x768	60,70,72,75,85	60,70,72,75,85	60,70,75,85
1152x864	60,70,72,75,85	60,70,72,75,85	60,70,75,85
1280x720	60,75,85	60,75,85	60,75,85
1280x960	60,75,85	60,75,85	60,75,85
1280x1024	60,70,72,75,85	60,70,72,75,85	60,70,75,85
1600x900	60,75,85	60,75,85	-
1600x1200	60,70,72,75,85	-	-

Video Memory

Standard video operation on the NL810 uses system memory for video memory. Enhanced video performance for the NL810 is available with the optional display cache. This is a manufacturing option, not a field upgrade. This option requires a specific configuration of the GMCH and two 16Mb x 1 100MHz SDRAM chips for a total of 4MB video memory.

Video (Monitor) Connector

Connection to VGA monitor is via a connector on the rear panel on the system PWA.

Reference: J15 (Video)
Connector Type: female, high density DB15S, 15-pin AT-compatible

Table 2.10. Video Monitor Connector Pinout

PIN	Description
1	RED
2	GREEN
3	BLUE
4	N/C
5	LOGIC-GROUND
6	RED GROUND RETURN
7	GREEN GROUND RETURN
8	BLUE GROUND RETURN
9	+5V PULL-UP
10	LOGIC GROUND
11	N/C
12	DDC DAT
13	HORIZONTAL-SYNC
14	VERTICAL-SYNC
15	DDC CLK
16	LOGIC-GROUND[1]
17	LOGIC-GROUND[1]

1: Pins 16 and 17 are connector mounting holes connected to logic ground.

Digital Flat Panel Connector (Option)

This connector provides an interface to support the Digital Flat Panel (DFP) capability. The connector allows a riser card to be added to the board which contains the circuitry to provide this feature.

Table 2.11 JU1 – DFP

Pin	Description	Pin	Description
1	TX1+	2	TX1-
3	GND	4	GND
5	TXC+	6	TXC-
7	GND	8	VCC
9	N/C	10	N/C
11	TX2+	12	TX2-
13	GND	14	GND
15	TX0+	16	TX0-
17	N/C	18	EDGE/CHG
19	VFTSDA	20	VFTSCL
21	CASE GDN	22	CASE GND

Sound Subsystem

The NL810 provides audio using the I/O Controller Hub (ICH) and an AC'97 audio codec.

Audio using ICH

The ICH is an AC'97 2.1 compliant controller that communicates with companion codecs via a digital serial link called AC-link. All digital audio streams and commands.status information is communicated over the AC-link.

The ICH supports the following features:

- Independent PCI functions for audio and modem
- Independent channels for PCM in and PCM out, microphone in
- Left and right audio channels
- 16 bit sample resolution
- Multiple sample rates

Microphone In Connector

An external accessible jack connector is soldered to the PWA to allow the connection of a microphone for voice input.

Reference: J4 (MIC IN)

Line Out Connector

An external accessible jack connector is soldered to the PWA to allow the connection of a Line-Out for speaker.

Reference: J1 (Line-Out)

Aux – In (Optional)

An internal accessible header is soldered to the PWA to allow the connection of a Line-In for input.

Reference: J2 (Aux-In)

Line – In (Optional)

An internal accessible header is soldered to the PWA to allow the connection of a Line-In for input.

Reference:: J7 (Line-In)

PCI/ISA Expansion Slots

NLX ISA/PCI Expansion Slots

The NL810 motherboard support ISA and PCI expansion buses through an NLX Edge type connector. The NLX riser card also has the IDE, Floppy and front panel connectors. The Edge connector mates with a NLX riser card containing the needed ISA/PCI connectors to match the chassis used. The NXL expansion connector supplies all the necessary signals to implement up to four (4) ISA and four (4) PCI slots. The NL810 will support an ISA only, PCI only or shared ISA/PCI NLX riser card.

ISA Interface

The NL810 incorporates a fully ISA (AT) bus compatible master and slave interface that is compatible with the IEEE 996 specification. The ISA interface also provides byte swap logic and I/O recovery support.

The ISA interface supports the following types of cycles:

- PCI master-initiated I/O and memory cycles to the ISA bus
- DMA compatible cycles between main memory and ISA I/O and between ISA I/O and ISA memory
- Enhanced DMA cycles between PCI memory and ISA I/O
- ISA refresh cycles initiated by either the controller or an external master
- ISA master-initiated memory cycles to PCI and ISA master-initiated I/O cycles to the controller registers

ISA Bus Speed

Dividing the PCI clock by 4 generates the ISA system clock. The divide by 4 setting is used for 30MHz and 33MHz PCI bus speed. The frequencies supported are 7.5MHz and 8.33MHz.

AT Bus Refresh

The NL810 system board supports *hidden* refresh cycles which allows the CPU to continue to execute unless an AT bus cycle is attempted coincident with the AT bus refresh cycle (ISA Bus refresh cycles are completely de-coupled from DRAM Refresh). Transactions driven by PCI masters that target ISA or IDE resources while refresh is active are held off with wait states until the refresh is complete.

NXL Card Edge Connector

The NLX motherboard connects to the riser with a 340-pin (2x170), card edge connector. The "A" side is the bottom (secondary) side of the motherboard, and the "B" side is the top (primary) side of the motherboard.

Reference: P1
Connector Type: Edge type, 340 pins, and double-sided edge connector

Table 2.14. NLX Riser Card Connector

PIN	SIGNAL NAME	PIN	SIGNAL NAME
B1	NC	A1	-12V
B2	+12V	A2	P_REQ4#
B3	SPKROUT	A3	+12V
B4	+12V	A4	P_GNT4#
B5	PCLKS0	A5	+3.3V
B6	GND	A6	PIRQD#
B7	PCLKS1	A7	+3.3V
B8	SER_IRQ	A8	PIRQA#
B9	PIRQC-	A9	PIRQB#
B10	+3.3V	A10	PCLKS2
B11	PCLKS3	A11	+3.3V
B12	GND	A12	PCIRST#
B13	P_GNT3#	A13	P_GNT0#
B14	+3.3V	A14	PCLK54
B15	P_GNT2-	A15	GND
B16	A_D31	A16	P_GNT1#
B17	P_REQ0-	A17	+3.3V
B18	GND	A18	P_REQ2#
B19	A_D29	A19	P_REQ3#
B20	A_D28	A20	A_D30

B21	A_D26	A21	GND
B22	+3.3V	A22	A_D25
B23	A_D24	A23	P_REQ1#
B24	C_BE3-	A24	A_D27
B25	A_D22	A25	+3.3V
B26	GND	A26	A_D23
B27	A_D21	A27	A_D20
B28	A_D19	A28	A_D18
B29	A_D16	A29	GND
B30	+3.3V	A30	A_D17
B31	C_BE2-	A31	IRDY#
B32	FRAME-	A32	DEVSEL#
B33	TRDY-	A33	+3.3V
B34	GND	A34	STOP#
B35	NC	A35	NEC
B36	PLOCK-	A36	SERR#
B37	NC	A37	GND
B38	+3.3V	A38	C_BE1#-
B39	A_D15	A39	A_D13
B40	PAR	A40	A_D10
B41	A_D14	A41	GND
B42	GND	A42	C_BE03
B43	A_D11	A43	A_D0
B44	A_D12	A44	A_D6
B45	A_D9	A45	+3.3V
B46	+3.3V	A46	A_D5
B47	A_D8	A47	A_D1
B48	A_D7	A48	A_D3
B49	A_D4	A49	GND
B50	GND	A50	A_D2
B51	NC	A51	VCC
B52	VCC	A52	RSTDRV
B53	IRQ9	A53	IOCHK3#
B54	DREQ2	A54	SD6
B55	SD3	A55	SD7
B56	ZEROWS-	A56	SD4
B57	SD1	A57	VCC
B58	AEN	A58	SD2
B59	IOCHRDY	A59	SD5
B60	SA18	A60	SD0
B61	SMEMR-	A61	SMEMW#
B62	SA16	A62	SA19
B63	IOR-	A63	IOW#
B64	DREQ3	A64	SA17
B65	SA15	A65	GND
B66	GND	A66	DACK3#
B67	SA13	A67	SA14
B68	VCC	A68	DACK1#
B69	REFRESH-	A69	DREQ1
B70	SA11	A70	SA12
B71	SA10	A71	SLSCLK
B72	IRQ7	A72	SA9
B73	IRQ6	A73	VCC
B74	SA8	A74	IRQ5
B75	SA6	A75	SA7
B76	DACK2-	A76	IRQ3
B77	SA4	A77	IRQ4

B78	GND	A78	SA5
B79	SA3	A79	TC
B80	SA2	A80	BALE
B81	SA1	A81	GND
B82	SA0	A82	OSC_0
B83	SBHE-	A83	IOCS16#
B84	LA23	A84	MEMCS16#
B85	LA22	A85	IRQ11
B86	LA21	A86	IRQ10
B87	LA20	A87	IRQ15
B88	LA19	A88	IRQ12
B89	LA18	A89	GND
B90	LA17	A90	IRQ14
B91	DACK0-	A91	DREQ0
B92	DACK5-	A92	MEMR#
B93	SD8	A93	MEMW#
B94	DACK6-	A94	SD9
B95	SD10	A95	DREQ5
B96	VCC	A96	DREQ6
B97	SD11	A97	VCC
B98	DREQ7	A98	SD12
B99	SD13	A99	DACK7#
B100	SD15	A100	SD14
B101	GND	A101	RMASTER#
B102	GND	A102	DDA8
B103	DDA7	A103	BRSTDRV#
B104	DDA6	A104	DDA9
B105	DDA5	A105	VCC
B106	DDA11	A106	DDA4
B107	DDA12	A107	DDA10
B108	GND	A108	DDA3
B109	DDA14	A109	DDA13
B110	DDA2	A110	DDA1
B111	DDA0	A111	GND
B112	DDA15	A112	PDIOW#
B113	PDIOR-	A113	PDDREQ
B114	IDEA_CSEL	A114	PIORDY
B115	IRQ14	A115	PDDACK#
B116	VCC	A116	NC
B117	DAP1	A117	DAP2
B118	DAP0	A118	TCS1P#
B119	TCS3P-	A119	VCC
B120	DDB8	A120	NC
B121	DDB7	A121	BRSTDRV#
B122	GND	A122	DDB9
B123	DDB10	A123	DDB6
B124	VCC	A124	DDB5
B125	DDB4	A125	DDB11
B126	DDB3	A126	DDB12
B127	DDB13	A127	GND
B128	DDB14	A128	DDB2
B129	DDB1	A129	DDB15
B130	DDB0	A130	SDIOW#
B131	SDIOR-	A131	SDDREQ
B132	IDEB_CSEL	A132	SIORDY
B133	IRQ15	A133	GND
B134	DAS1	A134	SDDACK#

B135	DAS2	A135	NC
B136	TCS3S-	A136	DAS0
B137	NC	A137	TCS1S#
B138	GND	A138	NC
B139	DRATE0#	A139	VCC
B140	DR1#	A140	NC
B141	DR0#	A141	DENSEL
B142	DIR#	A142	MTR0#
B143	NC	A143	INDEX#
B144	GND	A144	MTR1#
B145	WDATA#	A145	GND
B146	TRK0#	A146	WGATE#
B147	NC	A147	STEP#
B148	RDATA#	A148	WP#
B149	DSKCHG#	A149	HDSEL#
B150	GND	A150	NC
B151	NC	A151	NC
B152	NC	A152	FANTACH1
B153	IR_MODE	A153	FNATACH2
B154	IR_TX	A154	NC
B155	IR_RX	A155	FAN-CTL
B156	FP_SLEEP#	A156	VCC
B157	FP_RST	A157	NC
B158	GND	A158	NC
B159	GRN/PWR-	A159	NC
B160	PWRGOOD	A160	NC
B161	S_ON/OFF	A161	NC
B162	PS_ON#	A162	NC
B163	LAN_WAKE	A163	GND
B164	NC	A164	NC
B165	MODEM WAKE	A165	TAMP_DET-
B166	NC	A166	NC
B167	NC	A167	NC
B168	NC	A168	NC
B169	NC	A169	5VSB
B170	-5V	A170	3.3VSEN

PCI DEVICES (ON-BOARD)

PCI Device Name	PCI Device Number	Function Number	PCI Device Type	PCI IDSEL Line	PCI Interrupt Line	
					Device	Bus
GMCH	00h	0	System and Graphic Controller	N/A	N/A	N/A
GMCH	01h	0	Integrated Graphics Device	N/A	INTA#	PIRQ0#
					ACPI Interrupt 16	
ICH	1Fh	0	LPC Bridge	AD31	N/A	N/A
		1	IDE controller		INTA#	IRQ14
					ACPI Interrupt 14	
		2	USB controller		INTC#	PIRQ2#
					ACPI Interrupt 18	
		3	SMbus Controller		INTB#	PIRQ1#

		4 5 6 7	Reserved AC97 Audio Ctrl AC97 Modem Ctrl Reserved		ACPI Interrupt 17 N/A INTB# PIRQ1# ACPI Interrupt 17 INTB# PIRQ1# ACPI Interrupt 17 N/A
ICH	1Eh	0	PCI Bridge	AD30	
PCI to ISA IT8888F	Bus 1 06h	All	Master REQA#/GNTA#	AD22	Serial IRQ Serial IRQ
LAN	Bus1 08h	All	Master REQB#/GNTB#	AD24	INTA# PIRQ2#
PCI Slot 0	Bus1 0Fh	All	REQ0#/GNT0#	AD31	INTA# PIRQ0# INTB# PIRQ1# INTC# PIRQ2# INTD# PIRQ3#
PCI slot1	Bus1 0Dh	All	Master PREQ1#/PGNT1#	AD29	INTA# PIRQ1# INTB# PIRQ2# INTC# PIRQ3# INTD# PIRQ0#
PCI slot2	Bus1 09h	All	Master PREQ3#/PGNT3#	AD25	INTA# PIRQ3# INTB# PIRQ0# INTC# PIRQ1# INTD# PIRQ2#
PCI slot3	Bus1 07h	All	Master PREQ4#/PGNT4#	AD23	INTA# PIRQ0# INTB# PIRQ1# INTC# PIRQ2# INTD# PIRQ3#
Riser 82559 LAN	Bus1 0Bh	All	Master PREQ2#/PGNT2#	AD27	INTA# PIRQ2#

GPI/O

GPI: The NL810 ICH provides the following GPIs:

ICH GPI Port	Purpose	Usage
GPIO0	ISA REQ pin	REQA#
GPIO1	LAN REQ pin	REQB#
GPIO6	Clear Password	1 = normal operation mode 0 = clear password.

GPIO7	PCI signal - PERR#	PERR#
GPIO8	Sleep button	0 -> 1 transition will toggle sleep mode.
GPIO9	AC97 CODEC 2nd data input	AC_SDIN1
GPIO5/10/12	None	None
GPIO13	LPC super I/O Power Management Event	1 = normal operation mode 0 = power management event happened.

GPO: The NL810 ICH provides the following GPOs:

ICH GPO Port	Purpose	Usage
GPIO16	ISA GNT pin	GNTA#
GPIO17	LAN GNT pin	GNTB#
GPIO21	IT8888F NOGO control	NOGO
GPIO23	Audio output control	0 = Normal operation. 1 = No sound output.
GPIO24	ACPI S3 state power control	0 = Indicate system is in S3 (STR) state. 1 = Normal operation
GPIO25/27/28	None	None
GPIO26	Suspend clock in S3/S5 state	Suspend clock output

Storage Subsystem

IDE Interface (NLX connector)

The NL810, via the I/O Controller Hub, (ICH) provides:

- independent timing of up to 4 drives
- PIO Mode 4 transfers
- Supports UltraDMA/66 mode (66 MB/sec)
- Supports UltraDMA/33 mode (33 MB/sec)
- Separate IDE connection for primary and secondary connectors

Floppy Disk Drive Interface (NLX connector)

The NL810, via the Winbond LPC I/O, provides an integrated floppy disk controller compatible with the industry standard 82077/765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic.
The FDC can control one (720KB, 1.2, 1.44 or 2.88 in 3.5 inch format only) floppy disks or compatible tape drives.

I/O Subsystem

The I/O Subsystem consists of a single component from Winbond. The NL810 uses the Winbond LPC I/O "W83627HF" (or W83627F if hardware monitoring features are not required).

The LPC I/O device provides two async serial ports (UARTs) with high speed 16550 and 16-byte FIFO, one Parallel port supporting EPP, ECP and Centronics Bi-directional modes, PS/2 keyboard port (using Phoenix MultiKey Firmware), mouse port and game/MIDI port. W83627HF also includes system hardware monitor functions.

Serial Ports

The NL810 has two (2) UARTs compatible serial ports configured as Data Terminal Equipment (DTE). The electrical characteristics are compliant with the EIA-232-D Serial Communications Specifications
One port (COM1) is available through a connector and is located on the rear panel of the system PWA. The second port (COM2) is available through a header on the PWA.

Reference: J11(COM1)
Connector Type: male, 9 pin metal shell D-SUB

Table 2.12. COM1 Connector Pinout.

PIN	DESCRIPTION
1	DATA-CARRIER-DETECT (DCD)
2	RECEIVE-DATA (RXD)
3	TRANSMIT-DATA (TXD)
4	DATA-TERMINAL-READY (DTR)
5	LOGIC-GROUND
6	DATA-SET-READY (DSR)
7	REQUEST-TO-SEND (RTS)
8	CLEAR-TO-SEND (CTS)
9	RING-INDICATOR (RI)
10	SHELL-GROUND[1]
11	SHELL-GROUND[1]

[1]: Pins 10 and 11 (Shell Ground) are mounting holes connected to the metal connector housing on serial port 1.

Table 2.13. COM 2 Header Pinout. (J12)

Pin	Description	Pin	Description
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI	**10**	**NO-PIN(KEY)**

There will be no-pin in position 10 on motherboard.
Cable will have a key in position 10

Parallel Port

The system PWA has a single, bi-directional parallel port (EPP/ECP compatible). The parallel port is capable of being disabled or remapped to either the secondary LPT address or the tertiary LPT address through BIOS if other parallel ports are installed in the system
A connector is located on the rear panel of the system PWA for the external connection to the port. The parallel port interface contains 12mA source output drivers on the drive interface, and incorporates circuitry for protection against damage due to printer Power-On.

Reference: J13 (PARALLEL)
Connector Type: female, 25 pin metal shell D-SUB

Table 2.14. Printer Port Connector Pinout

PIN	DESCRIPTION
1	STROBE*
2	PD0
3	PD1
4	PD2
5	PD3
6	PD4
7	PD5
8	PD6
9	PD7
10	ACKNOWLEDGE*
11	BUSY
12	PAPER-END (PE)
13	SELECT
14	AUTO-FEED*
15	ERROR*
16	INIT*
17	SELECT -IN*
18	LOGIC-GROUND
19	LOGIC-GROUND
20	LOGIC-GROUND
21	LOGIC-GROUND
22	LOGIC-GROUND
23	LOGIC-GROUND
24	LOGIC-GROUND
25	LOGIC-GROUND
26	SHELL-GROUND[1]
27	SHELL-GROUND[1]

1: Pins 26 and 27 are connector-mounting holes connected to the metal connector housing.

Keyboard Interface

The system PWA has a PS/2-compatible keyboard interface. The shielded keyboard interface connector has a PS/2-compatible pinout and is located on the rear panel on the system PWA, this connector is a dual package with the Mouse connector residing on top. To meet the requirements for UL compliance, the Vcc pin (pin 4) is connected through a fuse prior to connection to the external connector.

Reference: J8 (KEYBOARD) closest to NLX connector
Connector Type: female, 6-pin metal shield mini-DIN

Table 2.15. Keyboard Connector Pinout

PIN	DESCRIPTION
1	KEYBOARD-DATA
2	N/C
3	LOGIC-GROUND
4	KEYBOARD-Vcc
5	KEYBOARD-CLOCK
6	N/C
7	SHELL-GROUND[1]
8	SHELL-GROUND[1]
9	SHELL-GROUND[1]

1: Pins 7-9 are, connector-mounting hole pins connected to the metal connector housing

Mouse Interface

The system PWA has a PS/2-compatible mouse interface. A connector, utilizing PS/2 pinouts, is located on the rear panel on the system PWA. To meet the requirements for UL compliance the Vcc pin (pin 4) was connected through a fuse prior to connection to the external connector.

Reference: J9 (MOUSE)
Connector Type: female, 6-pin metal shield mini-DN

Table 2.16. Mouse Connector Pinout

PIN	DESCRIPTION
1	MOUSE-DATA
2	N/C
3	LOGIC-GROUND
4	MOUSE-Vcc
5	MOUSE-CLOCK
6	N/C
7	SHELL-GROUND[1]
8	SHELL-GROUND[1]
9	SHELL-GROUND[1]

1: Pins 7-9 are connector-mounting hole pins connected to the metal connector housing.

Universal Serial Bus Connectors

The Universal Serial Bus (USB) is a communications architecture that gives a PC the ability to interconnect a variety of devices via a simple four-wire cable. The USB is actually a two-wire serial communication link that runs at 12 megabits (Mbs) per second.

The NL810 is equipped with two USB Serial Ports. Both of these ports are available at the back panel via industry-standard USB connectors. The NL810 also has a USB header which may be used to provide a USB port, via system cable, at the front of the system.

Reference: J (USB1,top + USB2,bottom)
Connector Type: USB CONN, DUAL

Table 2.17. USB-1 & 2 Connector Pinout

PIN	DESCRIPTION	COMMENT
1	VCC	Cable power
2	- Data	
3	+ Data	
4	Ground	Cable ground

Real-Time Clock

The Real Time Clock (RTC) is integrated into the ICH chip. The RTC provides battery backed-up date and time keeping device with two banks of static RAM with 128 bytes each. The design is meant to be functionally compatible the Motorola MS146818B. The ICH supports Year 2000 rollover.
The static RAM can be set to specific values or cleared to the system default values using the BIOS SETUP program. Also, to prevent a lock-up situation the RAM values can be cleared to the system defaults by using the CLR CMOS jumper on the PWA.

Non-volatile CMOS Memory Battery

An external coin-cell style battery provides power to the RTC and CMOS memory when system power is removed. The battery has an estimated lifetime of seven years and is socketed for easy replacement.

Reference: BT1
Socket Type: COIN TYPE

Miscellaneous Connectors

CPU Fan Connector

A 1 x 3 straight header is available on the PWA to drive the CPU mounted cooling fan and provide the system with the Fan's tachometer input.

Reference: J14 (FAN)
Connector Type: 1 x 3 male straight 0.100

Pin	Description
1	GND
2	Fan Ctrl(+12V)
3	Fan Sensor

IRDA/Consumer IR header (option)

J5 provides the interface for infrared devices

Pin 1: SB5V
Pin 2: NC
Pin 3: IRRX
Pin 4: GND
Pin 5: IRTX
Pin 6: CIRRX

User Configurable Jumpers

JP5: FWH Lock. (Default is OFF)

This feature provides a "boot-block" protection feature so that the primitive BIOS loader in the FWH can not be erased

ON: Unlock

OFF: Lock

JP3: Clear Password (Default is OFF)

1-2: Clear Password

JP2: On board Codec select jumper. (Default is 1-2)

This feature is used to select the on-board codec for the AMR riser card.

1-2: Enable

2-3: Disable

3

Configuration

Product Configuration

The PWA component will be produced by BCM without the microprocessor installed. It is assumed that the microprocessor will be installed during the customer's integration process. The same applies to the system memory DIMMs.

Processor Speed Select Jumpers

There are no CPU speed selection jumpers since the Intel Celeron™ processor has its speed fixed internally.

DRAM Subsystem Configurations

The NL810 supports 8 MB to 256MB of system RAM. The allowable memory configurations are shown below:

Table 3.2. DIMMs Configurations

DIMM0	DIMM1	Total Memory
8MB	EMPTY	8MB
8MB	8MB	16MB
16MB	EMPTY	16MB
16MB	8MB	24MB
16MB	16MB	32MB
32MB	EMPTY	32MB
32MB	8MB	40MB
32MB	16MB	48MB
32MB	32MB	64MB
64MB	EMPTY	64MB
64MB	8MB	72MB
64MB	16MB	80MB
64MB	32MB	96MB
64MB	64MB	128MB
128MB	EMPTY	128MB
128MB	8MB	136MB
128MB	16MB	144MB
128MB	32MB	176MB
128MB	64MB	192MB
128MB	128MB	256MB
256MB	256MB	512MB

For simplicity other memory configurations were not included on this table.

4

Electrical, Environmental and Mechanical Specifications

This section specifies Electrical and Environmental parameters for the NL810 motherboard and describes its Mechanical characteristics.

Absolute Maximum Ratings

Stresses beyond those shown in the following table may cause permanent damage to the system (provided for stress testing only).

Table 4.1. Absolute Maximum Ratings

Operating Temperature	0°C to + 55°C
Storage Temperature	-55°C to + 150°C
Voltage on any Signal with Respect to VSS	-0.3 to Vcc +0.3 V
Supply Voltage with Respect to VSS (5v)	-0.3 to +5.5 V
Supply Voltage with Respect to VSS (3.3V)	-0.3 to +3.6 V

The topics in this section specify the normal operating conditions for the NL810 motherboard. Exposure to absolute maximum rating conditions for extended periods may affect the system reliability.

Electrical

NL810 DC specifications are summarized here, for motherboard signaling environment, power connectors and 5V power budget. Refer to PCI Local Bus Specification Rev. 2.2, and ISA Bus Specification for PCI and ISA DC and AC electrical specifications. Refer also to the documentation for the devices used on the NL810 motherboard.

DC Specifications for 5V and 3.3V Signals

The following table, shows the required DC specifications for 5V and 3.3V power rails.

Table 4.2. 3.3 Volt and 5 Volt DC Specifications

Symbol	Parameter	Condition	Min	Max	Units
Vcc (5v)	Supply Voltage		4.75	5.25	V
Vcc3 (3.3v)	Supply Voltage		3.168	3.432	V
Vcc3.3SB	Supply Voltage		3.168	3.432	V

Power Supply

Power Supply Connector

The input power is supplied via the NLX edge connector. The NLX riser incorporates the power supply connector for the system.

Power Budget

The maximum motherboard power consumption is shown in the table below.

Table 4.4. NL810 Motherboard Power Budget

Voltage		Current Load(A)
Input	**Tolerance**	**Maximum**
-12V	+/-5%	0.2 amp
-5V	+/-5%	0.2 amp
+5V	+/-5%	9 amp
+12V	+/-5%	0.8 amp
3.3V	+/-4%	6.5 amp
3.3SB	+/-4%	.70 amp (1)

(1) without wakeup USB from S5

Environmental

The NL810 motherboard is intended for use in a Class B environment (residential). The following table summarizes environmental limits for the NL810, operating and non-operating.

Table 5.6. Environmental Specifications

Temperature	**Specification**
Non-operating	-40^0 C to 70^0 C
Operating Temperature	0^0 C to 50^0 C
Thermal Map	Must not exceed maximum IC junction temperature as specified in the component data sheets (CPDs).
Thermal Shock	**Specification**
Non-operating	-40^0 C to 70^0 C
Vibration	**Specification**
Non-operating	Random input, 0.01 g2/Hz at 5Hz, sloping to 0.02 g2/Hz at 20Hz and maintaining 0.02 g2/Hz from 20Hz to 500Hz
Shock	**Specification**
Non-operating	50g, 11msec, 1/2 sine
Operating	Not applicable
Altitude	**Specification**
Non-operating	50K feet (pressure altitude)
Operating	10K feet (pressure altitude)
ESD	**Specification**
Operating	Indirect (radiated) only. Test to 15KV with limited errors and to 25KV with no damage.
EMI	**Specification**
Operating	Required to meet EMI emission requirements, tested as part of the system.

Mechanical

System Interfaces

User-Accessible Sockets:
The following user accessible sockets are located on the top of the system PWA:

Table 4.5. Accessible Sockets

U17 (BIOS)	System and Video BIOS PROM (During development only)
MICROPROCESSOR UPGRADE	370 pin processor socket
DIMM0, DIMM1	DIMM sockets

Back-Panel Interfaces

The following interface connections are located on the rear panel of the system PWA:

Table 4.6. Back-Panel Interfaces

J15	SVGA Connector
J8 (top)	PS/2 Mouse connector
J9 (bottom)	Keyboard connector
J11	COM 1
J6	USB connectors
J1	Line-Out
J4	Mic-In
J13	Printer port
J12	COM2 header
J10	LAN (optional)
JU1	DF Panel (optional)

Manufacturability /Serviceability

NL810 is designed to be both easy to manufacture and service. The items specifically related to the system PWA are:

- Connector location & labeling
- Jumper location & labeling
- PWA bar code label (part number and revision)
- Flash BIOS
- DIMM sockets labeling & location

Regulatory

BCM will supply information and resource to assist in the NL810 product qualification testing for compliance with the regulatory agency approvals.