NCR

NCR 386 Card

Technical Reference

Preface

The Technical Reference manual for the 386 Card is a detailed presentation of technical information about the card. It assists the system integrator, programmer, engineer, designer, or other technical personnel that design applications of the card. The manual describes the card architecture and the technical detail of its implementation. It is organized to enable quick access to specific data.

The card uses an 80386-16 32-bit microprocessor as its CPU, operating at 16 MHz or at a lower optional speed. There are sockets for an optional coprocessor which can be either 80287 or 80387. The board design uses split-board computer architecture. That is, the microprocessor with its supporting chips and interfaces are on the 386 Card, while memory and external interfaces are on other cards. The 386 Card is functionally compatible with industry standard 80286 personal computers including the PC/AT. The card fits into a standard PC/AT expansion slot. BIOS allows maximum compatibility with currently existing designs and supports the MS-DOS operating system.

RAM memory cards are the same physical size and shape as the 386 card and they have the same edge connectors. Therefore, memory cards fit into the same bus connectors and mounting hardware as the 386 card. Memory cards are 32-bit DRAM memory, and this manual also covers their design. The 32-bit memory connects to the 386 card through a separate and additional 36-pin edge connector. Sockets for the separate connectors are on a small independent bus board. The 386 Card can also use eight- and 16-bit memory cards, connecting through the standard bus sockets.

The manual has eight chapters, dividing the material for easy reference. The chapters have the following subjects:

Chapter 1 is background descriptive information about the card features. It includes physical size, layout, power requirements, environmental limits, and a list of reference material.

Chapter 2 presents functional descriptions of each of the major components. Charts, timing diagrams, and memory maps complement the written material. The chapter includes listings of the card connectors and the signals on the pins.

Chapter 3 identifies switches and their settings, jumpers, and adjustments.

Chapter 4 is diagnostics, including error messages, test points, and test point codes.

Chapter 5 shows integrated circuit outlines with their pin numbers and signal names.

Chapter 6 is specifications for the qualitative properties of the major integrated circuit components.

Chapter 7 is the logic diagrams of the card.

Chapter 8 presents the 80386 instruction set.

An index completes the manual and makes an easy reference guide to the location of the subject material.

386 Card

Chapter 2 Functional Description

Chapter 3 Switches, Jumpers, Adjustments

Chapter 4 Diagnostics

General Information

This chapter presents information of an overall nature about the 386 Card and about the companion RAM memory card. The 386 card is referred to throughout this manual as the Main Processor Board (MPB) or on occasions simply as "board". The type of information included in this chapter is a description of the split-board architecture, board size, component placement, power and environment specifications, regulatory agency notices, and reference documentation.

INTRODUCTION

The 386 Main Processor Board is an 80386-16 based 32-bit computer that is functionally compatible with the industry standard 80286 PC/AT. Functionally compatible refers to the ability to use application and operating software written for earlier microcomputers in the same series such as the 8086 and the 80286. It also refers to the ability to use 16-bit hardware such as peripherals, busses, and memory boards. The board supports the MS-DOS operating system. The MPB uses a split-board architecture and fits into a standard PC/AT expansion slot. The split-board feature places the CPU and its supporting chips and interfaces on the MPB while memory is on another board. Peripheral controllers and interfaces are also on another board. The split-board architecture provides modularity and flexibility in the design of computer systems.

Supporting chips on the 386 board include ROM memory but not RAM memory, DMA controllers, interval timer, real time clock, sixteen levels of interrupts, and the keyboard port. Operating speed is normally 16MHz with a low performance option available. The low performance option permits speed-dependent disk applications to load correctly.

RAM memory is implemented on separate plug-in boards that are the same size and use the same edge connectors as the MPB. RAM can be 32-bit, 16-bit, or 8-bit, or combinations of those. The 32-bit memory is connected to the MPB through a special bus that uses an additional 36-pin edge connector on each of the boards. The special bus is implemented with a series of 36-pin connectors mounted on a small push-on board. Models of the bus board with 36-pin connectors are currently available for installing up to four memory boards. Memory that is 16-bit or 8-bit uses the standard PC/AT bus and connectors.

Construction is state-of-the-art technology using application-specific integrated circuits (ASIC), very large scale integrated circuits (VLSI), surface mount technology (SMT) and multilayered printed circuit board design.

Features of the main processor board include the following:

- Intel 80386-16 Microprocessor
- Math coprocessor socket - 80387 or 80287
- DMA - 7 channels
- System clock - 16MHz
- Timers - 3 channels
- Enhanced timers - 3 channels
- Interrupts - 16 levels
- DMA speed selection
- 28-bit address bus
- 32-bit memory bus
- 256 Megabyte physical address space
- 64 Gigabyte virtual address space
- ROM memory - 64KB, 64KB expansion
- RAM memory - external boards
- RAM memory - 32-bit, 16-bit, or 8-bit
- Pipelined bus interface
- Universal peripheral interface
- Hardware speed switch - 16 or 8/16Mhz
- Software speed switch - 4.77 to 16Mhz
- Keyboard port
- Reset connector
- Real time clock
- Keyboard inhibit control connection
- Speaker volume control connection
- Battery backup
- Power_Good source selection
- PC/AT standard card size

PHYSICAL DESCRIPTION

The overall dimensions of the boards are 13.15 inches long by 4.80 inches wide. The MPB is six-layer construction, and the memory board is four-layer construction. Components are soldered to the top side of each, and the bottom sides are without components to allow the boards to be installed with minimum spacing between them. Center to center design distance between boards is 0.8 inches minimum.

The bottom right half of each board is constructed with gold plated edge connectors on the front and back. The right-most connector is 31 pins front and 31 pins back to mate with the 62-pin PC and XT bus connector. It is identified as connector P1A on the front side and P1B on the back side. In the center area are 18 pins front and 18 pins on the back to mate with the 36-pin PC/AT connector. They are identified as P2C on the front side and P2D on the back side. To the left and slightly up are another 18 pins front and 18 pins on the back to mate with the 36-pin special bus connectors for the 32-bit bus. They are identified as P3E on the front side and P3F on the back side.

A general outline drawing of the basic board shape is shown in Figure 1-1.

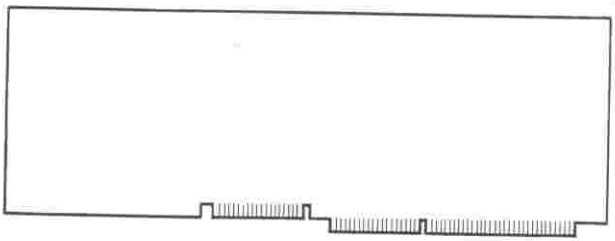


Figure 1-1 Board outlines

MPB COMPONENT PLACEMENT

Figure 1-2 shows the relative placement of the major components mounted on the Main Processor Board. In the right-most quarter of the board at the top are two sockets for EPROM extension ROM, labeled U10 and U28. Just below them is the BIOS EPROM in U44. Just to the left of the sockets is the VLSI Time-of-Day and timer labeled U9. The adjustable capacitors for the VLSI are adjacent to it. VC1 is to the top left of the VLSI and VC2 is just below it.

In the third quarter of the board from the left are the keyboard controller U27 near the top, the DMA controllers U49 and U50 near the center, and the page register U75 near the bottom.

In the quarter of the board farthest to the left are the sockets for the 80386, U47, and the coprocessor, U14. The coprocessor socket is designed for the 80387 chip, and a plug-in adapter is required to install the 80287 coprocessor in its place. The 32MHz crystal oscillator, Y3, is located in the lower left corner of the board.

Adjacent to each of the three edge connectors is a header with the same pin connections as the edge connectors. They are identified as J1A, J1B, J2C, J2D, J3E, and J3F. The headers are usable for piggyback board attachments or for other external connections. Along the right edge of the board is the battery connector, J2, the keyboard connector, J5, and the reset connector, J1. Along the left edge of the board is the speaker connector, J4, and keyboard lock and speed indication connector, J3.

MEMORY BOARD COMPONENT PLACEMENT

Figure 1-3 shows the relative placement of the components on the memory board. The edge connectors and the headers near the edge connectors are the same as the MPB.

The chips for the two megabytes of memory are soldered to the board and none are removable. The first megabyte occupies the 2nd, 4th, 6th, and 8th columns of chips. The second megabyte occupies the 1st, 3rd, 5th, and 7th columns of chips. In each column of chips the top chip is parity, and the other eight chips are data bits. The chips are each 256k by 1 Dynamic RAM (DRAM). A model of the board with only one-megabyte of memory is also available. Chips for the second megabyte are omitted in its construction.

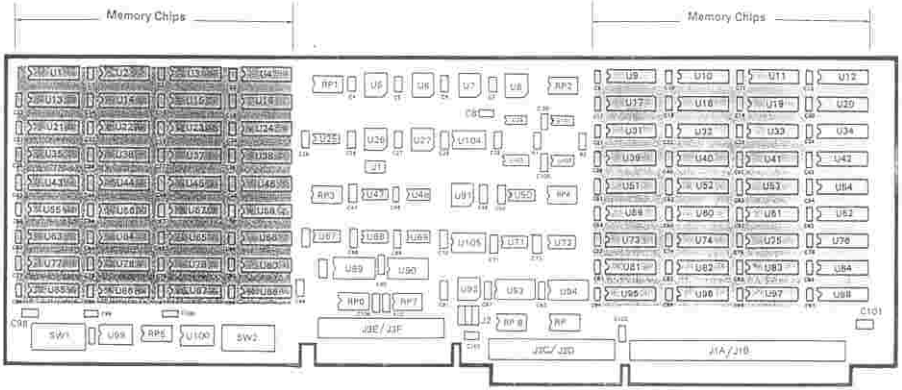


Figure 1-3 Memory board component placement

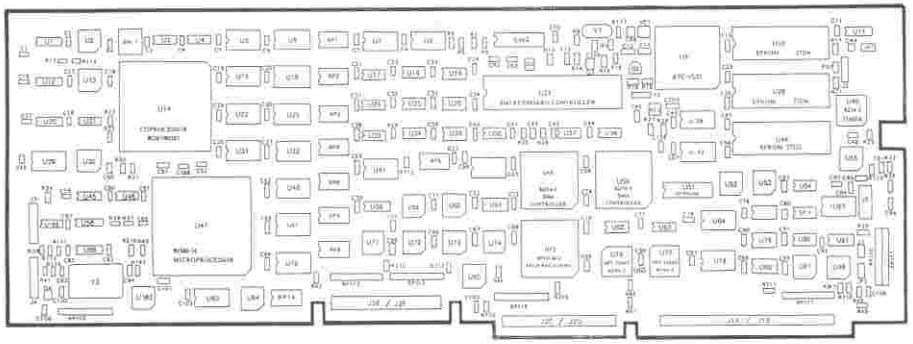


Figure 1-2. MPB component placement

POWER REQUIREMENTS

DC power is provided to the boards through the bus connectors. The following table shows the pin connections for all of the voltages.

PIN	VOLTAGE
B1	Ground
B3	+5 VDC
B5	−5 VDC
B7	−12 VDC
B9	+12 VDC
B10	Ground
B29	+5 VDC
B31	Ground
D16	+5 VDC
D18	Ground
F18	Ground

Figure 1-4 Bus connector voltages

VOLTAGE AND CURRENT

Only the +5 volts DC and ground are used on the these boards. Pins are reserved for the other voltages to comply with the standard bus connections, but they are not used in the logic. The following table shows the voltage and current requirements for the boards.

Maximum current is for a fully populated board. For the MPB it includes an 80387 coprocessor and two extra EPROMs. For the memory board it includes all memory chips. Typical current indicates the average current during a typical operation at common room-ambient temperature.

BOARD	VOLTAGE	VOLTAGE TOLERANCE	TYPICAL CURRENT	MAXIMUM CURRENT
MPB	+5 VDC	+/– 5%	3.0 AMPS	4.0 AMPS
MEMORY	+5 VDC	+/– 5%	3.0 AMPS	4.0 AMPS

Figure 1-5 Current and voltage requirements

LOGIC LEVELS

The following voltage logic levels are used on the boards.

BINARY LEVEL	SYMBOL	VOLTAGE LEVEL MIN.	MAX.
LOGIC 0	V_{IL}		0.8
	V_{OL}		0.5
LOGIC 1	V_{IH}	2.0	
	V_{OH}	2.4	

Figure 1-6 Logic levels

LOADING CHARACTERISTICS

SIGNAL TYPE	LEVEL	SYMBOL	LOAD (MAX.)
DATA	logic 0	I_{IL}	0.100 mA
	logic 1	I_{IH}	0.100 mA
ADDRESS	logic 0	I_{IL}	0.250 mA
	logic 1	I_{IH}	0.250 mA

Figure 1-7 Memory board loading characteristics

BACKUP BATTERY CHARACTERISTICS

The backup battery provides power for the Time-Of-Day/Timer VLSI chip while system power is removed. Data for system setup is retained along with time and date information during power-off periods. System setup data includes memory size, disk configuration, and display type.

Lithium battery packs are recommended for long life. Observe and comply with installation and disposal notices provided by battery suppliers. The following battery characteristics apply.

Battery voltage 5.7 volts
Current drain 100 microamps

Battery voltage above 6.0 volts will decrease battery life because of increased current drain.

ENVIRONMENTAL REQUIREMENTS

The limits shown in the table below pertain to both the Main Processor Board and the Memory Board.

RANGE	DRY BULB TEMPERATURE	RELATIVE HUMIDITY	BAROMETRIC PRESSURE
Operating	10°C to 55°C 10°C Change Per Hour	20% to 80% 10% Change Per Hour	105 to 69000 Pascals (Up to 9850 FT)
Extreme Power On (See Note)	0°C to 55°C 10°C Change Per Hour	10% to 95% Without Condensation	Same
Storage	−10°C to 50°C 15°C Change Per Hour	10% to 90% Without Condensation	Same
Transit	−40°C to 60°C 20°C Change Per Hour	5% to 95% Without Condensation	Same

Figure 1-8 Environmental requirements

NOTE: The extreme power-on range does not represent an operating range, but is intended to indicate limits which are likely to exist if the building heating or air conditioning system fails or has not yet brought the room to operating conditions. Operation to the limits of this range will not damage the boards, but may provide impaired results. Media may be damaged and protective devices may operate. It is considered unlikely that the boards will operate properly outside of this range. Conditions must be limited to one hour in any one period.

SAFETY CERTIFICATIONS

The boards are constructed of U.L. recognized material and are processed by a U.L. recognized etching house. They meet or exceed 94V1 flammability rating and are marked in accordance with U.L. procedures.

FCC NOTICE

The MPB and the Memory Board, when operating in the final product configuration are subject to FCC part 15J (USA) and/or FTZ (Germany) measurements of conducted and radiated radio frequency emissions, depending on the product classification. The boards, as delivered, are neither Class A VERIFIED nor Class B CERTIFIED. The final product must be tested to establish compliance with the applicable emissions regulations.

SOCKET-MOUNTED COMPONENTS

The MPB has provision for the following socket-mounted components which can be removed and replaced.

- 80386 Microprocessor (U47)
- 80387 Coprocessor (U14)
- EPROM (U10, U28)
- BIOS EPROM (U44)
- Keyboard controller (U27)
- ID Prom (U51)

The memory board has no socket-mounted components.

SHIPPING SPECIFICATIONS

The boards are designed to withstand the following forces without any protective packaging.

- Force 1.2 G's input
- Frequency 7 to 100 cycles per second
- Time 2.5 hours
- Shock 30 G's in any plane

The boards are packaged for shipment to comply with the National Safe-Transit Association.

REFERENCES

The following list of reference material is suggested as more tutorial and detailed sources that may be used to supplement the information in this manual. The books are published by Intel.

- Microsystem Components, volumes I and II
- Microprocessor and Peripheral Handbook
- Introduction to the 80386, including the 80386 data sheet
- 80386 Hardware Reference Manual
- 80386 Programmers Reference Manual
- iAPX 386 Operating System Writer's Guide.

Functional Description

This chapter contains a short description of each of the major functional components of the board. The paragraphs describe in a general way what the components do and how they relate to each other. More specific detail information is presented in the accompanying charts, timing diagrams, memory maps, block diagrams, and illustrations.

BOARD DESCRIPTION

The major components of the board and their functions are identified in the following list:

- Processor
- Coprocessor
- RAM
- ROM
- DMA
- Timers
- Interrupts
- Keyboard interface
- Speed control
- Reset support
- Real-Time Clock/Timer VLSI
- Extended bus
- Connectors

Additional detailed descriptions of many of the components are available in the reference material listed in Chapter 1 and in the component manufacturer's catalogues. The block diagram of the board, presented in Figure 2-1, shows the interrelationship between the functions.

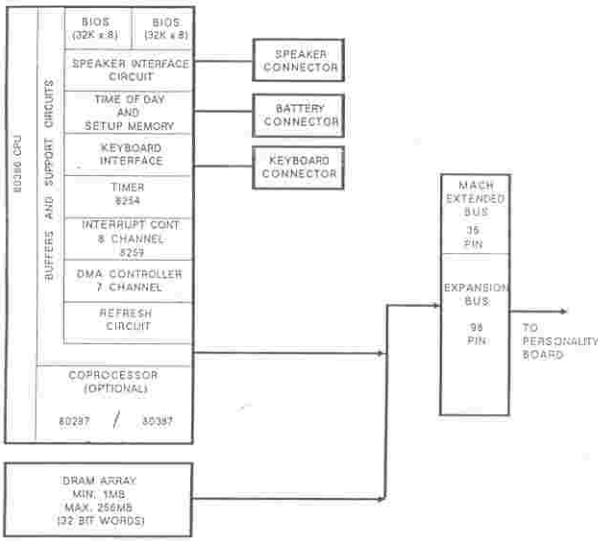


Figure 2-1 80386 Card block diagram

80386 MICROPROCESSOR

The Central Processing Unit (CPU) is an 80386-16. It is a high performance, state of the art microprocessor, socket mounted in position U47. The 80386 is a 32-bit processor using 32-bit registers, instructions, and busses and supports multiuser and multitasking systems. It has object code compatibility with other processors in the family including the 8086 and the 80286. This insures compatibility with the large amount of software that is available for the earlier processors. Maximum clock speed is 16 megahertz, using no wait states, and speeds from 4.77 megahertz to 16 megahertz can be programmed with software. At the maximum speed it processes 3 to 4 million instructions per second.

Physical address space is four gigabytes (four times 2^{32} bytes) and logical address space is 64 terabytes (64 times 2^{46} bytes). There are eight 32-bit wide general registers that use 8-, 16-, and 32-bit data. Words are understood as 16 bits wide and the 32-bit width is understood as "doublewords" or "dwords".

Its virtual memory capability enables use of maximum size programs, governed by disk space instead of RAM memory. The virtual memory is based on segments and pages which afford a flexibility for programmers. Pages are four kilobytes long and are called in from disk as required. Segments can be up to four gigabytes long using this architecture. The virtual memory allows the 80386 to switch between programs controlled by different operating systems such as MS-DOS and Unix.

The 80386 can process multiple instructions simultaneously by pipelining its functional units. One instruction is executed while another is being decoded and a third is being fetched from memory. There is an on-chip memory management unit (MMU) that translates logical to physical addresses as part of the pipeline function.

There are four levels of protection that operating systems can use selectively. They are: 1, a separation that prevents application tasks from interfering with each other; 2, protecting the operating system from the application code; 3, protecting one part of the operating system from other parts; and 4, protecting a task from some of its own errors. The protection facilities are based on a privilege hierarchy. There are up to four levels of privilege that can be assigned to operate with the levels of protection.

The microprocessor can run programs in four different modes. Two of them allow existing MS-DOS applications and add-on boards to be used in 80386-based machines. The first mode is an 8088 real mode in which the 80386 runs MS-DOS programs just like all of the earlier versions of '86 series processor.

The second is an 8088 virtual mode which allows users to create a large number of computing sessions, each with approximately 800KB of memory for running MS-DOS applications.

The other two modes involve protected mode DOS. One is an 80286 protected mode, in which the 80386 runs applications written specifically for 80286 machines. The other is the 80386 protected mode which runs programs written specifically for the 80386 at the greatest efficiency.

The microprocessor supports an optional numeric coprocessor for increased performance. The coprocessor can be either an 80387 or an 80287.

NUMERIC COPROCESSOR

The 80386 CPU supports a numeric coprocessor for higher performance numeric processing. Either the 80287, or the higher performance 80387, may be used. The 80387 plugs directly into the socket as U14, and the 80287, being a different physical shape, is mounted on a small adapter board that plugs into the U14 socket. Figure 2-2 shows a diagram of the adapter board and its orientation to the MPB. The coprocessors are invisible to the application programs and enhance the performance significantly. They add eight 80-bit registers in a floating point register stack.

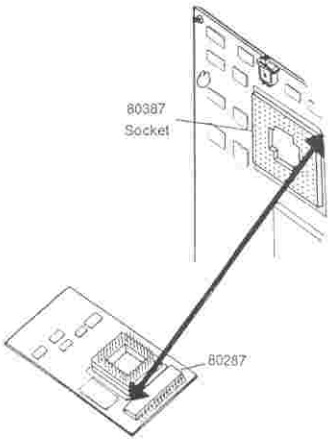


Figure 2-2 Coprocessor Adapter Board

The coprocessor interface driven by the 80386 uses three dedicated signals, BUSY#, ERROR#, and PEREQ. The processor tests BUSY and ERROR before sending the next instruction. These signals synchronize the instructions and eliminate need for wait codes in the 80386. The I/O map of the coprocessor interfaces is shown in the table in Figure 2-3.

80386 I/O space address	80287 register	80387 register
800000F8H	Opcode Register 16-bit port	Opcode Register 32-bit port
800000FCH	Operand Register 16-bit port	Operand Register 32-bit port

Figure 2-3 Coprocessor port address

RANDOM ACCESS MEMORY (RAM)

All of the dynamic RAM is mounted on separate memory boards, and none is on the MPB. The memory board and MPB are connected through the regular bus used for 8- and 16-bit systems and also through the extended bus for 32-bit systems. Figure 2-26 shows the shape and orientation of the extended bus board. Memory used with the MPB may be 32-bit for the highest performance, or may optionally be 16- or even 8-bit if lower performance is acceptable. Memory itself may be different speeds, with 70 nanosecond and 120 nanosecond boards available.

Memory boards are constructed in both one-megabyte and two-megabyte types. Both types use the same circuit board with chips installed only in one bank for the one-megabyte board and in both banks for the two-megabyte board. As described previously, the first bank occupies columns of chips 2, 4, 6, and 8 on the board, and the second bank occupies columns 1, 3, 5, and 7. Each column of chips contains nine chips that are 256K by 1 bit. The top chip is parity, and the eight chips beneath it are data. A parity error generates a non-maskable interrupt to the 80386.

System memory is addressable in the range from zero to 255 megabytes. DOS operating system requires that the first megabyte of memory in the system be in the zero location as addressed by the switches on the memory board. Other megabytes must follow in order, contiguous with the first. The one-megabyte board, if used in a multi-board memory system, must be the last address as described in chapter 3 on setting switches. Operating systems other than DOS may have different requirements. The first megabyte of memory must also have a write protected area from 0E0000H to 0FFFFFH for the system to copy ROM BIOS into the RAM. Expansion bus connector boards are currently available to accommodate up to four of the 32-bit memory boards.

The 80386 will operate in two addressing modes: real and protected. In the real mode there is one megabyte of address space. The 80386 is object code compatible with the 8088 and 8086 in this mode.

The protected mode has four gigabytes of physical address space with 64 gigabytes of virtual address space. In this mode some object code for the 8088 and 8086 may require modification to support the virtual addressing requirements. Only 28 of the available 32 address bits are used, allowing for the 256-megabyte address space.

Refresh requires one memory cycle every 15 microseconds.

The system memory map is given in the table in Figure 2-4.

MEMORY ADDRESS	MEMORY TYPE	LOCATIONS
00000000H – 0009FFFFH	640KB RAM	Expansion board
000A0000H – 000BFFFFH	128KB RAM	Video Display
000C0000H – 000DFFFFH	128KB ROM	Expansion ROM for I/O boards
000E0000H – 000EFFFFH	64KB RAM	System Protected RAM
000F0000H – 000FFFFFH	64KB RAM	System BIOS
00100000H – 0FFFFFFFH	128MB RAM	Expansion RAM Space
FFFF0000H – FFFFFFFFH	64KB ROM	Boot and BIOS ROM

Figure 2-4 Memory address map

READ ONLY MEMORY (ROM)

The MPB has sockets for three EPROM (Erasable Programmable Read Only Memory) chips. The lowest one, U44, is Boot ROM using a 27512 chip, 64K by 8. The upper two, U10 and U28, are optional and may contain 27256 chips, 32K by 8, for existing 16-bit PC/AT expansion ROMs. Since the ROM is 16-bit and the chips are 8-bit, both chips must be installed together. Selection is user defined. Total ROM can be 128K by 8 using all three sockets.

Boot ROM is located in the last segment in memory. Following reset, the 80386 starts executing from this ROM at location FFFFFFF0H. It executes level 0 diagnostics and then copies BIOS from the 8-bit ROM to the 32-bit DRAM at location 000F0000H. Then the program jumps to 000F0000H to continue.

Firmware located in the expansion ROM sockets is copied from ROM memory into the system protected RAM similarly to BIOS ROM. It is copied to the location between 0E0000H and 0EFFFF for execution. Firmware may also be executed directly from ROM but system performance will be lower.

The ROM memory map is given in the table in Figure 2-5.

DIRECT MEMORY ACCESS (DMA)

Direct Memory Access (DMA) provides a means for data to be transferred between system memory and system peripherals, such as flexible disk. The circuitry has two options that are selectable by jumper connection and switch settings. They are DMA device speed, and page register address control. The addressing allows the DMA page registers to be set for 16 megabytes to be PC/AT compatible, or 256 megabytes for enhanced system operation.

ROM NO.	ROM SIZE	ADDRESS RANGE
1	64KB	FFFF0000H – FFFFFFFFH
2	32KB	FFFE0000H – – –
3	32KB	– – FFFEFFFFH

Figure 2-5 ROM Address map

DMA Channels

The MPB has two 8237 DMA controllers (U49 and U50), each with four channels, and a 74LS612 Page Register control (U75). Controller 1 (U49) controls channels 0 through 3 and supports eight-bit data transfers between eight-bit I/O devices and system memory. It controls addresses A0 to A15 and the associated page register controls addresses A16 to A27. For 16-bit memory, BHE is the inverse of A0, and for 32-bit memory, the signals BE0 to BE3 are activated dependent on the address on the bus.

Controller 2 (U50) controls channels 4 through 8. Channel 4 is reserved. Channels 5 through 8 support 16-bit data transfers between 16-bit I/O devices and system memory. Data is transfered in blocks which may be up to 128Kbits long and transfer on even-byte boundaries only. The controller handles addresses A1 through A16, and its associated page register handles A17 through A27. For 16-bit memory BHE and A0 are both logic level zero. For 32-bit memory either BE0 or BE1 are logic zero or BE2 and BE3 are logic zero dependent on the address where transfer occurs. DMA channel addresses do not increment across page boundaries.

DMA Speed

The 8237 DMA controllers can operate at either four or eight megahertz. Different chips are used for the different speeds; 8237-5 or equivalent for 4 megahertz, and Harris 82C37-8 or equivalent for eight megahertz. The clock speed is selected by setting Jumper JP2 to the position indicated in Chapter 3.

DMA Page Register

The DMA Page Register has two modes of operation; PC/AT compatible, and extended mode. They are set by Switch 3 on Switch Block 2 as described in Chapter 3. Chips used are a manufacturing option, and it is not practical to change them in the field.

Extended Mode - The extended mode allows the DMA page register to address the entire 256-megabyte range of system memory. The BIOS or operating system can access anywhere within the first 16 megabytes of system memory by writing just to the PC/AT compatible page register at address 8XH. The address lines A24 to A27 are automatically written as zeros. To write to system memory above 16 megabytes, write first to a four-bit holding register at address 9XH, and then write to the page register as address 8XH. The four bits of holding register are written as the upper four bits of the 12-bit address "A27 to A16" that is held in the page register. The holding register is automatically cleared to zero by the hardware following a write to the page register. DMA page register I/O addresses for this mode are shown in Figure 2-6.

CHANNEL	CHIP	FUNCTION	PAGE REGISTER ADDRESS	4-BIT HOLDING REGISTER ADDRESS
0	1	Undedicated	087H	097H
1	1	SDLC	083H	093H
2	1	Flexible Disk	081H	091H
3	1	Undedicated	082H	092H
4	2	Reserved		
5	2	Undedicated	08BH	09BH
6	2	Undedicated	089H	099H
7	2	Undedicated	08AH	09AH
-	-	Refresh register	08FH	09FH

Figure 2-6 DMA Page Register I/O Addresses

PC/AT Compatible mode - The DMA addresses only the range of zero to 16 megabytes of system memory in the 16-bit mode. The hardware effectively removes the holding register from the circuit and maps the page register to both address 8XH and also 9XH. Software that address the page register directly at 9XH can operate correctly in this mode. DMA page register I/O addresses for this mode are given in Figure 2-7.

CHANNEL	CHIP	FUNCTION	PAGE REGISTER ADDRESS
0	1	Undedicated	087H
1	1	SDLC	083H
2	1	Flexible Disk	081H
3	1	Undedictated	082H
4	2	Reserved	
5	2	Undedicated	08BH
6	2	Undedicated	089H
7	2	Undedicated	08AH
--	--	Refresh register	08FH

Figure 2-7 DMA Page Register I/O Addresses

DMA 16-Bit Channel Control - DMA page registers for channels 5 through 7 contain the address bits A17 through A27. The addresses are output in data bits D1 through D7. D0 is not used for 16-bit transfers. The base addresses for these channels are the real addresses divided by two. The command code addresses are shown in figure 2-8.

ADDRESS	COMMAND
0C0H	CH0 base and current address
0C2H	CH0 base and current word count
0C4H	CH1 base and current address
0C6H	CH1 base and current word count
0C8H	CH2 base and current address
0CAH	CH2 base and current word count
0CCH	CH3 base and current address
0CEH	CH3 base and current word count
0D0H	Read status reg. or write command reg.
0D2H	Write request register
0D4H	Write mask register (single bit)
0D6H	Write mode register
0D8H	Clear byte pointer
0DAH	Read temporary reg. or master clear
0DCH	Clear mask register
0DEH	Write mask register, all bits

Figure 2-8 DMA controller command code addresses

TIMERS

Three PC/AT compatible timers and three additional enhanced timers are used on the MPB. All are 16-bit and independently programmable.

Compatible Timer

Three channels are included in the VLSI chip U9. Channel 0 is tied to interrupt 0; channel 1 is used for dynamic RAM refresh; and channel 2 is used for the speaker tone.

Enhanced Timer

Three additional channels are available on the 8254 interval timer, U40. Channel 0 is tied to the non-maskable-interrupt (NMI) failsafe interrupt; channel 1 is connected to IRQ 10, IRQ 11, or IRQ 12; and channel 2 is used in conjunction with the speed switch. The timers are controlled by Switch Block SW2 switches S4 through S7 as shown in chapter 3. Figure 2-9 shows the counter uses in tabular form.

TIMER	COUNTER	CLOCK INPUT	OUTPUT
VLSI Compatible	Channel 0	1.190 MHz	8259A IRQ0
	Channel 1	1.190 MHz	Refresh Request
	Channel 2	1.190 MHz	Speaker Drive
Enhanced	Channel 0	1.190 MHz	NMI – Failsafe Timer
	Channel 1	1.190 MHz	8259A IRQ 10, 11, or 12
	Channel 2	8.000 MHz	Speed Switch

Figure 2-9 Timer Counters

INTERRUPT CONTROL

Two 8259A-2 interrupt controllers (U76 and U77) regulate the interrupt requests from external devices. They are cascaded to provide 16 levels of interrupts as shown in Figure 2-10.

INTERRUPT	USE
(U77) 0	Timer Channel 0
1	Keyboard output buffer full
2	Cascade input from second controller
3	Auxiliary serial port number 2
4	Primary serial port number 1
5	Auxiliary parallel port number 2
6	Flex disk drive controller
7	Primary parallel port number 1
(U76) 8	Realtime clock interrupt
9	Software redirected to INT 0AH (IRQ2)
10	Reserved
11	Reserved
12	Reserved
13	80287/80387 Coprocessor
14	Fixed Disk drive controller
15	Reserved

Figure 2-10 Hardware interrupt assignments

Note: Internal to the MPB, interrupt channel 2 is reserved to cascade the ports of the second interrupt controller into the total number of interrupts. For board application, however, channel 2 (IRQ2) is operational. Channel 9 is internally connected through the BIOS to respond as if it were channel 2. This is done to be compatible with existing 8-bit and 16-bit hardware and software.

A non-maskable interrupt (NMI) is activated when either:

- A parity error occurs when reading RAM from one of the expansion slots.
- An error has occurred in a device in one of the expansion slots.
- A power-fail condition is reported.

KEYBOARD INTERFACE

An 8742 Universal Peripheral Interface (UPI) chip, U27, provides status and interface to the serial keyboard. The chip has two 8-bit ports. Port 1 is a dedicated input port containing system configuration information. Port 2 is an output port containing system control bits and keyboard interface. The bit usage is shown in Figure 2-11.

BIT	INPUT PORT	OUTPUT
0	DMA Mode	Reset system board
1	High/Auto speed	Gate address 20
2	Unused	Unused
3	Coprocessor detect	RAM Write protect
4	Unused	Output buffer full
5	Tied to ground	Input buffer empty
6	Monitor type 0 = Color/graphics 1 = monochrome	Keyboard clock out
7	Keyboard disable switch	Keyboard data out

Figure 2-11 UPI description

The keyboard connector is a ten-pin header connector, J5. The pin connections are identified in Figure 2-12.

PIN	SIGNAL	DIRECTION
1	+ clock	Bi – directional
3	+ data	Bi – directional
5	Power good	Input
7	+ 5 volts	Output
2,4,6, 9,10	Ground	
8	Key	

Figure 2-12 Keyboard connector pin-outs

Two pins on the chip can be used to sample data from the keyboard. The pins are named Test 0 and Test 1 on the chip diagram.

CHIP PIN	FUNCTION
Test 0	Keyboard clock input
Test 1	Keyboard data input

The keyboard can be disabled through the Keyboard Lock and Speed Indicator connector described later in this chapter. Grounding pin 4 of J3 disables any keyboard action.

RESET SUPPORT

The 80386 MPB supports 80286 operating systems and the 80286 hardware shutdown and reset circuitry. This is done to be operationally compatible with the 80286.

The 80386 MPB also supports an external resest switch. The reset connector is a 2-pin header, J1. Its pin-out sequence is shown in Figure 2-13.

PIN	SIGNAL NAME
1	Ground
2	Reset

Figure 2-13 Reset connector pin-outs

SPEED CONTROL

Processor speed can be reduced from the 16 megahertz rate to an emulated 4.77 megahertz rate in discreet increments. Reduced speeds are necessary for: 1, protected programs that use a "key" disk operating at a slower (PC/AT) speed, and 2, programs such as some communication packages that are speed dependent. A hardware switch on the board determines two speed modes, and software can override

the modes.This allows changing the speed without actually having physical access to the board. The software setting is lost, however, when the processor powers down, and must be reinitialized after power-up to be used again. Speed is controlled by extending the amount of time the processor is in "hold" or "non executing" state. It is in "hold" state during the memory refresh period. An extended refresh, then, holds the processor longer and has the effect of making it process slower. Actual bus speed is not changed by the action, just the number of operations completed in a period of time.

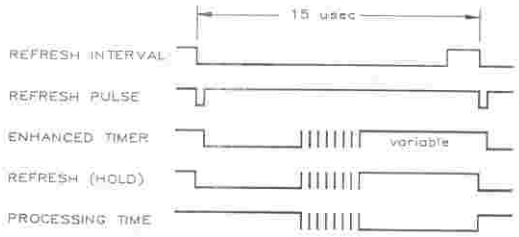


Figure 2-14 Speed Control Timing

The fundamental interval for the memory refresh cycle is 15 microseconds. VLSI Compatible Timer Channel 1 generates that time to start each cycle. The part of that 15 microseconds used by the refresh is the refresh pulse plus the time generated by the Enhanced Timer Channel 2. The rest of the refresh interval is processing time. Figure 2-14 illustrates the simplified time relationship, not necessarily to scale or in exact signal polarity. The refresh pulse is only one clock cycle long, but the timer, operating in one-shot mode, can be set to count a wide range of clock cycles for variable time. The speed switch port is enabled or disabled to let the timer control or not control the refresh extension. A "zero" in port 69H enables the timer, and a "one" disables the timer.

Switch S8 of Switch Block SW2 controls the mode when the system is powered-up. Mode can be either High or Auto (Automatic). In High speed mode the system operates at 16 megahertz all of the time. In Auto mode it powers-up for 16 megahertz speed and drops back to 8 megahertz any time the flex disk is accessed. Speed returns to 16 megahertz when the disk access is completed. Enhanced timer Channel 2 is set by the BIOS to a count that simulates 8 megahertz operation and the timer is enabled when the disk is accessed. Switch positions are identified in Chapter 3.

Software can override the High or Auto mode by inserting a different count into Enhanced Timer Channel 2. Approximately 100 incremental counts of clock cycles can be programmed into the counter to vary the effective processor speed. The programmed reduction is effective when the channel is enabled through port 68H.

Indication of the speed setting is available from the Keyboard Lock and Speed Indicator connector described later in this chapter. LED "B" is the High Speed indicator, 16 MHz, and LED "A" indicates any other speed.

REAL-TIME CLOCK VLSI

The Real-Time Clock (RTC) VLSI chip, U9, contains the functional equivalent of both the Motorola MC146818 Time-of-Day chip and the Intel 8254 Timer chip. It supports all of the time-of-day modes provided by the MC146818; three user programable counters; and battery back-up. The chip is packaged in a 68-pin plastic leaded chip carrier (PLCC). Figure 2-15 is a block diagram of the RTC VLSI chip. This section includes a block diagram, an I/O address map, a list of significant features of the chip, and a description of the interface to the chip.

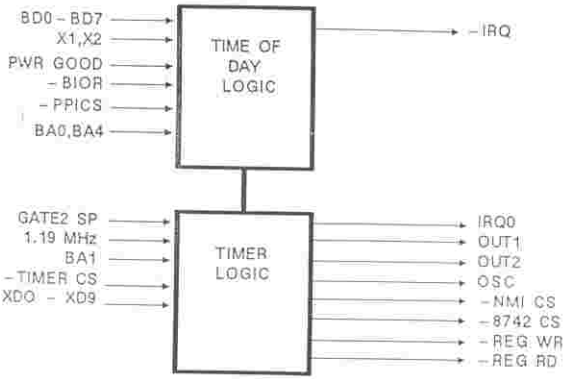


Figure 2-15 RTC VLSI block diagram

The real-time clock logic contains 14 bytes used by the RTC chip for time and date control. The remaining 50 bytes are used by the processor board to store various parameters required for system operation. The function of each of these bytes is outlined in Figure 2-16.

I/O ADDRESS	FUNCTION
00H	RTC Seconds*
01H	RTC Seconds alarm*
02H	RTC Minutes*
03H	RTC Minutes alarm*
04H	RTC Hours*
05H	RTC Hours alarm*
06H	RTC Day of the week*
07H	RTC Day of the month
08H	RTC Month
09H	RTC Year
0AH	RTC Status register A
0BH	RTC Status register B
0CH	RTC Status register C
0DH	RTC Status register D
0EH	Status byte (Diagnostic)*
0FH	Status byte (Shutdown)*
10H	Flex disk drive (type)
11H	Unused
12H	Fixed disk drive (type)
13H	Unused
14H	Equipment flag
15H	Base memory byte (Low)
16H	Base memory byte (High)
17H	Expansion memory byte (Low)
18H	Expansion memory byte (High)
19H – 2DH,	Unused
2EH – 2FH,	Checksum
30H	Expansion memory byte (Low)*
31H	Expansion memory byte (High)*
32H,	Century data*
33H,	Power on Flags*
34H – 3FH,	Unused

* These bytes are not included in the checksum caculations.

Figure 2-16 RTC RAM I/O address map

The following is a list of significant features of the RTC VLSI chip:

- Internal Time Base and Oscillator
- Counts Seconds, Minutes, and Hours of the Day.
- Counts Days of the Week, Date, Month, and Year
- Time Base Input: 32.768 KHz
- Time Base Oscillator for Parallel Resonant Crystals
- Binary or BCD Representation of Time, Calendar, and Alarm
- 12 or 24 Hour Clock with AM and PM in 12 Hour Mode
- Automatic End of Month Recognition
- Automatic Leap Year Compensation
- Interfaced as 64 RAM Locations
- 14 Bytes of Clock and Control Registers
- 50 Bytes of General Purpose RAM
- Status Bit Indicates Data Integrity
- Three software-maskable and testable interrupts:
  - Time of Day Alarm, Once-per-Second to Once-per-Day
  - Periodic Interrupt Rates from 122.070 μS to 500 mS
  - End-of-Clock Update Cycle

REAL-TIME CLOCK INTERFACE PROGRAMMING

The following sections present descriptions of interface signals to the Real-Time Clock. They are important to understanding its operation and to the programming functions related to its use. In a general sense, the descriptions relate to memory using an address map, and then give details of the time/calendar bits, and finally describe in detail the registers that are involved.

Input and Output Control Line Functions

The functions of the input and output control lines are described in the paragraphs to follow.

Multiplexed Bidirectional Address/Data Bus (AD0-AD7) – The bus presents the address during the first phase of the bus cycle, and the data during the second phase. The valid address must be presented just before the fall of ALE. Valid write data must be presented and held stable at the end of the write cycle. In a read cycle, 8 bits of data are output near the end of the cycle.

ALE - Multiplexed Address Strobe – ALE is a positive strobe pulse input that demultiplexes the bus. The falling edge of ALE causes the address to be latched within this device.

IRQ - Interrupt Request – IRQ is an output that is active when high and interrupts the processor as needed. The IRQ output remains High as long as the status bit enabling the interrupt is set. When the processor reads register C, it clears IRQ. RESET also clears pending interrupts. IRQ is low when no interrupt is active, or Tri-Stated according to the way the RTC is programmed.

RESET – RESET clears the following signals and sets them to zero.

- Periodic Interrupt Enable (PIE)
- Alarm Interrupt Enable (AIE)
- Update Ended Interrupt Enable (UIE)
- Update Ended Interrupt Flag (UF)
- Interrupt Request Status Flag (IRQF)
- Periodic Interrupt Flag (PF)
- Alarm Interrupt Flag (AF)
  and
- IRQ is Tri-Stated

RESET input does not affect the clock, calendar, or RAM functions.

PS - Power Sense – PS input controls the Valid RAM and Time (VRT) bit in Status Register D. When PS is low, the VRT bit is cleared to zero. During power-up, the PS pin must be externally held low for a minimum of 5 microseconds. As power is applied, the VRT bit remains LOW indicating that the contents of RAM, time registers, and calendar are not guaranteed.

Address Map – Memory consists of 50 bytes of user RAM, 10 more bytes for time, calendar, and alarm data; and four more bytes for control and status. All 64 bytes can be read or written, with the following exceptions. Registers C and D, Bit 7 of Register A, and the seconds byte are read-only. Bit 7 of the seconds byte is always "0". Figure 2-17 shows the RAM address map and control registers in this chip.

The processor obtains time and calendar information by reading the corresponding RAM locations. Those locations can be initialized by writing to them. The contents of the ten bytes for time, calendar, and alarm can be either binary or binary coded decimal (BCD). Figure 2-18 shows the binary and BCD formats of those ten bytes.

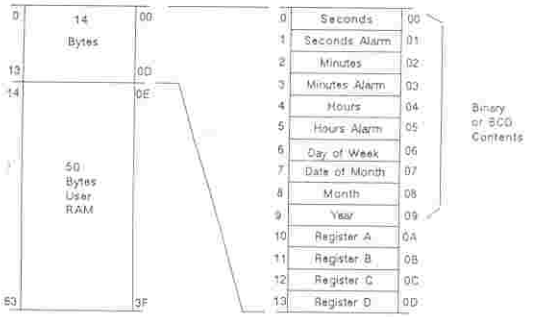


Figure 2-17 RTC RAM and control registers address map

Address Location	Function	Decimal Range	Range		Example*	
			Binary Data Mode	BCD Data Mode	Binary Data Mode	BCD Data Mode
0	Seconds	0 – 59	$00 – $3B	$00 – $59	15	21
1	Seconds Alarm	0 – 59	$00 – $3B	$00 – $59	15	21
2	Minutes	0 – 59	$00 – $3B	$00 – $59	3A	58
3	Minutes Alarm	0 – 59	$00 – $3B	$00 – $59	3A	58
4	Hours Alarm (12 Hour Mode)	1 – 12	$01 – $0C (AM) and $81 – $8C (PM)	$01 – $12 (AM) and $81 – $92 (PM)	05	05
	Hours Alarm (24 Hour Mode)	0 – 23	$00 – $17	$00 – $23	05	05
5	Hours Alarm (12 Hour Mode)	1 – 12	$01 – $0C (AM) and $81 – $8C (PM)	$01 – $12 (AM) and $81 – $92 (PM)	05	05
	Hours Alarm (24 Hour Mode)	0 – 23	$00 – $17	$00 – $23	05	05
6	Day of the Week Sunday = 1	1 – 7	$01 – $07	$01 – $07	05	05
7	Date of the Month	1 – 31	$01 – $1F	$01 – $31	0F	15
8	Month	1 – 12	$01 – $0C	$01 – $12	02	02
9	Year	0 – 99	$00 – $63	$00 – $99	4F	79

* Example 5:58:21 Thursday 15 February 1979 (time in AM)

Figure 2-18 RTC Time, calendar, and alarm data modes

Periodic Interrupt Selection – The periodic interrupt allows the IRQ pin to be triggered once every 122.070 microseconds to 500 milliseconds. It is separate from the alarm interrupt which can output once per second to once per day. Figure 2-19 shows the selection of the Register A bits that set the periodic interrupt frequency. The periodic interrupts must be enabled by the PIE bit in Register B.

Rate Select Control Register A				32.768 KHz Time Base Periodic Interrupt Rate tPI	Rate Select Control Register A				32.768 KHz Time Base Periodic Interrupt Rate tPI
RS3	RS2	RS1	RS0		RS3	RS2	RS1	RS0	
0	0	0	0	None	1	0	0	0	3.90625 mS
0	0	0	1	3.90625 mS	1	0	0	1	7.8125 mS
0	0	1	0	7.8125 mS	1	0	1	0	15.625 mS
0	0	1	1	122.070 uS	1	0	1	1	31.25 mS
0	1	0	0	244.141 uS	1	1	0	0	62.5 mS
0	1	0	1	488.281 uS	1	1	0	1	125 mS
0	1	1	0	976.562 uS	1	1	1	0	250 mS
0	1	1	1	1.953125 mS	1	1	1	1	500 mS

Figure 2-19 Register A rate selection bit settings

Alarm Interrupt Selection – The three alarm bytes can be used in two ways. The processor can insert an alarm time in the appropriate hours, minutes, and seconds alarm locations and set the alarm enable bit to enable the alarm interrupt to occur at the specified time each day.

A "Don't Care" ("DC") code can also be inserted in any of the three alarm bytes to obtain different results. A "DC" code is any hexadecimal byte, from C0 to FF, with its two most significant bits set to 1. An alarm interrupt occurs each hour if a "DC" is inserted in the hours alarm byte, each minute if inserted in the hours and minutes bytes, or each second if inserted into all three alarm bytes.

The processor selects which interrupts, if any, it wishes to receive. A "1" written to the appropriate register B bit locations enables one of the three interrupts. A "0" in a bit location prohibits the corresponding interrupt from occurring. If an interrupt flag is already set when the interrupt is enabled, the IRQ pin is immediately activated, even though the interrupt that initiated the event may have occurred much earlier. Therefore, the processor should clear earlier initiated interrupts before enabling new interrupts. When an interrupt occurs, a flag bit is set to "1" in Register A. Each of the

interrupts have a bit in Register A which is set independent of the state of the corresponding enable bits in Register B. The flags may be used with or without enabling the corresponding enable bits. However, there is one precaution: all of the flag bits in Register A are cleared when Register A is read.

Static CMOS RAM– The 50 bytes of RAM included in the RTC are not dedicated to any particular function. They may be used by the processor and are accessible during the update cycle. They can be used to store essential non-volatile data since the RAM can be kept valid by use of battery backup.

Update Cycle– The RTC executes an update cycle once per second assuming one of the proper time bases is in place and the SET bit in Register B is clear. When the SET bit is a "1", the processor can initialize the time and calendar bits by stopping any existing update and by preventing a new one from beginning. The most important functions of the update cycle are to increment the seconds byte, check for an overflow condition, increment the minutes byte when needed, and so on through to the year of the century byte. Also, each alarm byte is compared to its corresponding time byte, and an alarm is executed if there is a match or if a "DC" code (11XXXXXX) is present in all three positions. A 32.768 KHz time base update takes 1,984 microseconds. During the update cycle, the time, calendar, and alarm bytes are inaccessible. The Update In Progress (UIP) status bit is set at this time.

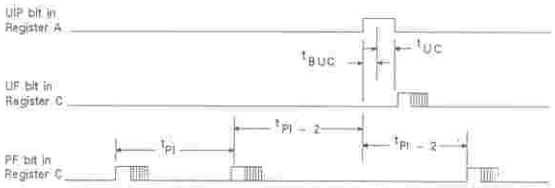
There are three routines the processor may use to avoid the update cycle.

If the Update-Ended interrupt is enabled, an interrupt occurs every update cycle and over 999 milliseconds are available to read valid data. Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared.

The second routine uses the Update-In-Progress bit (UIP) in Register B to determine the status of the update. The UIP bit is set once per second. After the UIP bit goes High, the update begins 244 microseconds later. Therefore, the user has at least 244 microseconds

if the UIP bit is Low, to read valid data. Once the UIP bit is set, data is not valid and should not be used by the processor. Also, the user should avoid interrupt service routines that cause it to take longer than 244 microseconds to read time/calendar data.

The third routine uses the periodic interrupt to determine if an update cycle is in progress. The UIP bit is set High between the setting of the PF bit in Register C. Periodic interrupts that occur at a rate greater than tBUC + tUC allow valid information to be read at each occurrence of the periodic interrupt. The reads should be done within (tPI + 2) + tBUC to insure valid data. See Figure 2-20 for more information on the update cycle.



tPI = Periodic Interrupt Time Interval (500 ms, 250 ms, 125 ms, 62.5 ms, etc. per Figure 2-18)
tUC = Update Cycle Time (248 μs or 1984 μs)
tBUC = Delay Time Before Update Cycle (244 μs)

Figure 2-20 Update-ended and periodic interrupt relationships

RTC Registers

The RTC has four registers, A,B,C, and D, which are accessible by the processor during the update cycle. These registers are described below.

Register A – A diagram of register A's bit functions is shown in Figure 2-21. These functions are described in the following paragraphs.

b7	b6	b5	b4	b3	b2	b1	b0
UIP	X	X	X	RS3	RS2	RS1	RS0

Figure 2-21 Register A bit functions

Update In Progress Bit (UIP) – UIP is a status bit that can be monitored by the processor. If set to "1", the update cycle is in progress or will be shortly. If "0", an update will not occur for at least 244 microseconds. The time, calendar, and alarm data is all valid and accessible when the bit is "0". This bit is read-only and ignores RESET; however, writing a "1" in the SET bit of Register B will prohibit updates and clear the UIP status bit.

Rate Selection Bits (RS3,RS2,RS1,RS0) – These four bits select the rate the periodic interrupts will occur if the PIE bit in Register B is set to "1". These four bits are read/write, are not affected by RESET and are never changed by the RTC. See Figure 2-21.

Register B – A diagram of register B's bit functions is shown in Figure 2-22. These functions are described in the following paragraphs.

b7	b6	b5	b4	b3	b2	b1	b0
SET	PIE	AIE	UIE	X	DM	24/12	DSE

Figure 2-22 Register B bit functions

SET – When the SET bit is a "0", the update cycle advances the count once per second. When SET is a "1", any update cycle in progress is aborted and the processor may initialize the time and calendar bytes without an update occurring. SET is a read/write bit and is not modified by RESET.

Periodic Interrupt Enable Bit (PIE) – PIE is a read/write bit that allows the periodic interrupt flag (PF) bit to cause the IRQ pin to be driven High. The processor writes a "1" to the PIE bit in order to receive periodic interrupts at the rate selected by RS3, RS2, RS1, and RS0 in Register A. A "0" in PIE keeps IRQ inactive by a periodic interrupt, but the PF bit is still set at the periodic rate. PIE is cleared to "0" by RESET.

Alarm Interrupt Enable Bit (AIE) – The AIE bit is a read/write bit which, when set to a "1", permits the alarm flag (AF) to assert IRQ. An alarm interrupt occurs for each second that the three time bytes equal their corresponding alarm bytes including the "DC" state. When AIE is "0", the AF bit does not set IRQ. The RESET pin clears AIE to "0".

Update-ended Interrupt Enable bit (UIE) – The UIE bit is a read/write bit which enables the update-end flag (UF) bit to set IRQ. If the RESET pin or the SET bit is set to a "1", the UIE bit is cleared.

Data Mode Bit (DM) – The DM bit indicates whether the time and data updates are to use binary or BCD formats. It is dependent only on the processor. A "1" indicates binary data, a "0" indicates BCD data.

24/12 Bit – The 24/12 bit sets the format of the hours bytes as either the 24 hour mode, set to a "1" or the 12 hour mode, set to a "0". It is affected only by the processor.

Daylight Savings Enable Bit (DSE) – The DSE bit is a read/write bit which allows the processor to enable two special updates when DSE is a "1". On the last Sunday in April, the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October, the time changes from 1:59:59 AM to 1:00:00 AM. These times do not change when DSE is "0". DSE is not changed by any internal operations or RESET. For any other dates than those given above, Daylight Savings time changes must be input manually.

Register C – A diagram of register C's bit functions is shown in Figure 2-23. These functions are described in the following paragraphs.

b7	b6	b5	b4	b3	b2	b1	b0
IRQF	PF	AF	UF	0	0	0	0

Figure 2-23 Register C bit functions

Interrupt Request Flag (IRQF) – The IRQF flag is set to "1" if one or more of the following occur:

- PF = PIE = "1"
- AF = AIE = "1"
- UF = UIE = "1"

When IRQF is set to "1", the IRQ pin is driven High. All flag bits are cleared after Register C is read or RESET is activated.

Periodic Interrupt Flag (PF) – The PF flag is a read only bit. It is set to "1" when a particular edge is detected on the divider chain. This flag is cleared when Register C is read or by RESET.

Alarm Interrupt Flag (AF) – When the AF bit is set to "1", the current time has matched the alarm time. A "1" causes IRQ to go High if AIE is also High ("1"). This also sets the IRQF bit. A RESET or Register C read clears AF.

Update-Ended Interrupt Flag (UF) – This flag bit is set at the end of each update cycle. When UF and UIE are a "1", IRQF is set to "1" and IRQ goes High. UF is cleared by RESET or a Register C read.

B3 to B0 – Unused bits of Register C, read as "0's". They cannot be written.

Register D – A diagram of register D's bit functions is shown in Figure 2-24. These functions are described in the following paragraphs.

b7	b6	b5	b4	b3	b2	b1	b0
VRT	0	0	0	0	0	0	0

Figure 2-24 Register D bit functions

Valid RAM and Time Bit (VRT) – The VRT bit indicates the condition of the contents of RAM provided the power sense (PS) pin of the chip is properly connected. A "0" appears when the PS pin is Low. The processor can set the VRT bit when the time and calendar are initialized. The VRT is a read only bit that cannot be modified by the RESET pin. The VRT bit can only be set by reading Register D.

b6 to b0 – These bits are unused and are always read as "0's". They cannot be written.

EDGE CONNECTORS

The main processor board and the memory board have edge connectors to correspond with the industry standard PC/AT boards. Therefore they can be plugged into units that use the industry standard 80286 and 8088 boards. The MPB and memory boards also have an additional edge connector to supply the remainder of the 32-bit bus. Just above each of the edge connector on the board is a header with the same number of pins as the edge connector. It is available for piggyback or other connections to the busses. Figure 2-25 illustrates the location of the connectors.

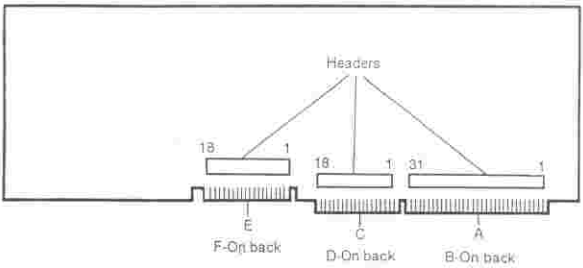


Figure 2-25 Location of edge connectors

The first edge connector is the standard 62-pin double sided connection with sections A and B for the eight-bit bus. Section A includes the 31 pins on the component side of the boards and section B is the 31 pins on the solder side of the boards.

The second edge connector is the standard 36-pin double sided connector with sections C and D for the 16-bit bus. Section C is the 18 pins on the component side and section D is the 18 pins on the solder side of the boards.

The third edge connector is unique for the 32-bit bus. It is also a 36-pin connector and has sections E and F. Section E is the 18 pins on the component side and section F is the 18 pins on the solder side of the board.

Sections E and F are recessed from the line of sections A, B, C, and D and have room to be fitted with a separate small independent bus board. The independent bus board connects only the MPB and any memory boards, or any other boards specifically designed to connect to the 32-bit bus. Figure 2-26 illustrates an example implementation of such a bus board.

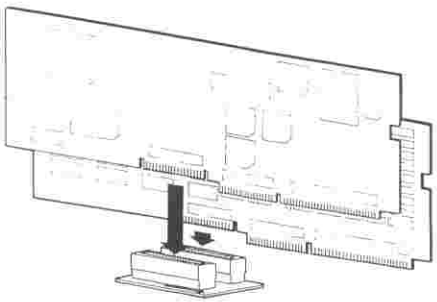


Figure 2-26 Bus board for 32-bit bus

The data and interface control signals on the busses are compatible with standard TTL levels. Input and output levels are defined in the table in Figure 2-27.

SYMBOL	LOGIC STATE	VOLTAGE LEVEL MIN.	MAX.
V_{IL}	0		0.8
V_{OL}			0.5
V_{IL}	1	2.0	
V_{OH}		2.4	

Figure 2-27 Signal levels

Loading characteristics for the signals are defined in Figure 2-28. The MPB is designed to drive up to eight expansion slots.

SYMBOL	LOGIC LEVEL	LOAD (MAX.)
I_{IL}	0	0.10MA
I_{IH}	1	0.25MA

Figure 2-28 Signal loading

The signals on the edge connectors and their corresponding pin numbers are given in figures 2-29, 2-30, and 2-31.

SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER
-I/O CH CK	A1	GROUND	B1
SD7	A2	RESET	B2
SD6	A3	+5 VOLTS	B3
SD5	A4	IRQ9	B4
SD4	A5	-5 VOLTS	B5
SD3	A6	DRQ2	B6
SD2	A7	-12 VOLTS	B7
SD1	A8	0 WS	B8
SD0	A9	+12 VOLTS	B9
-I/O CH RDY	A10	GROUND	B10
AEN	A11	-SMEMW	B11
SA19	A12	-SMEMR	B12
SA18	A13	-IOW	B13
SA17	A14	-IOR	B14
SA16	A15	-DACK3	B15
SA15	A16	DRQ3	B16
SA14	A17	-DACK1	B17
SA13	A18	DRQ1	B18
SA12	A19	-REFRESH	B19
SA11	A20	CLK	B20
SA10	A21	IRQ7	B21
SA9	A22	IRQ6	B22
SA8	A23	IRQ5	B23
SA7	A24	IRQ4	B24
SA6	A25	IRQ3	B25
SA5	A26	-DACK2	B26
SA4	A27	T/C	B27
SA3	A28	BALE	B28
SA2	A29	+5 VOLTS	B29
SA1	A30	OSC	B30
SA0	A31	GROUND	B31

Figure 2-29. 62-pin card edge connector, 8-bit bus interface

SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER
SBHE	C1	-MEM CS16	D1
LA23	C2	-I/O CS16	D2
LA22	C3	IRQ10	D3
LA21	C4	IRQ11	D4
LA20	C5	IRQ12	D5
LA19	C6	IRQ15	D6
LA18	C7	IRQ14	D7
LA17	C8	-DACK0	D8
-MEMR	C9	DRQ0	D9
-MEMW	C10	-DACK5	D10
SD08	C11	DRQ5	D11
SD09	C12	-DACK6	D12
SD10	C13	DRQ6	D13
SD11	C14	-DACK7	D14
SD12	C15	DRQ7	D15
SD13	C16	+5 VOLTS	D16
SD14	C17	-MASTER	D17
SD15	C18	GROUND	D18

Figure 2-30 36-pin edge connector, 16-bit bus interface

SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER
SD16	E1	LA27	F1
SD17	E2	LA26	F2
SD18	E3	LA25	F3
SD19	E4	LA24	F4
SD20	E5	-SBE0	F5
SD21	E6	-SBE1	F6
SD22	E7	-SBE2	F7
SD23	E8	-SBE3	F8
SD24	E9	+MEMS	F9
SD25	E10	-XMEMW	F10
SD26	E11	-XMEMR	F11
SD27	E12	-MEMCS32	F12
SD28	E13	-IOCS32	F13
SD29	E14	RAM_PROT	F14
SD30	E15	+OCLK	F15
SD31	E16	-LW/R	F16
-PL32	E17	-OCLK	F17
-ENRAM	E18	GROUND	F18

Figure 2-31 36-pin card edge connector, 32-bit bus interface

EXTERNAL CONNECTORS

The Main Processor Board has five external connectors. There are none on the memory board. The locations of the external connectors are shown in Figure 2-32, and the Pinouts of each connector are given in the figures that follow.

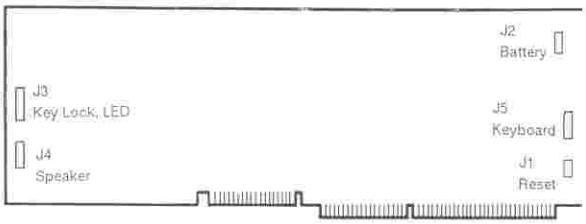


Figure 2-32 Location of MPB external connectors.

External Reset Connector J1

J1 is a 2-pin header type of connector.

PIN	DESCRIPTION
1	Ground
2	Reset

Figure 2-33 External Reset Connector

Battery Backup connector J2

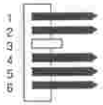
J2 is a 4-pin right-angled header type of connector.

PIN	DESCRIPTION
1	+ Voltage
2	Key
3	Power Good (Active High)
4	Ground

Figure 2-34 Battery Backup Connector

Keyboard Lock and Speed Indicator Connector J3

J3 is a 6-pin right-angled header type of connector.



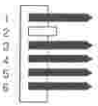
PIN	DESCRIPTION
1	LED "A" Power
2	Ground
3	Key
4	+ Inhibit Keyboard
5	Ground
6	LED "B" Power

Figure 2-35 Keyboard Lock and Speed Indicator J3

Pin 6 can drive an LED to indicate High, 16MHz, processor operation. Pin 1 can can drive an LED indicating any processor speed other than 16MHz. Grounding pin 4 will inhibit any input from the keyboard.

Speaker Connector J4

J4 is a 6-pin right-angled header type of connector.



PIN	DESCRIPTION
1	Speaker Signal (– terminal)
2	Key
3	Ground
4	+5 Volts
5	Volume Control
6	Volume Control

Jumpering pins 5 and 6 together disables the volume circuitry.
External volume control—470 OHM, 1/2 watt Potentiometer between pin 6 and pin 3 with wiper on pin 5.

Figure 2-36 Speaker connector J4

Keyboard Connector J5

J5 is a 10-pin header type of connector.

PIN	DESCRIPTION
1	+ Clock
2	Ground
3	+ Data
4	Ground
5	Power_Good
6	Ground
7	+5 Volts
8	Key
9	Ground
10	Ground

Figure 2-37 Keyboard Connector J5

LOGIC SIGNALS AND THEIR FUNCTIONS

The logic signals listed here are the signals found on the board edge connectors.

SIGNAL	DIRECTION	FUNCTION
RESET	Out	System reset.
IRQ3 - IRQ15	In	Interrupt ReQuest lines. Lines 3 through 7, and 9 through 14 signal the microprocessor that an I/O device needs attention. Interrupt 9 has the highest priority and interrupt 7 the lowest. Signals must be held high until acknowledged by the CPU.
DRQ0 - DRQ7	In	Direct memory access ReQuest lines. Lines 0 through 3, and 5 through 7 allow asynchronous devices in the I/O connectors to request DMA service. +DRQ0 has the highest priority and +DRQ7 has the lowest. A request must remain high until the corresponding DACK is received.
-DACK0 - -DACK7	Out	DACK ACKnowledge lines. They acknowledge DMA requests.
T/C	Out	Terminal Count. This signal indicates that a DMA channel has reached its terminal count.

SIGNAL	DIRECTION	FUNCTION
-MEMW, -SMEMW, -XMEMW	I/O	These control signals indicate a processor or DMA MEMory Write cycle. -SMEMW is active for the 0 to 1MB memory range. -MEMW is active for the 0 to 16MB memory range. -XMEMW is active for the 0 to 256MB range.
-MEMR, -SMEMR,	I/O	This control signal indicates a processor or DMA MEMory Read cycle. -SMEMR is active for 0 to 1MB memory range. -MEMR is active for 0 to 16MB memory range. -XMEMR is active for 0 to 256MB range.
-IOW	I/O	This control signal indicates a processor or DMA I/O Write cycle.
-IOR	I/O	This control signal indicates a processor or DMA I/O Read cycle.
-I/OCH RDY	In	This open collector line is forced low (not ready) by devices in the I/O slot requiring extended memory or I/O cycles. Upon the line returning high (ready), completion of the cycle will occur. The cycle is extended in multiples of clock cycles (62.5ns). This line should not be held low longer than 2.5 microseconds.
OSC	Out	This is a 14.31818 MHz clock with a 50% duty cycle.

SIGNAL	DIRECTION	FUNCTION
+OCLK -OCLK	Out	This is the 16.0 MHz system clock. It has a 50% duty cycle.
AEN	Out	When this line is high, the DMA chip has control of the bus.
-I/O CH CK	In	This line is used to indicate that there is an error on a device in the expansion bus. Activating this line results in an NMI interrupt to the CPU. Memory expansion options commonly use this line to indicate parity errors.
BALE	Out	This signal is used to indicate when the address bus is valid. Processor addresses are latched on the falling edge of BALE.
SD0 - SD31	I/O	Data bus signals
SA0 - SA19	Out	Address bus signals
LA17 - LA27	Out	Address bus signals
0WS	In	The Zero Wait State signal indicates that the present bus cycle can be completed without generating additional waitstates. For 16-bit devices 0WS is generated by anding a decoded address with a read or write command. For 8-bit devices 0WS must become active one CLK cycle after a read or write command.

SIGNAL	DIRECTION	FUNCTION
-REFRESH	I/O	The refresh cycle is driven by the CPU or the expansion bus.
-MASTER	In	This signal tri-states the system boards address, data, and control signals allowing an external device to gain control of the bus.
-MEM CS16	In	This signal indicates a 16-bit memory cycle.
-MEM CS32	In	This signal indicates a 32-bit memory cycle.
-I/O CS16	In	This signal indicates a 16-bit I/O cycle
-I/O CS32	In	This signal indicates a 32-bit I/O cycle.
SBHE	I/O	This signal indicates a data transfer is occurring on SD08-SD16. It is used by 16-bit devices only.
-SBE0 - -SBE3	I/O	Byte enables, which are used by 32-bit devices. -SBE0 - data transfer on SD0-SD7 -SBE1 - data transfer on SD8-SD15 -SBE2 - data transfer on SD16-SD23 -SBE3 - data transfer on SD24-SD31
+MEMS	Out	Similar to BALE, but is only generated for memory cycles. It is intended to be used for an advance decode when using dynamic RAMs.

SIGNAL	DIRECTION	FUNCTION
-PL32	In	This signal is pulled low by a board operating in pipeline mode.
-ENRAM	Out	Disables 32-bit RAM.
-LW/R	Out	Latched CPU Read/Write status.

MEMORY MAPPED I/O ASSIGNMENTS

The CPU dedicates ten address bits, A0 to A9, to address 1K bytes of address space for I/O instructions. The address map defined is shown in Figure 2-38.

ADDRESS	DEVICE
000 – 01FH	DMA chip 1 (8237A – 5)
020 – 03FH	Interrupt controller 1 (8259A – 1)
040 – 05FH	Timer chip 8254 – 2
060 – 06FH	Keyboard controller (8742)
070 – 07FH	T – O – D chip, DMA mask
080 – 08FH	DMA page register (74LS612)
090	DMA holding latch to address memory above 16MB
0A0 – 0BFH	Interrupt controller 2 (8237A – 5)
0C0 – 0DFH	DMA chip 2 (8237A – 5)
0F0H	Clear math coprocessor busy
0F1H	Reset math coprocessor
0F8 – 0FFH	Math coprocessor

Figure 2-38. I/O Memory Map

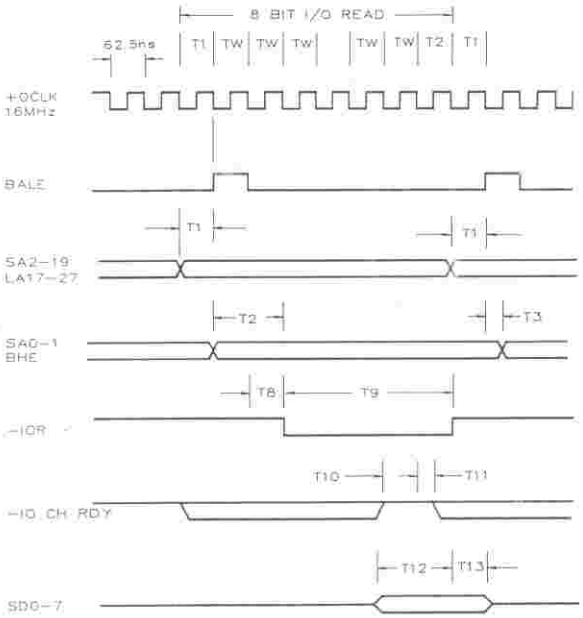
Reserved I/O addresses for specific devices in the expansion slots are shown in Figure 2-39.

ADDRESS	DEVICE
1F0 – 1F8H	Fixed disk controller
200 – 20FH	Game adapter
278 – 27FH	Parallel printer port (secondary)
2F8 – 2FFH	Serial port (secondary)
300 – 31FH	Prototype card
330 – 35FH	Reserved
360 – 36FH	Reserved
378 – 37FH	Parallel printer port (primary)
380 – 38FH	SDLC/BISYNC (pimary)
390 – 39FH	Reserved
3A0 – 3AFH	SDLC/BISYNC (primary)
3B0 – 3BFH	Monochrome CRT and Parallel port
3C0 – 3CFH	Reserved
3D0 – 3DFH	Color/graphics CRT adapter
3E0 – 3EFH	Reserved
3F0 – 3FFH	Flex disk adapter
3F8 – 3FFH	Serial Port (primary)

Figure 2-39 Reserved I/O addresses

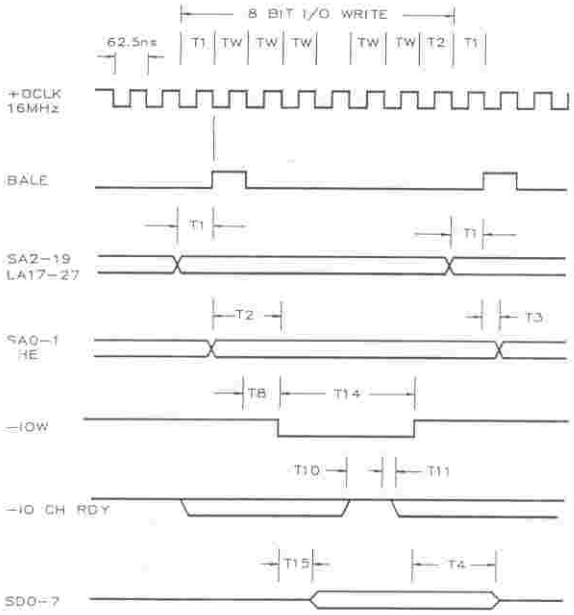
SYSTEM TIMING

The following diagrams show the system timing. Figures 2-40 through 2-50 cover 8-, 16-, and 32-bit read and write cycles.



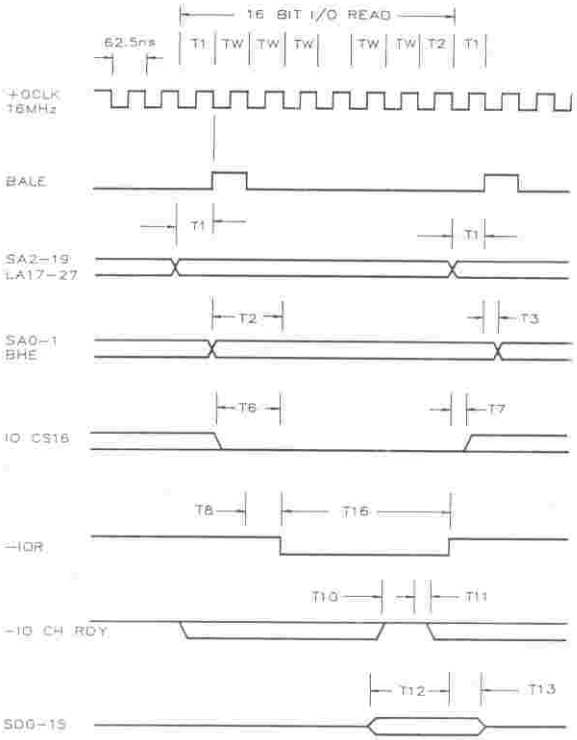
8-bit I/O Read to 8-bit I/O device

Figure 2-40 Timing diagram



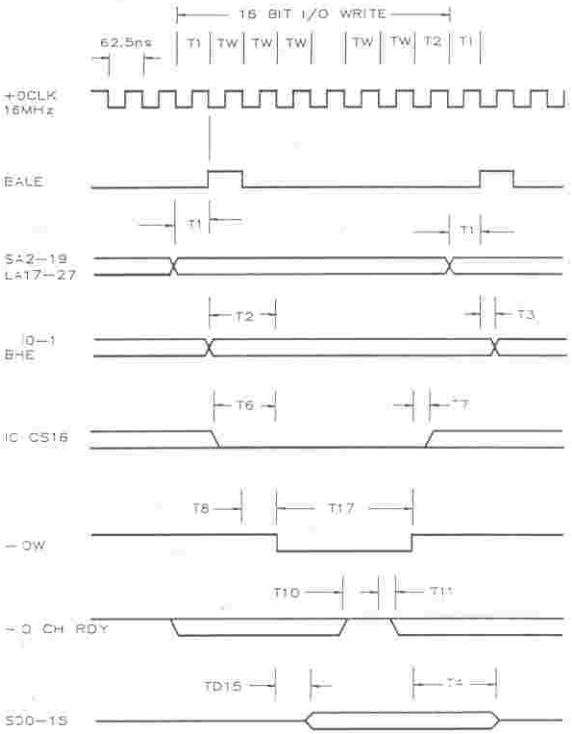
8-bit I/O Write to 8-bit I/O device

Figure 2-41 Timing diagram



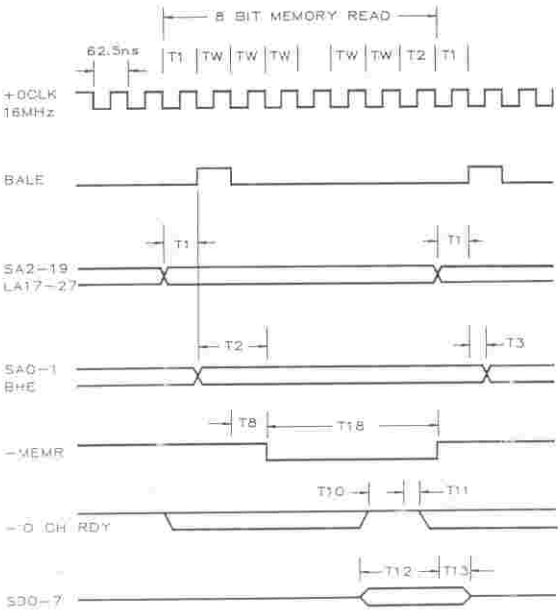
16-bit I/O Read to 16-bit I/O device

Figure 2-42 Timing diagram



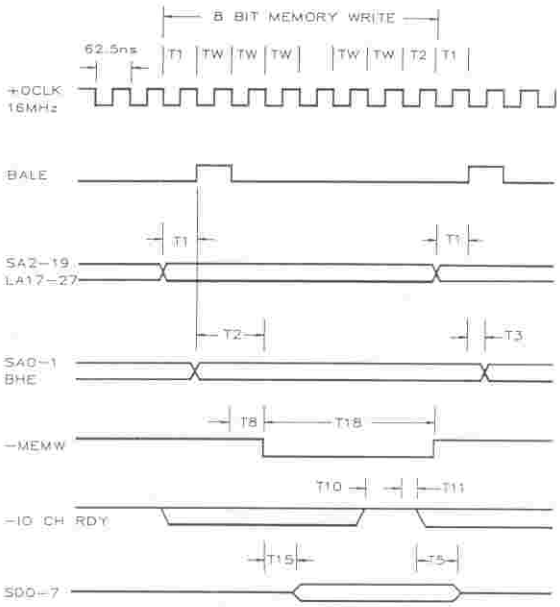
16-bit I/O Write to 16-bit I/O device

Figure 2-43 Timing diagram



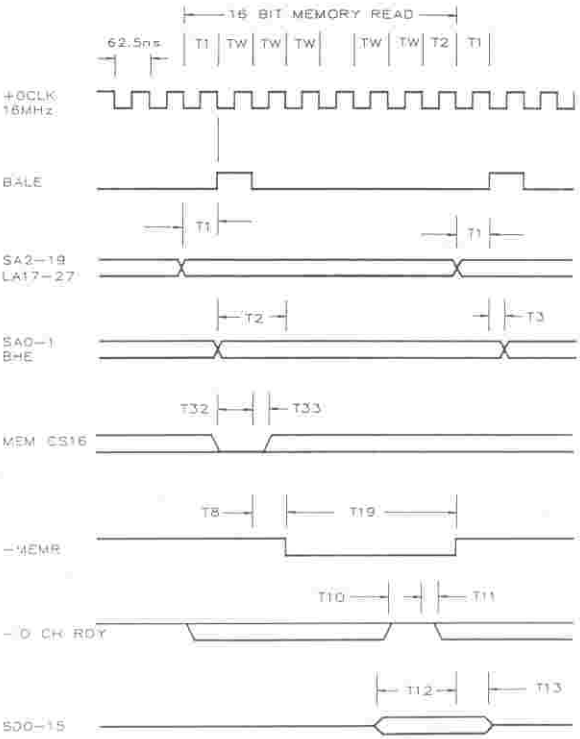
8-bit Memory Read to 8-bit Memory

Figure 2-44 Timing diagram



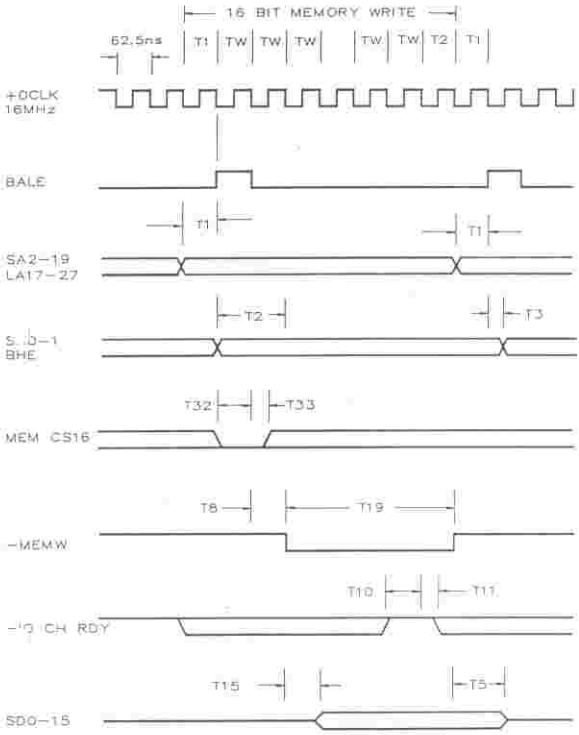
8-bit Memory Write to 8-bit Memory

Figure 2-45 Timing diagram



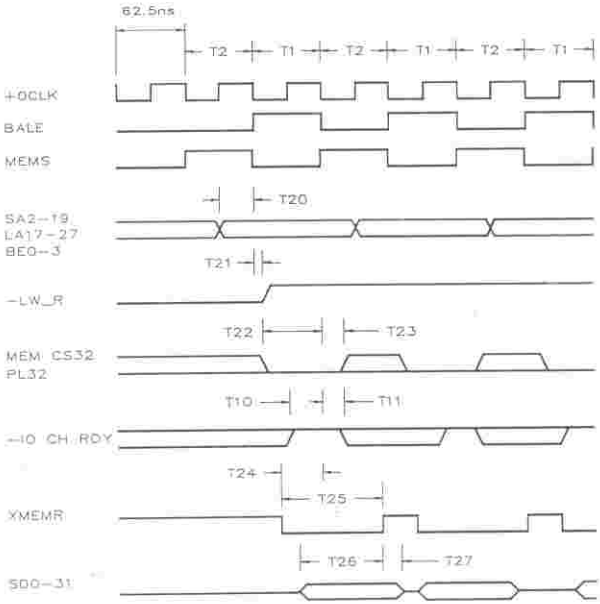
16 bit Memory Read to 16-bit Memory

Figure 2-46. Timing diagram



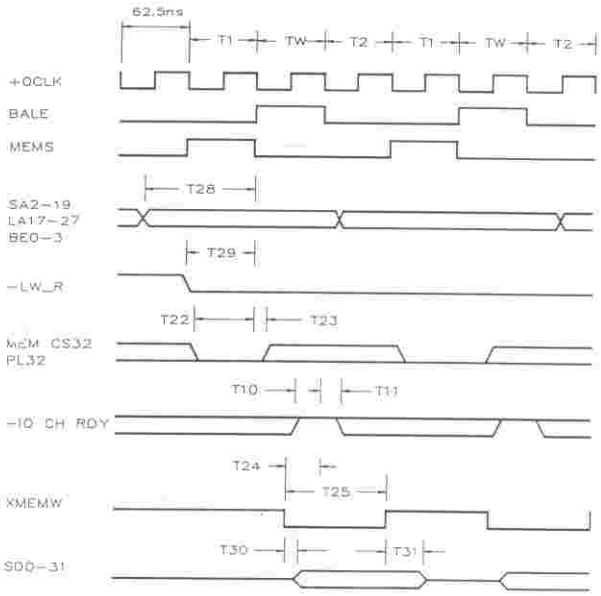
16-bit Memory Write to 16-bit Memory

Figure 2-47 Timing diagram



32-bit Memory Read to 32-bit Memory

Figure 2-48 Timing diagram



32-bit Memory Write to 32-bit Memory

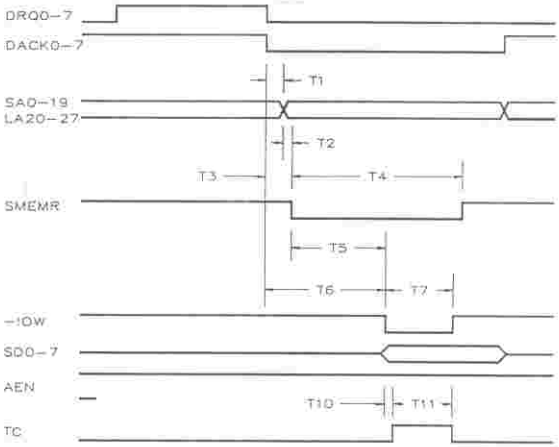
Figure 2-49 Timing Diagram

Figure 2-50 is a timing chart for the previous timing diagrams.

Time	Name	Min.	Typ.	Max.
T1	SA2-19,LA17-27 valid before BALE active		50.0	
T2	SA0-1,BHE valid before command active		125.0	
T3	SA0-1,BHE valid after BALE active		15.0	
T4	SD0-7 hold time after IOW inactive		80.0	
T5	SD0-15 hold time after MEMW inactive		20.0	
T6	IOCS16, MEMCS16 setup time before command		25.0	
T7	IOCS16, MEMCS16 hold time after command		0.0	
T8	IOR,IOW,MEMR,MEMW active after BALE inactive		65.0	
T9	8 bit IOR pulse width		687.5	
T10	IO CH RDY setup time		20.0	
T11	IO CH RDY hold time		10.0	
T12	SD0-7, SD0-15 setup time		50.0	
T13	SD0-7, SD0-15 hold time		0.0	
T14	8 bit IOW pulse width		625.0	
T15	SD0-7, SD0-15 valid after IOW,MEMW active		0.0	
T16	16 bit IOR pulse width		437.5	
T17	16 bit IOW pulse width		375.0	
T18	8 bit MEMR, MEMW pulse width		500.1	
T19	16 bit MEMR, MEMW pulse width		250.0	
T20	SA2-19,LA17-27 valid before BALE active		50.0	
T21	-LW_R setup time		7.0	
T22	MEMCS32, PL32 setup time		25.0	
T23	MEMCS32, PL32 hold time		10.0	
T24	32 bit XMEMR, XMEMW active before BALE inactive		20.0	
T25	32 bit XMEMR, XMEMW pulse width		92.0	
T26	SD0-31 setup time		40.0	
T27	SD0-31 hold time		0.0	
T28	SA2-19,LA17-27 valid before BALE active		112.0	
T29	-LW_R setup time		69.0	
T30	SD0-31 valid after 32 bit XMEMW active		0.0	
T31	SD0-31 hold time		10.0	
T33	MEMCS16 setup time		15.0	
T33	MEMCS16 hold time		0.0	

Figure 2-50 Timing chart

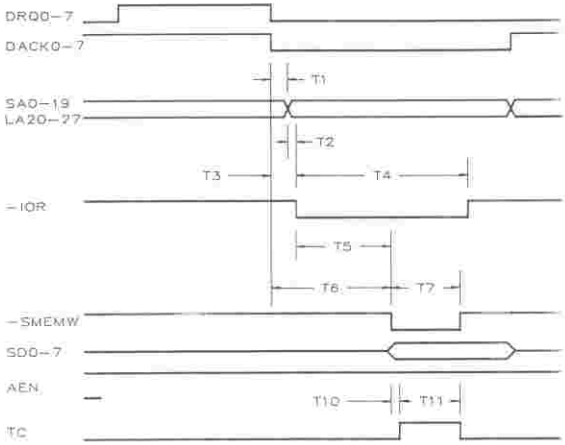
The following six timing diagrams, Figures 2-51 through 2-56 show the 4-megahertz DMA Read and Write cycles for 8-, 16-, and 32-bit memorys. Eight-megahertz DMA cycles are a future development and are not covered in this manual.



Time	Name	Min.	Typ.	Max.
T1	DACK active before SA0-19,LA19-27 valid	-167.5		365.5
T2	SA0-19,LA19-27 valid before SMEMR active	17.0		470.5
T3	DACK ACTIVE before SMEMR active	80.0		473.0
T4	SMEMR pulse width		750	
T5	SMEMR active before IOW active		250	
T6	DACK active before IOW active	330.0		723.0
T7	IOW pulse width		500	
T10	TC valid after IOW active	-223.0		173.4
T11	TC pulse width	326.6		673.4

DMA Read from 8-bit memory to 8-bit I/O

Figure 2-51 Timing diagram

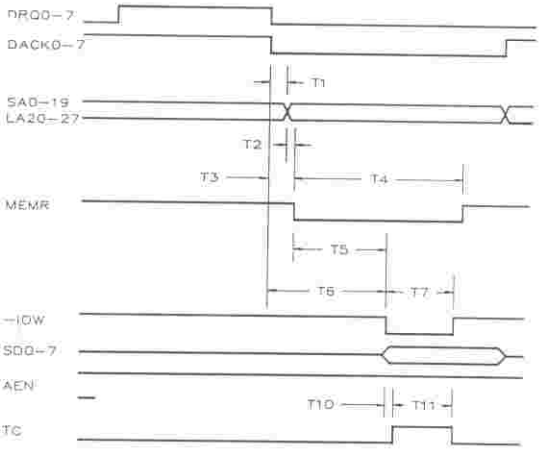


Time	Name	Min.	Typ.	Max.
T1	DACK active before SA0-19,LA19-27 valid	-167.5		365.5
T2	SA0-19,LA19-27 valid before IOR active	17.0		470.5
T3	DACK ACTIVE before IOR active	80.0		473.0
T4	IOR pulse width		750	
T5	IOR active before SMEMW active		250	
T6	DACK active before SMEMW active	330.0		723.0
T7	SMEMW pulse width		500	
T10	TC valid after SMEMW active	-223.0		173.4
T11	TC pulse width	326.6		673.4

I/O Memory

DMA Write from 8-bit memory to 8-bit ~~I/O~~

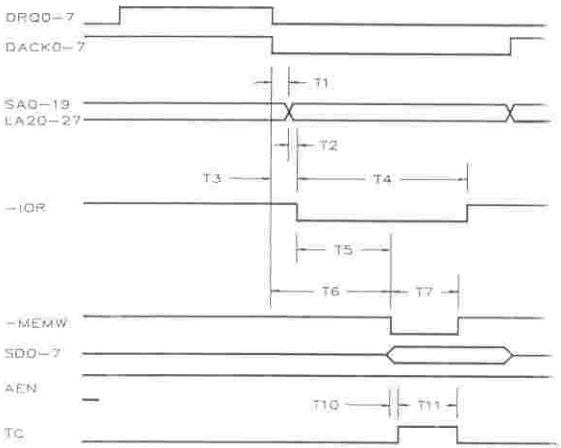
Figure 2-52 Timing diagram



Time	Name	Min.	Typ.	Max.
T1	DACK active before SA0-19,LA19-27 valid	-167.5		365.5
T2	SA0-19,LA19-27 valid before /MEMR active	17.0		470.5
T3	DACK ACTIVE before /MEMR active	80.0		473.0
T4	MEMR pulse width		710	
T5	MEMR active before IOW active		250	
T6	DACK active before IOW active	330.0		723.0
T7	IOW pulse width		500	
T10	TC valid after IOW active	-223.0		173.4
T11	TC pulse width	326.6		673.4

DMA Read from 16-bit memory to 8-bit I/O

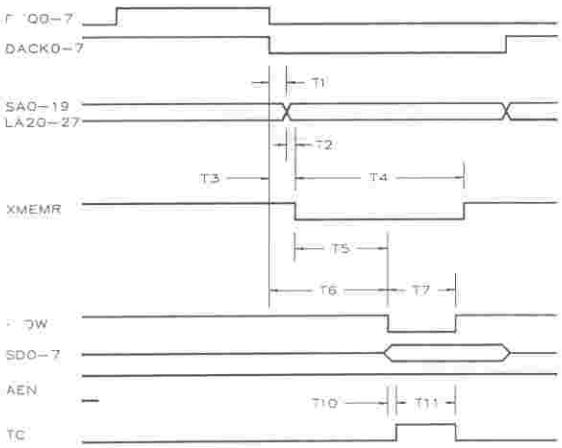
Figure 2-53 Timing diagram



Time	Name	Min.	Typ.	Max.
T1	DACK active before SA0-19,LA19-27 valid	-187.5		365.5
T2	SA0-19,LA19-27 valid before IOR active	17.0		470.5
T3	DACK ACTIVE before IOR active	80.0		479.0
T4	IOR pulse width		750	
T5	IOR active before MEMW active		250	
T6	DACK active before MEMW active	330.0		723.0
T7	MEMW pulse width		500	
T10	TC valid after MEMW active	-223.0		173.4
T11	TC pulse width	326.5		673.4

DMA Write from 16-bit memory to 8-bit I/O

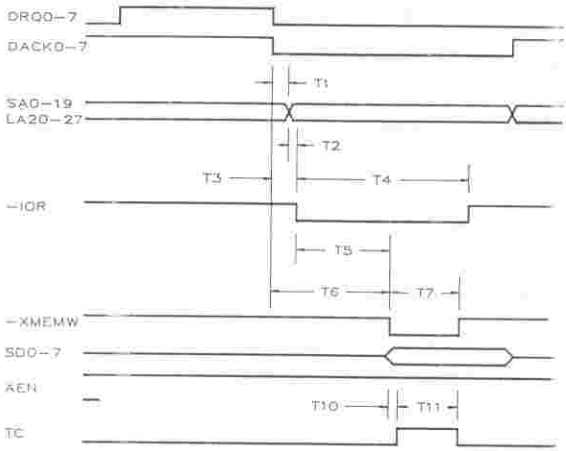
Figure 2-54 Timing diagram



Time	Name	Min.	Typ.	Max.
T1	DACK active before SA0-19,LA19-27 valid	-167.5		365.5
T2	SA0-19,LA19-27 valid before XMEMR active	17.0		470.5
T3	DACK ACTIVE before XMEMR active	80.0		473.0
T4	XMEMR pulse width		750	
T5	XMEMR active before IOW active		250	
T6	DACK active before IOW active	330.0		723.0
T7	IOW pulse width		500	
T10	TC valid after IOW active	-223.0		173.4
T11	TC pulse width	76.6		423.4

DMA Read from 32-bit memory to 8-bit I/O

Figure 2-55 Timing diagram



Time	Name	Min.	Typ.	Max.
T1	DACK active before SA0-19,LA19-27 valid	-167.5		365.5
T2	SA0-19,LA19-27 valid before IOR active	17.0		470.5
T3	DACK ACTIVE before IOR active	80.0		473.0
T4	IOR pulse width		250	
T5	IOR active before XMEMW active		250	
T6	DACK active before XMEMW active	330.0		723.0
T7	XMEMW pulse width		500	
T9	Data tri-state after XMEMW active	50.0		
T10	TC valid after XMEMW active	-223.0		173.4
T11	TC pulse width	76.6		423.4

DMA Write from 32-bit memory to 8-bit I/O

Figure 2-56 Timing diagram

DESCRIPTION OF I/O CHANNEL BUS TIMING

MEMORY READ OPERATION

A memory read operation is performed when a -MEMR command is sent to the I/O channel. The CPU places the address of the memory location on the address bus. The address is valid for some minimum time period before -MEMR goes low. The I/O device (a memory device in this case) must place the data from the corresponding memory location onto the data bus within a specified length of time. If the memory device is unable to provide the data soon enough, it pulls I/O Channel Ready low. I/O CH RDY going inactive causes the READY line to the processor to go low, thus effecting extra wait states. These wait states extend the memory cycle, giving the memory device enough time to place data on the bus. The memory device should hold I/O CH RDY low until it places valid data on the bus. Data should remain valid until -MEMR becomes inactive.

MEMORY WRITE OPERATION

A memory write operation occurs when a -MEMW command is sent across the I/O channel. The CPU places the address of the memory location to which it is writing on the bus prior to the -MEMW command. The CPU places the data on the data bus by at least some known time period after -MEMW becomes active. The memory device must read the data from the bus within a specified length of time. If the device needs more time to retrieve the data from the bus, it may drive I/O Channel Ready low. This action causes the READY line to the CPU to go low and thus causes wait states to be generated. The wait states extend the memory cycle, giving the device more time to access the data.

I/O READ OPERATION

The I/O read operation involves the CPU placing the address of the corresponding I/O peripheral onto the address bus. The -IOR command is sent onto the channel after the address is valid. The I/O peripheral must place its data on the bus within the specified default

period. If the peripheral is not fast enough, it can drive I/O Channel Ready low (inactive). I/O Channel Ready being inactive causes the CPU to be in a wait state and thus extends the I/O cycle. The device should hold I/O CH RDY low until it has placed the data on the bus. Valid data should remain on the bus until -IOR goes inactive.

I/O WRITE OPERATION

The I/O write operation begins with the CPU placing the address of the I/O peripheral on the address bus. The -IOW command is then sent onto the bus. After -IOW becomes active, the CPU must put the data onto the data bus. The I/P peripheral is required to retrieve this data within the time specified for the default case. If the device cannot read the data quickly enough, it drives I/O Channel Ready low to introduce wait states. The device should hold I/O CH RDY low until it has received all of the data.

DMA READ OPERATION

The DMA read operation is initiated by the -DACK (DMA Acknowledge) signal becoming active. The DMA controller also sends out the address of the memory location to be read. Since a memory location will be read and data will be written to an I/O device, -MEMR becomes active, followed by -IOW becoming active. Data becomes valid no later than 250 nanoseconds after -MEMR goes low. The I/O device has until 50 nanoseconds after the rising edge of the -IOW pulse to latch in the data. The device will receive a T/C signal to indicate that the terminal count has been reached.

DMA WRITE OPERATION

The DMA write operation also begins with the 8237 DMA controller sending a -DACK to the device requesting the DMA transfer. The DMA controller sends out to the I/O address bus the memory address at which the device's data must be written. Some time after this address becomes valid the 8237 sends a -IOR pulse onto the I/O channel and subsequently a -MEMW pulse as well. The I/O device must place valid data on the bus no later than 250 nanoseconds after -IOR becomes valid. Data must remain valid until -MEMW goes high. The I/O device receives a T/C pulse to indicate that the DMA controller reached its terminal count.

Switches, Jumpers, and Adjustments

The following sections identify the switches and jumpers that are on the MPB and the Memory Board and give the settings for each of them. In this manual the name "jumper" is used to mean the small push-on connector that connects two or more pins together electrically, or any other movable connection performing that function. The term "strap" or "strapping" is sometimes used in other descriptions to mean the same thing.

MPB SWITCHES

Switch and jumper locations are shown on the simplified MPB diagram in Figure 3-1. Switch block SW1 is a slide handle switch located in the upper left area. Switch block SW2 is an eight position DIP switch located in the upper center area. Jumper JP1 is in the upper right corner, and jumper JP2 is in the lower right corner.

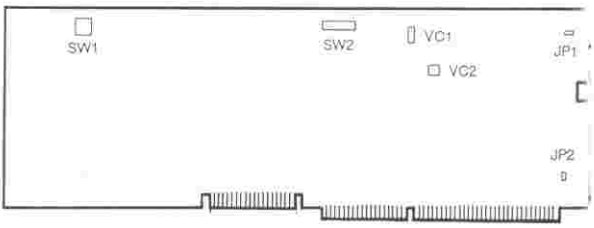


Figure 3-1 MPB Switch locations

MPB SWITCH BLOCK 1 (SW1)

SW1 is a single pole slide handle switch mounted in the upper left corner of the board with the handle protruding above the board edge.

The switch controls the type of display that is active. Figure 3-2 illustrates the switch and defines the settings in the table.

SW1 POSITION	DISPLAY
HANDLE RIGHT	MONOCHROME, 80 Characters, 25 lines
HANDLE LEFT	COLOR/GRAPHICS

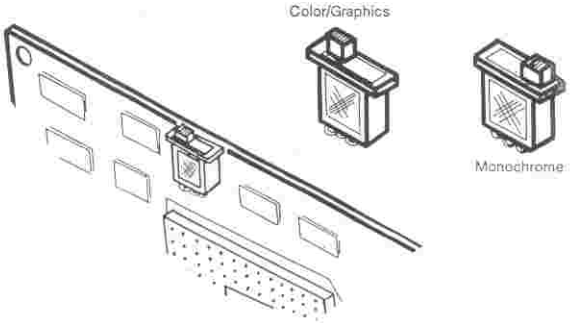


Figure 3-2 MPB SW1 Positions

MPB SWITCH BLOCK 2 (SW2)

SW2 is an eight position Dual-Inline-Package (DIP) switch mounted at the top center area of the board. The individual switches are constructed so that the switch is "on" or "closed" when the handle is toward the top of the board or the top portion of the rocker is depressed. Actual switch construction may vary.

The switch positions control several user selectable options. The table in Figure 3-3 lists the switch positions and uses, and Figure 3-4 shows the same settings in a quick reference form. In the diagrams, switches not involved in the function being explained are left blank to avoid confusion.

Positions 1 and 2 identify the type of coprocessor installed, 80387 or 80287, if any. Only one type can be installed at one time.

Position 3 selects the mode of the DMA Page Register. Either the Extended mode or the PC/AT compatible mode may be chosen.

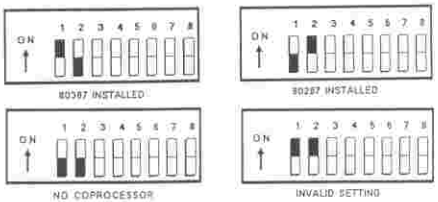
Position 4 controls whether a Non Maskable Interrupt (NMI) is allowed to be generated from the fail-safe timer.

Positions 5,6, and 7 control which, if any, of the interrupt request lines (IRQ) are connected to channel 4 of the enhanced timer. Only one of the IRQ lines may be connected at any one time, and only one of the switches may be in the "on" position.

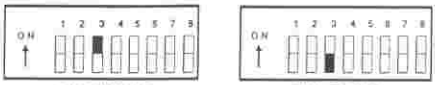
Position 8 controls processor speed. High speed is 16 MHz all of the time. Automatic speed is 16 MHz except when the flex disk is accessed and 8 MHz during flex disk access. The option allows disk protection schemes which are dependent on processor speed to load correctly on the system.

SWITCH NUMBER	FUNCTION	POSITION
1	80387 Coprocessor	ON = Installed OFF = Not Installed
2	80287 Coprocessor	ON = Installed OFF = Not Installed
3	DMA Mode	ON = PC/AT Compatible OFF = Extended Mode
4	Fail-safe Interrupt	ON = Enabled OFF = Not Enabled
5	IRQ 10	ON = Selected OFF = Not Selected
6	IRQ 11	ON = Selected OFF = Not Selected
7	IRQ 12	ON = Selected OFF = Not Selected
8	Processor Speed	ON = High Speed 16 MHz OFF = Automatic 8/16 MHz

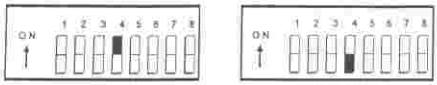
Figure 3-3 MPB SW2 Settings



COPROCESSOR SWITCHES

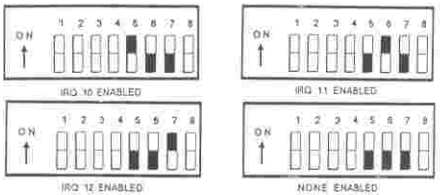


DMA MODE SWITCH

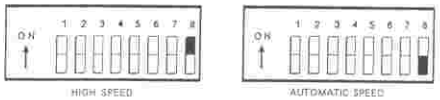


FAIL-SAFE INTERRUPT SWITCH

Figure 3-4 MPB SW2 settings (1 OF 2)



INTERRUPT REQUEST LINES SWITCHES



PROCESSOR SPEED SWITCH

Figure 3-4. MPB SW2 settings (2 of 2)

MPB JUMPERS

Jumpers JP1 and JP2 control user selectable options. The jumpers are small plastic push-on caps with metal sockets that connect two pins together electrically when installed. They are approximately 1/4 inch wide by 1/8 inch thick and 1/2 inch tall. When a jumper is installed on the pins it connects the pins together, and when the jumper is removed the pins are disconnected from each other.

MPB JUMPER JP1

JP1 is located in the top right corner of the board. Do not confuse it with J1 which is similar in appearance but in the lower right corner. The JP1 jumper block is a two-pin header used for selection of the source of the Power_Good signal. Power_Good is internally connected from the power supply to the logic without going through the jumper. If the power supply does not have the Power_Good signal, an RC circuit on the board can supply a substitute signal. Install the jumper JP1 on the pins to connect the RC circuit to the logic. The jumper must not be installed if the power supply provides the Power_Good signal. Hardware damage could result if both sources are present and connected together by the jumper. One or the other of the sources must be used because if neither source is present, the system may not power up. The table in Figure 3-5 shows the JP1 settings.

JP1	POWER_GOOD SOURCE
ON	RC CIRCUIT
OFF	POWER SUPPLY

Figure 3-5 MPB JP1 Settings

MPB JUMPER JP2

JP2 is located in the lower right corner of the board. It selects the DMA operating speed as shown in the table in Figure 3-6. Do not confuse JP2 with J1 which is adjacent and similar in appearance. DMA speed is not user selectable on all boards. If JP2 is not populated, then the DMA speed is fixed at 4 MHz.

JP2	DMA SPEED
OFF	4 MHz
ON	8 MHz

Figure 3-6 MPB JP2 Settings

MPB ADJUSTMENTS

The board contains an adjustable capacitor VC1 to trim the 14.31818 MHz clock. It is located in the upper right-center area of the board as shown in Figure 3-1. The clock signal frequency is used by the color video and other boards. The capacitor should be adjusted to 14.31818 MHz + or - 500 Hz at pin B30 on the I/O bus connector.

The board also contains an adjustable capacitor VC2 for the Time-of-Day clock. It also is located in the upper right-center area of the board but below VC1 as shown in Figure 3-1. The capacitor, VC2, should be adjusted to 32.768 KHz + or - 1 Hz at pin 63 on U9.

MEMORY BOARD SWITCHES

Switch and jumper locations for the Memory Board are shown in the simplified board diagram in figure 3-7. Switch blocks SW1 and SW2 are each 8-position DIP switches mounted on the board. SW1 is located in the extreme lower left corner of the board, and SW2 is to the right of SW1 near the 36-pin edge connector.

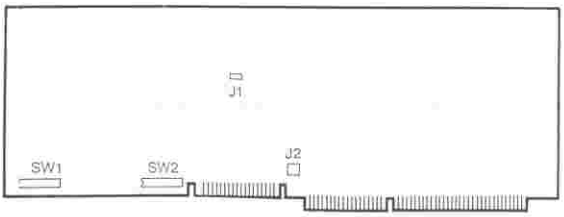


Figure 3-7 Memory Board switch locations

MEMORY BOARD SWITCH BLOCK 1 (SW1)

Switch block 1 has two functions. First, switches S1 through S7 assign the memory on each board to a location in the memory space. Second, switch S8 identifies the board that has the first megabyte of memory.

Memory Board SW1, S1 through S7

The seven switches, S1 through S7, on switch block SW1 control the assigned location of the memory on each board. Locations are allocated in two-megabyte boundaries within the memory space. The

system can address a total of 256 megabytes of memory space using its 128 binary switch combinations and the two-megabyte boundaries. Expansion bus connector boards are currently available to accommodate up to four of the 32-bit memory boards. Figure 3-8 shows the memory space identification.

The DOS operating system recognizes memory in a continuous sequence without any empty spaces. The MPB searches for memory starting at the zero megabyte location and continues in numerical order until it finds an empty location. When it finds an empty location it stops searching. Other operating systems may allow different memory assignments and are not described here.

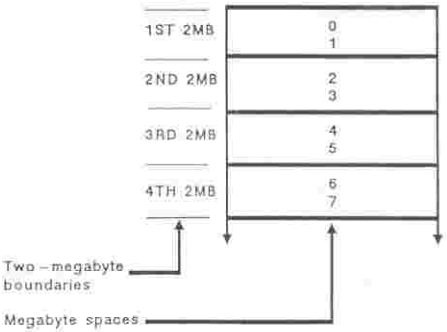


Figure 3-8 Memory space identification

Both two-megabyte and one-megabyte boards can be used in a system. If a one-megabyte board is used, however, it must be assigned the last megabyte location in the configuration. Otherwise the one-megabyte memory would appear within its two-megabyte boundary with no memory in the other part of the boundary. The MPB would stop the search for memory at the empty location and any additional memory would be lost.

Further, each board must be assigned a separate location in the memory space. If sections of memory overlap, that is, if more than one section of memory is assigned the same address, the memory chips will effectively be in parallel, and will act as if only one of the boards is installed.

To set the switches of SW1, the "on", or "up", position of the individual switches is binary "one" and the "off", or "down", position binary "zero". The switches number from left to right with switch "1" being the least significant. The combinations of settings progress in inverse binary sequence through the range of zero through 127. The inverse of zero combination (all "on") locates the boundary for the two megabytes, 0 and 1; the inverse of "one" setting (S1 "off", all others "on") is for the boundary for the two megabytes 2 and 3; and so on continuing in inverse binary sequence. Thus with these memory boards in the DOS operating system, switches S1 and S2 count locations for the first eight megabytes (0 through 3 in two megabyte boundaries) and switches S3 through S7 are always in the "on" position. Figure 3-9 illustrates the way the switches are assigned, and Figures 3-11 through 3-16 show some example settings.

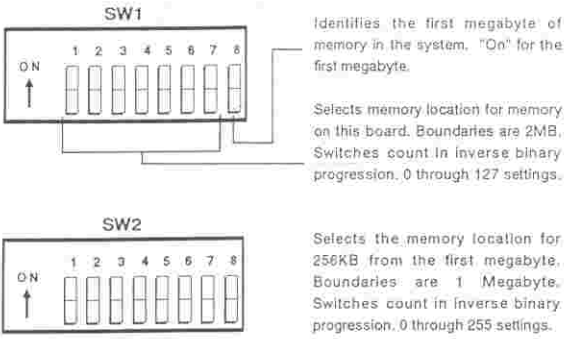


Figure 3-9 Allocation of switch positions

Memory Board SW1, Switch S8

Switch S8 identifies the first megabyte in the system because it is organized separately from the others. The first megabyte is divided into three separate parts while all other megabytes are available intact to the user. The first part is 640KB of user memory that is available for programs. The second part is 256KB for video display and expansion ROM. The third part is 128KB where BIOS and BIOS extensions are read into RAM memory at startup. The memory map in Figure 3-10 shows the layout of memory on an example board.

The actual 256KB of memory used for the video and expansion ROM functions resides within that hardware, and as a result the 256KB from 000A0000H to 000DFFFFH is displaced. To use that displaced 256KB and not waste it, the 256KB must be positioned at the very end of installed memory. Switch S8 identifies the board that contains the 256KB that is to be relocated. The "on" or "up" position of S8 indicates the first megabyte, and the "off" or "down" position is for all other megabytes. The setting of SW2 determines where the 256KB will be located as described in the following paragraphs. Figure 3-9 also illustrates the S8 switch assignment.

MEMORY BOARD SWITCH BLOCK 2 (SW2)

SW2 positions the 256KB of memory transferred from the first megabyte of memory to the end of the installed memory. The eight switches, S1 through S8, control the assigned location in one-megabyte boundaries. Thus, with its eight switches in all of their binary combinations, SW2 covers the 256 megabyte locations in memory space.

For the memory board that has the first megabyte of memory, the SW2 settings locate the 256KB as described above. For any other memory boards, all eight switches of SW2 must be set to "off". The total memory may give unpredictable results with incorrect settings. No permanent damage will happen to the hardware, however, by incorrect settings. Figure 3-9 also illustrates SW2 schematically. Figures 3-11 through 3-16 show example switch settings.

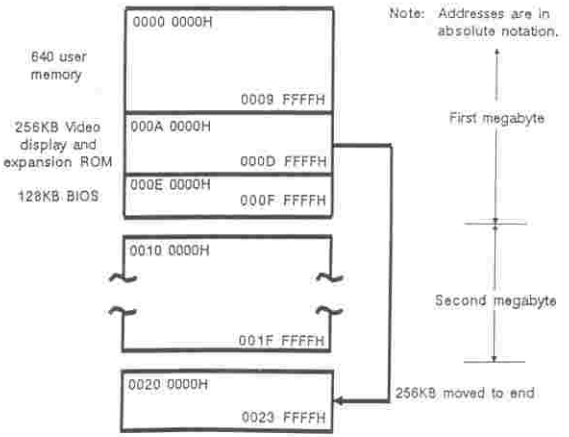
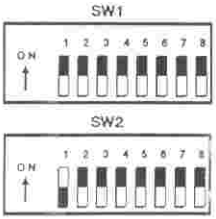


Figure 3-10 Memory map of first board

To set the switches of SW2, the "on", or "up", position of the individual switches is binary "one" and the "off", or "down", position binary "zero". The switches number from left to right with switch "1" being the least significant. The combinations of settings progress in inverse binary sequence through the range of 0 through 255. Fix the switch combinations to the number of the next megabyte that can be installed. If megabyte "zero" is the only one installed, set the switches for the inverse of "1", S1 "off" and all others "on". If megabyte "one" is the last one installed set the switches for the inverse of "2", S2 "off", all others "on", and so on.

One-megabyte board in first megabyte space

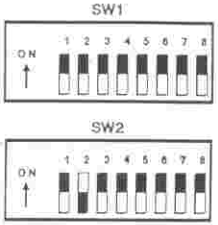


Set for the first 2MB boundary. (megabyte space zero)

Set to locate the 256KB in the second (# one) megabyte space.

Figure 3-11 Example switch settings

Two-megabyte board in the first two-megabyte boundary

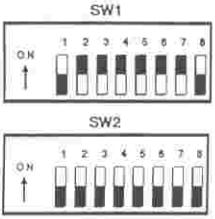


Set for the first 2MB boundary. (megabyte spaces 0 and 1)

Set to locate the 256KB in the third (# two) megabyte space.

Figure 3-12 Example switch settings

Two megabyte board in the second two-megabyte boundary

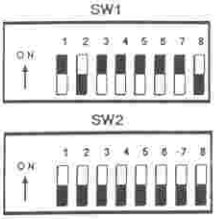


Set for the second 2MB boundary. (megabyte spaces 2 and 3)

All switches off— not the first megabyte in the system.

Figure 3-13 Example switch settings

Two megabyte board in the third two-megabyte boundary

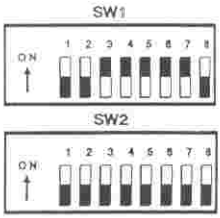


Set for the third 2MB boundary. (megabyte spaces 4 and 5)

All switches off— not the first megabyte in the system.

Figure 3-14 Example switch settings

Two megabyte board in the fourth two-megabyte boundary

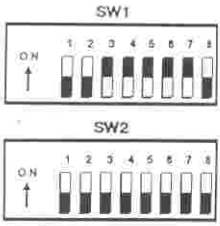


Set for the fourth 2MB boundary (megabyte spaces 6 and 7)

All switches off–not the first megabyte in the system.

Figure 3-15. Example switch setting

One-megabyte board in the fourth two-megabyte boundary



Set for the fourth 2MB boundary. (megabyte space 6)

All switches off– not the first megabyte in the system.

Figure 3-16 Example switch setting

MEMORY BOARD JUMPERS

Jumpers on the memory board are small plastic push-on connectors similar in appearance to the jumpers used on the MPB. They slip over two protruding pins in the jumper block to connect the pins together electrically.

MEMORY BOARD JUMPER J1

Jumper block J1 is a three-pin header located approximately in the center of the board. The jumper selects memory chip speed for 70-nanosecond or 120-nanosecond RAM. Connect the left and center pins of the set for 70-nanosecond operation, and the right and center pins for 120-nanosecond operation. Figures 3-17 and 3-18 show the jumper pin identification and jumper installation positions.

Figure 3-17 J1 Jumper pin identification

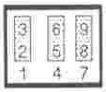
MEMORY SPEED	PINS JUMPERED
70 nanosecond	left – center
120 nanosecond	right – center

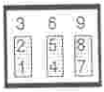
Figure 3-18 J1 Jumper settings

MEMORY BOARD JUMPER J2

Jumper block J2 is located in the bottom center area of the board between the two 36-pin edge connectors, and has provision for three push-on jumper connectors. The jumper block consists of three 3-pin headers arranged in a three by three square. Push-on connectors join two of the pins in each vertical column to select either one-megabyte or two-megabyte memory. Figures 3-19 and 3-20 show the jumper positions and their connection assignments. Avoid mixing up and down settings of the jumpers because incorrect operation may result. Improper settings will not permanently damage the hardware, however.

Figure 3-19 J2 Jumper pin numbering





MEMORY SIZE	PINS JUMPERED
1MBYTE	2–3, 5–6, 8–9
2MBYTE	1–2, 4–5, 7–8

Figure 3-20 J2 Jumper settings

OTHER MEMORY BOARDS

Memory boards of other types of 16- or 32-bit design may also be used with the MPB when installed after the first megabyte. The first megabyte must be divided into sections as described previously and must connect to the 32-bit bus to act correctly with the MPB. The other boards must also be PC/AT compatible and plug into the standard bus. For those boards of other design, set the memory board switches in accordance with the manufacturers instructions, directing the memory to the megabyte locations contiguous with the installed memory. The processor determines if they are 16- or 32-bit construction and accommodates for the type. The 256KB transferred from the first megabyte can be set to the end of installed memory, but can only be moved in one megabyte boundaries. Memory increments as small as 64KB can be recognized by the MPB as long as there are no gaps in the locations. Memory with either 70- or 120-nanosecond chips can be used, but if they are mixed they must all be used at the slower speed.

MEMORY BOARD ADJUSTMENTS

The memory board is constructed using fixed components, and no field adjustments are required.

Diagnostics

LEVEL 0 DIAGNOSTICS

Diagnostics tests execute each time the 386 Board powers-on and before any other activity starts. The tests are "Level 0 Diagnostics", or "Power-On Self Tests" (POST). This chapter describes those level 0 tests that are about the MPB and the memory board. Other levels of diagnostics, such as Service Diagnostics, test complete processor systems and their peripherals in greater detail. This manual does not describe those other diagnostics. The test routines are resident in the ROM BIOS and are an integral part of the board.

The tests aid in determining that a system is properly operational, or in identifying there is a failure. If there is a failure, the test results give help in finding the general area of the failure. Normal messages and error messages are customarily output to the video display and the audio device. Although these tests are only for the MPB and Memory boards, the system must include enough support hardware to operate the boards. It must also include enough support hardware to communicate the output to the user. Support hardware includes power supply, busses, keyboard, and other basic equipment.

A testpoint code is also output through the MPB. This is especially helpful in instances when a malfunction prevents a useful video display. The testpoint code on the bus is available to read with a plug-in LED test board. Figure 4-2 shows an example of the LED test board. Later in this chapter there is a complete list of Testpoint Code Numbers and their use.

Power fail/recovery circuitry is not implemented on this board.

LEVEL 0 DIAGNOSTICS MESSAGES

There are three forms of Level 0 Diagnostics messages in this set. Two are the visible and audible signals, and the third form is the testpoint output. The first is "Beeps" from the audio device.

Audio Beeps

Audio signals give the following information:

- Five short beeps indicate an unrecoverable error and the system halts.
- Three short beeps indicate a recoverable error, and the system continues to run.
- One long beep indicates successful completion of Level 0 Diagnostics. If the signature "CA" is present in the first two bytes of a ROM at segment address E000H, control is in that ROM. If there is no ROM at that address, control goes to the boot vector, interrupt 19H.

Video Display Messages

The second form of Level 0 Diagnostics messages is the video display. Messages on the video display give more information and on a much wider range of possible errors. The complete list of errors and meanings appears later in this chapter.

Testpoint Indications

The third form of messages is the Testpoint Codes. Specific codes are output on both the 8-bit bus and the parallel port. They are presented at DMA Page Register address 80H and parallel port address 378H. The parallel port is not available on the MPB but would be on a board such as a printer driver. The codes indicate a variety of possible errors or instructions. The table of codes and meanings also appears later in this chapter.

LEVEL 0 DIAGNOSTIC PHASES

There are three phases of Level 0 diagnostics:

1. Initial MPB diagnostics – verifies that the Main Processor Board is functioning properly.
2. System test and initialization – tests and initializes system boards for normal operation.
3. System configuration verification – compares defined configuration with hardware actually installed.

Initial 386 Board Tests

Before Level 0 routines load the operating system, they make some basic checks on the Main Processor Board. If they detect an error, the system attempts to sound five beeps and to display one of the following error messages.

System ROM Error
The sumcheck of the processor board ROM BIOS is not correct.

DMA Page Register Error
DMA Page register verification failed.

Timer One Error
Counters 0 or 2 of the first 8254 failed.

8042 Controller Error
The 8742 self-check failed.

Timer Two Error
Counters 0 and 1 of second 8254 failed.

Speed Switching Error
Counter 2 of second 8254, keyboard controller, failed.

RAM Error in Segment F000
There is an error in RAM segment F000

Descriptor Table Register Error
Global and interrupt descriptor table registers can't latch.

ROM BIOS Copy Failure
RAM BIOS does not match ROM BIOS

System Port Error
The I/O Port at address 61H was read and verified as defective.

Refresh Error
The refresh logic did not provide refresh pulses.

0-64KB Ram Error
An error was detected in the first 64-KB of RAM.

Bus 8-16 Error
The 8 bit to 16 bit bus converting logic failed.

Interrupt Controller Error
The interrupt mask registers do not verify.

CMOS RAM Error
The Real Time Clock Controller failed.

Protected Mode Error (System Halt)
System could not successfully enter the protected mode and return to the real mode.

Primary CRT Error
The video display indicated by the MPB switch block SW1 is not correctly set.

The primary CRT error display does not halt the system. The system halts after five beeps or after any other of the above messages or errors.

When the initial level 0 diagnostic tests have run successfully, the following status message is displayed and additional processor board tests are then run to verify and initialize the installed system hardware.

LEVEL 0 DIAGNOSTICS
MAIN BOARD DIAGNOSTICS COMPLETE,
TEST AND INITIALIZE.

System Test and Initialize

After the initial phase, the Level 0 diagnostic routines determine what system hardware is installed and test and initialize that hardware. They display test messages throughout this phase to show progress. Test names, preceded by an underscore (_), are displayed at the beginning of the tests. When a test fails, the system stops and/or attempts to sound five beeps and to display an error message.

_Interrupt Controllers
Both interrupt controllers are tested and initialized.

_DMA Controllers
Both DMA controllers are tested and initialized.

_Timer One
Timer one is tested.

_Timer Two
Timer Two is tested.

_Memory
The routine conducts the memory test in 64KB increments. In normal operation, the upper boundry of the bank of memory tested is displayed as shown in the following.

BASE MEMORY TEST
xxxx KB

EXPANSION MEMORY TEST
Memory Error
Bit
Address
Parity

TOTAL MEMORY XXXX KB
The routines test the entire memory. Base memory is normally memory below 640KB; expansion memory is the memory area above 1MB.The memory from 640 KB to 1 MB (for example, CRT RAM and add-on ROM) is tested during other tests. The amount of good memory is shown by xxxx KB, in steps of 64KB. Total memory is the sum of base memory and expansion memory.

The following representations are used in the memory error display examples.

- xxxxxx= Address of observed memory error
- eeee= Expected data
- oooo= Observed data

xxxxxx Memory Error Bit eeee oooo
One or more bits of a memory cell are faulty.

xxxxxx Memory Error Address eeee oooo
An error has been detected in the address test.

xx0000 Memory Error Parity
A parity error has been detected in a 64KB memory bank.

Memory Address Error (System Halt)
An address error for address lines A16 to A23 has been detected. This is an unrecoverable error, and the system stops processing.

Memory Error in Segment E000:0000
A check of RAM area for system ROM fails.

_FLEX DISK
The flex disk controller and drives are tested and initialized. The heads of drives are moved; however, bit read or write cycles are not performed. If an error is detected, the routine displays one of the following messages.

Flex Controller Error
Error on flexible disk drive controller.

Disk A Error
Access to disk drive A failed (controller or drive error).

Disk B Error
Access to disk drive B failed (controller or drive error).

_FIXED DISK
The fixed disk controller is tested and initialized. If an error is detected, the routine displays one of the following error messages.

Disk 0 Failure
Disk drive 0 configured, but not present.

Disk 1 Failure
Disk drive 1 configured, but not present.

Disk 0 Error
Disk not formatted, or controller error.

Disk 1 Error
Disk not formatted, or controller error.

_EXTERNAL ROMS
xxxx ROM Error
The external ROM checksum is not correct: xxxx is the code segment address of the ROM.

_KEYBOARD
The keyboard interface is tested to verify that a compatible keyboard is attached. Also, the keyboard performs a self-check-test and initialization. When an error is detected, the system displays one of the following error messages.

Keyboard Clock Line Error
Keyboard clocking is not functional.

xx Key Code Received
The system received an unexpected scan code from the keyboard: xx is the received scan code.

Keyboard Controller 8042 Error
The keyboard controller does not accept keyboard commands.

Keyboard Interface Error
The keyboard controller can not control the keyboard interface lines.

Keyboard Error
The keyboard failed the self-check test.

System Keylock is Locked
The Keyboard Lock is in the locked position.

NO COPROCESSOR INSTALLED
Coprocessor is not installed.

_80287 COPROCESSOR INSTALLED
An 80287 coprocessor is installed.

_80387 COPROCESSOR INSTALLED
An 80387 coprocessor is installed.

_SPEED SET FOR AUTO MODE
Speed is set to power-up in 8/16 MHz speed.

_SPEED SET FOR FIXED MODE
Speed is set for one of 16,8,6,or 4.77 MHz speed.

_SPEED SET FOR HIGH MODE
Speed is set for 16 MHz speed.

System Configuration Verification

After the diagnostic routines initialize the system, the routines compare actual hardware found with the definition of expected hardware contained in battery-protected CMOS memory. If they are

the same, Level 0 Diagnostics are complete. If they are different, the system displays one of the following messages for each error and then displays the SETUP message.

**** Battery Power Lost (Run SETUP)**
Battery power has been lost. Reconfigure the system with the Setup Utility.

**** Configuration not set (Run SETUP)**
The configuration of the system is not set correctly.

**** Time and Date not set (Run SETUP)**
The Real-Time-Clock does not run.

**** Memory Size Error (Run SETUP)**
Detected and configured memory sizes do not agree. Check the memory configuration in the CMOS RAM.

**** Disk Configuration not Correct**
Disk configuration in CMOS and detected disk configuration on Level 0 do not agree.

**** Unlock System Keylock**
The system is locked, unlock and restart with keyboard available.

**** Check Keyboard (System Halt)**
The keyboard does not function properly.

** Press <F1> if hardware SETUP is desired.
** Press <F1> for SETUP or <ENTER> to continue.
Press <ENTER> to continue.

SETTING THE SYSTEM CONFIGURATION

The system has a battery that maintains a part of ROM memory and the time-of-day clock. This memory provides time, date, memory and attached device information to the system.

SETUP is the name of a resident utility that initializes configuration data in this memory. This memory is initialized during assembly so that the system can be used for the first time.

During system startup, at the completion of Level 0 Diagnostics, the contents of the ROM memory are checked for changes. If a change is detected, the system asks if reinitializing is desired. Pressing <F1> automatically executes the SETUP utility. Once the data is initialized, it is battery maintained even while the computer system is turned off.

When the battery must be replaced or a change is made in the configuration it is nescessary to run SETUP again. Press <F1> to execute the SETUP utility and reinitialize data to the current values.

The SETUP utility is made up of a series of easy to understand displays which:

- set the date and time
- define the flexible disk drive configuration
- define the fixed disk drive configuration,
- define the base and extension memory sizes,
- define the primary video display adapter
- define the screen width

NOTE: The table of possible fixed disk drive configurations is at the end of this chapter for reference.

The upper portion of the SETUP screen, [1] as shown in figure 4-1, contains three sections. Each device that can be connected to the system is shown on the left-hand third of the screen. The center third of the screen defines the current settings for each of these devices. The right-hand third of the screen contains the "New settings" for each change.

The middle portion of the SETUP screen, [2] shows the prompts for the selected line of the upper portion of the screen. The right-hand window contains the format of data, or data choices to describe each device. After inputting descriptive data and pressing <ENTER>, the new data shows under "New settings" in the upper right-hand third of the screen.

As shown in the lower portion of the screen, [3], the up and down arrow keys move the indicator at the left of the device names.

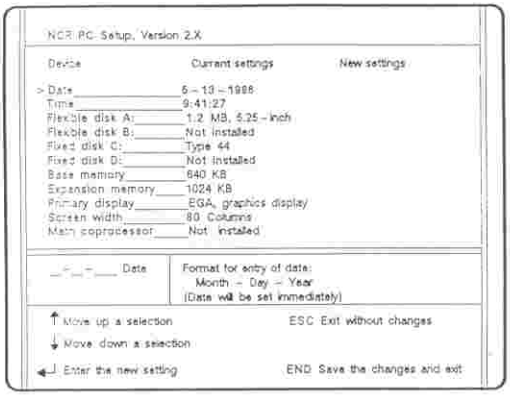


Figure 4-1 SETUP menu

For example, Figure 4-1 shows the Date selected. The center section shows the date format to be Month - Day - Year.

TESTPOINTS

At the start of each test, the level 0 diagnostic routines load a testpoint number into the system. This number remains in the system until the diagnostic routines successfully complete the related tests. The following section describes how to read test points for troubleshooting.

Reading Testpoints

If the system fails to load operating system software and does not display a message, Level 0 Diagnostics outputs an error code. The code (testpoint number) is addressed to location 80H. These codes can be monitored with a diagnostic test LED board. The test board has 8 LEDs to indicate the code in binary form (ON = 1) and three LEDs for voltage condition. Test board circuitry reads and latches the data so that it is visible during tests. Figure 4-2 shows the board and arrangement of the LEDs.

The signals are from ground to data bus lines SD-0 through SD-7. They are on Pins A2 through A9 (ON=high) of the 62 pin edge connector (P1) on the processor board. Pin 2 is the least significant digit (corresponding to LED 0) and Pin 9 is the most significant digit (corresponding to LED 7).

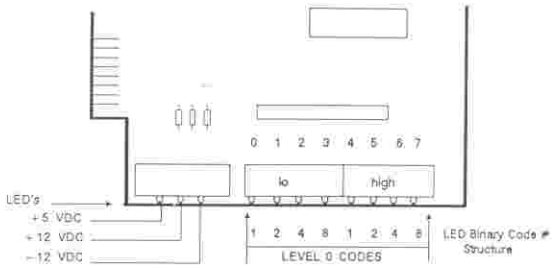


Figure 4-2 Diagnostic LED test board (component side up)

Testpoint Code Numbers

The following list shows all testpoint code numbers. The codes are in numeric order for convenience in locating them. The processor generates them in an order different from numeric.

Test Code	Halt on Error	Test
01	Y	CPU Register Test, Reset Video Cards, Display Diagnostics Message
02	Y	Verify Port 61H, Disable NMI, Start Speaker Timer
03	Y	ROM BIOS Checksum Test
04	Y	DMA Page Register Test
05	Y	Test Refresh Counter
06	Y	Test Speaker Counter
07	Y	Test Refresh
08	Y	Test Base 64K RAM
09	Y	Test Bus Converting Logic, Initialize Interrupt Controllers
0A	Y	Test Interrupt Mask Register A
0B	Y	Test Interrupt Mask Register B, Write Temporary IVT
0C	Y	8742 Self Test
0D	Y	Verify CMOS Shutdown Byte
0E	N*	Test CMOS Battery
0F	N*	Verify CMOS Checksum and Initialize Periodic Rate
10	N	Protected Mode Test
11	Y	Test CRT Configuration, Look for Advanced Video Card, Initialize S/W Interrupt Vectors
12	N	Initialize and Test CRT Controller
13	N	CRT Controller Error, Try another Video Card
14	Y	Test Turning Speed Switch Off
15	Y	Test Timer 2 - Counter 2, Start Refresh Timer, Disable Speed Switch Counter
16	Y	Test Enabling Speed Switch
17	Y	Clear Write Protect Bit
18	Y	Write/Verify GDTR and IDTR, Copy ROM BIOS to RAM

Test Code	Halt on Error	Test
19	Y	Verify RAM Compares to ROM BIOS After Copy, Reinitialize Restart Vector, Check for Burn-In ROM, Disable RTC, Reset Video
1A	Y	Self-Test 8042
1B	Y	Verify RAM in Segment F000
1C-1F		Reserved
20	N	Display Tested Parts
21	Y	Test DMA Controller a
22	Y	Test DMA Controller b; Initialize All Channels
23	Y	Test Timer 1 - Counter 0
24	N	Initialize Interrupt Controller
25	N	Check for Unexpected Interrupts
26	N	Wait for Interrupt
27	N*	Test Timer 2 - Counter 0
28	N*	Test Timer 2 - Counter 1
29-2F		Reserved
30	N	Configure Memory 0-640K
31	N	Configure Memory 1M-16M
32	N	Test for Mirror Addresses
33	N*	Test 64K 640K RAM
34	N*	Test 1M-16M RAM
35	N*	Test RAM at E0000
36-3F		Reserved
40	N	Keyboard Test - Enable/Disable Keyboard
41	Y****	Keyboard Test - Reset Keyboard
42	Y****	Keyboard Test - Check Keyboard Clock Low
43	Y****	Keyboard Test - Check for Keyboard Interrupt, Enable Keyboard, Initialize Pointers, Write out Subcommand
44	N	Set A20 to 0
45-4F		Reserved
50	N	Initialize Hardware Interrupt Vectors

Test Code	Halt on Error	Test
51	N	Enable Interval Timer Interrupt
52		(See note at end of table)
53-5F		Reserved
60	N	Configure Flexible Disk, Check for Fixed/Flex Adapter Card
61	N	Check Cylinder Register for Fixed/Flex Adapter Card
62	N	Initialize Flex Drives
63	N	Initialize Fixed Drive
64-6F		Reserved
70	N*	Test Real-Time-Clock
71	N	Set Interval Timer RAM Counts
72	N	Test and Configure Parallel Ports
73	N	Test and Configure Serial Ports
74	N	Check for Expansion ROMS
75	N*	Coprocessor Test
76	N	Enable RTC Interrupt and Keyboard Interrupt
77-7F		Reserved
F0	N**	Display Logged Errors
F1	N	Test System Code at E0000H
F2	N	Boot the System
F3	N***	Go to SETUP
F4	N	Display Speed Setting
F5	N	Initialize Counter 2 for Speed Requested
Not Included		
52		CA ROM Installed Test

* Halt on Error with Keyboard Turnaround Connector in Place

** Halt if Locked, Loop if Keyboard Turnaround Connector is Present

*** Go to SETUP, If <F1> was Pressed

**** Halt on Error, If No Keyboard Turnaround Connector is Present

Address A20 Override Enable

Address line A20 allows use of memory above 1MB. When enabled, memory above 1MB can be used; when not enabled, memory above 1MB cannot be used. Enabling is normally through the keyboard controller which requires approximately 100 microseconds. The 386 card design allows an override in port 68H to also enable the higher memory. That is, the keyboard controller and the A20 Override are "or-ed" together into A20. Port 68H bypasses the keyboard controller and performs the enable in a few microseconds. The difference is very useful in moving back and forth between memories under and over 1MB in a DOS environment.

The override for A20 can be tested by writing a test byte to an address above 1MB. If the override is operating, the address will stay as written. If not operating correctly, the address will wrap, and as a result, will change.

The major error code is 12. The detail codes are as follows:

10 KBD A20 on, override off
20 KBD A20 on, override on
30 KBD A20 off, override off
40 KBD A20 off, override on

FIXED DISK DRIVE TYPES

The table that follows identifies the types of fixed disk drives that are available.

DRIVE TYPE	NUMBER OF CYL.	NUMBER OF HEADS	CONTROL BYTE	PRE-COMP	LAND. CYL.	SECTORS/ TRACK
1	306	4	0	128	305	17
2	615	4	0	300	615	17
3	615	6	0	300	615	17
4	940	8	0	512	940	17
5	940	6	0	512	940	17
6	615	4	0	-1	615	17
7	462	8	0	256	511	17
8	733	5	0	-1	733	17
9	900	15	8	-1	901	17
10	820	3	0	-1	820	17
11	855	5	0	-1	855	17
12	855	7	0	-1	855	17
13	306	8	0	128	319	17
14	733	7	0	-1	733	17
15	0	0	0	0	0	0
16	612	4	0	0	663	17
17	977	5	0	300	977	17
18	977	7	0	-1	977	17
19	1024	7	0	512	1023	17
20	733	5	0	300	732	17
21	733	7	0	300	732	17
22	733	5	0	300	733	17
23	306	4	0	0	336	17
24	612	4	0	305	663	17
25	306	4	0	-1	340	17
26	612	4	0	-1	670	17
27	698	7	32	300	732	17
28	976	5	32	488	977	17
29	306	4	0	0	340	17
30	611	4	32	306	663	17
31	732	7	32	300	732	17
32	1023	5	32	-1	1023	17
44	1024	8	0	512	1023	17
45	615	8	0	128	664	17
46	754	11	8	0	754	17
47	699	7	0	256	700	17

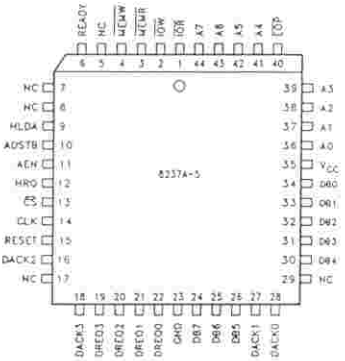
Note: Entries 33 through 43 are all zeros.

Figure 4-3. Fixed Disk Drive Types

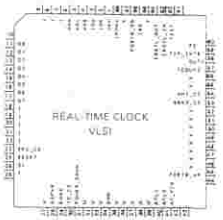
Chapter 5

Integrated Circuit Component Pin-Out Configurations

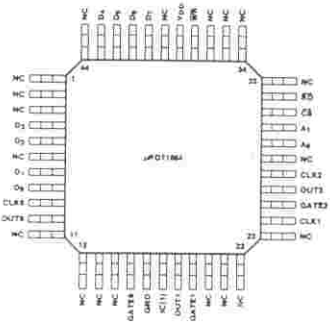
The diagrams on the following pages represent the pin-out configurations of selected integrated circuit components that are used on the MPB and the Memory cards.



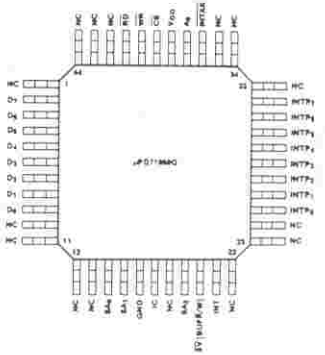
8237-A
44-Lead PLCC Pin Configuration



Real-Time Clock VLSI
68-Lead PLCC Pin Configuration



d71054 (I8254)
28-Lead PLCC Configuration



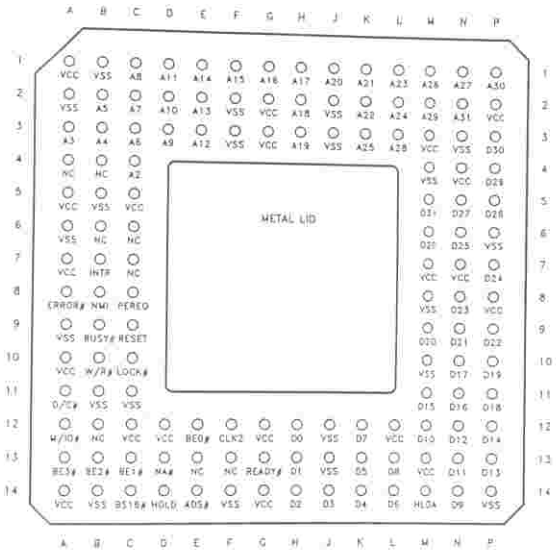
d71059G (82C59A-2)
28-Lead PLCC Configuration

8742

IMS 2801-70

27256

27512



80386
PIN VIEW (Enlarged view)

Specifications

SPECIFICATIONS

This section presents brief descriptive specifications for selected integrated circuit components used on the boards. The descriptions are qualitative to give an overall understanding of the functions of the chips without great detail. The selected circuits include the most significant ones that are referenced in the functional descriptions of the boards. The specifications also serves as an easy reference aid for use with the logic diagrams. The diagrams have chip identification without any of the functional information. Manufacturers data sheets on the chips give the complete specifications when they are needed.

MAIN PROCESSOR BOARD

80386-16 MICROPROCESSOR

- State-of-the-art technology
- Increased performance
  - 16-Megahertz clock speed
  - reduced speeds can be programmed

- 32-bit processor
- 32-bit registers, instructions, busses
- compatibility with earlier '86 microprocessors
  - Object code compatible with 8088 and 80286

- Large address space
  - Physical address space 4 X 2^{32} bytes
  - Logical address space 64 X 2^{46} bytes

- On-chip memory management unit
- Pipelining for simultaneous multiple instructions
- Four levels of protection
- Four operating modes

NUMERIC COPROCESSOR

- Coprocessor is an option
  - 80387 plugs in directly
  - 80287 mounted on small plug-in adapter

- Faster numeric processing
- Invisible to application programs
- Eight 80-bit registers in floating point stack

8237 PROGRAMMABLE DMA CONTROLLER

- Four independent channels in each controller
- Controller 2 cascaded into a controller 1 channel
- Four- or eight-megahertz optional types
- Memory-to-memory transfer
- System memory to external device transfer
- Designed for use with an external 8-bit address register
- each channel 64K address and word count
- Surface mount technology (PLCC)

SN74LS612 PAGE REGISTER CONTROLLER

- Paged Memory Mapper
- 3-State output
- Open collector
- Expands four address lines to 12 address lines

8259A-2 PROGRAMMABLE INTERRUPT CONTROLLER

- Eight Interrupts each controller
- Two controllers cascaded for 16 interrupts
- Programmable interrupt modes
- Static circuitry – no clock input required
- Single 5 volt supply
- NMOS construction
- Surface Mount technology (PLCC)

RTC VLSI

- Includes both Time-of-Day and Timer functions
  - Equivalent of Time-of-Day chip Motorola MC146818
  - Equivalent of Timer 8254
- Battery backup for time and date
- Programmable operation
- Internal time base oscillator
- 12 or 24 hour clock
- Three time-related interrupts
- Surface Mount technology (68-pin PLCC)
- Glue logic

8254-2 PROGRAMMABLE INTERVAL TIMER

- Three independent 16-bit counters
- HMOS technology
- Inputs up to 10 megahertz
- Six programmable counter modes
- All modes are software programmable
- Surface mount technology (PLCC)

8742 UNIVERSAL PERIPHERAL INTERFACE MICROCONTROLLER

- 8-bit CPU with ROM, RAM, I/O, timer/counter, and clock
- 2048 X 8 ROM/EPROM, 128 X 8 RAM, 8-bit time/controller, 18 programmable I/O pins
- One 8-bit status and two data registers for asynchronous slave-to-master interface

27256 ERASABLE/PROGRAMMABLE READ ONLY MEMORY (EPROM) OPTION

- 32K bytes of storage capacity
- Two-line control
- HMOS II-E construction
- Moisture resistant

27512 ERASABLE/PROGRAMMABLE READ ONLY MEMORY (EPROM)

- 64K bytes of storage capacity
- 200 nanosecond access time
- Two-line control
- HMOS II-E construction

MEMORY BOARD

IMS AAA 2801 DYNAMIC RAM

- 256K x 1 bits
- 70 or 120 nanosecond RAS
- CMOS construction
- Single 5 volt supply