MS-7012 uATX

***INTEL mPGA 478B Processor**

***INTEL Springdale GMCH / ICH5 Chipset**
(DDR 333 / AGP 8X) / (integrated serial ATA)

***VIA/6105L**

***VIA/6306,IEEE1394 3port**

***Winbond 83627HF LPC I/O**

***Audio codec 6 channel support**

***USB 2.0 support x6 (integrated into ICH5)**

Micro Star Restricted Secret

Title: Cover Sheet | Rev: 1.0A

Document Number: MS-7012

MICRO-STAR INT'L
No. 69, Li-De St, Jung-He City,
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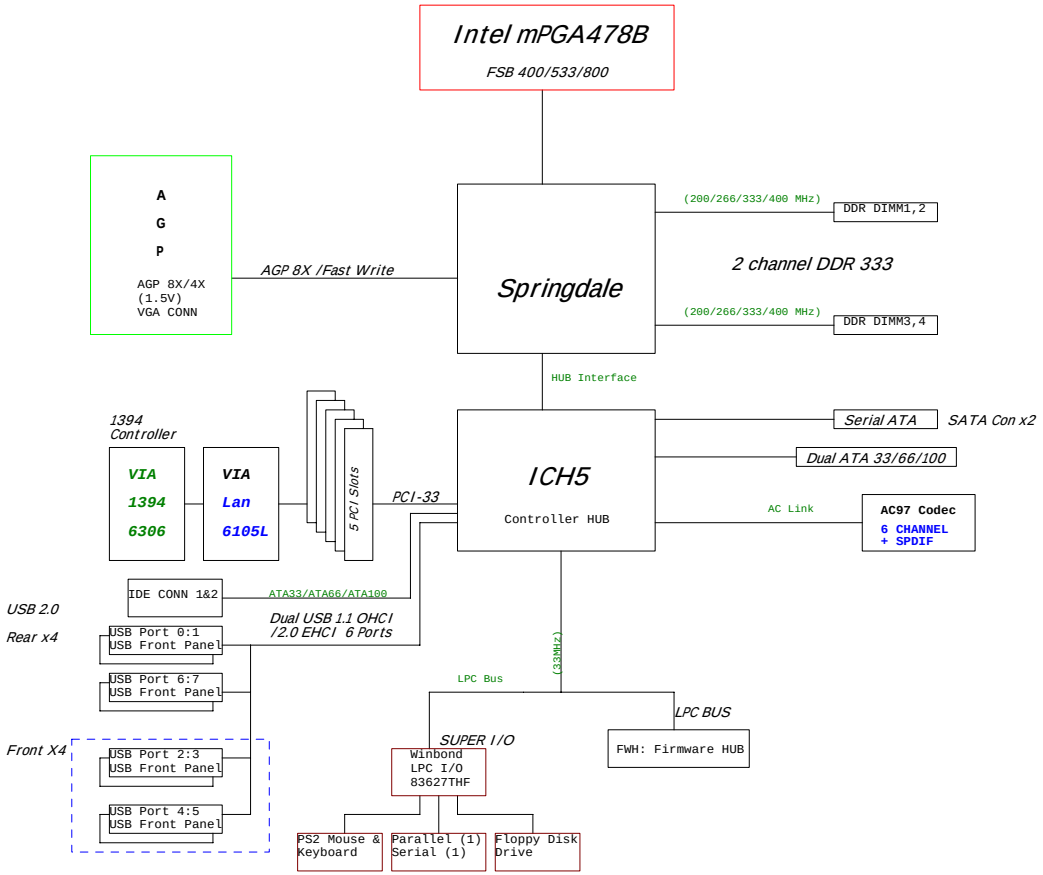
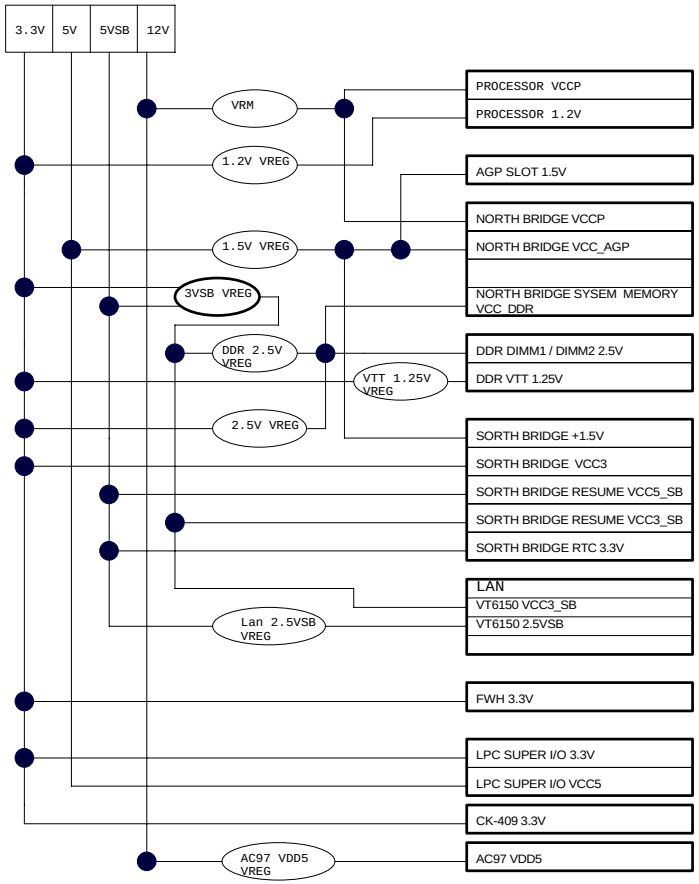
Block Diagram

+5V : VCC5
+3.3V : VCC3
+12V : +12V
5VSB : VCC5_SB
-12V : -12V
+2.55V for DDR : VCC_DDR
1.275V for DDR VTT : VTT_DDR
Dual 3.3V : 3VDUAL
1.2V for CPU VID : VCC_VID
1.5V for AGP VI/O : VCC_AGP
Dual 5V : 5VDUAL
CPU Vcore : VCCP
+5V for analog CODEC : AVDD5
2.5V for LAN : 2_5VSB
+12V for 1394 bus power : CPWR



POWER DELIVERY MAP



Micro Star Restricted Secret		
Title: Block Diagram		Rev: 1.0A
Document Number: MS-7012		
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GPIO FUNCTION

ICH5

GPIO Pin	Type	Function	Power well	
GPIO 0	I	PREQ#B	MAIN	
GPIO 1	I	PREQ#B	MAIN	
GPIO 2	I	PIRQ#E	MAIN	
GPIO 3	I	PIRQ#F	MAIN	
GPIO 4	I	PIRQ#G	MAIN	
GPIO 5	I	PIRQ#H	MAIN	
GPIO 6	I	GPI6	MAIN	
GPIO 7	I	GPI7	MAIN	
GPIO 8	I	GPI8	RESUME	
GPIO 9	I	OC4#	RESUME	
GPIO 10	I	OC5#	RESUME	
GPIO 11	I	**SIO_SMI#**	RESUME	
GPIO 12	I	**EXTSMI#**	RESUME	
GPIO 13	I	**SIO_PME#**	RESUME	
GPIO 14	I	OC#6	RESUME	
GPIO 15	I	OC#7	RESUME	
GPIO 16	O	PGNT#A	MAIN	
GPIO 17	O	PGNT#B	MAIN	
GPIO 18	O	GPO18	MAIN	
GPIO 19	O	**BIOS_WP#**	MAIN	
GPIO 20	O	GPO20	MAIN	
GPIO 21	O	GPO21	MAIN	
GPIO 22	OD	GPO22	MAIN	
GPIO 23	O	GPO23	MAIN	
GPIO 24	I/O	GPIO24	RESUME	default output
GPIO 25	I/O	GPIO25	RESUME	default output
GPIO 27	I/O	GPIO27	RESUME	default output
* GPIO 28	I/O	GPIO28	RESUME	default output
GPIO 32	I/O	GPIO32	MAIN	default output
GPIO 33	I/O	GPIO33	MAIN	default output
GPIO 34	I/O	GPIO34	MAIN	default output
GPIO 40	I	PREQ#4	MAIN	
GPIO 41	I	GPI41	MAIN	
GPIO 48	O	PGNT#4	MAIN	
GPIO 49	OD	CPUPWRGD	MAIN	

FWH

GPIO Pin	Type	Function
GPI 0	I	PD_DET
GPI 1	I	SD_DET
* GPI 2	I	BOM strapping for Bit 0
GPI 3	I	Pull down through 1K ohms (unused)
* GPI 4	I	BOM strapping for Bit 1

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	MCLK_A0/MCLK_A0# MCLK_A1/MCLK_A1# MCLK_A2/MCLK_A2#
DIMM 2	1010001B	MCLK_A3/MCLK_A3# MCLK_A4/MCLK_A4# MCLK_A5/MCLK_A5#

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 3	1010010B	MCLK_B0/MCLK_B0# MCLK_B1/MCLK_B1# MCLK_B2/MCLK_B2#
DIMM 4	1010011B	MCLK_B3/MCLK_B3# MCLK_B4/MCLK_B4# MCLK_B5/MCLK_B5#

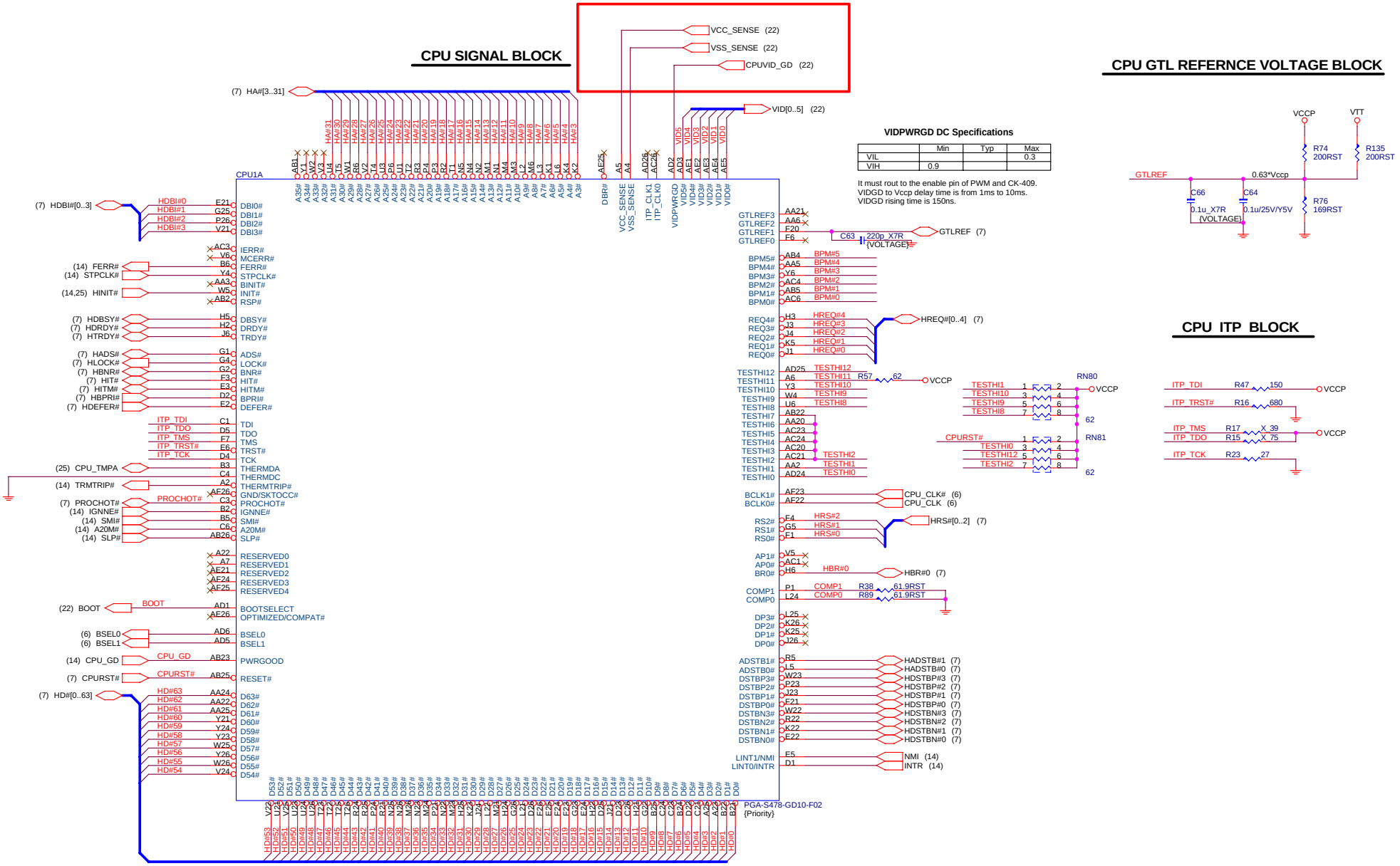
PCI RESET DEVICE

Signals	Target
PCIRST#_ICH5	AGP,FWH,MS-5
PCIRST#1	Springdale,LAN, Super I/O,1394,MS-1
PCIRST#2	PCI slot 1-3 & Mini PCI
HD_RST#	Primary, Scondary IDE

PCI *Clock NC pin : PCI 33MHz(Pin 19 ,20) , 66MHz(Pin 27)*

DEVICES	INT#	IDSEL	REQ#/GNT#	CLOCK
Mini PCI 1	INT#A INT#B	AD16	PREQ#1 PGNT#1	PCICLK1-Pin-14
PCI SLOT 1	INT#B INT#C INT#D INT#A	AD17	PCI1PREQ#1 PCI1PGNT#1	PCICLK2-Pin-15
PCI SLOT 2	INT#C INT#D INT#A INT#B	AD18	PREQ#3 PGNT#3	PCICLK3-Pin-20
PCI SLOT 3	INT#D INT#A INT#B INT#C	AD19	PCI3PREQ#3 PCI3PGNT#3	MS1 (MS1PCLK-Pin-8)
PCI SLOT 4	INT#G	AD20	PREQ#5 PGNT#5	PCICLK5-Pin-21
Lan 6105L	INT#E	AD25	PREQ#4 PGNT#4	Lan_PCLK-Pin-16
1394	INT#F	AD26	PREQ#2 PGNT#2	1394_PCLK-Pin-12
MS-1			PREQ#0 PGNT#0	MS1PCLK-Pin-8

CPU SIGNAL BLOCK



VIDPWRGD DC Specifications

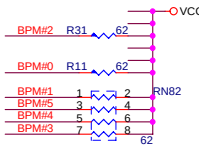
	Min	Typ	Max
VIL			0.3
VIH	0.9		

It must rout to the enable pin of PWM and CK-409.
VIDGD to Vccp delay time is from 1ms to 10ms.
VIDGD rising time is 150ns.

CPU GTL REFERNCE VOLTAGE BLOCK

CPU ITP BLOCK

CPU STRAPPING RESISTORS



ALL COMPONENTS CLOSE TO CPU

Micro Star Restricted Secret		
Title	*Intel mPGA478B - Signals*	Rev 1.0
Document Number	*MS-7012*	
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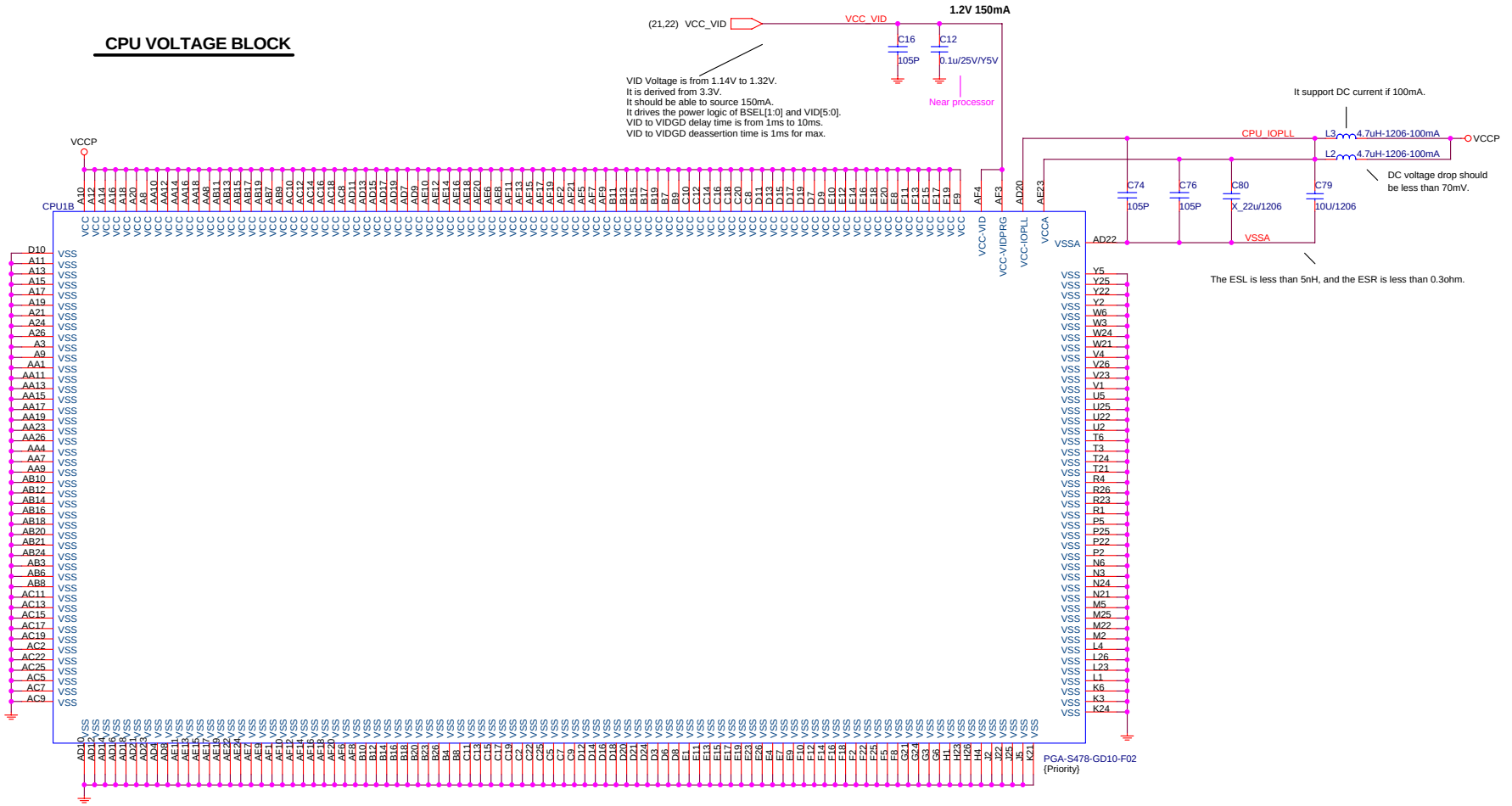
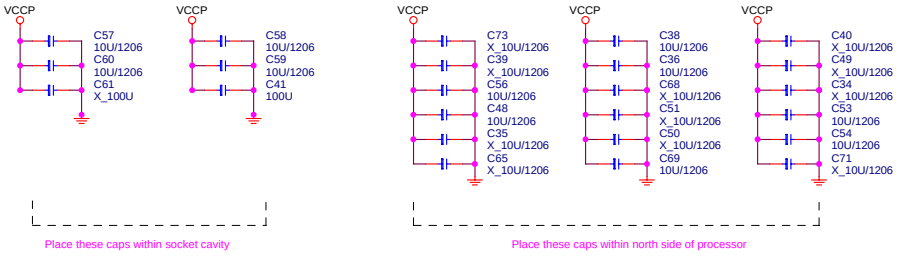
CPU VOLTAGE BLOCK



CPU DECOUPLING CAPACITORS



Micro Star Restricted Secret		
Title	***Intel mPGA478B - Power***	Rev 1.0A
Document Number	*MS-7012*	
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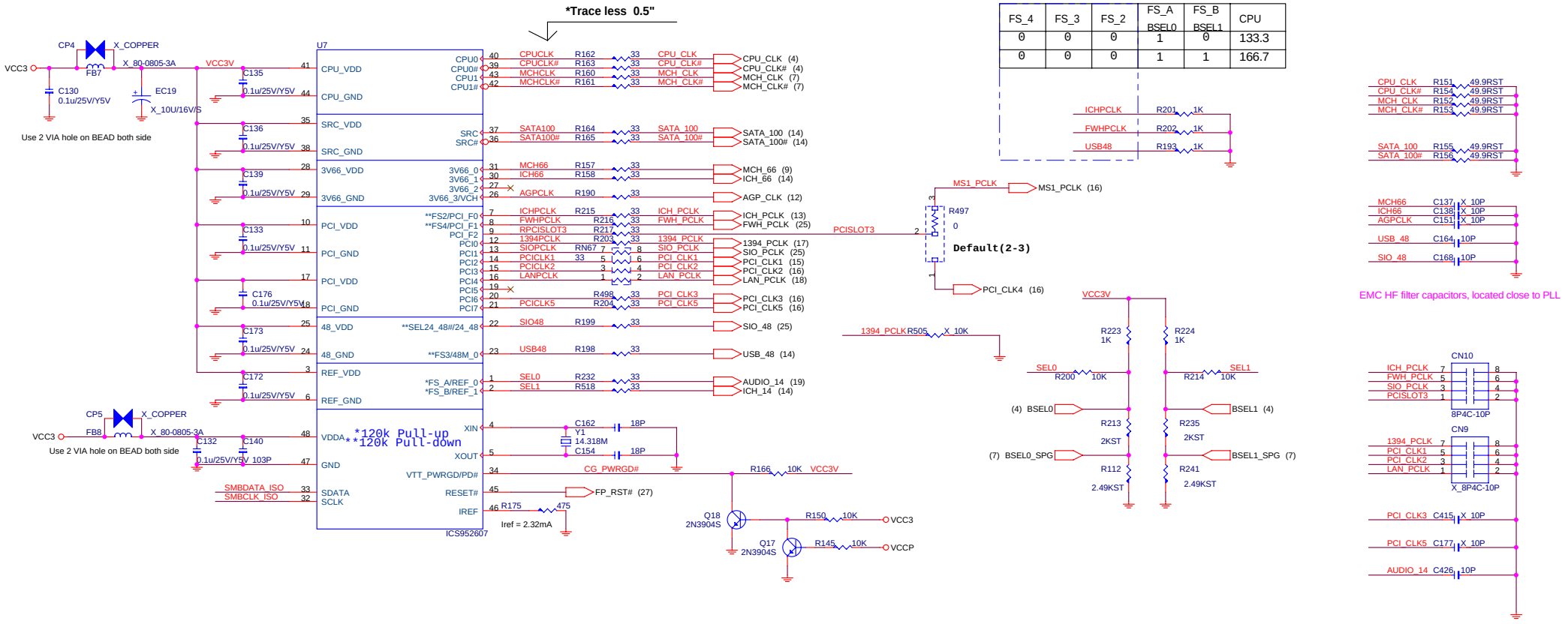
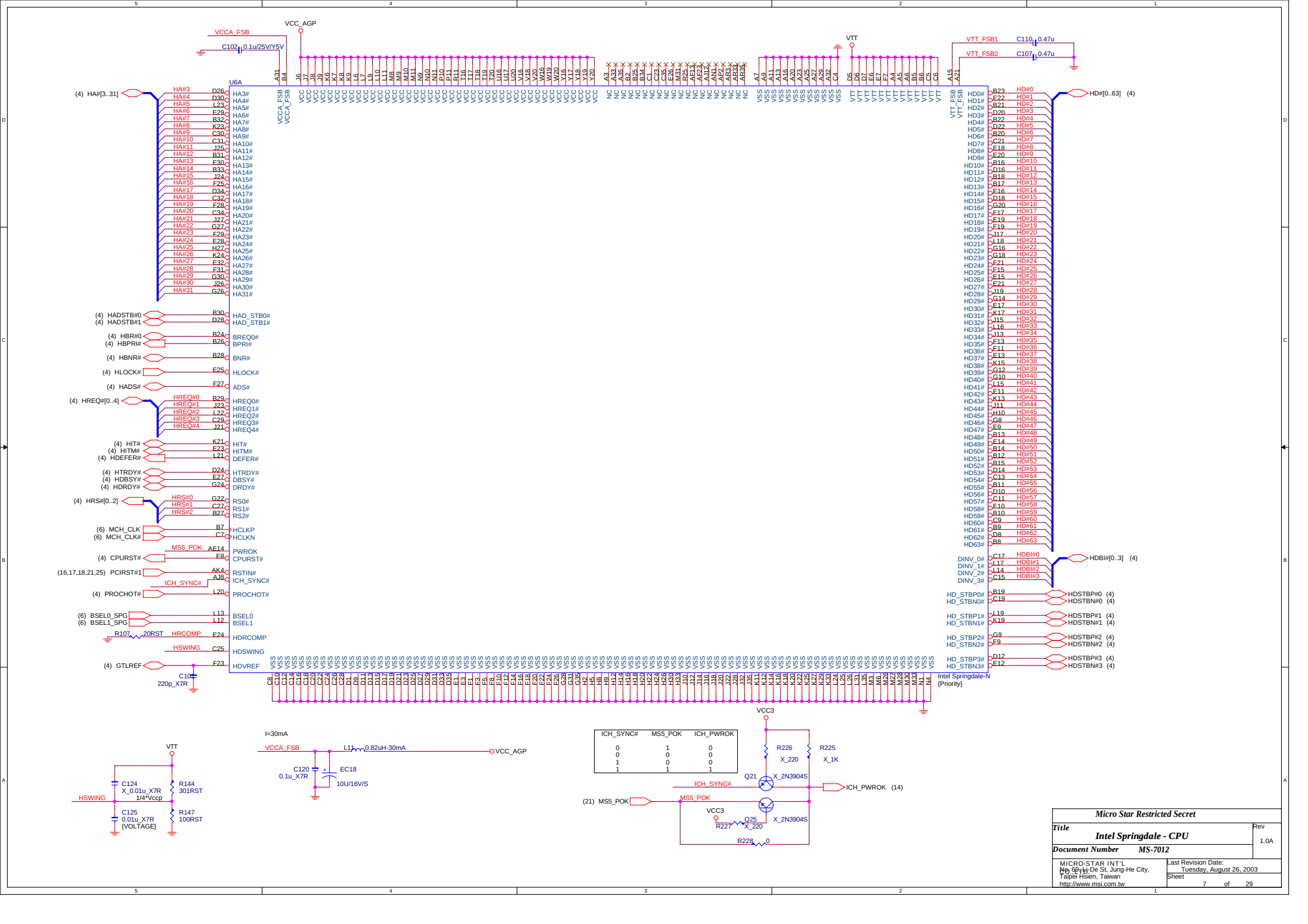
Clock Synthesizer



Micro Star Restricted Secret	
Title: Clock Synthesizer	Rev: 1.0A
Document Number: MS-7012	
MICRO-STAR INT'L No 69-1 Li De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, August 26, 2003 Sheet 6 of 29


VCCA_FSB
C102 0.1u/25V/Y5V
VCC_AGP
VTT
VTT_FSB1
C110 0.47u
VTT_FSB2
C107 0.47u
U6A
(4) HA#[3..31]
HA#3 HA#4 HA#5 HA#6 HA#7 HA#8 HA#9 HA#10 HA#11 HA#12 HA#13 HA#14 HA#15 HA#16 HA#17 HA#18 HA#19 HA#20 HA#21 HA#22 HA#23 HA#24 HA#25 HA#26 HA#27 HA#28 HA#29 HA#30 HA#31
(4) HADSTB#0
(4) HADSTB#1
HAD_STB0#
HAD_STB1#
(4) HBR#0
(4) HBPRI#
BREQ0#
BPRI#
(4) HBNR#
BNR#
(4) HLOCK#
HLOCK#
(4) HADS#
ADS#
(4) HREQ#[0..4]
HREQ#0 HREQ#1 HREQ#2 HREQ#3 HREQ#4
HREQ0# HREQ1# HREQ2# HREQ3# HREQ4#
(4) HIT#
(4) HITM#
(4) HDEFER#
HIT#
HITM#
DEFER#
(4) HTRDY#
(4) HDBSY#
(4) HDRDY#
HTRDY#
DBSY#
DRDY#
(4) HRS#[0..2]
HRS#0 HRS#1 HRS#2
RS0# RS1# RS2#
(6) MCH_CLK
(6) MCH_CLK#
HCLKP
HCLKN
MS5_POK
(4) CPURST#
PWROK
CPURST#
(16,17,18,21,25) PCIRST#1
RSTIN#
ICH_SYNC#
(4) PROCHOT#
PROCHOT#
(6) BSEL0_SPG
(6) BSEL1_SPG
BSEL0
BSEL1
R107 20RST
HRCOMP
HDRCOMP
HSWING
HDSWING
(4) GTLREF
HDVREF
C101 220p_X7R
HD#[0..63] (4)
HDBI#[0..3] (4)
HDSTBP#0 (4)
HDSTBN#0 (4)
HDSTBP#1 (4)
HDSTBN#1 (4)
HDSTBP#2 (4)
HDSTBN#2 (4)
HDSTBP#3 (4)
HDSTBN#3 (4)
Intel Springdale-N
{Priority}
VCC3
VTT
C124 X_0.01u_X7R
1/4*Vccp
R144 301RST
HSWING
C125 0.01u_X7R
{VOLTAGE}
R147 100RST
I<30mA
VCCA_FSB
L11 0.82uH-30mA
VCC_AGP
C120 0.1u_X7R
EC18 10U/16V/S
ICH_SYNC# MS5_POK ICH_PWROK
0 1 0
0 0 0
1 0 0
1 1 1
R226 X_220
R225 X_1K
Q21 X_2N3904S
ICH_SYNC#
ICH_PWROK (14)
(21) MS5_POK
MS5_POK
VCC3
R227 X_220
Q25 X_2N3904S
R228 0
Micro Star Restricted Secret
Title
Intel Springdale - CPU
Rev
1.0A
Document Number MS-7012
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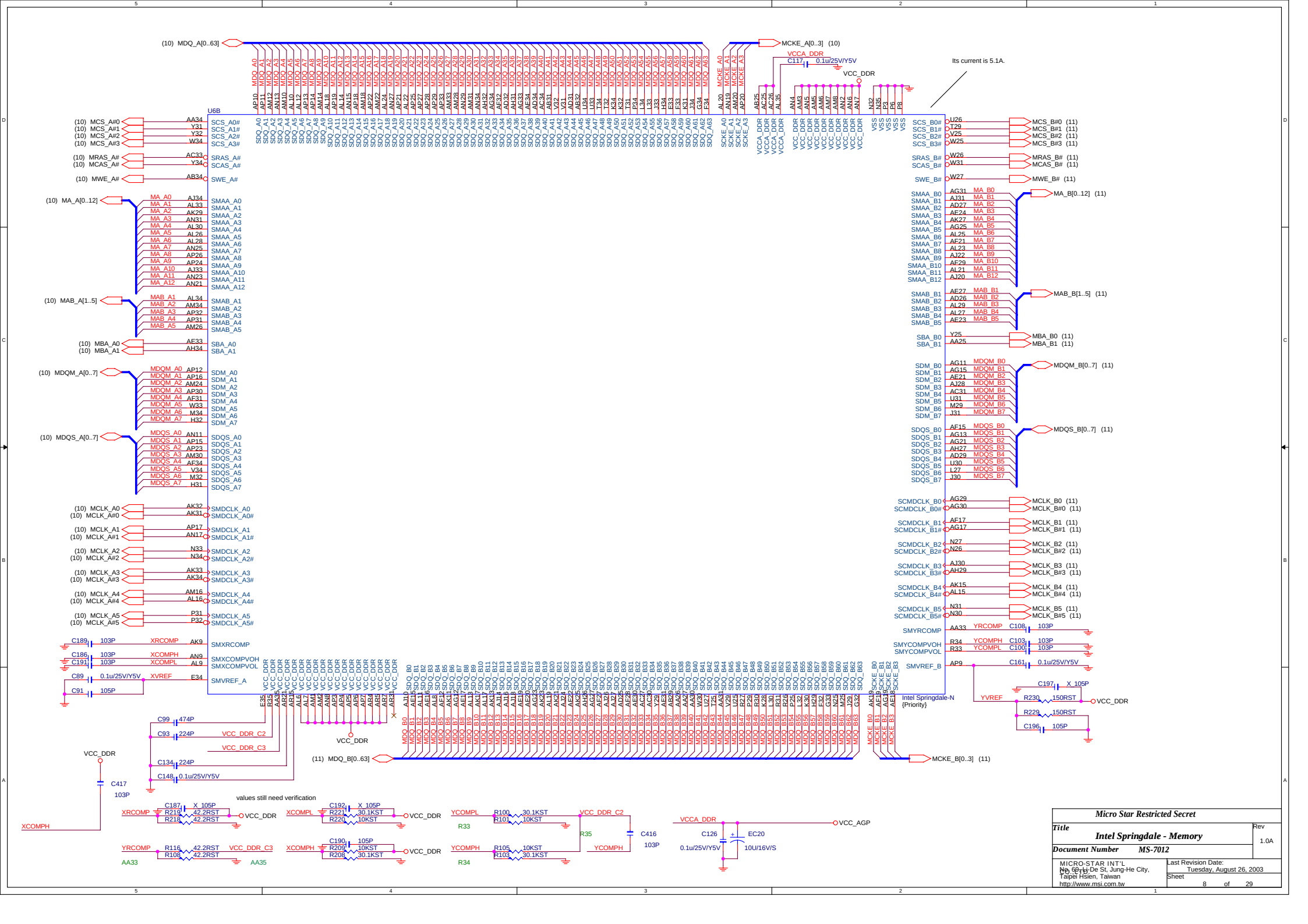
(10) MDQ_A[0..63]
MCKE_A[0..3] (10)
VCCA_DDR
C117 0.1u/25V/Y5V
VCC_DDR
Its current is 5.1A.
U6B
(10) MCS_A#0
(10) MCS_A#1
(10) MCS_A#2
(10) MCS_A#3
(10) MRAS_A#
(10) MCAS_A#
(10) MWE_A#
(10) MA_A[0..12]
(10) MAB_A[1..5]
(10) MBA_A0
(10) MBA_A1
(10) MDQM_A[0..7]
(10) MDQS_A[0..7]
(10) MCLK_A0
(10) MCLK_A#0
(10) MCLK_A1
(10) MCLK_A#1
(10) MCLK_A2
(10) MCLK_A#2
(10) MCLK_A3
(10) MCLK_A#3
(10) MCLK_A4
(10) MCLK_A#4
(10) MCLK_A5
(10) MCLK_A#5
SMXRCOMP
SMXCOMPVOH
SMXCOMPVOL
SMVREF_A
SMYRCOMP
SMYCOMPVOH
SMYCOMPVOL
SMVREF_B
Intel Springdale-N
{Priority}
(11) MDQ_B[0..63]
MCKE_B[0..3] (11)
MCS_B#0 (11)
MCS_B#1 (11)
MCS_B#2 (11)
MCS_B#3 (11)
MRAS_B# (11)
MCAS_B# (11)
MWE_B# (11)
MA_B[0..12] (11)
MAB_B[1..5] (11)
MBA_B0 (11)
MBA_B1 (11)
MDQM_B[0..7] (11)
MDQS_B[0..7] (11)
MCLK_B0 (11)
MCLK_B#0 (11)
MCLK_B1 (11)
MCLK_B#1 (11)
MCLK_B2 (11)
MCLK_B#2 (11)
MCLK_B3 (11)
MCLK_B#3 (11)
MCLK_B4 (11)
MCLK_B#4 (11)
MCLK_B5 (11)
MCLK_B#5 (11)
VCC_DDR_C2
VCC_DDR_C3
values still need verification
VCC_AGP
VCC_DDR
Micro Star Restricted Secret
Title
Intel Springdale - Memory
Rev
1.0A
Document Number
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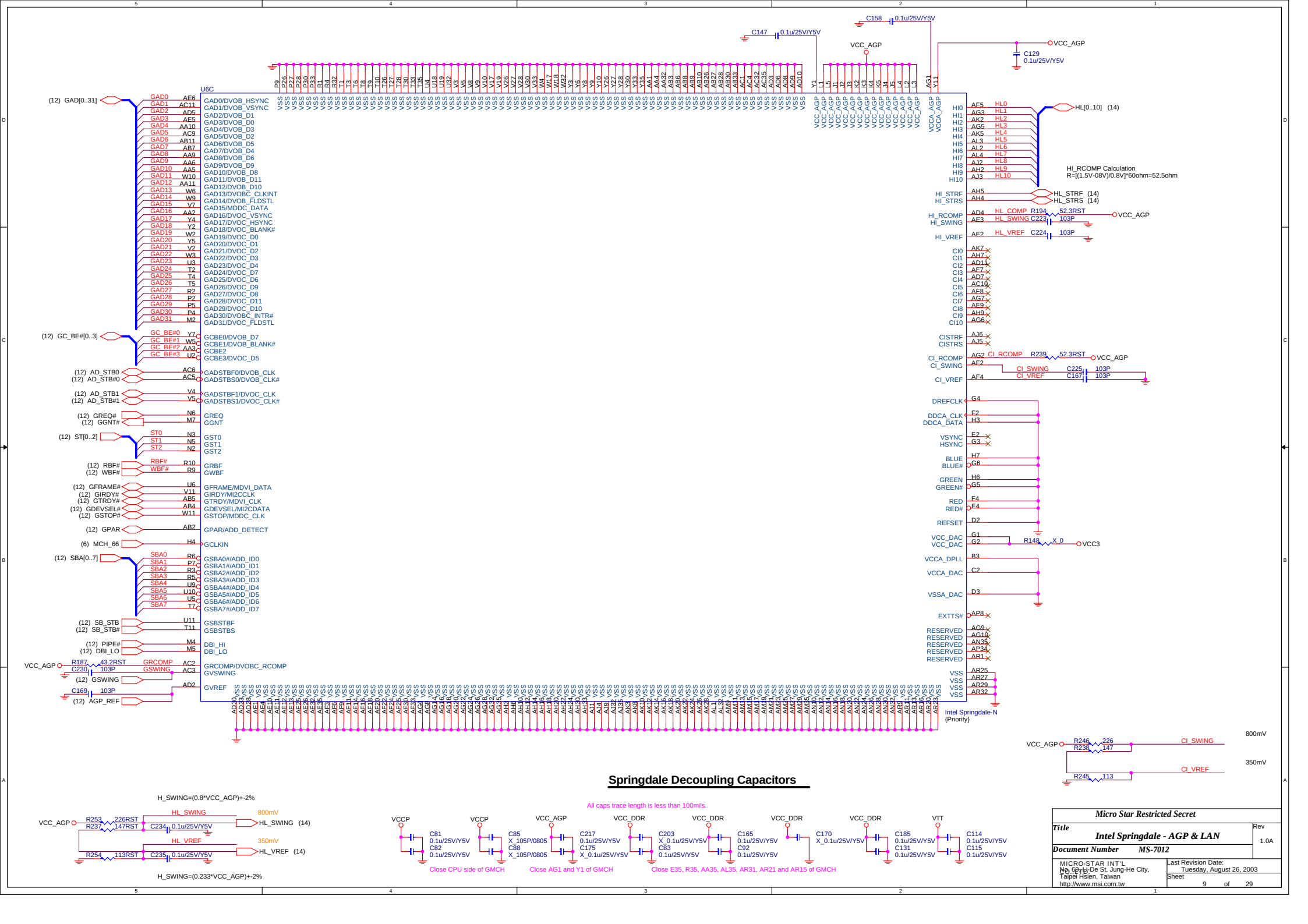
U6C
GAD0/DVOB_HSYNC
GAD1/DVOB_VSYNC
GAD2/DVOB_D1
GAD3/DVOB_D0
GAD4/DVOB_D3
GAD5/DVOB_D2
GAD6/DVOB_D5
GAD7/DVOB_D4
GAD8/DVOB_D6
GAD9/DVOB_D9
GAD10/DVOB_D8
GAD11/DVOB_D11
GAD12/DVOB_D10
GAD13/DVOBC_CLKINT
GAD14/DVOB_FLDSTL
GAD15/MDDC_DATA
GAD16/DVOC_VSYNC
GAD17/DVOC_HSYNC
GAD18/DVOC_BLANK#
GAD19/DVOC_D0
GAD20/DVOC_D1
GAD21/DVOC_D2
GAD22/DVOC_D3
GAD23/DVOC_D4
GAD24/DVOC_D7
GAD25/DVOC_D6
GAD26/DVOC_D9
GAD27/DVOC_D8
GAD28/DVOC_D11
GAD29/DVOC_D10
GAD30/DVOBC_INTR#
GAD31/DVOC_FLDSTL
(12) GAD[0..31]
GCBE0/DVOB_D7
GCBE1/DVOB_BLANK#
GCBE2
GCBE3/DVOC_D5
(12) GC_BE#[0..3]
GADSTBF0/DVOB_CLK
GADSTBS0/DVOB_CLK#
GADSTBF1/DVOC_CLK
GADSTBS1/DVOC_CLK#
(12) AD_STB0
(12) AD_STB#0
(12) AD_STB1
(12) AD_STB#1
GREQ
GGNT
(12) GREQ#
(12) GGNT#
GST0
GST1
GST2
(12) ST[0..2]
GRBF
GWBF
(12) RBF#
(12) WBF#
GFRAME/MDVI_DATA
GIRDY/MI2CCLK
GTRDY/MDVI_CLK
GDEVSEL/MI2CDATA
GSTOP/MDDC_CLK
(12) GFRAME#
(12) GIRDY#
(12) GTRDY#
(12) GDEVSEL#
(12) GSTOP#
GPAR/ADD_DETECT
(12) GPAR
GCLKIN
(6) MCH_66
GSBA0#/ADD_ID0
GSBA1#/ADD_ID1
GSBA2#/ADD_ID2
GSBA3#/ADD_ID3
GSBA4#/ADD_ID4
GSBA5#/ADD_ID5
GSBA6#/ADD_ID6
GSBA7#/ADD_ID7
(12) SBA[0..7]
GSBSTBF
GSBSTBS
(12) SB_STB
(12) SB_STB#
DBI_HI
DBI_LO
(12) PIPE#
(12) DBI_LO
GRCOMP/DVOBC_RCOMP
GVSWING
(12) GSWING
GVREF
(12) AGP_REF
R187 43.2RST
C230 103P
C169 103P
VCC_AGP
HL[0..10] (14)
HL_STRF (14)
HL_STRS (14)
HL_COMP R194 52.3RST
HL_SWING C223 103P
HL_VREF C224 103P
HI_RCOMP Calculation
R=[(1.5V-08V)/0.8V]*60ohm=52.5ohm
CI_RCOMP R239 52.3RST
CI_SWING C225 103P
CI_VREF C167 103P
R148 X_0
VCC3
Intel Springdale-N
{Priority}
R246 226
R238 147
R245 113
800mV
350mV
Springdale Decoupling Capacitors
All caps trace length is less than 100mils.
Close CPU side of GMCH
Close AG1 and Y1 of GMCH
Close E35, R35, AA35, AL35, AR31, AR21 and AR15 of GMCH
H_SWING=(0.8*VCC_AGP)+-2%
H_SWING=(0.233*VCC_AGP)+-2%
R253 226RST
R237 147RST
C234 0.1u/25V/Y5V
R254 113RST
C235 0.1u/25V/Y5V
HL_SWING
HL_VREF
800mV
350mV
HL_SWING (14)
HL_VREF (14)
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Intel Springdale - AGP & LAN
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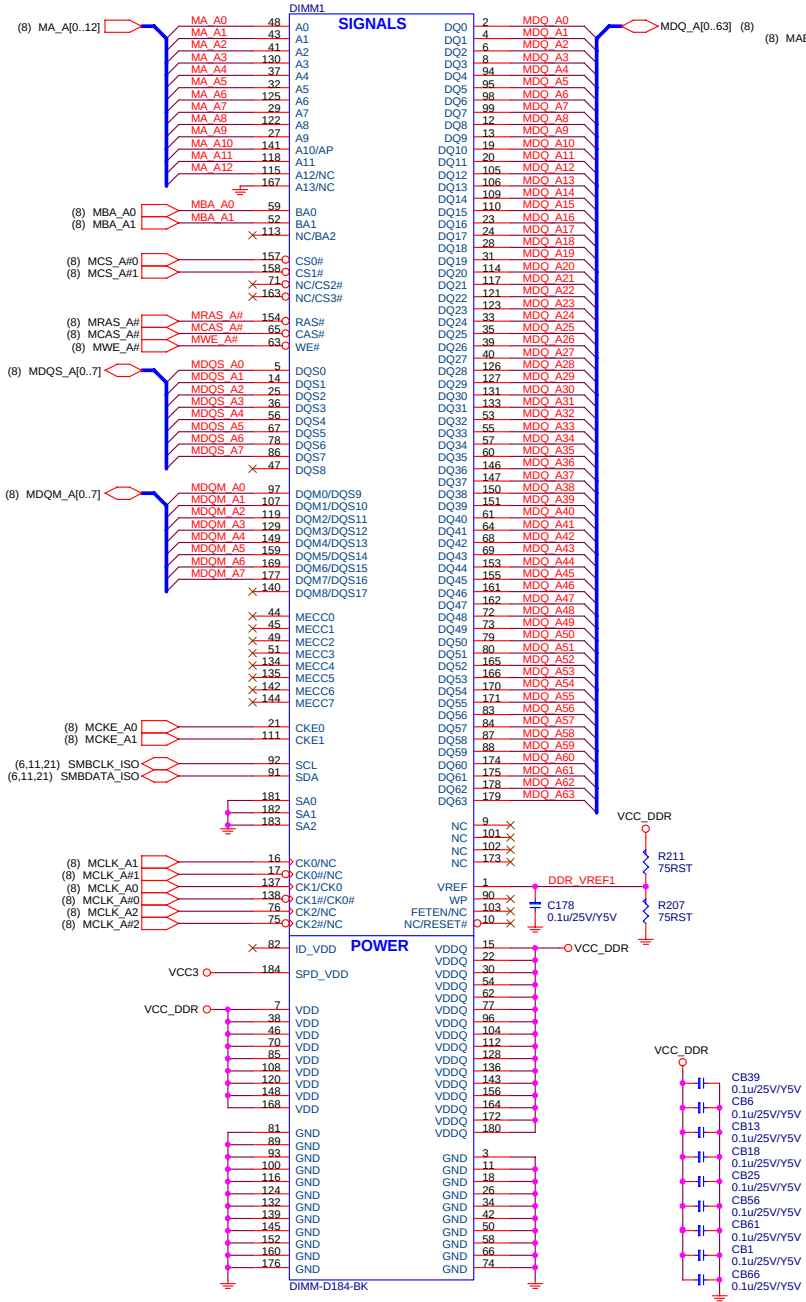
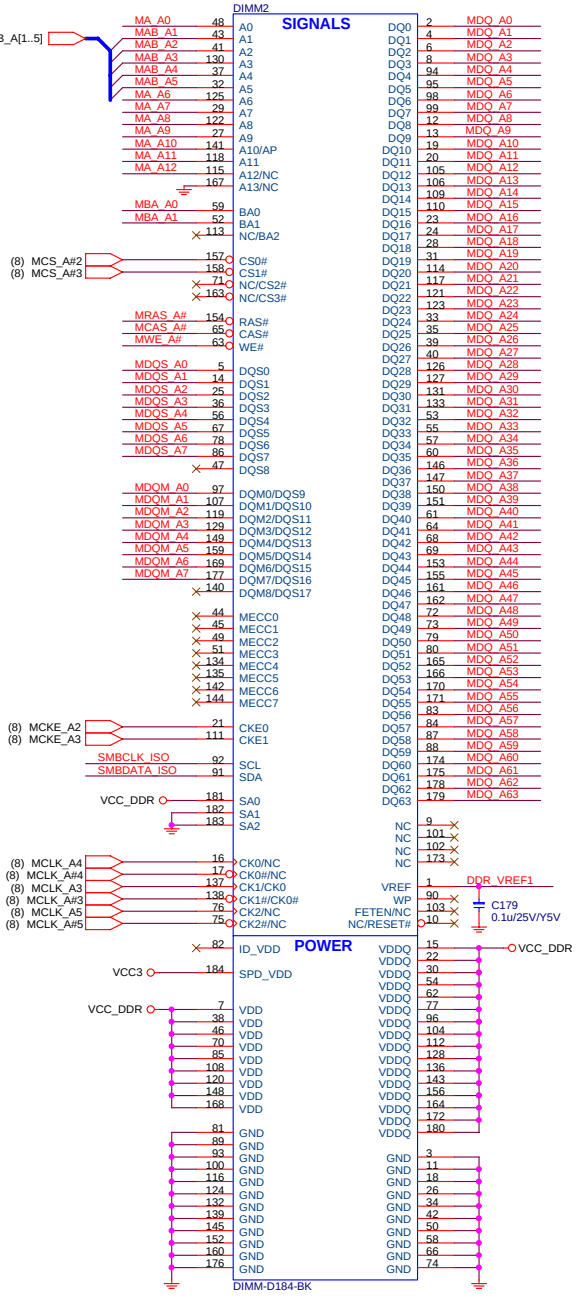
DDR DIMM1



ADDR.=1010000B

DDR DIMM2



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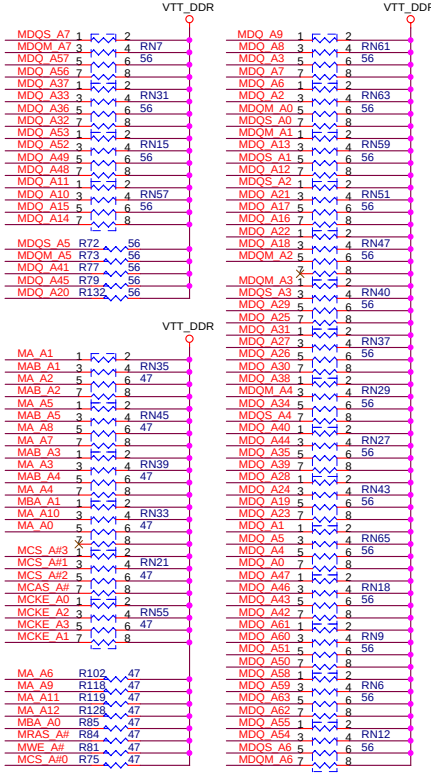
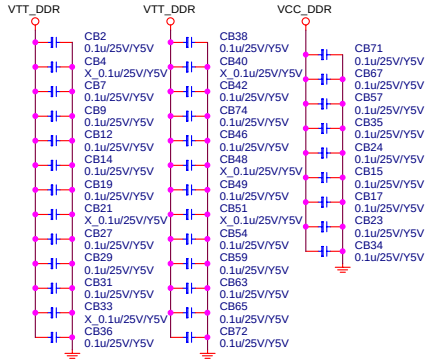
DDR Terminational Resisitors



DECOUPLING CAPACITORS



Place these decoupling capacitors close to VTT_DDR termination resistors.
One decoupling capacitor for each R-pack.

Title	*DDR DIMM 1,2*
Rev	1.0A
Document Number	*MS-7012*

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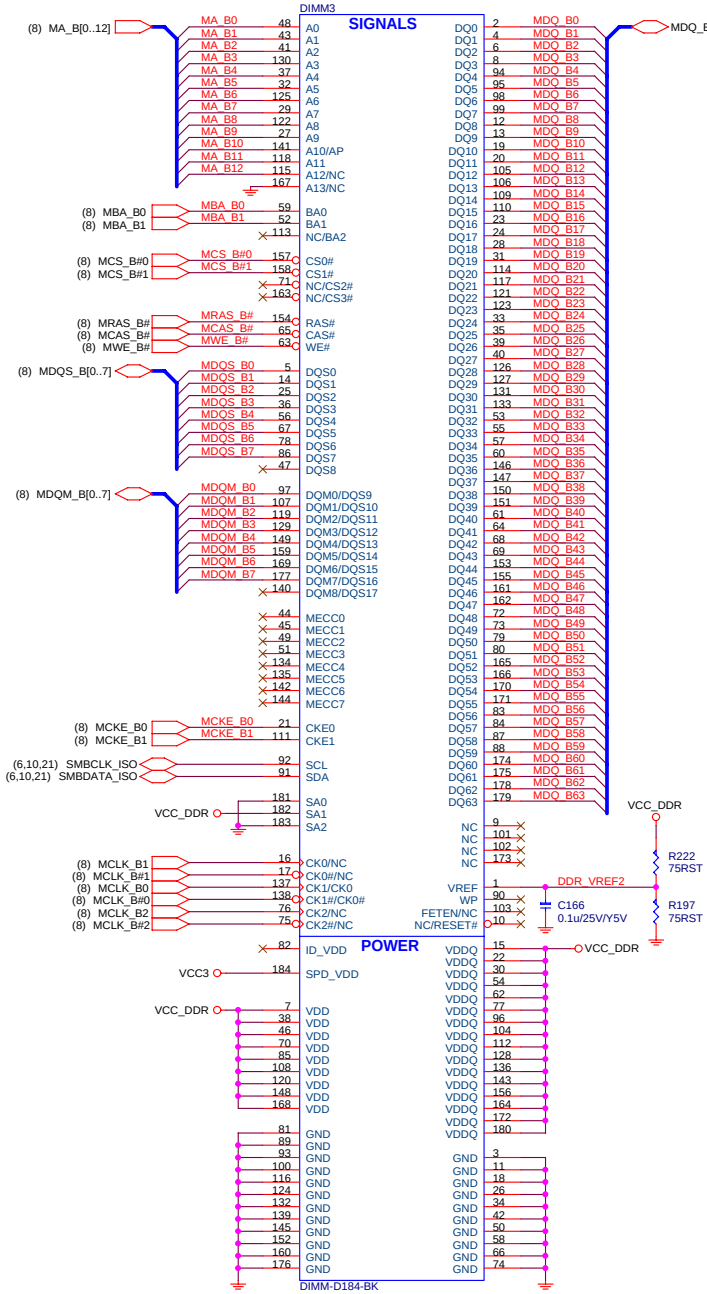
SYSTEM MEMORY

DDR DIMM3



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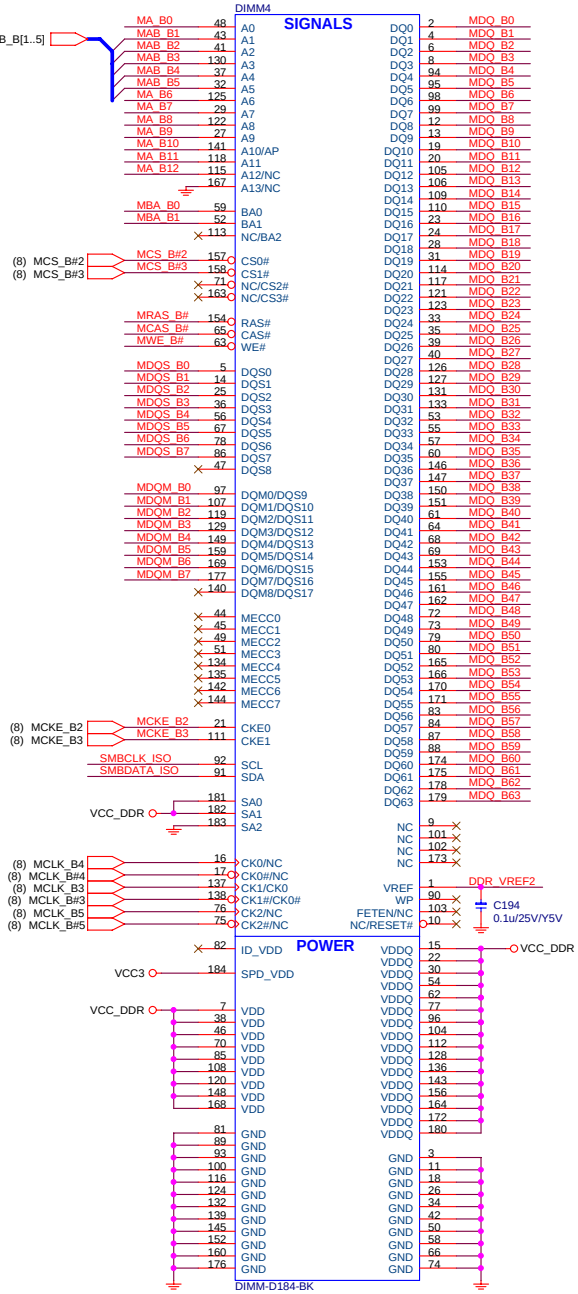
DDR DIMM4



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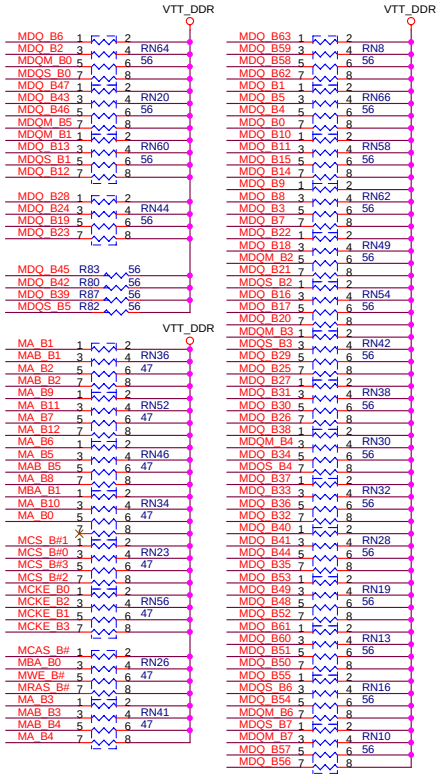
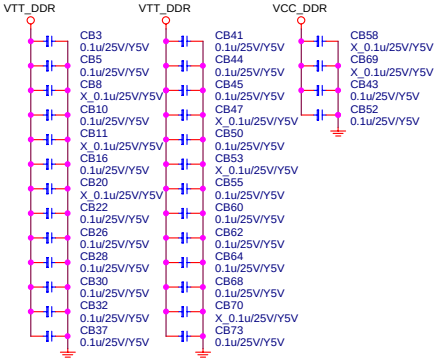
DDR Terminational Resisitors



DECOUPLING CAPACITORS



Place these decoupling capacitors close to VTT_DDR termination resistors.
One decoupling capacitor for each R-pack.

Micro Star Restricted Secret		
Title: DDR DIMM 3,4		Rev: 1.0A
Document Number: MS-7012		
MICRO-STAR INT'L No.69-Li De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, August 26, 2003	Sheet 11 of 29

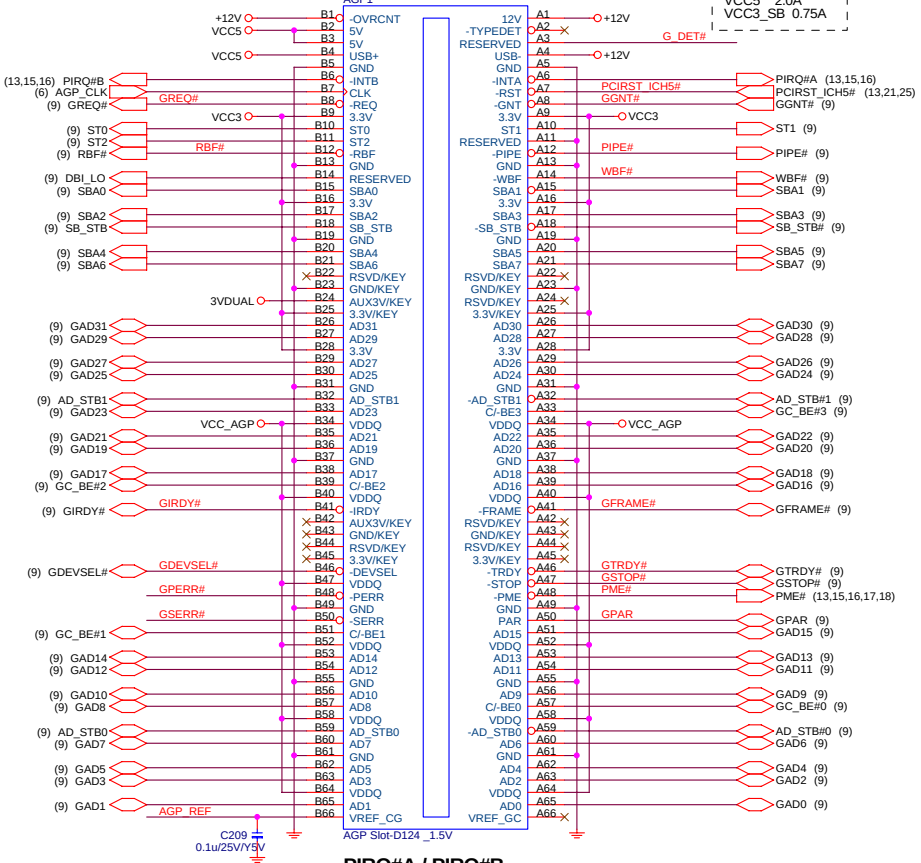
B1 == 12V
A4 == 12V
B4 == 5V

AGP 1.5V 4X/8X SLOT(AGP VER:3.0)

VCC5 = 60mils trace / 15 mils space

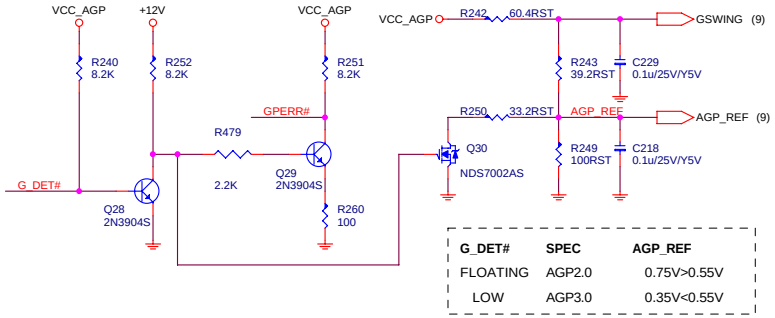
AGP Slot Imax

VCCg	2.0A
VCC3	6.0A
VCC12	1.0A
VCC5	2.0A
VCC3_SB	0.75A



PIRQ#A / PIRQ#B

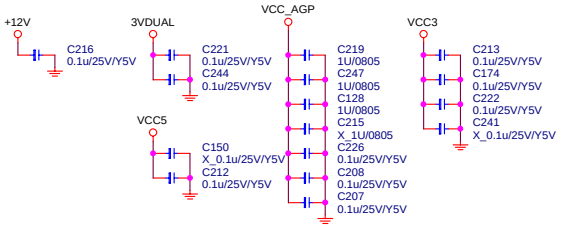
Springdale Reference & Swing Voltage Circuit



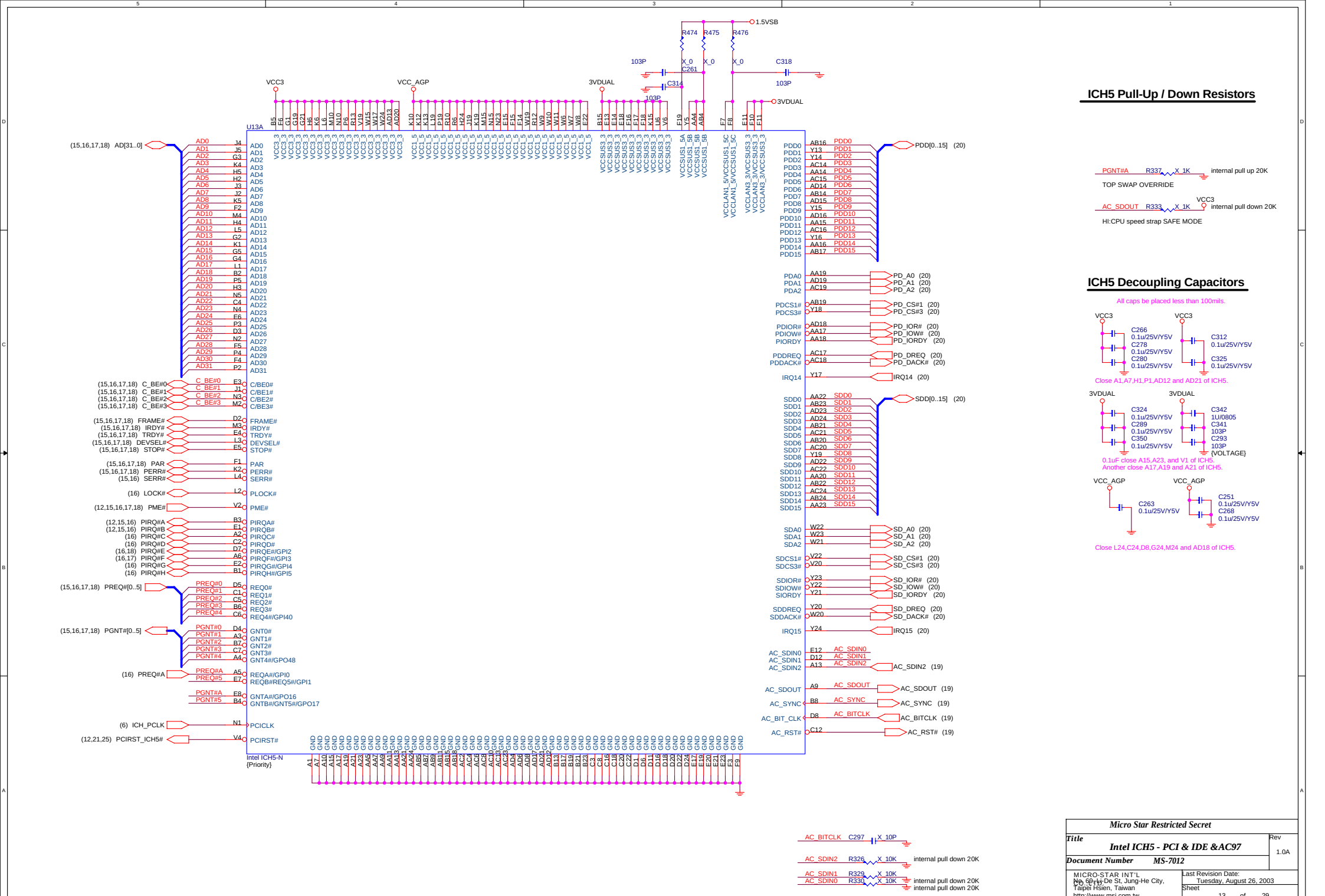
G_DET#	SPEC	AGP_REF
FLOATING	AGP2.0	0.75V>0.55V
LOW	AGP3.0	0.35V<0.55V

AGP TERMINATION RESISTORS

AGP SLOT DECOUPLING CAPACITORS



Micro Star Restricted Secret			
Title	*AGP SLOT*		Rev 1.0A
Document Number	*MS-7012*		
MICRO-STAR INT'L No.69-1,De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, August 26, 2003 Sheet 12 of 29	


U13A
Intel ICH5-N
{Priority}
1.5VSB
3VDUAL
VCC3
VCC_AGP
R474
R475
R476
C261
C314
C318
103P
X_0
AD[31..0]
C_BE#[0..3]
PDD[0..15]
SDD[0..15]
PREQ#[0..5]
PGNT#[0..5]
PCICLK
PCIRST#
ICH5 Pull-Up / Down Resistors
PGNT#A
R337
X_1K
internal pull up 20K
TOP SWAP OVERRIDE
AC_SDOUT
R333
internal pull down 20K
HI:CPU speed strap SAFE MODE
ICH5 Decoupling Capacitors
All caps be placed less than 100mils.
C266
C278
C280
C312
C325
0.1u/25V/Y5V
Close A1,A7,H1,P1,AD12 and AD21 of ICH5.
C324
C289
C350
C342
1U/0805
C341
C293
{VOLTAGE}
0.1uF close A15,A23, and V1 of ICH5.
Another close A17,A19 and A21 of ICH5.
C263
C251
C268
Close L24,C24,D8,G24,M24 and AD18 of ICH5.
AC_BITCLK
C297
AC_SDIN2
R326
AC_SDIN1
R329
AC_SDIN0
R330
Micro Star Restricted Secret
Title
Intel ICH5 - PCI & IDE &AC97
Rev
1.0A
Document Number
MS-7012
MICRO-STAR INT'L
No 69-1 Li De St, Jung-He City,
Taipei Hsien, Taiwan
http://www.msi.com.tw
Last Revision Date:
Tuesday, August 26, 2003
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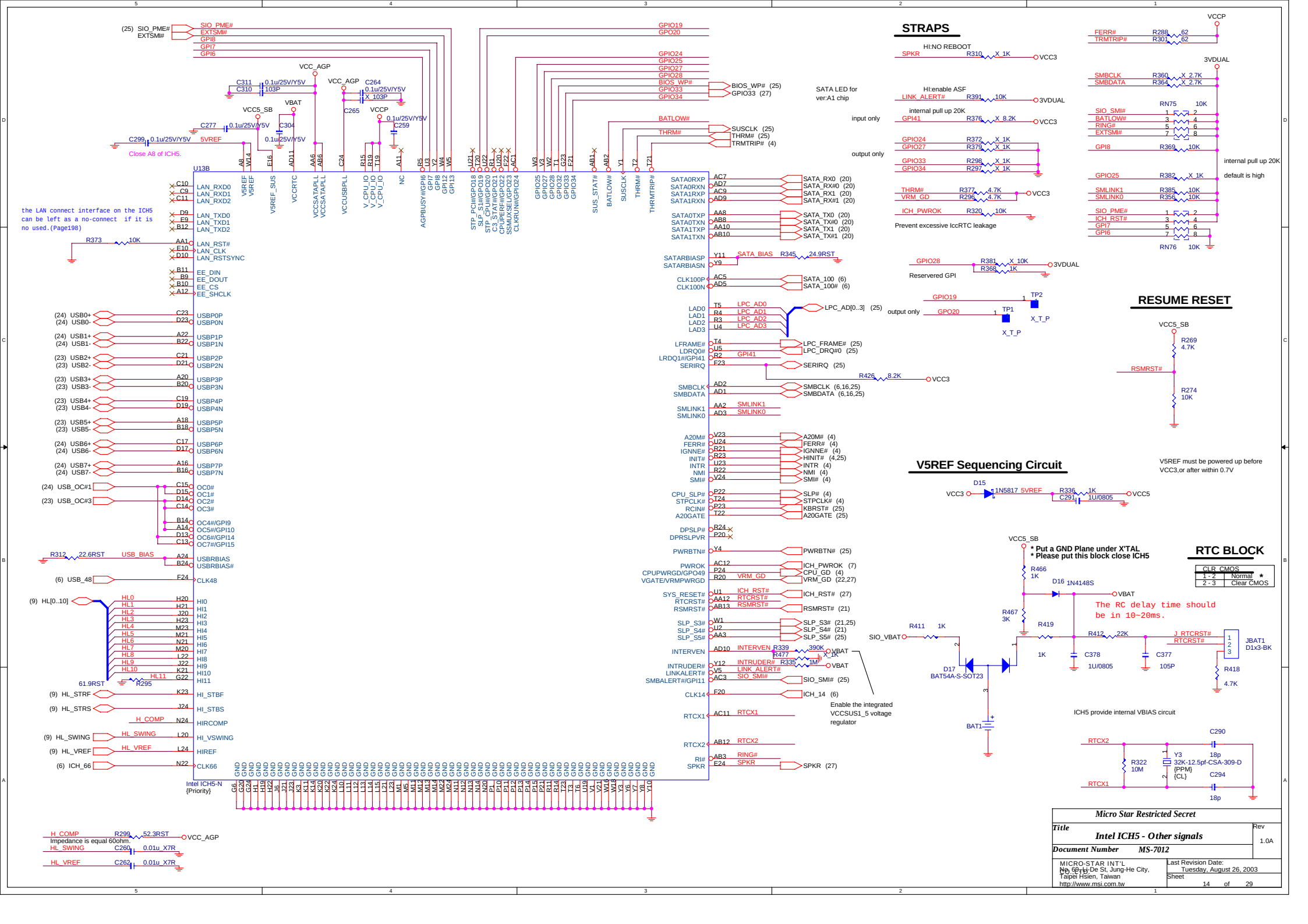
13
of
29

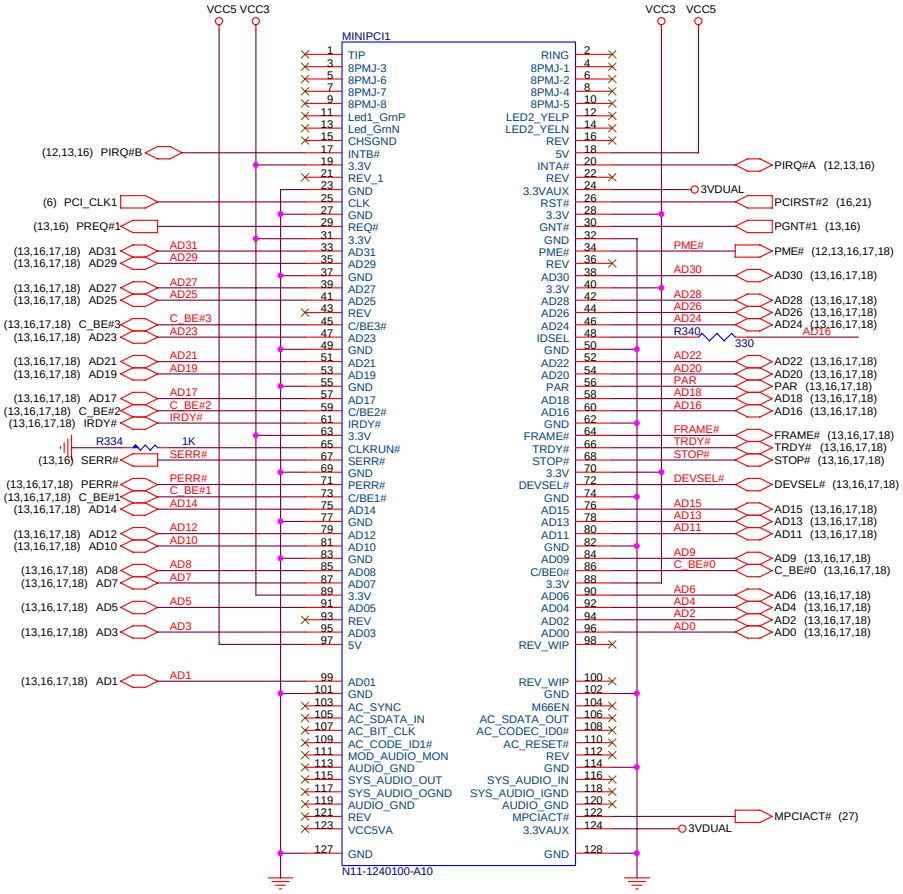

STRAPS
HI:NO REBOOT
SPKR
R310 X_1K
VCC3
HI:enable ASF
LINK_ALERT#
R391 10K
3VDUAL
internal pull up 20K
GPI41
R376 X_8.2K
GPIO24
GPIO27
GPIO33
GPIO34
R372 X_1K
R379 X_1K
R298 X_1K
R297 X_1K
THRM#
VRM_GD
R377 4.7K
R296 4.7K
ICH_PWROK
R320 10K
Prevent excessive IccRTC leakage
GPIO28
R381 X_10K
R368 1K
Reserved GPI
GPIO19
GPO20
TP2
TP1
X_T_P
output only
input only
SATA LED for ver:A1 chip
RESUME RESET
VCC5_SB
R269 4.7K
RSMRST#
R274 10K
V5REF Sequencing Circuit
D15
1N5817_5VREF
VCC3
R336 1K
C291 1U/0805
VCC5
V5REF must be powered up before VCC3,or after within 0.7V
RTC BLOCK
VCC5_SB
* Put a GND Plane under X'TAL
* Please put this block close ICH5
R466 1K
D16 1N4148S
VBAT
The RC delay time should be in 10~20ms.
R467 3K
R419 1K
R412 22K
C378 1U/0805
C377 105P
J_RTCRST#
RTCRST#
JBAT1
D1x3-BK
R418 4.7K
R411 1K
SIO_VBAT
D17 BAT54A-S-SOT23
BAT1
CLR_CMOS
1 - 2 Normal
2 - 3 Clear CMOS
ICH5 provide internal VBIAS circuit
RTCX2
RTCX1
R322 10M
Y3 32K-12.5pf-CSA-309-D {PPM} {CL}
C290 18p
C294 18p
U13B
Intel ICH5-N {Priority}
the LAN connect interface on the ICH5 can be left as a no-connect if it is no used.(Page198)
Close A8 of ICH5.
SIO_PME#
EXTSMI#
GPI8
GPI7
GPI6
VCC_AGP
VBAT
VCC5_SB
VCCP
5VREF
C311 0.1u/25V/Y5V
C310 103P
C264 0.1u/25V/Y5V
X_103P
C265
C259 0.1u/25V/Y5V
C277 0.1u/25V/Y5V
C304 0.1u/25V/Y5V
C299 0.1u/25V/Y5V
BIOS_WP# (25)
GPIO33 (27)
GPIO19
GPO20
GPIO24
GPIO25
GPIO27
GPIO28
BIOS_WP#
GPIO33
GPIO34
BATLOW#
THRM#
SUSCLK (25)
THRM# (25)
TRMTRIP# (4)
SATA0RXP
SATA0RXN
SATA1RXP
SATA1RXN
SATA0TXP
SATA0TXN
SATA1TXP
SATA1TXN
SATA_RX0 (20)
SATA_RX#0 (20)
SATA_RX1 (20)
SATA_RX#1 (20)
SATA_TX0 (20)
SATA_TX#0 (20)
SATA_TX1 (20)
SATA_TX#1 (20)
SATARBIASP
SATARBIASN
R373 10K
SATA_BIAS
R345 24.9RST
CLK100P
CLK100N
SATA_100 (6)
SATA_100# (6)
LAD0
LAD1
LAD2
LAD3
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_AD[0..3] (25)
LFRAME#
LDRQ0#
LRDQ1#/GPI41
SERIRQ
LPC_FRAME# (25)
LPC_DRQ#0 (25)
GPI41
SERIRQ (25)
R426 8.2K
SMBCLK
SMBDATA
SMBCLK (6,16,25)
SMBDATA (6,16,25)
SMLINK1
SMLINK0
A20M# (4)
FERR# (4)
IGNNE# (4)
INIT# (4,25)
INTR (4)
NMI (4)
SMI# (4)
CPU_SLP#
STPCLK#
RCIN#
A20GATE
SLP# (4)
STPCLK# (4)
KBRST# (25)
A20GATE (25)
DPSLP#
DPRSLPVR
PWRBTN#
PWRBTN# (25)
PWROK
CPUPWRGD/GPO49
VGATE/VRMPWRGD
ICH_PWROK (7)
CPU_GD (4)
VRM_GD (22,27)
SYS_RESET#
RTCRST#
RSMRST#
ICH_RST# (27)
RSMRST# (21)
SLP_S3#
SLP_S4#
SLP_S5#
SLP_S3# (21,25)
SLP_S4# (21)
SLP_S5# (25)
INTERVEN
R339 390K
R477 X_1K
R335 1M
INTRUDER#
LINKALERT#
SMBALERT#/GPI11
SIO_SMI# (25)
CLK14
ICH_14 (6)
RTCX1
RTCX2
RI#
SPKR
SPKR (27)
Enable the integrated VCCSUS1_5 voltage regulator
USB_BIAS
R312 22.6RST
USBRBIAS
USBRBIAS#
CLK48
(6) USB_48
(9) HL[0..10]
HL0
HL1
HL2
HL3
HL4
HL5
HL6
HL7
HL8
HL9
HL10
HL11
R295 61.9RST
HI0
HI1
HI2
HI3
HI4
HI5
HI6
HI7
HI8
HI9
HI10
HI11
(9) HL_STRF
(9) HL_STRS
HI_STBF
HI_STBS
H_COMP
HIRCOMP
(9) HL_SWING
HL_SWING
HI_VSWING
(9) HL_VREF
HL_VREF
HIREF
(6) ICH_66
CLK66
H_COMP R299 52.3RST
Impedance is equal 60ohm.
HL_SWING C260 0.01u_X7R
HL_VREF C262 0.01u_X7R
VCC_AGP
USB0+ USB0-
USB1+ USB1-
USB2+ USB2-
USB3+ USB3-
USB4+ USB4-
USB5+ USB5-
USB6+ USB6-
USB7+ USB7-
USBP0P USBP0N
USBP1P USBP1N
USBP2P USBP2N
USBP3P USBP3N
USBP4P USBP4N
USBP5P USBP5N
USBP6P USBP6N
USBP7P USBP7N
USB_OC#1
USB_OC#3
OC0#
OC1#
OC2#
OC3#
OC4#/GPI9
OC5#/GPI10
OC6#/GPI14
OC7#/GPI15
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN_RST#
LAN_CLK
LAN_RSTSYNC
EE_DIN
EE_DOUT
EE_CS
EE_SHCLK
SIO_PME# (25)
EXTSMI#
FERR# R288 62
TRMTRIP# R301 62
SMBCLK R360 X_2.7K
SMBDATA R364 X_2.7K
RN75 10K
SIO_SMI#
BATLOW#
RING#
EXTSMI#
GPI8 R369 10K
GPIO25 R382 X_1K
SMLINK1 R385 10K
SMLINK0 R356 10K
SIO_PME#
ICH_RST#
GPI7
GPI6
RN76 10K
internal pull up 20K
default is high
3VDUAL
VCCP

IDSEL = AD16

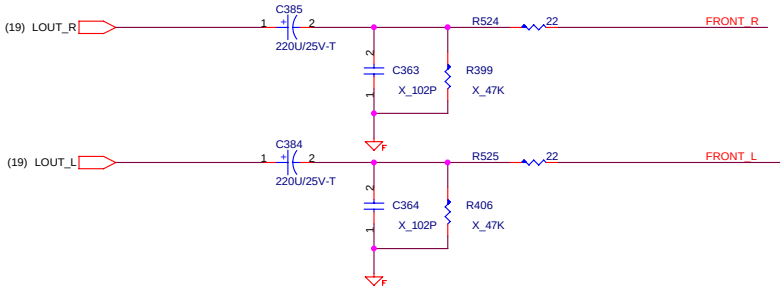
MASTER = PREQ#1/PGNT#1

PIRQ#A CLK-gen-Pin14

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



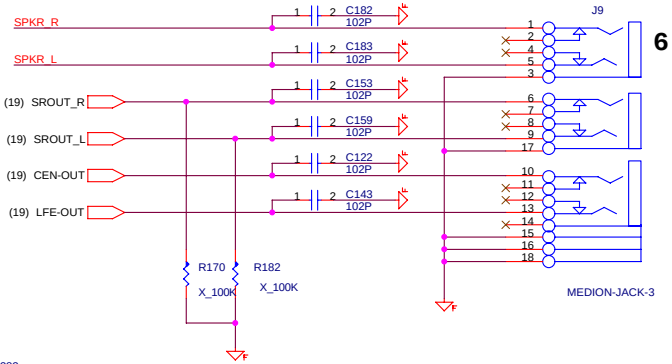
SPEAKER OUT CIRCUIT



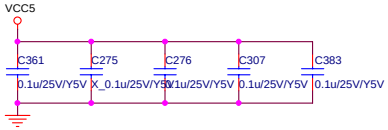
Audio Connector

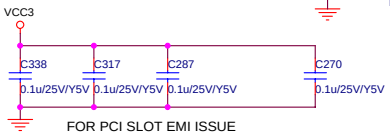
N54-13F0011-K06

CN-IOC-JACKx3+PHONE-D13

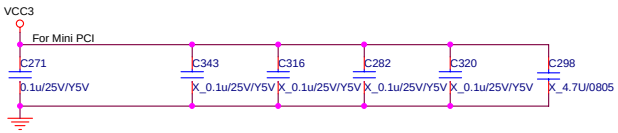


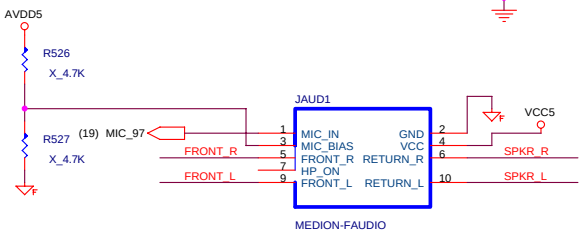
6 CHANNEL

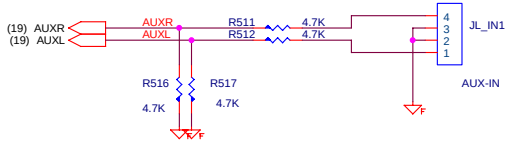




FOR PCI SLOT EMI ISSUE



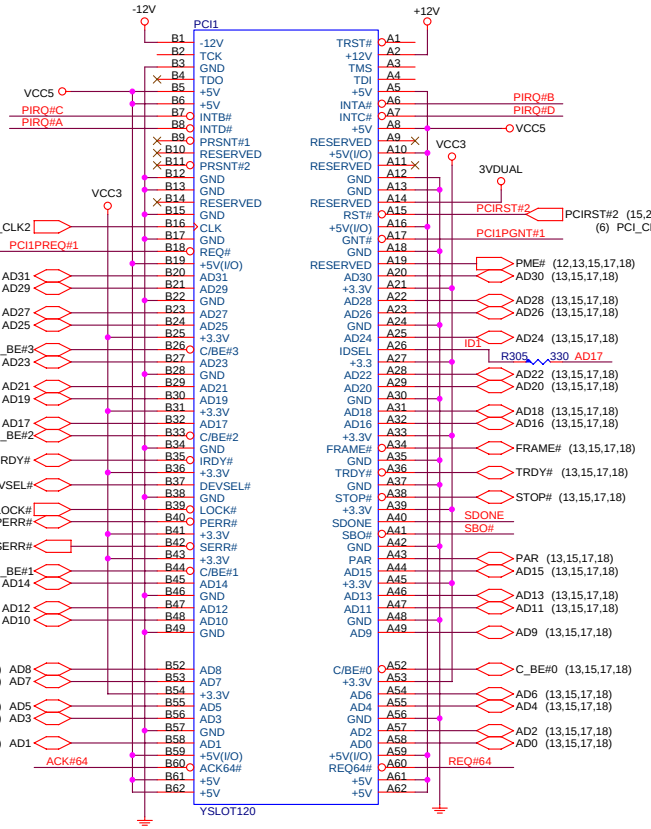




Micro Star Restricted Secret		
Title: Mini PCI & Audio conn.		Rev: 1.0A
Document Number: MS-7012		
MICRO-STAR INT'L No 69-Li De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, August 26, 2003 Sheet 15 of 29	

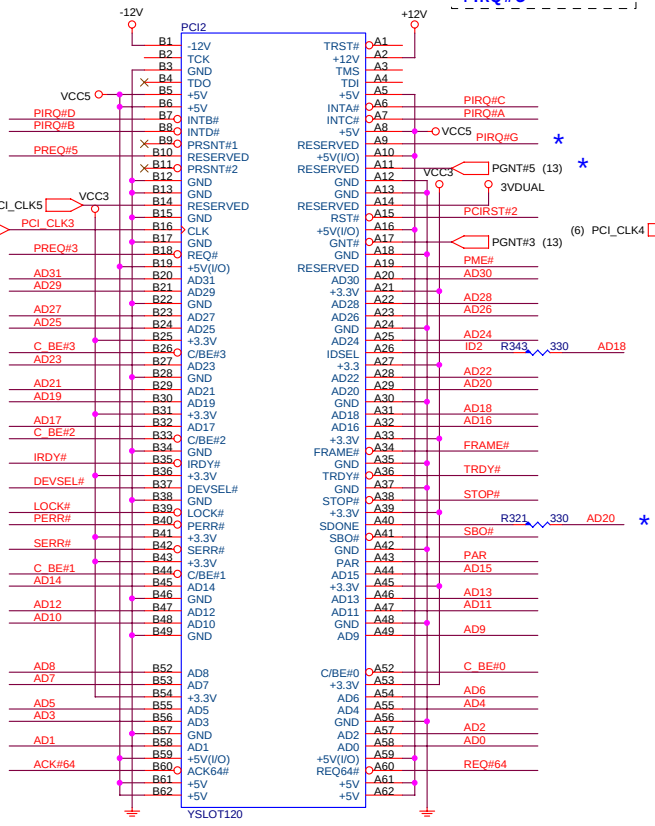
IDSEL = AD17
MASTER = MS1 or PREQ#0
PIRQ#B

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



IDSEL = AD18
MASTER = PREQ#3
PIRQ#C

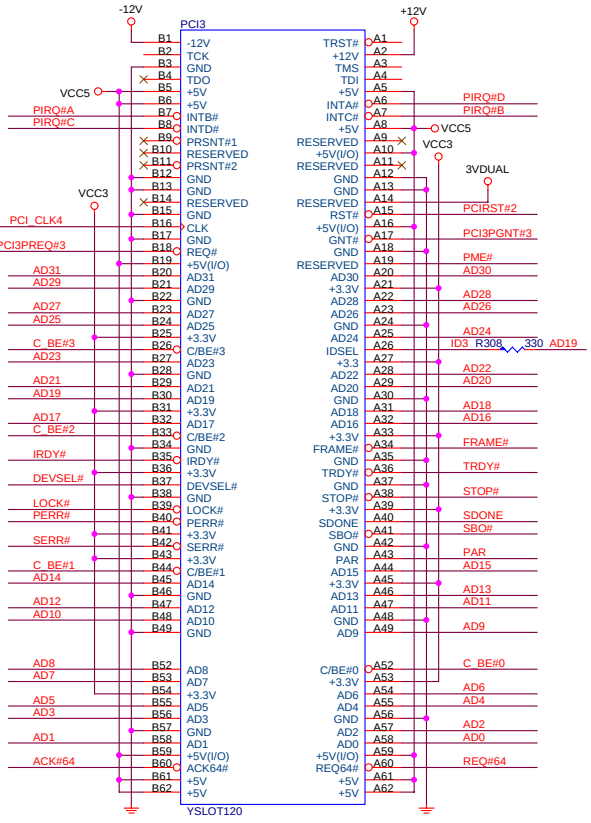
PCI SLOT 2 (PCI VER: 2.2 COMPLY)

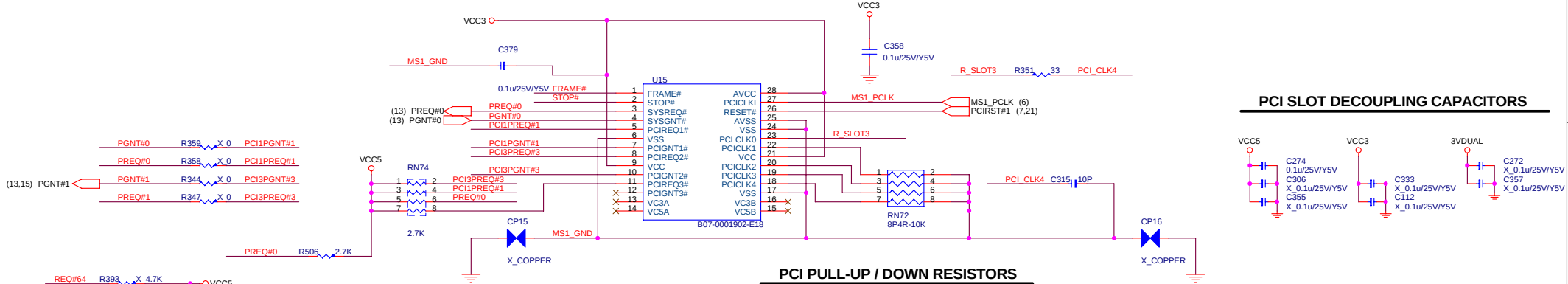


MEDION SPEC
PCI4: IDSEL = AD20
MASTER = PREQ#5
PIRQ#G

IDSEL = AD19
MASTER = MS1 or PREQ#1
PIRQ#D

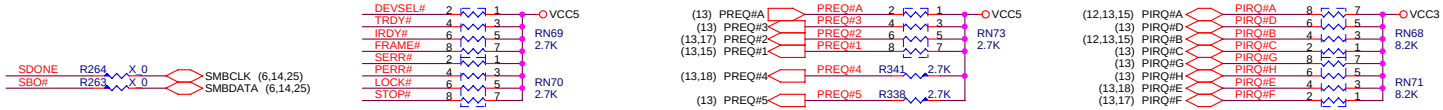
PCI SLOT 3 (PCI VER: 2.2 COMPLY)





PCI SLOT DECOUPLING CAPACITORS

PCI PULL-UP / DOWN RESISTORS



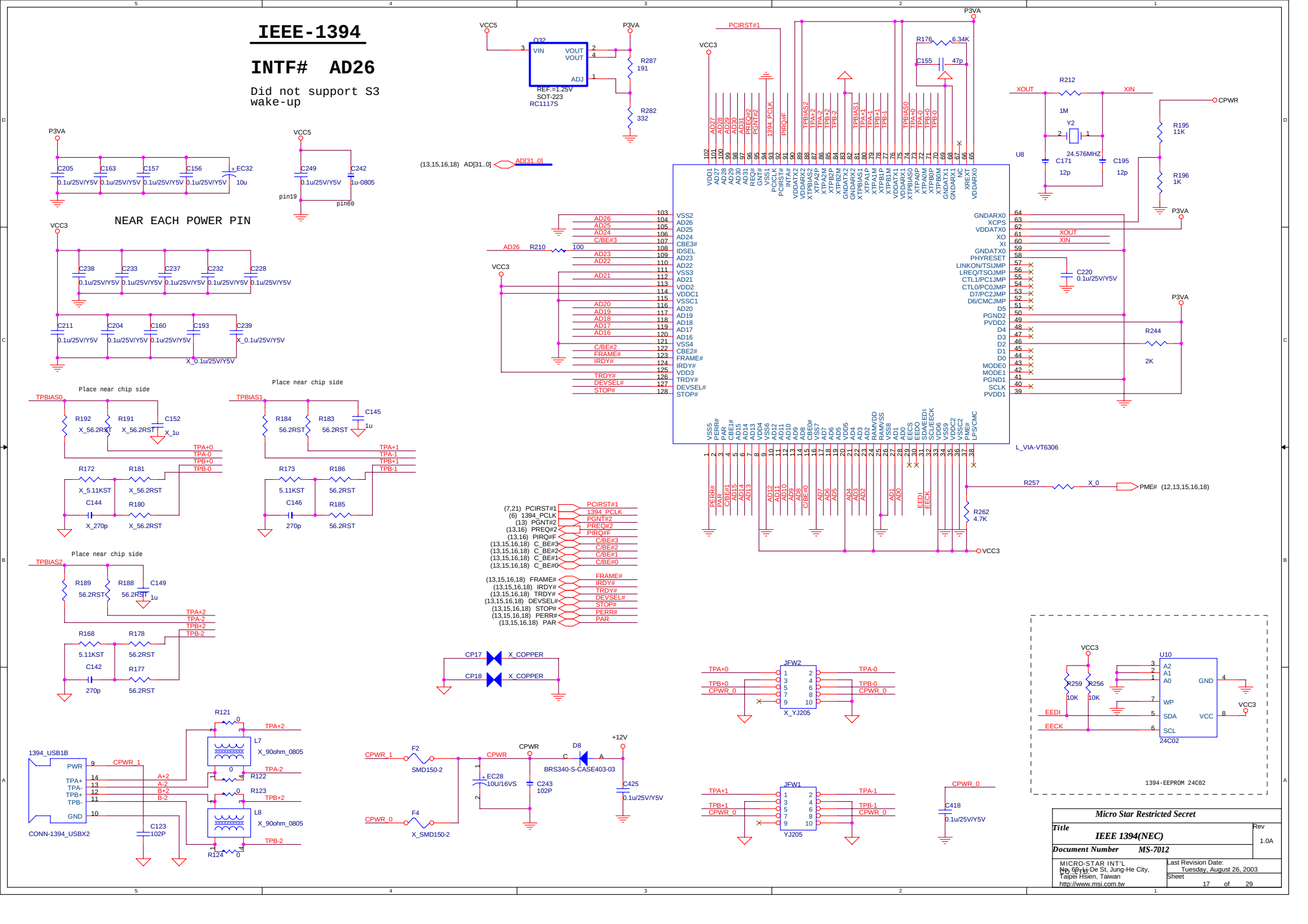
Micro Star Restricted Secret	
Title: PCI Slot 1 & 2 & 3	Rev: 1.0A
Document Number: MS-7012	
MICRO-STAR INT'L No.69-1, De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, August 26, 2003 Sheet 16 of 29

IEEE-1394

INTF# AD26

Did not support S3 wake-up

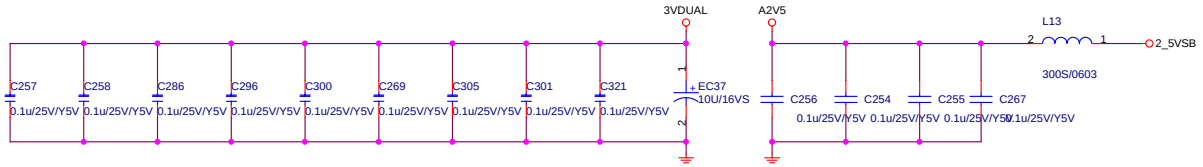
NEAR EACH POWER PIN

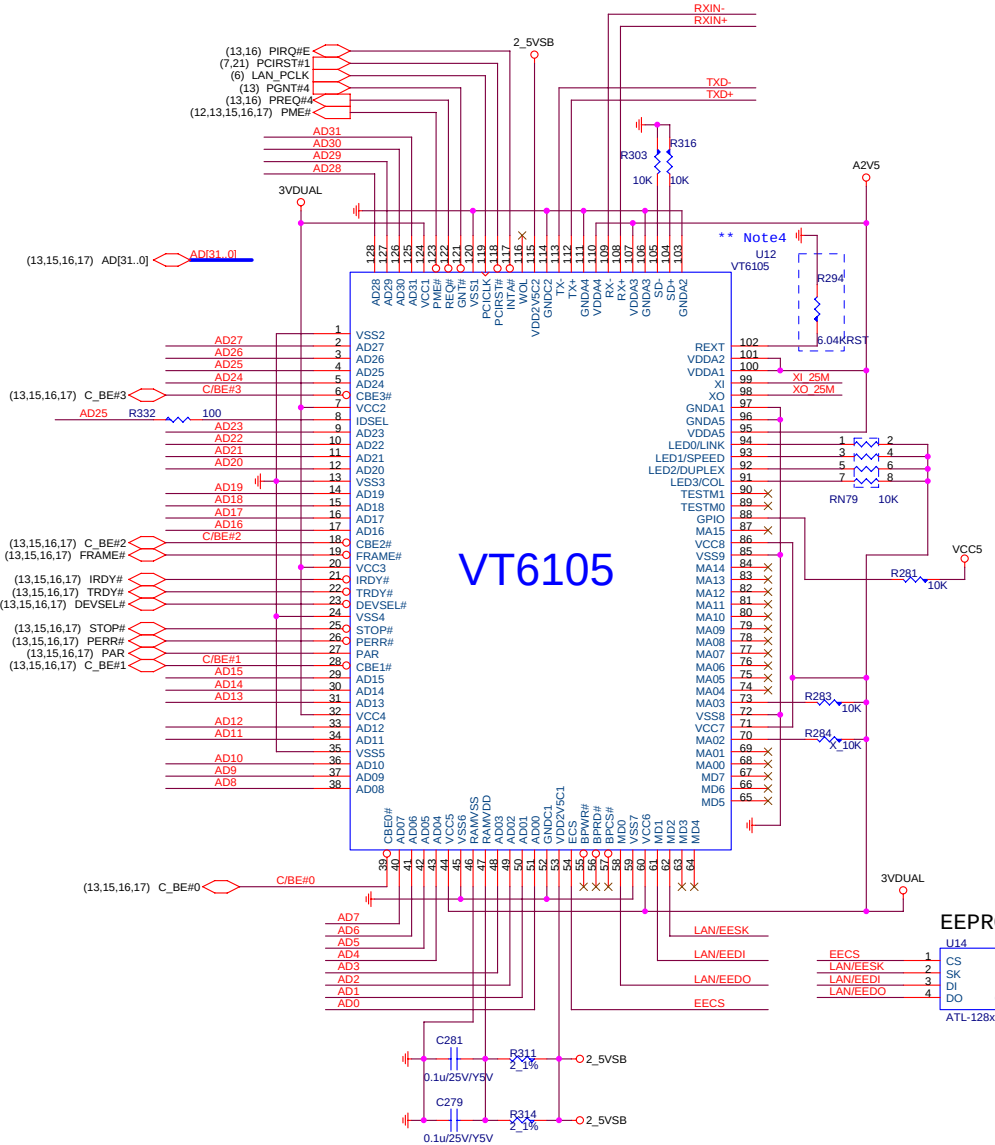


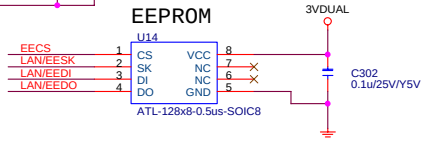
Micro Star Restricted Secret	
Title: IEEE 1394(NEC)	Rev: 1.0A
Document Number: MS-7012	
MICRO-STAR INT'L No 69-Li De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, August 26, 2003 Sheet 17 of 29

Lan - VIA6105

REQ#/GNT#4
INTE# AD25

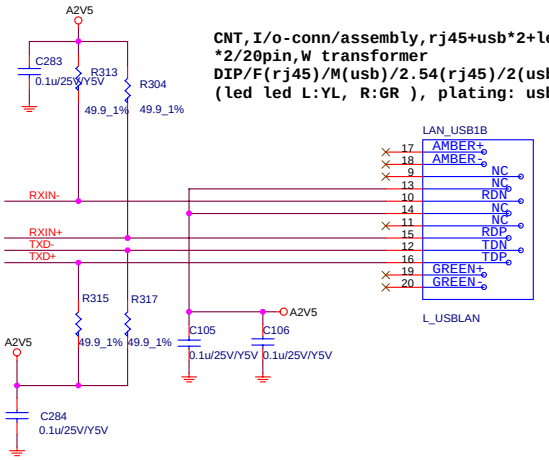




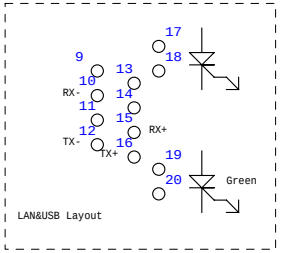


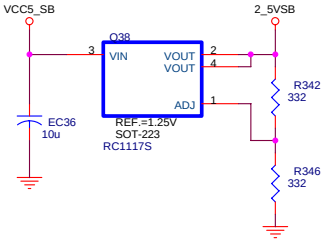
40 : 6 : 8 : 6 : 40 mil

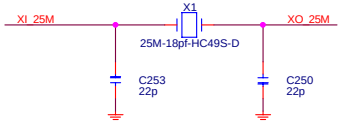
** Note 5



CNT,I/o-conn/assembly,rj45+usb*2+led
***2/20pin,W transformer**
DIP/F(rj45)/M(usb)/2.54(rj45)/2(usb)/2.54(led),black,P-B/PBT, led on the top
(led led L:YL, R:GR), plating: usb/rj45 30u-in,PIN=3.3

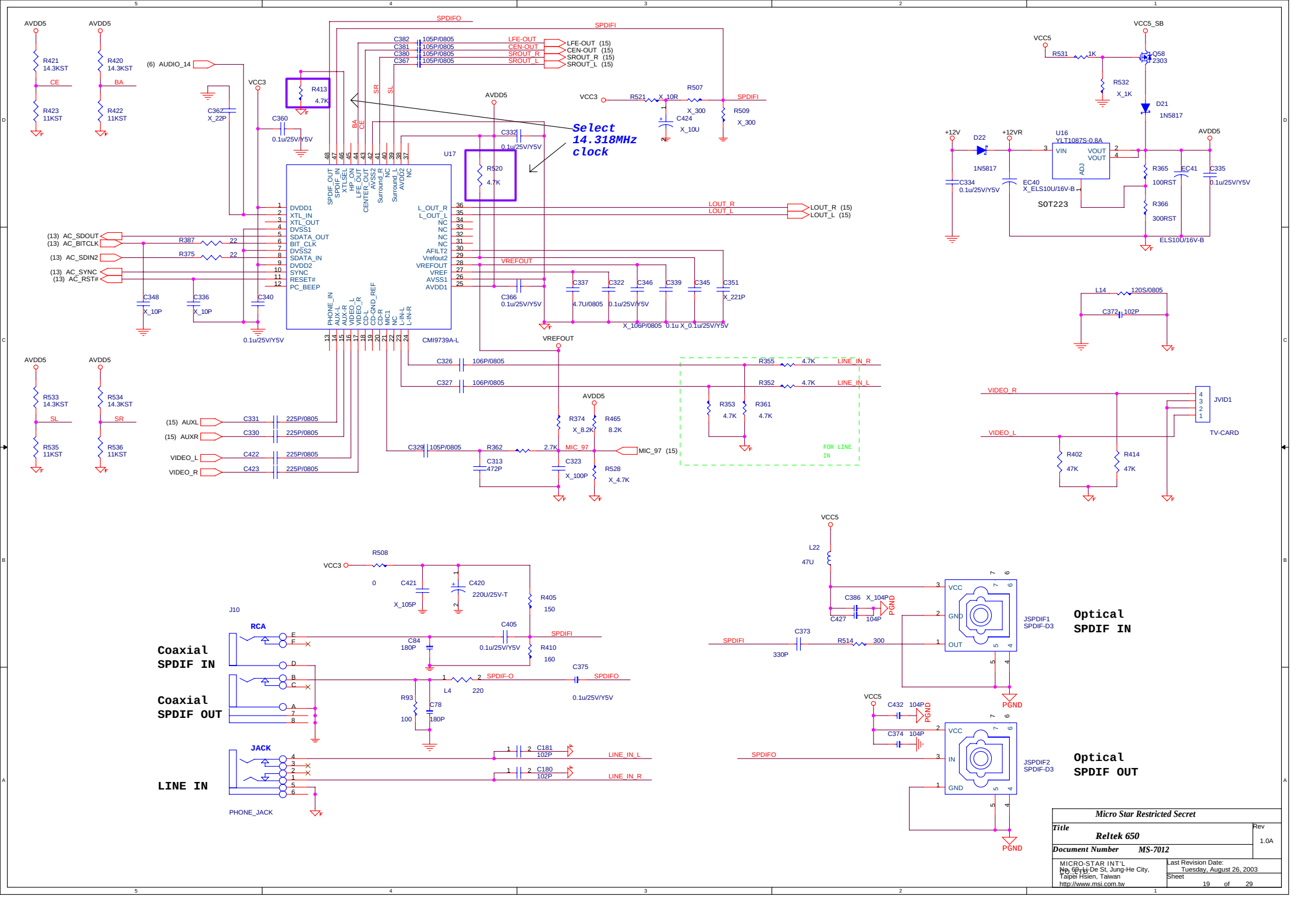






Micro Star Restricted Secret

Title: Broadcom 4401		Rev: 1.0A
Document Number: MS-7012		
MICRO-STAR INT'L No. 69-1, De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, August 26, 2003	Sheet 18 of 29


CMI9739A-L
U17
Select 14.318MHz clock
Coaxial SPDIF IN
Coaxial SPDIF OUT
LINE IN
Optical SPDIF IN
Optical SPDIF OUT
RCA
JACK
PHONE_JACK
TV-CARD
JVID1
JSPDIF1 SPDIF-D3
JSPDIF2 SPDIF-D3
YLT1087S-0.8A
2303
1N5817
SOT223
ELS10U/16V-B
FOR LINE IN
Micro Star Restricted Secret
Reltek 650
MS-7012
1.0A
MICRO-STAR INT'L
No 69-1 Li De St, Jung-He City, Taipei Hsien, Taiwan
http://www.msi.com.tw
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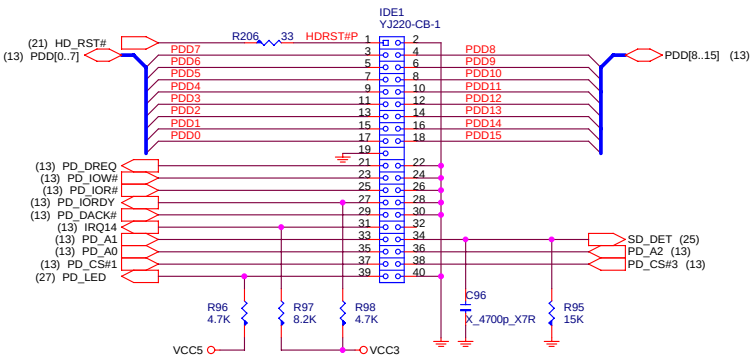
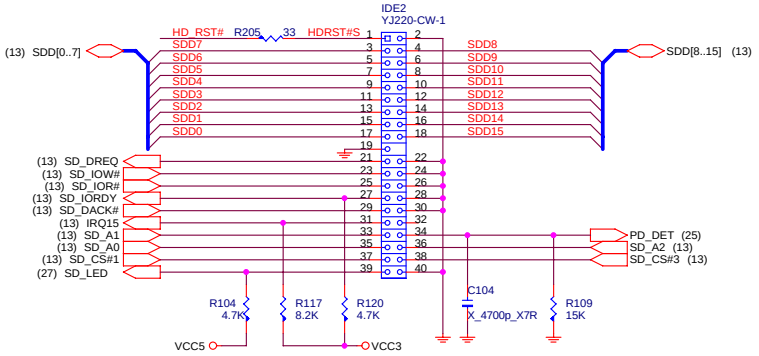
ATA 33/66/100 Connector

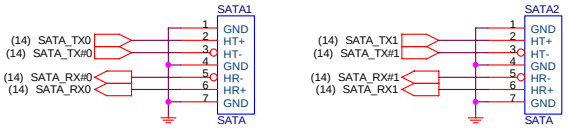
PRIMARY IDE BLOCK

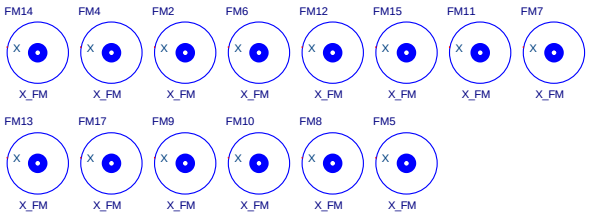


SECONDARY IDE BLOCK

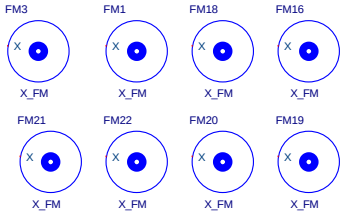


SERIAL ATA CONNECTOR BLOCK

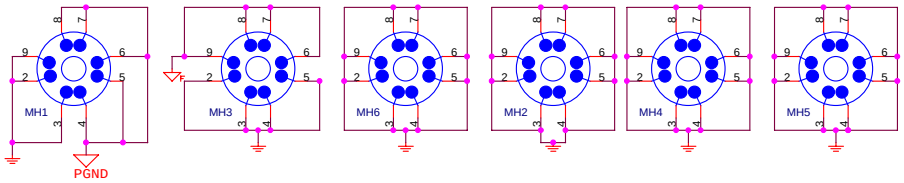




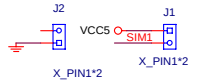
Optics Orientation Holes



Mounting Holes



Simulation



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Title	*ATA 33/66/100 Connector*	Rev 1.0A
Document Number	*MS-7012*	
MICRO-STAR INT'L No 69-1 Li De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, August 26, 2003	Sheet 20 of 29

ACPI Controller

5V DUAL Power

SEL0	5VUSB
H	2 MOSFET
L	1 MOSFET

**S50# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)
5VUSB USE 2 MOSFET

VCC 1.5 Voltage Regulator

1.7V@250mA

Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
MEM_STR	Main	Standby	0V

**INPUT 2 AND 3 MUST BE HI LEVEL WHEN USE
OUTPUT 1 AND 2 FOR GPIO FUNCTION

Near 302E

Low RDS ON MOSFET

1.5V/4A(NB)+1A(SB)+2A(AGP)

DDR VTT Power

1.25V/2.1A

SEL1	VRAM	VRAM_2.5
H	3.3VDUAL	2.5V
TRI-STATE	3.3VSB	2.5V
L	3.3VSTR	1.25V

FOR 3VSB OR 3VSTR
SETTING BY SEL1

FOR 3VDUAL
SETTING BY
SEL1

Wide Trace

Pin 15,19,22,32 Must
reserve capacitor.

ICH5 300mA
PCI 375+20+20= 415mA
VCC3_SB 715mA

** SETTING 3VSTR THEN VRAM_2.5
BECOME TO 1.25 VREF

CHARGE PUMP VOLTAGE OUTPUT

VCC_VID / VID_GOOD

Place MOSFET near CPU

VCC_VID (5,22)
1.2V/150mA

THIS PIN IS OPEN DRAIN OUTPUT

DDR 2.5V Power

2.5V/7A(DIMM)+5A(NB)

Micro Star Restricted Secret		
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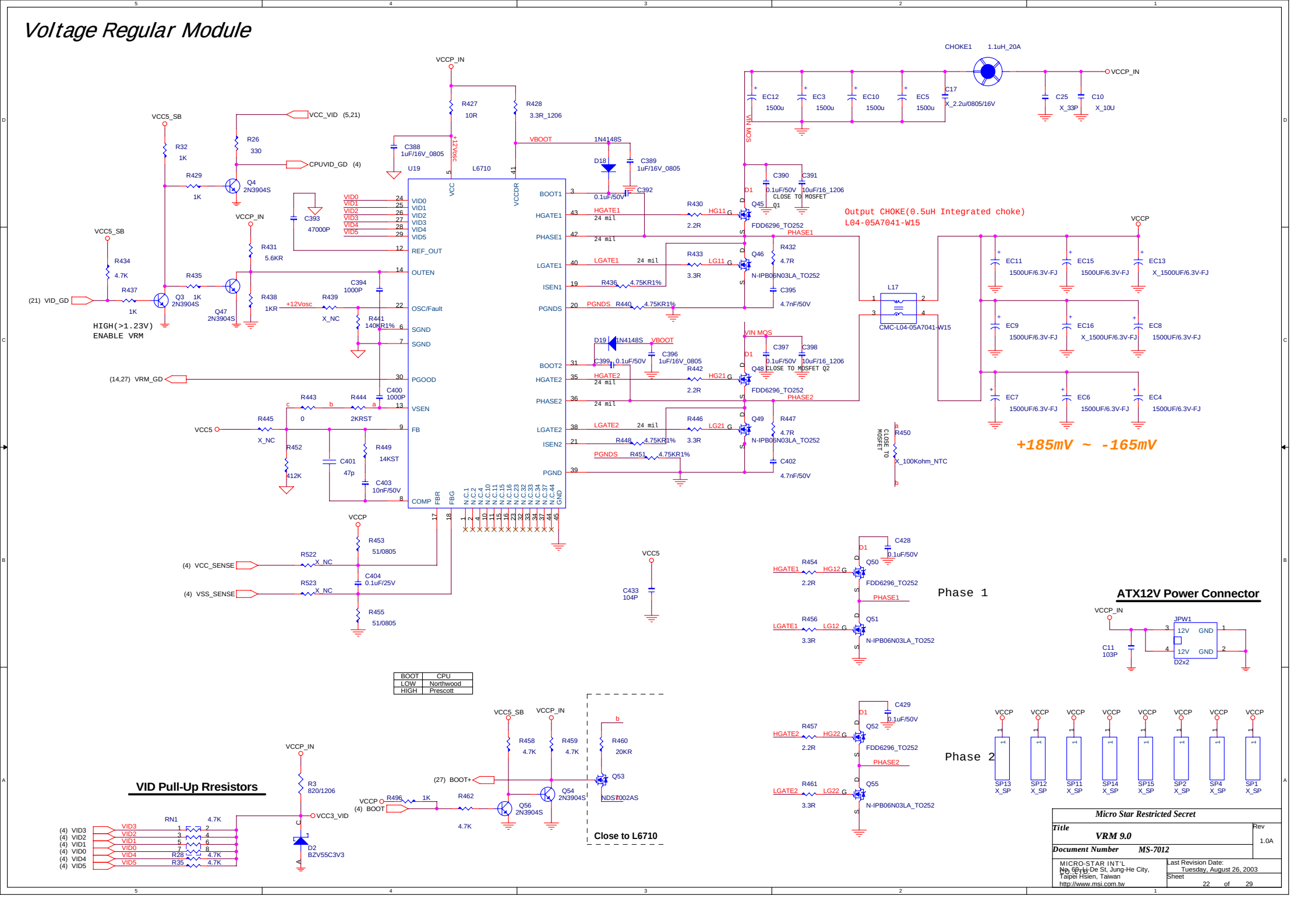
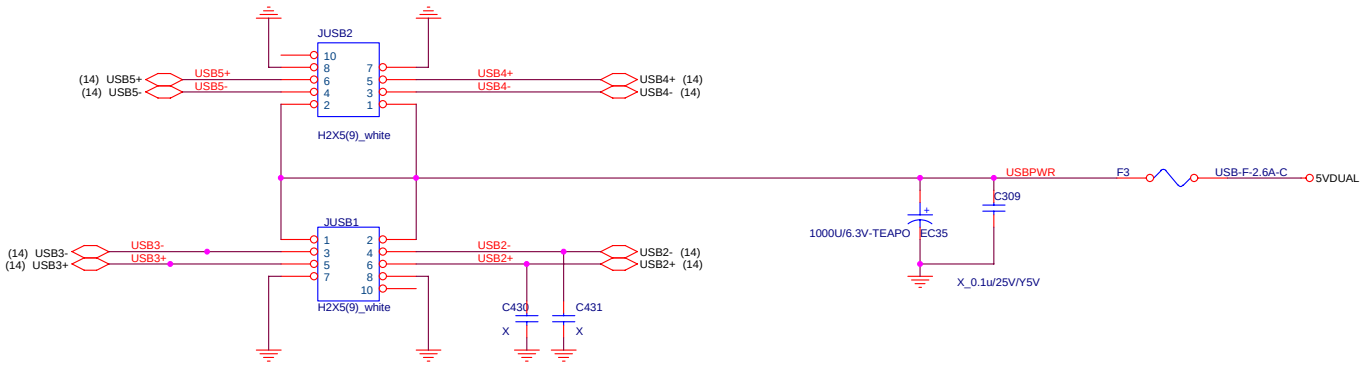
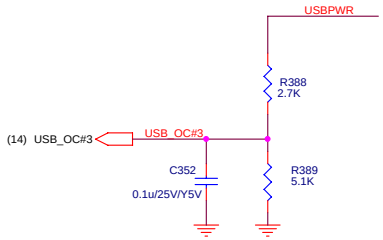
Voltage Regular Module



FRONT USB PORT





*** USB Trace width : 7.5 mils**

*** USB Trace Spacing : 20 mils**

*** Differential USB Signlas Trace, Spacing : 7.5 mils**

Micro Star Restricted Secret		
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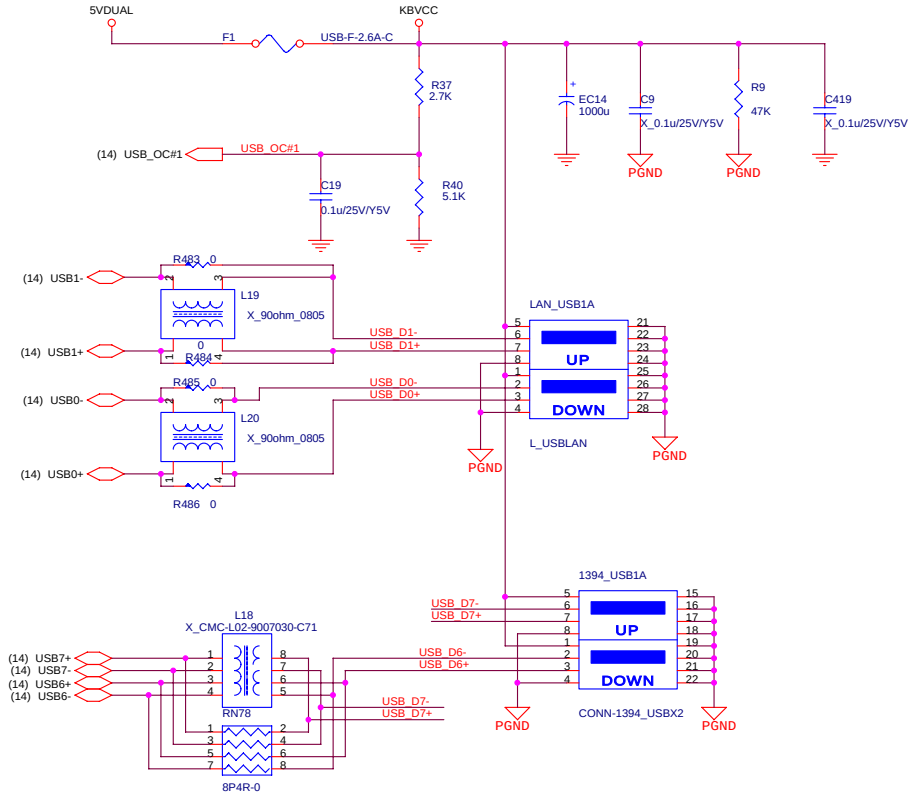
REAR USB PORT



Micro Star Restricted Secret		
Title **Rear USB Port**		Rev 1.0A
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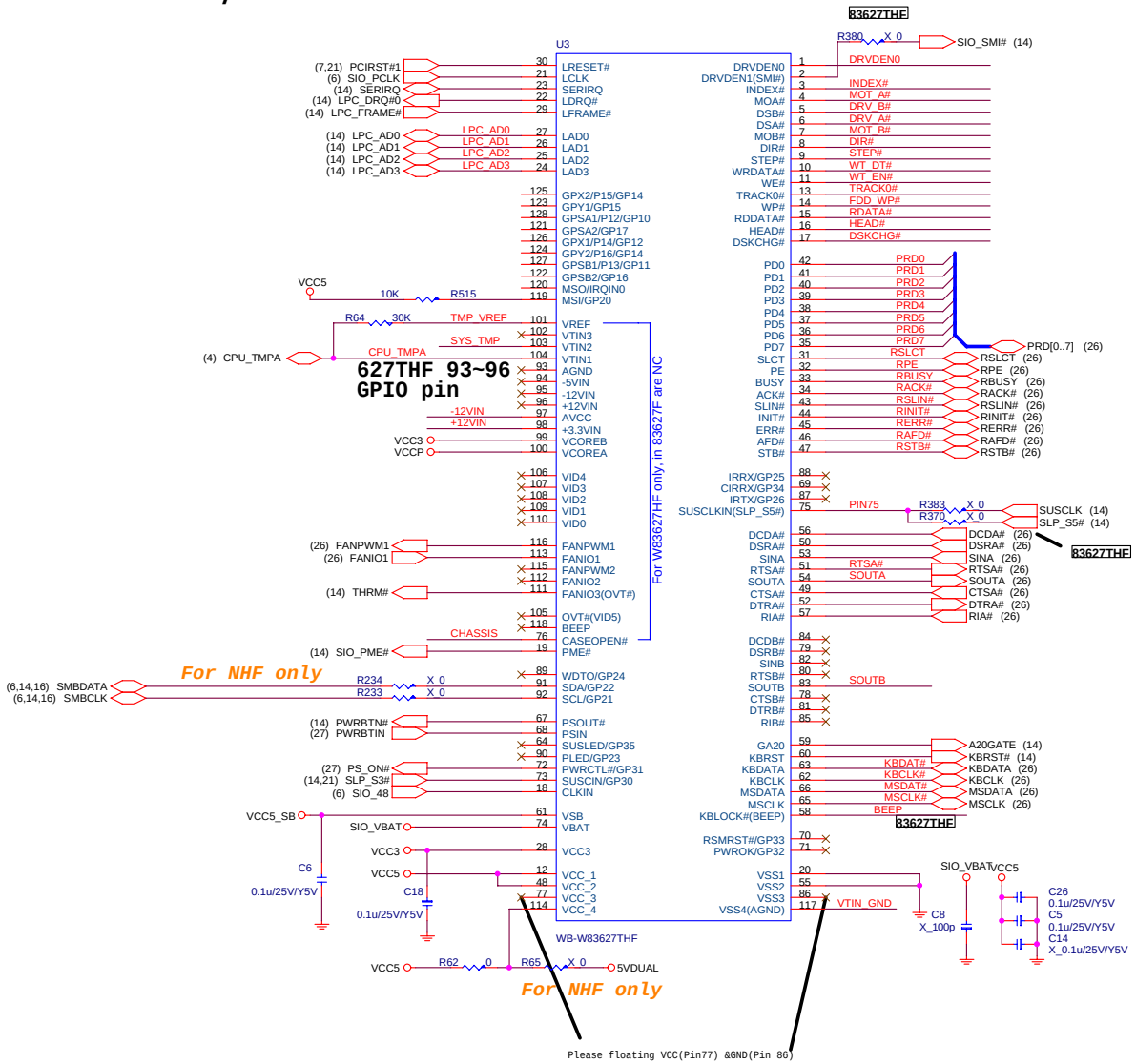
Super I/O

LPC SUPER I/O W83627F/HF/THF



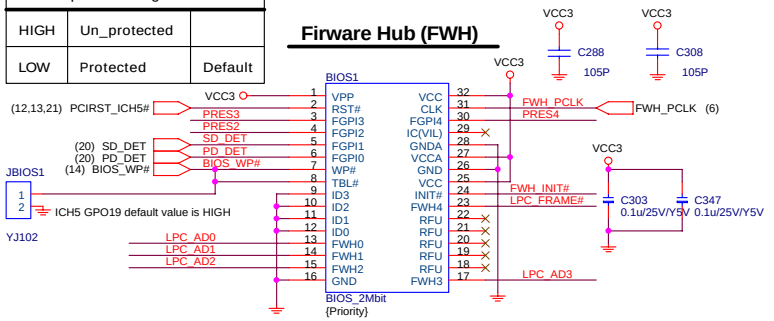
BIOS PROTECT BLOCK

BIOS Update Config.		
HIGH	Un_protected	
LOW	Protected	Default

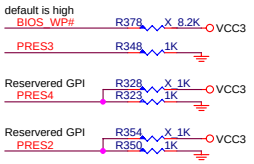
FWH DECOUPLING CAPACITORS

Place Cap. as Close to FWH< 350 mil

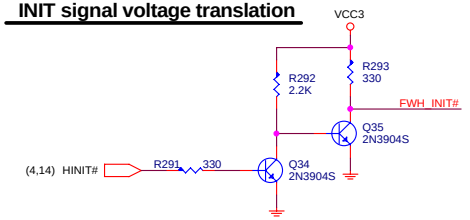
Firware Hub (FWH)



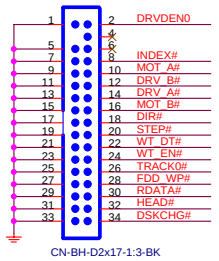
FWH Resistors

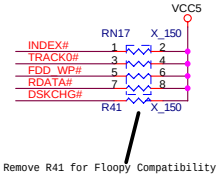


INIT signal voltage translation



FLOPPY CONNECTOR

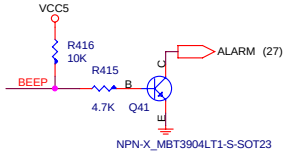




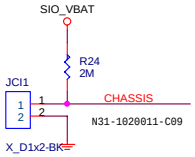
LPC I/O STRAPPING RESISTOR

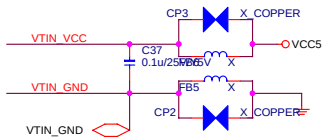
SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

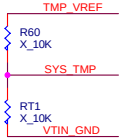
SPEAKER BLOCK



Chasiss Intrusion

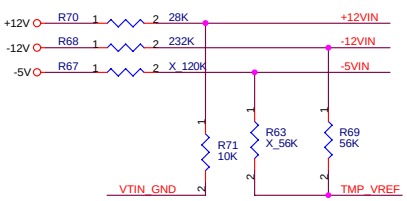






NOTE: LOCATE CLOSE STATUS PANEL

Thermal Resistor



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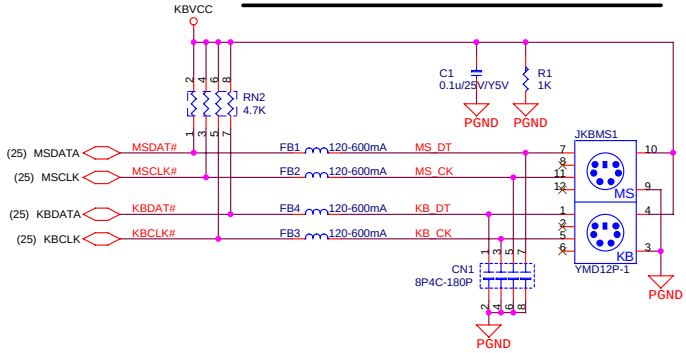
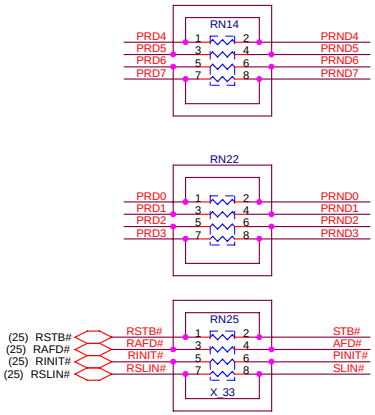
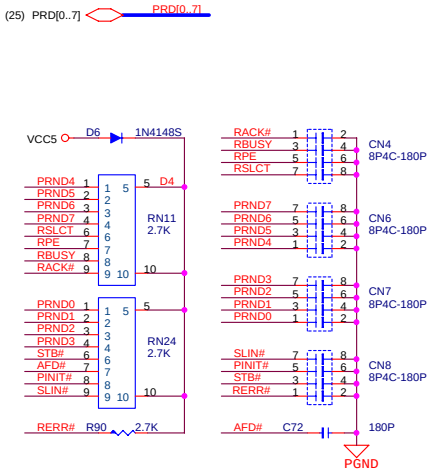
KB/MS/LPT/COM Port/FAN

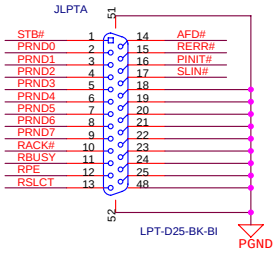
PS2 KEYBOARD & MOUSE CONNECTOR

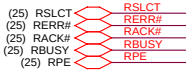


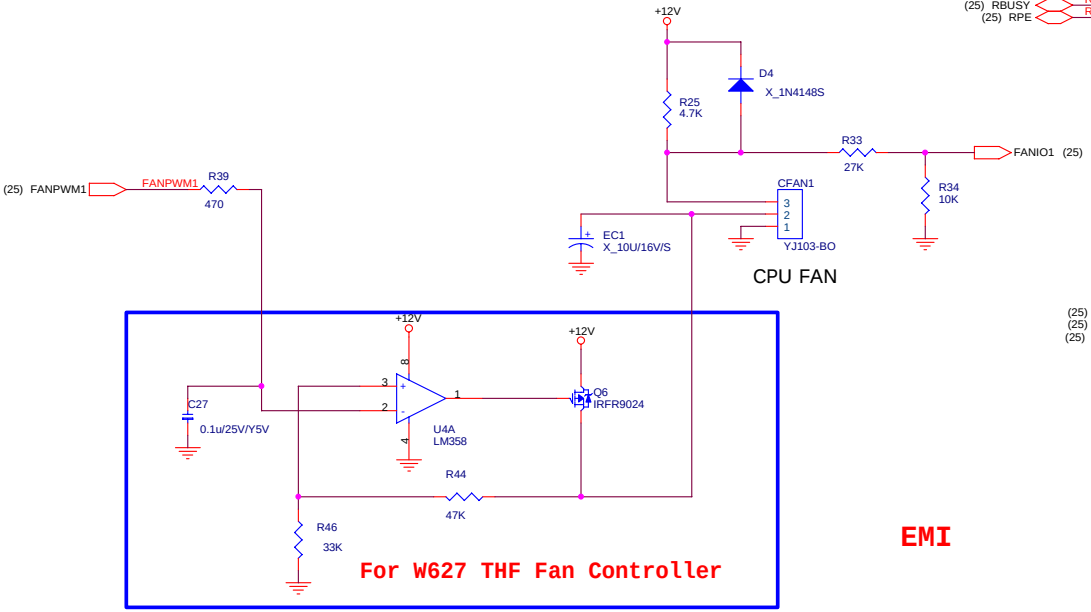




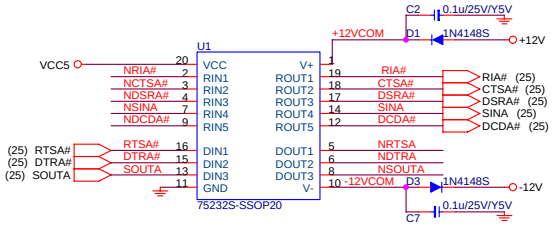
PARALLAL PORT



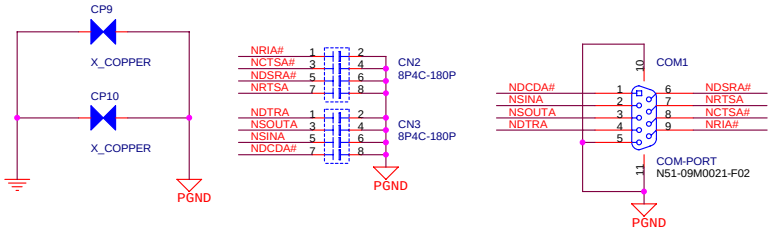




SERIAL PORT 1



EMI



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Title: KB/MS/LPT/COM Port/FAN		Rev: 1.0A
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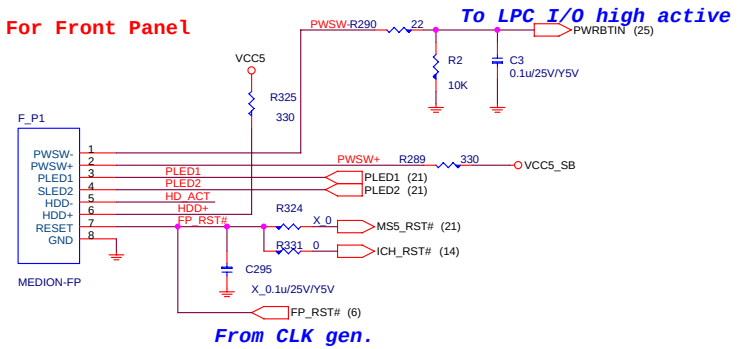
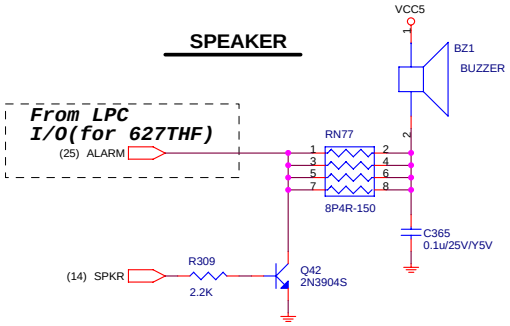
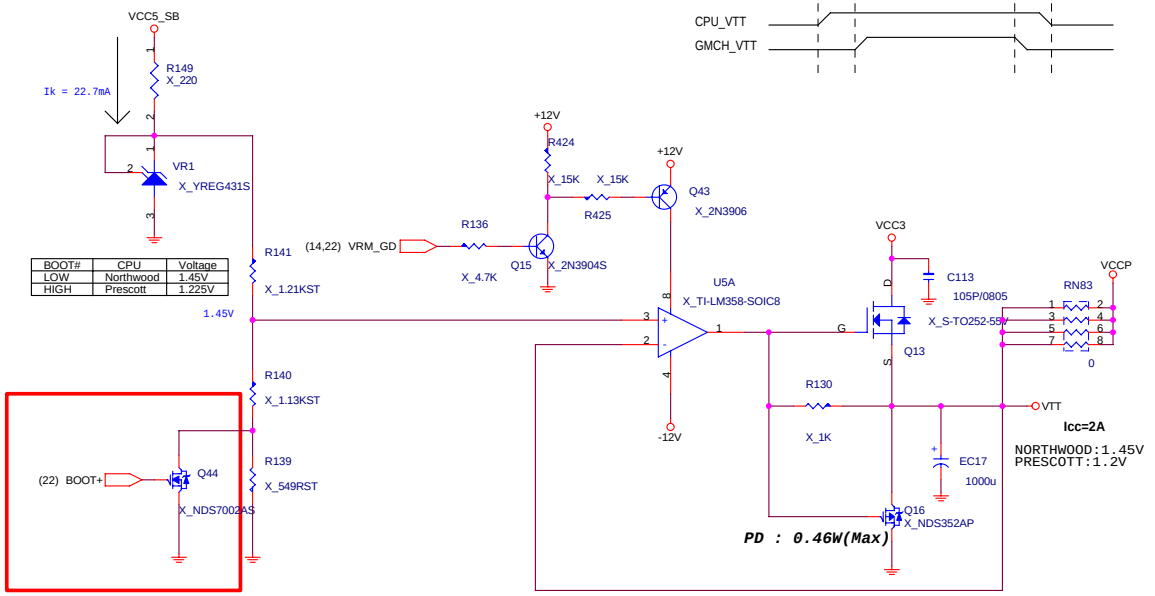
ATX connector / Front Panel



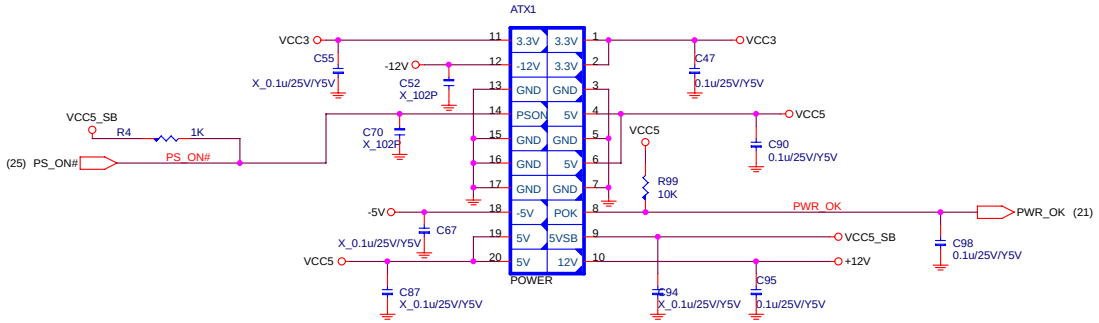
SPEAKER

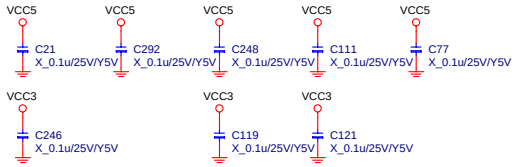


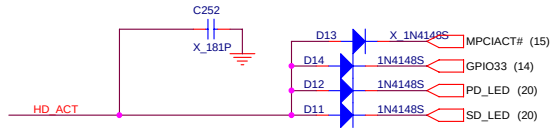
Intel reference GMCH VTT power cirucit



ATX Connector







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JAUDIO1(1-2),(3-4)

YJUMPER-MG JAUD1(5-6)

YJUMPER-MG JAUD1(9-10)

YJUMPER-MG JBAT1_1(1-2)

YJUMPER-MG JBIOS1(1)

BAT1_1

YSKTBT

P01-701210A-C48

PCB1

BIOS1_S

PLCC32-SMT

CPU1_B

P4-BRACKET

CPU1_S1

P4-SCREW

CPU1_S2

P4-SCREW

CPU1_S3

P4-SCREW

CPU1_S4

P4-SCREW

CPU1_S

P4-RM

Q50_1

X_MOS_Heatsink

Q46_1

MOS_Heatsink

R497(2-3)

0

R497(1-2)

0

U6_B
D1x3-BK

U6_C
X_D1x3-BK

U6_A
X_D1x3-BK

U6_D
D1x3-BK

U6_HS1

Q48_1

X_MOS_Heatsink

Q55_1

MOS_Heatsink

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Title *Manual Part*		Rev 1.0A
Document Number *MS-7012*		
MICRO-STAR INT'L CO.,LTD. No.69-1,Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Tuesday, August 26, 2003	
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00A to 00B Schematic change list		Page
1	Due to the vcore high side MOSFET burn down, the roo cause is the PWM pin17 interfere with noise. Phenomenon : the PWM gate waveform will vibrated Solution : the PWM pin 17 are isolated.	22
2	Due to thermal issue,i have to change placement to fix the DDR volatge(2.55V) control circuit too hot issue.	21
3	Due to EMI requirement, the EMI engineer will change placement with MS1.	16
4	Due to MEDION engineer requirement, the MIC pull-up power source change from AVDD5.	19
5		
6		
7		
8		
9		
10		

00B to 100 Schematic change list		Page
1	Due to circuit error, to modify usb port 6 and port 7 circuit.	24
2		
3		
4		
5		
6		
7		
8		
9		
10		

Micro Star Restricted Secret

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MICRO-STAR INT'L
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