System Board Specifications

CPU	Intel P54C - 75 /90 /100 /120 /133/150/166 MHz
Cache Memory	256K/512K/1MB cache with Asyn. SRAM 256K cache with Pipelined Burst SRAM option
Main Memory	Supports four memory banks using four 72-pin SIMM modules with 4M, 8M, 16M, 32M, and 64M FP / EDO DRAM Supports 32-bits DRAM memory operation
Slot	Three 32-bit PCI bus slots and Four 16-bit ISA bus slots in maximum combinations of: 4 ISA and 2 PCI, or 3 ISA and 3 PCI
On-Board Peripherals	PS/2 mouse option On-board SIS 6205 VGA chip with 1MB / 2MB Share System Memory architecture On-board peripherals include two serial port, one parallel port, FDC controller, and a 2-channel PCI IDE controller
Battery	3V on-board Lithium battery
Dimensions	28 cm x 22 cm x 4 layers
Mounting	7 mounting holes

System Board Layout

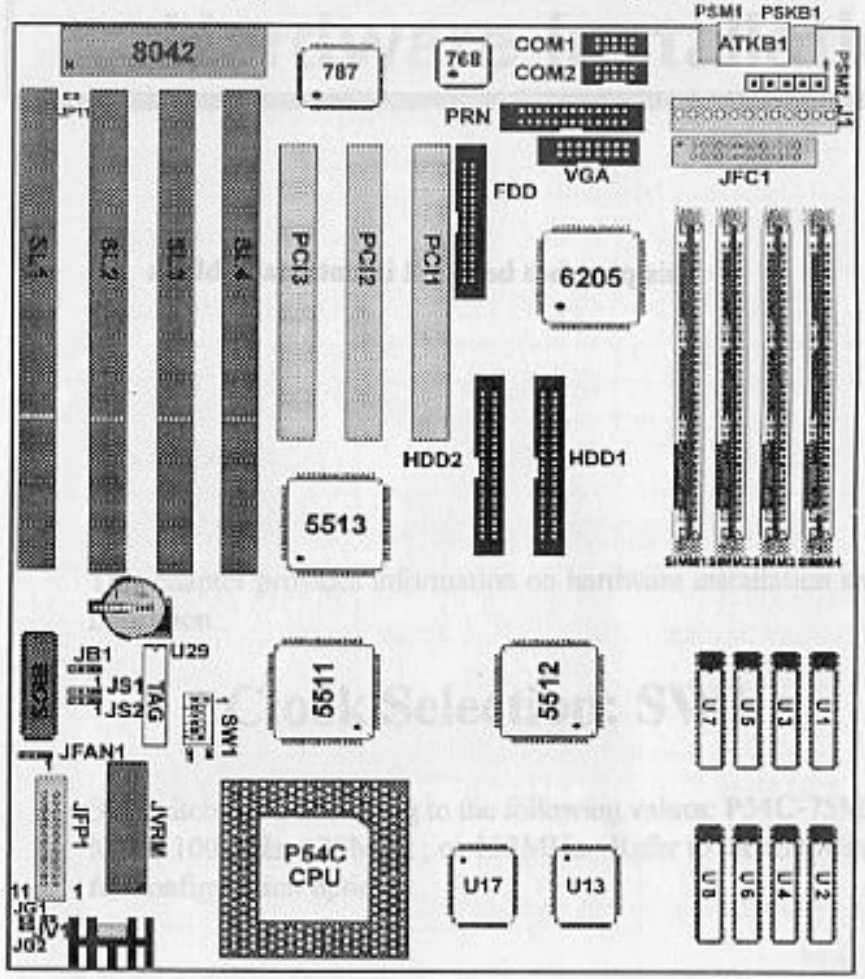

Figure 1-1: System Board Layout.

SW1 setting

CPU Internal Clock	SW1 1 2 3 (Int/Ext Ratio)	SW1 4 5 6 (External Clock)
75 MHz	O O O (1.5)	O S S (50MHz)
90 MHz	O O O (1.5)	O O S (60MHz)
100 MHz	O O O (1.5)	O O O (66MHz)
120 MHz	O S O (2)	O O S (60MHz)
133 MHz	O S O (2)	O O O (66MHz)
150 MHz	O S S (2.5)	O O S (60MHz)
166 MHz	O S S (2.5)	O O O (66MHz)
80 MHz (see note)	O O O (2)	S S S (40MHz)
120 MHz (see note)	S O O (3)	S S S (40MHz)

O ⇒ Open = *off* **S ⇒ Short** = *on*

Note! *The two settings are reserved for future M1 CPUs.*

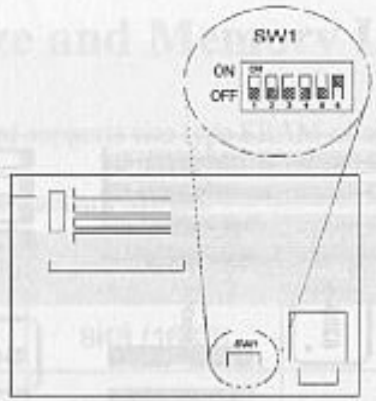

Figure 2-1 : SW1 Settings.

CPU Voltage Selector: JV1

For jumpers JV1 select either a 3.38 or 3.52 volt power source for the P54C.

CPU Voltage	JV1
3.38V	S
3.52V	O

O ⇒ Open

S ⇒ Short

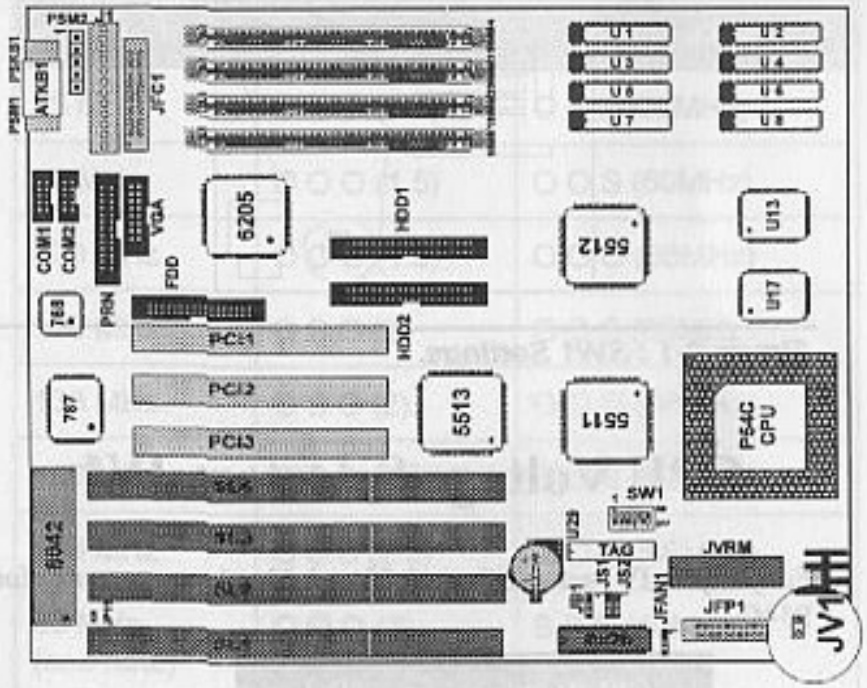

Figure 2-2 : CPU Voltage Selector JV1.

Cache Size and Memory Locations

The system board supports two type SRAM of cache memory.

1. Asynchronous standard SRAM

Cache Size	Tag RAM(U 29)	Data RAM(U1-U8)
256K	8K8 (16K8)	32K8
512K	16K8(128AK)	64K8
512K	16K8(129AK)	64K8
1M	32K8	128K8

2. Synchronous Pipelined Burst SRAM

Cache Size	Tag RAM(U 29)	DataRAM(U13,U17)
256K	8K8 (16K8)	32K32

Cache Selection: JS1, JS2

You can then set jumpers JS1 and JS2 as shown in the table below.

Cache Size	256K	512K (128AK)	512K (129AK)	1M
JS1	1-2	3-4	2-3	2-3
JS2	2-3	3-4	2-3	1-2

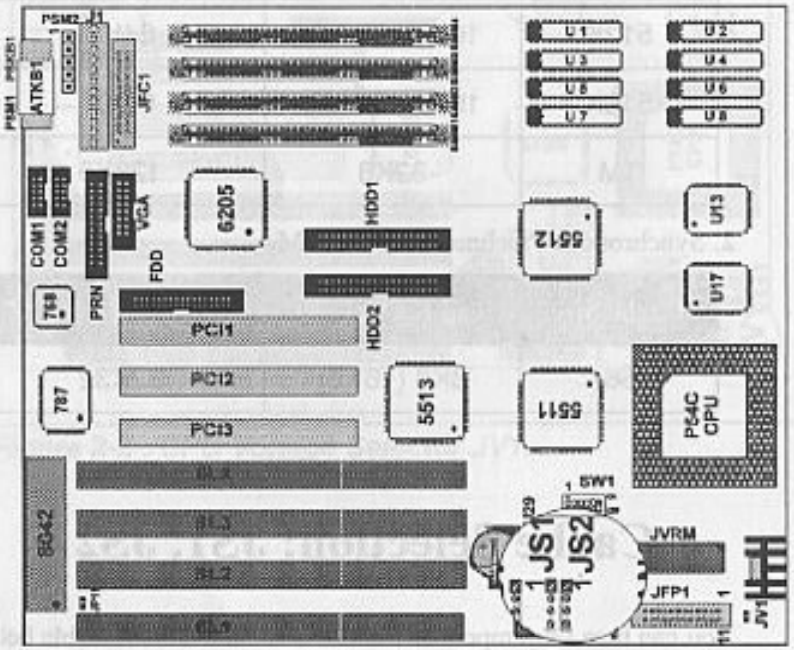

Figure 2-3: JS1 and JS2 Cache Size Settings.

Note! *All Asyn. Data SRAM used on the system board are special SRAM that use 5 volts for power input. However, all other I/O pins use 3.3 volts level for access interface.*

Suitable Asyn. *SRAM* include:

1. WINBOND W24M257AK-15 (32K8 mixed mode)
2. WINBOND W24M512AK-15 (64K8 mixed mode)
3. WINBOND W24M1024AK-15(128K8 mixed mode)

Tag *RAM* used below:

1. WINBOND W24128AK-15 (16K8)
2. WINBOND W24129AK-15 (16K8)
3. Aster AE88128AK-15 (16K8)
4. WINBOND W24257AK-15 (32K8)
5. WINBOND W24M257AK-15 (32K8)

Case Connector Block: JFP1

The Turbo LED, Turbo Switch, Hardware Reset, Keylock, Power LED, Power Saving Switch/LED, Speaker and HDD LED all connect to the JFP1 Connector Block as shown below. See figure 1-1 for JFP1's location.

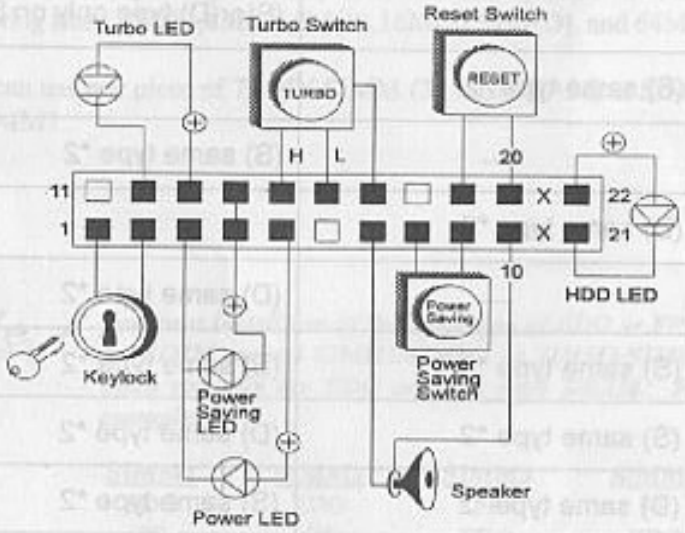

Figure 2-4: Case Connector Block - JFP1.

Note *The de-turbo function is not working now actually.*

Power Supply Connector: J 1

The power supply connector is a twelve-pin male connector. Dual connectors from the power supply can fit in only one direction. Make sure to attach the connectors with the two black wires at the center, as show in the diagram below. See Figure 1-1 for the connector's location.

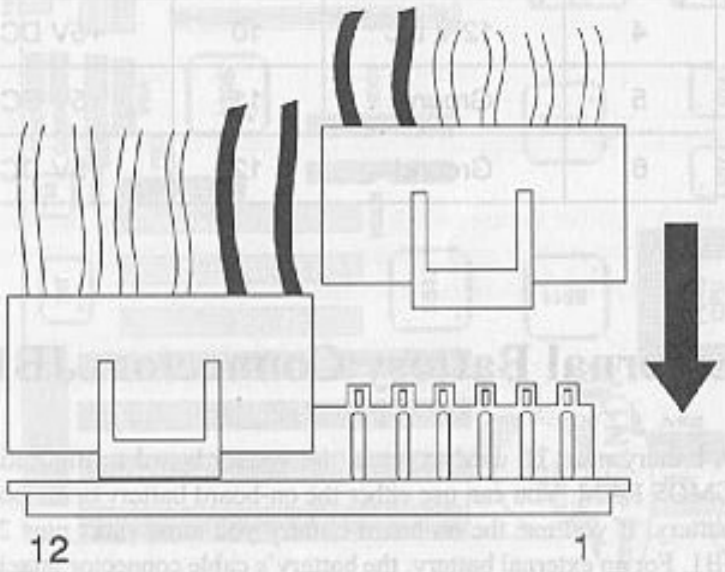

Figure 2-5: Attaching Power Supply Connectors.