Main memory:

- Supports four memory banks (two rows) using four 72-pin SIMM modules.
- Up to 128 Mbytes main memory.
- Supports EDO/Hyper Page Mode DRAM or Standard Fast Page mode DRAM.
- 4 Qword Deep Buffer for 3–1–1–1 Posted Write cycles. VRM Head Socket.

VRM Header Socket: (OPTIONAL)

- See page 14.

Slots:

- Three 32-bit Master PCI Bus slots and four 16-bit ISA bus slots.

On-Board Peripherals:

- On-board peripherals include
  - 1 floppy port supports 2 FDD
  - 2 serial ports
  - 1 parallel port supports ECP or EPP mode
  - 2 PCI Bus Master IDE ports (up to four IDE HDD)
    PIO Mode: mode 2, 3, 4
    DMA Mode: Single-word DMA Mode 2 or slower
               Multi-word DMA Mode 1
               Single word DMA Mode 2 or faster
               Multi-word DMA Mode 1 or faster
               Multi-word DMA Mode 2 or faster

Dimensions:

- 26 cm(L) x 22 cm(W) x 4 layer PCB

Mounting:

- 7 mounting holes

System Board Layout
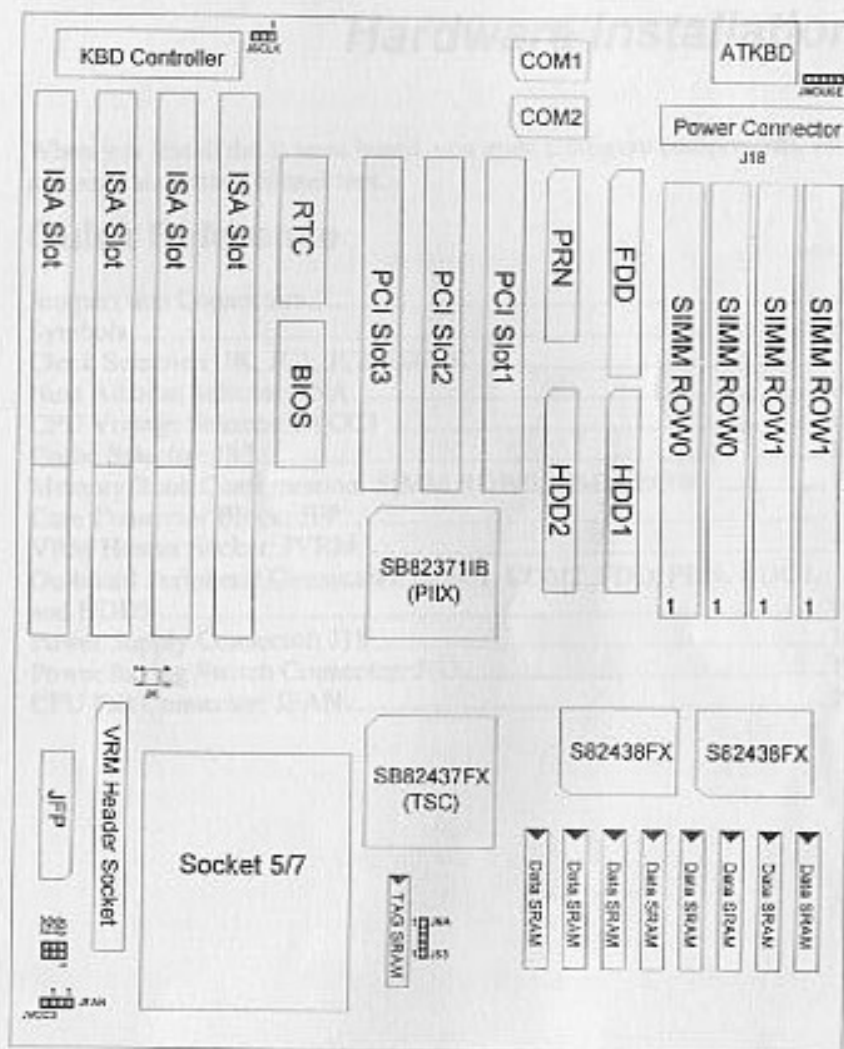
Figure 1-1. System board Layout

Jumpers and Connectors

Refer to Figure 1–1 for jumper and connector locations.

Jumpers Jumpers on the system board provide information to your operating system about installed options and system settings. You need to configure jumpers when you install the CPU, select cache size.

Connectors Connectors attach control panel switches and indicators, as well as the speaker, external battery, keyboard and power supply.
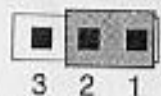
Setting Jumpers Configure system board options by setting jumper switches. Use your fingers to position a jumper cap over the desired pin setting and gently press down.
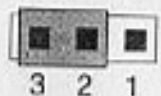
Note: *When you open a jumper, leave the plastic jumper cap attached to one of the pins so you don't lose it.*

Symbols:

For 3-pin jumpers, the following symbols are used:

— Close pins 1 and 2 with a jumper cap.

— Close pins 2 and 3 with a jumper cap.

For 2-pin jumpers, the following symbols are used:

— Close the jumper by inserting the jumper cap over the two pins of the jumper.

— Open the jumper by inserting the jumper cap over one or neither of the pins of the jumper.

Clock Selection: JK, JC2, JC1, JSCLK

Set jumper JK, JC2, JC1, and JSCLK according to the Pentium — 75MHz, 90MHz, 100MHz, 120MHz, or 133MHz. See Figure 1–1 for the jumper's location.

JK, JC2, JC1, JSCLK Settings

CPU Speed	JK Note 1	JC2 Note 2	JC1 Note 2	JSCLK Note 3
75 MHz				
90 MHz				
100 MHz				
120 MHz				
133 MHz				

Note1: *The 3 Host Clock frequencies that the system supports are 50MHz, 60MHz, and 66.6 MHz. See the following chart to set the jumper JK for the different Host Clock frequencies.*

JK	Host Clock Frequency
2 ▦ ▦ 4 / 1 ▦ ▦ 3	50 MHz
2 ▦ ▦ 4 / 1 ▦ ▦ 3	60 MHz
2 ▦ ▦ 4 / 1 ▦ ▦ 3	66.6 MHz

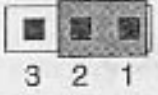Note 2   The jumpers JC2 and JC1 set the Bus/Core (Fraction) ration of the CPU. See below.

JC2	JC1	Bus/Core ratio	
		Previous P54C/CQS/CS	New P54CS POR (C-step)
▦ ▦	▦ ▦	2/3	2/3
▦ ▦	▦ ▦	1/2	1/2
▦ ▦	▦ ▦	1/3	1/3
▦ ▦	▦ ▦	1/4	2/5

The actual core speed of CPU is the Host Clock frequency multiply by Core/Bus ratio. For example, if the Host Clock frequency is 66.6 MHz and the Core/Bus ratio is 3/2, the Actual CPU core speed will be 66.6 x 3/2 = 100 MHz.

The system has reserved space for future usage of 150/60MHz and 180/60 MHz CPU. The Host Clock frequency is 60MHz and Bus/core ratio is 2/5 for the 150/60 MHz CPU, and, the Host Clock frequency is 60MHz and Bus/core ratio is 1/3 for the 180/60 MHz CPU.

Note 3   The PCI Bus Clock is the Host Clock Frequency divided by 2 and the ISA Bus Clock is the PCI Bus clock divided by 3 or 4. We recommend that the ISA Bus Clock is the PCI Bus Clock divided by 3 when the Host Clock frequency is 50 MHz and divided by 4 when the Host Clock frequency is 60 MHz or 66.6 MHz. The jumper JSCLK is to set the PCI Bus Clock either divided by 3 or 4 for the ISA Bus Clock.

JSCLK	
▦ ▦ ▦ / 3 2 1	PCI Bus Clock divided by 3
3 2 1 / ▦ ▦ ▦	PCI Bus Clock divided by 4

Next Address Selector: JNA

Jumper JP1 Enables/Disables NA#. See Figure 1-1 for the location of the jumper.

JNA Settings

Description	JNA
Disable NA# (Default)	
Enable NA#	

CPU Voltage Selector: JVCC3

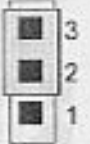Jumper JVCC3 selects a 3.4V/3.5V voltage power source for P54C. See figure 1-1 for the location of the jumper.

JVCC3 Settings

CPU Voltage	JVCC3
3.4V	
3.5V	

Cache Selection: JS3

The system board supports 256K or 512K of cache memory. You configure cache memory by installing 32K8 or 64K8 SRAM chips in Data RAM sockets U3, U4, U5, U7, U8, U9, U13, and U14, and a 8K8, or 16K8 SRAM chip in Tag socket U20. You then set jumpers JS3 as below.

JS3 Setting

Cache Size	256K	512K
JS3		

Note: All SRAM used on the system board are special SRAM that utilize 5 volts for power input. However, all other I/O pins use 3.3 volts when accessing the interface. Suitable SRAM includes:

        32Kx8 SRAM: Winbond W24M257AK-15
        64Kx8 SRAM: Winbond W24M512AK-15

Note: The Data SRAM sockets are 32pin, 300mil, DIP socket, but 32Kx8 SRAM is 28pin DIP chip. Therefore, you need to put the first pin of the 28pin Data SRAM chip into the position shown in the following drawing.
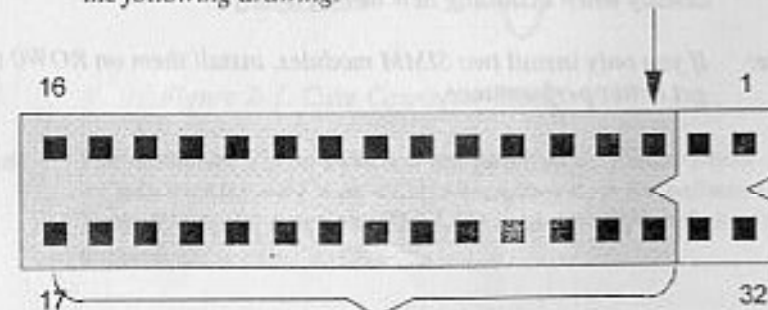
for 32Kx8 SRAM location

Memory Bank Configuration

The system board supports two rows, four memory banks (i.e., two banks per row) and provides four 72-pin Single In-line Memory Module (SIMM) sockets on-board. Each row accepts single density or double density banks in the following sizes: 4M, 8M, 16M, and 32M.

Note: Make sure the SIMMs are of the same type with equal size and density when installing new memory.

Note: If you only install two SIMM modules, install them on ROW0 to get better performance.

Case Connector Block: JFP

The Turbo LED, Turbo Switch, Hardware Reset, Keylock, Power LED, Power Saving LED, Sleep Switch, Speaker and HDD LED all connect to the JFP Connector Block as shown below. See Figure 1-1 for JFP's location.
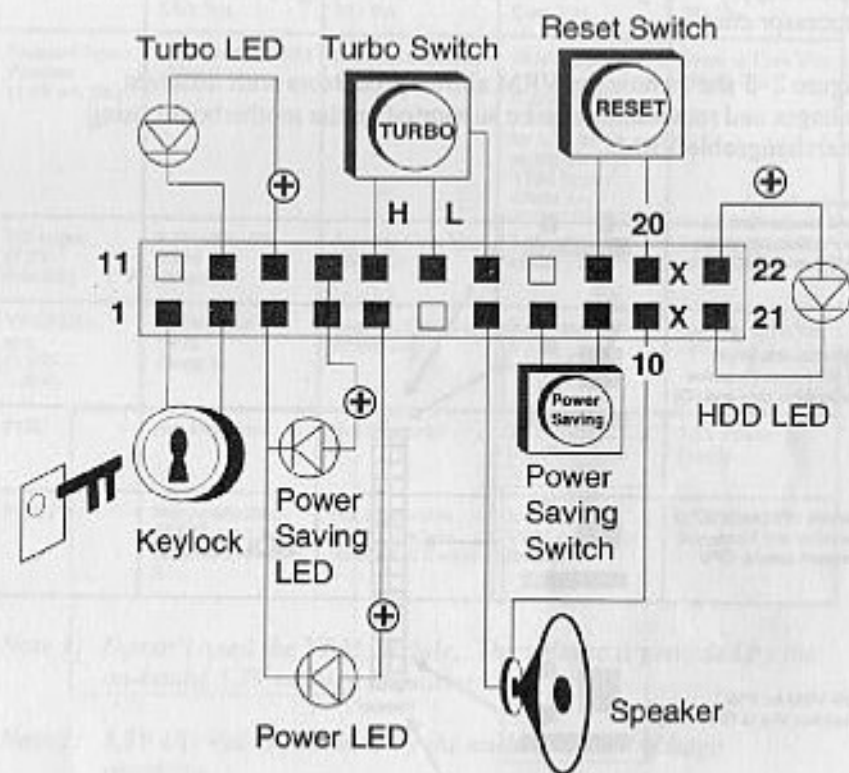

Figure 2-1. Case Connector Block – JFP

Note   The hardware Turbo switch is not functional. Please press
<Ctrl>+<Alt>+<+> or <Ctrl>+<Alt>+<–> for software
Turbo/De-turbo function. The LED is always ON and cannot be
toggled.