

HP Consumer Support

Motherboard layout and jumper settings for the 440LX chipset models 8275, 8276, 8280

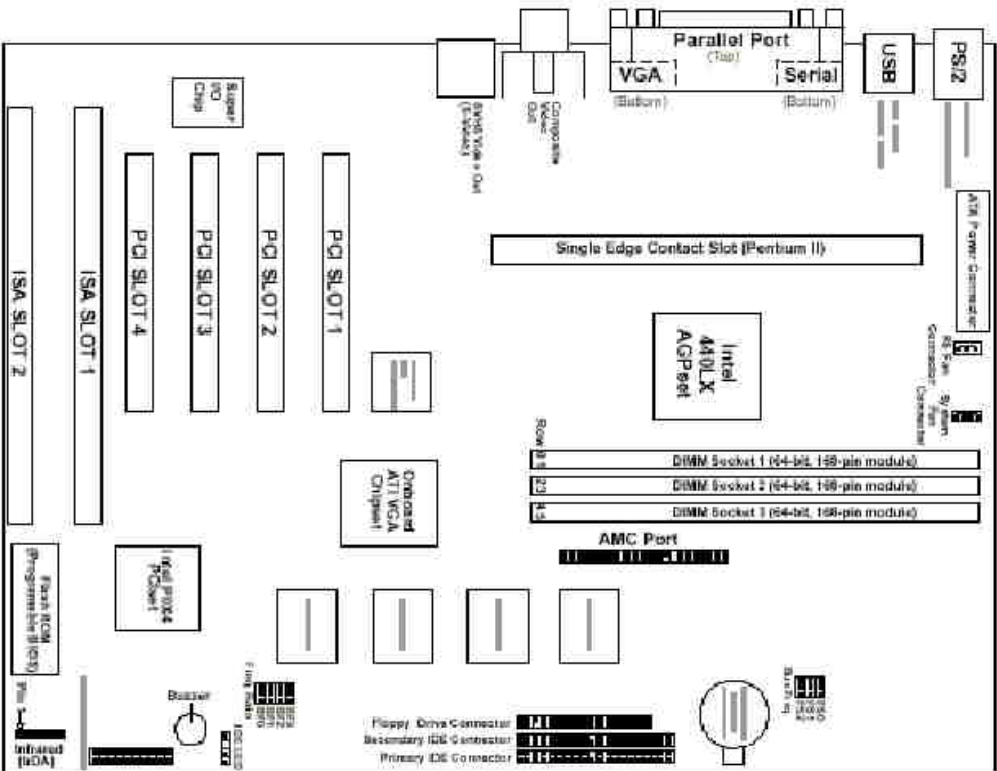
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System Board Layout

Figure 1: System Board

The system board has the following major components:



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CPU Frequency

Figure 2: Frequency ratio and Jumper locations

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Product (e.g. Deskjet D2680)

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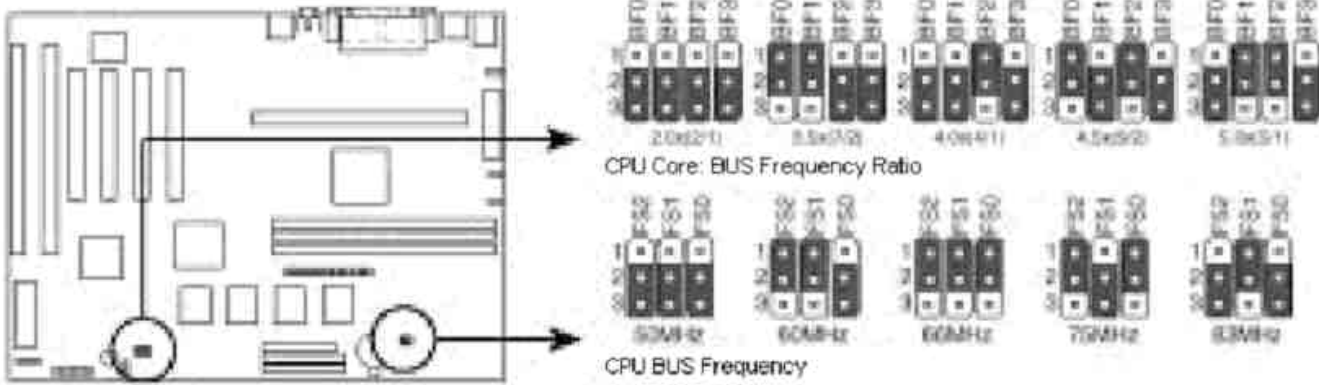
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CPU Frequency and Frequency Ratio Jumper Locations and Settings

CPU Freq. (MHz)	Ratio	BUS Freq. (MHz)	FS0	FS1	FS2	BF0	BF1	BF2	BF3
333	5.0x	66	1-2	1-2	1-2	2-3	1-2	1-2	2-3
300	4.5x	66	1-2	1-2	1-2	1-2	2-3	1-2	2-3
266	4.0x	66	1-2	1-2	1-2	2-3	2-3	1-2	2-3
233	3.5x	66	1-2	1-2	1-2	1-2	1-2	2-3	2-3

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Power Supply/System Fan Connectors

Figure 3: Power supply and system fan connectors

POWER SUPPLY FAN CONNECTOR

Pin	Signal Name
1	Ground
2	+12 V
3	Ground

Power Supply Fan Connector

SYSTEM FAN CONNECTOR

Pin	Signal Name
1	+12 V
2	Ground
3	FAN_SEN

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Front Panel Connector

The front panel connector includes headers for the following connections; Power

LED, Speaker, Reset switch, Power switch, Sleep switch.

Figure 4: Front panel connector

<i>Pin</i>	<i>Signal Name</i>	<i>Connector</i>
1	no connection	-
2	+5V	Message LED
3	MSG LED	
4	SMI	SMI Suspend Switch Lead
5	ground	
6	PWR SW	ATX Power Switch
7	ground	
8	no connection	-
9	RESET	Reset Switch
10	ground	
11	SPKR	Speaker
12	ground - not used	
13	ground - not used	
14	+5V	Connection
15	no connection	
16	no connection	
17	no connection	
18	PWR LED	Power
19	no connection	
20	+5V	LED

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Back Panel I/O Connectors

Figure 5: Back panel I/O connectors

<i>Pin</i>	<i>Signal Name</i>
1	Data
2	No Connect
3	Ground
4	+5 Vcc (fused)
5	Clock
6	No Connect

PS/2 Keyboard and Mouse Ports

USB CONNECTORS (USB 0 AND USB 1)

<i>Pin</i>	<i>Signal Name</i>
1	Power
2	USBP0# (USBP1#)
3	USBP0 (USBP1)
4	Ground

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Parallel Port

Figure 6: Parallel port

<i>Signal Name</i>	<i>Pin</i>	<i>Pin</i>	<i>Signal Name</i>
STROBE-	1	14	AUTO FEED
Data Bit 0	2	15	ERROR*
Data Bit 1	3	16	INIT*
Data Bit 2	4	17	SELECT IN*
Data Bit 3	5	18	Ground
Data Bit 4	6	19	Ground
Data Bit 5	7	20	Ground
Data Bit 6	8	21	Ground
Data Bit 7	9	22	Ground
ACK*	10	23	Ground
BUSY	11	24	Ground
Error	12	25	Ground
SELECT	13		

Figure 7: Parallel port

<i>Signal Name</i>	<i>Pin</i>	<i>Pin</i>	<i>Signal Name</i>
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Signal Name	Pin	Pin	Signal Name
Reset IDE	1	2	Ground
Host Data 7	3	4	Host Data 8
Host Data 6	5	6	Host Data 9
Host Data 5	7	8	Host Data 10
Host Data 4	9	10	Host Data 11
Host Data 3	11	12	Host Data 12
Host Data 2	13	14	Host Data 13
Host Data 1	15	16	Host Data 14
Host Data 0	17	18	Host Data 15
Ground	19	20	Key
DDRQ0(DDRQ1)	21	22	Ground
I/O Write	23	24	Ground
I/O Read	25	26	Ground
IORDY	27	28	Vcc pull-up
DDACK0(DDACK1)	29	30	Ground
IRQ14(IRQ15)	31	32	Reserved
Addr 1	33	34	Reserved
Addr 0	35	32	Addr 2
Chip Select 1P(1S)	37	38	Chip Select 3P (3S)
Activity	39	40	Ground

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Floppy Connector

Figure 8: Floppy connector

Signal Name	Pin	Pin	Signal Name
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Signal Name	Pin	Pin	Signal Name
Ground	1	2	DENSEL
Ground	3	4	Reserved
Key	5	6	FDEDIN
Ground	7	8	Index
Ground	9	10	Motor Enable A
Ground	11	12	Drive Select B
Ground	13	14	Drive Select A
Ground	15	16	Motor Enable B
MSEN1	17	18	DIR
Ground	19	20	STEP
Ground	21	22	Write Data
Ground	23	24	Write Enable
Ground	25	26	Track 00
MSEN0	27	28	Write Protect
Ground	29	30	Read Data
Ground	31	32	Side 1 Select
Ground	33	34	Diskette Change

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