Gator 550-G

Motherboard
Installation Guide

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First Edition.

Introduction

Thank you for your purchase of the Gator 550-G industrial embedded motherboard. The Gator 550-G design was based on the SiS550 SoC (System on Chip) providing the ideal platform to industrial low power applications.

With proper installation and maintenance, your Gator 550-G will provide years of high performance and trouble free operation.

This manual provides a detailed explanation into the installation and use of the Gator 550-G industrial embedded motherboard. This manual is written for the novice PC user/installer. However, as with any major computer component installation, previous experience is helpful and should you not have prior experience, it would be prudent to have someone assist you in the installation. This manual is broken down into 3 chapters and 4 appendixes.

Chapter 1 - System Board Pre-Configuration

This chapter provides all the necessary information for installing the Gator 550-G. Topics discussed include: installing the DRAM, jumper settings and connecting all the cables from the system board to the chassis and peripherals.

Chapter 2 - BIOS Configuration

This chapter shows the final step in getting your system firmware setup.

Chapter 3 - Upgrading

The Gator 550-G provides expansion options for the memory. All aspects of the upgrade possibilities are covered.

Appendix A - Technical Specifications

A complete listing of all the major technical specifications of the Gator 550-G is provided.

Appendix B - Flash BIOS Programming (optional)

Provides all the information necessary to program your optional AMIBIOS Flash BIOS.

Appendix C – On-board Video Controller

On-board CRT, LCD and LVDS (optional) video controller.

Appendix D - On-Board Industrial Devices

One on-board 10/100 Ethernet and four serial ports (one optional RS422/485).

Static Electricity Warning!

The Gator 550-G has been designed as rugged as possible but can still be damaged if jarred sharply or struck. Handle the motherboard with care.
The Gator 550-G also contains delicate electronic circuits that can be damaged or weakened by static electricity. Before removing the Gator 550-G from its protective packaging, it is strongly recommended that you use a grounding wrist strap. The grounding strap will safely discharge any static electricity build up in your body and will avoid damaging the motherboard. Do not walk across a carpet or linoleum floor with the bare board in hand.

Warranty

This product is warranted against material and manufacturing defects for two years from the date of delivery. Buyer agrees that if this product proves defective the manufacturer is only obligated to repair, replace or refund the purchase price of this product at manufacturer's discretion. The warranty is void if the product has been subjected to alteration, misuse or abuse; if any repairs have been attempted by anyone other than the manufacturer; or if failure is caused by accident, acts of God, or other causes beyond the manufacturer's control.

Gator 550-G - An Overview

The Gator 550-G represents the ultimate in industrial embedded motherboard technology. No other system board available today provides such impressive list of features:

SiS550 Overview

- The single chipset, SiS550 family, provides a high performance/low cost SoC (System on Chip) solution by integrating an x86 compatible processor (200MHz), high performance North Bridge, advanced hardware GUI engine and Super-South bridge.

Memory

- One μDIMM socket up to 256MB SDRAM, PC100/133.

On-Board I/O

- 1 Floppy up to 2.88 MB.
- Single channel PCI 32-bit EIDE controller - UDMA 33/66/100 supported.
- Four high speed RS-232 serial ports 16 Bytes FIFO (16550) (COM3 optional RS422/485) (COM2 optional RS-232 IrDA).
- One bidirectional parallel port. SPP mode compatible.
- One mouse and one keyboard interface.
- Two Universal Serial Bus interfaces.
- One PC104+ interface.
- One Ethernet interface.
- Power Button – advanced management support.
- Audio AC97 compliant. Microphone In, Stereo Line In, CD In, headphone Out.

ROM BIOS

- AMI BIOS™ BIOS HIFLEX with optional FLASH ROM

On-Board CRT & LVDS video controller

- Standard CRT video controller .
- Standard LCD interface.
- Dedicated Local Flat Panel (LFP) LVDS interface (optional).

On-Board Ethernet

- On-board 10/100 Ethernet.

Conventions Used in this Manual

Notes - Such as a brief discussion of memory types.

Important Information - such as static warnings, or very important instructions.

When instructed to enter keyboard keystrokes, the text will be noted by this graphic.

Chapter 1 Pre-Configuration

This chapter provides all the necessary information for installing the Gator 550-G. Topics discussed include: installing the DRAM and jumper settings.

Handling Precautions

The Gator 550-G has been designed to be as rugged as possible but it can be damaged if dropped, jarred sharply or struck. Damage may also occur by using excessive force in performing certain installation procedures such as forcing the system board into the chassis or placing too much torque on a mounting screw.

Take special care when installing or removing the system memory DIMM. Never force a DIMM into a socket. Screwdrivers slipping off a screw and scraping the board can break a trace or component leads, rendering the board unusable. Always handle the Gator 550-G with care.

Special Warranty Note:

Products returned for warranty repair will be inspected for damage caused by improper installation and misuse as described in the previous section and the static warning below. Should the board show signs of abuse, the warranty will become void and the customer will be billed for all repairs and shipping and handling costs.

Static Warning

The Gator 550-G contains delicate electronic semiconductors that are highly sensitive to static electricity. These components, if subjected to a static electricity discharge, can be weakened thereby reducing the serviceable life of the system board. BEFORE THE BOARD IS REMOVED FROM ITS PROTECTIVE ANTISTATIC PACKAGING,

TAKE PROPER PRECAUTIONS! Work on a conductive surface that is connected to the ground. Before touching any electronic device, ground yourself by touching an unpainted metal object or, and highly recommended, use a grounding strap.

Step 1 Setting the Jumpers

Your Gator 550-G is equipped with a large number of peripherals and has the ability to run at a variety of speeds without the need to change any crystals or oscillators (Speeds can be set in the BIOS, the maximum core speed is determined by the SoC installed). As such, there are a large number of configuration jumpers on the board. Taken step by step, setting these jumpers is easy. We suggest you review each section and follow the instructions.

Jumper Types

Jumpers are small copper pins attached to the system board. Covering two pins with a shunt closes the connection between them. The Gator 550-G examines these jumpers to determine specific configuration information. There are three different categories of jumpers on the Gator 550-G.

A. Two pin jumpers are used for binary selections such as enable, disable. Instructions for this type of jumper are open, for no shunt over the pins or closed, when the shunt covers the pins.

B. Three or four pin jumpers are used for multiple selections. Instructions for these jumpers will indicate which two pins to cover. For example: for JP*x* 2-3 the shunt will be covering pins 2 and 3 leaving pins 1 and 4 exposed.

C. Grouped jumpers are used when a certain function has multiple selections. There are two grouped jumpers on the board and careful attention should be given when setting these jumpers. Instructions for grouped jumpers are similar to those above.

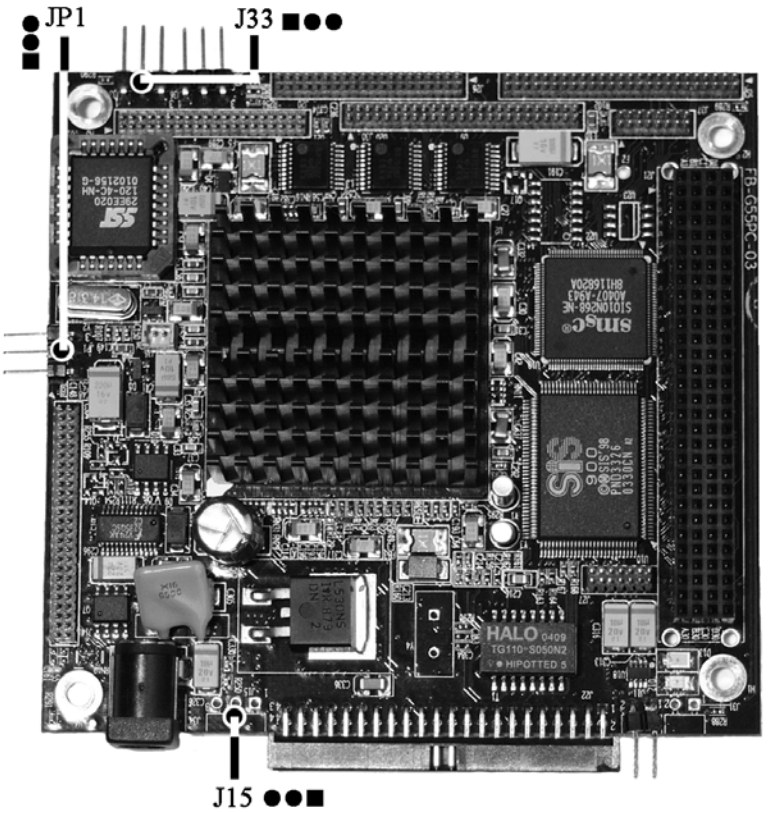
How to identify pin number 1 on *Figure 1-1*: Looking to the solder side (The board side without components) of the PCB (Printed Circuit Board), pin number 1 will have a squared pad ■. Other pins will have a circular pad ●. They are numbered sequentially.

Double row jumpers are numbered alternately, i.e. pin number 2 is in the other row, but in the same column of pin number 1. Pin number 3 is in the same row of pin 1, but in the next column and so forth.

Jumper Locations

Use the diagram below and the tables on the following pages to locate and set the on-board configuration jumpers.

Figure 1-1 Jumper Locations



CMOS Reset

This option is provided as a convenience for those who need to reset the CMOS registers. It should always be set to "Normal" for standard operation. If the CMOS needs to be reset, turn off the system, move JP33 to 2-3, turn the system on, move jumper to 1-2 and press reset.

Table 1-1 CMOS Reset

Reset CMOS	Normal	Clear CMOS
JP33	1-2*	2-3

** Manufacturer's Settings.*

ATA-Disk Connector Voltage Selection

The ATA-Disk Connector J22 can provide either 5Vcc or 3.3Vcc. The jumper JP1 selects the voltage.

Table 1-2 ATA-Disk Connector Voltage Select

ATA-Disk Voltage	5Vcc	3.3Vcc
JP1	1-2*	2-3

**Manufacturer's Settings.*

LCD Power Voltage Selection

The LCD Connector J14 can provide either 5Vcc or 3.3Vcc to the LCD panel. The jumper J15 selects the voltage.

Table 1-3 LCD VDD Power Voltage Select

LCD Voltage	3.3Vcc	5Vcc
J15	1-2*	2-3

**Manufacturer's Settings.*

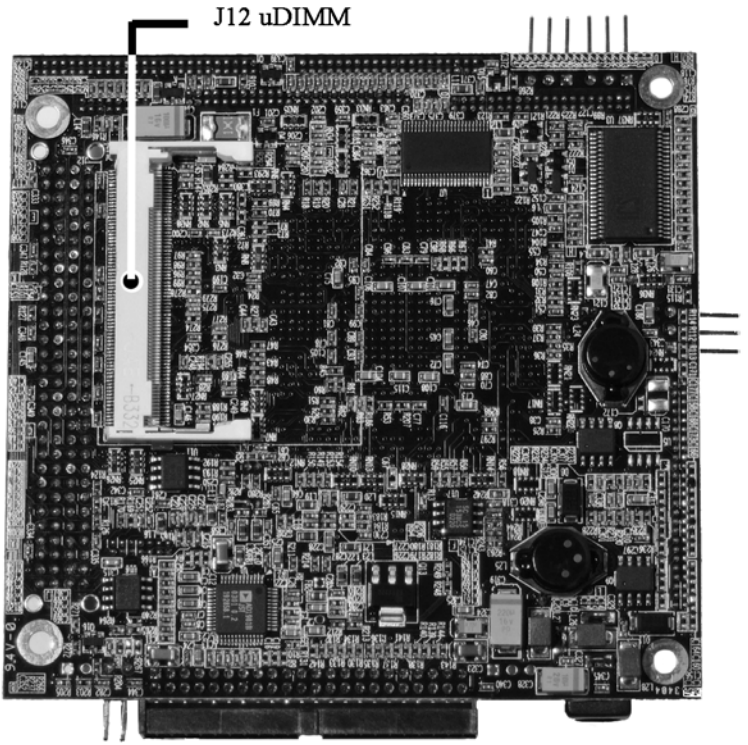
Step 2 DRAM and Cables Installation

Depending upon how your Gator 550-G is configured you may need to install the µDIMM.

Gator 550-G Memory Configuration

The Gator 550-G offers 1 µDIMM memory socket (Location J12 - Back side or solder side– *Figure 1-2*). It can be configured with 3.3V unbuffered SDRAM module. It is very important that the quality of the DIMM is good. Unreliable operation of the system may result if poor quality DIMMs are used. Always purchase your memory from a reliable source. Please, refer to chapter 3 for memory details.

Figure 1-2 µDIMM Location (Solder Side)



Installing Cables

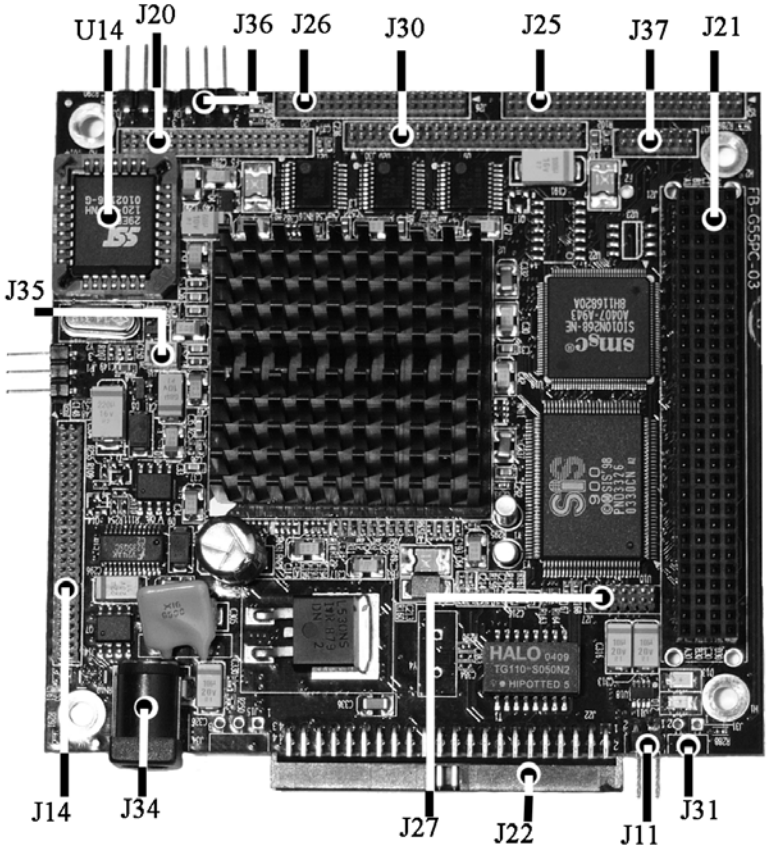
Power and Control Panel Cables

The Gator 550-G gets power from the power connector J34 (*Figure 1-3*).

Installing Peripheral Cables

Connect the combined flat cables to their connectors and to the other end. This concludes the hardware installation of your Gator 550-G system. Now it is a good time to re-check all of the cable connections to make sure they are correct.

Figure 1-3 Location of Components and Connectors



Index of Connectors

Please refer to Appendix A for pin-out descriptions.

Table 1-4 Connectors descriptions

Connector	Description
J11	Reset
J12	µDIMM Slot (Back side)
J14	LCD Panel
J20	LVDS Panel
J21	PC104+
J22	IDE 44pin
J25	Combined FDD/USB/COM4/IrDA
J26	Combined COM1/COM2/COM3/Audio
J27	Ethernet 10/100
J30	Combined VGA/Keyboard/Mouse/LPT
J31	Power Button
J34	Power +12Vcc
J35	RTC Battery
J36	LVDS Backlight
J37	LPC
U14	BIOS Socket

User's Notes:

User's Notes:

Chapter 2 HIFLEX BIOS Setup

Your Gator 550-G features AMI BIOS. The system configuration parameters are set via the HIFLEX AMIBIOS setup. Since HIFLEX BIOS Setup resides in the ROM BIOS, it is available each time the computer is turned on.

Starting BIOS Setup

As POST executes, the following appears:

```
Hit <DEL> if you want to run SETUP
```

Using the Keyboard with BIOS Setup

The BIOS Setup has a built-in keyboard driver that uses simple keystroke combinations:

Keystroke	Function
<Tab>	Move to the next window or field.
, , ,	Move to the next field to the right, left, above, or below.
<Enter>	Select in the current field.
+	Increments a value.
-	Decrements a value.
<Esc>	Closes the current operation and return to previous level.
<PgUp>	Returns to the previous page.
<PgDn>	Advances to the next page.
<Home>	Returns to the beginning of the text.
<End>	Advances to the end of the text.
<Alt> <H>	Access a help window.
<Alt> <Spacebar>	Exit WINBIOS Setup.
Alphabetic keys	A to Z are used in the Virtual Keyboard, and are not case-sensitive.
Numeric keys	0 to 9 are used in the Virtual Keyboard and Numeric Keypad.

BIOS Setup Main Menu

The BIOS Setup main menu is organized into 13 windows. Each window is discussed in this chapter.

Each window contains several options. Clicking on each option activates a specific function. The BIOS Setup options and

functions are described in this chapter. Some options may not be available in your BIOS. The windows are:

- Standard CMOS Setup
- Advanced CMOS Setup
- Advanced Chipset Setting
- Power Management Setup
- PCI/Plug and Play Setup
- Peripheral Setup
- Auto-Detect Hard Drive
- Change User Password
- Change Supervisor Password
- Auto Configuration with Optimal Settings
- Auto Configuration with Fail Safe Settings
- Save Settings and Exit
- Exit Without Saving

Standard Setup

Standard Setup options are displayed by choosing Standard option from the HIFLEX BIOS Setup menu. All Standard Setup options are described below.

Date/Time

Select the Date/Time option to change the date or time. The current date and time are displayed. Enter new values through the displayed window.

Floppy Drive A

Choose Floppy Drive A to specify the floppy drive type. The settings are *360 KB 5¼"*, *1.2 MB 5¼"*, *720 KB 3½"*, *1.44 MB 3½"* and *2.88 MB 3½"*.

Pri Master ***Pri Slave***

Select one of these options to configure the hard disk drive. Select Auto from the drive parameters screen to let AMIBIOS automatically configure the drive. Choose the desired option to

configure the drive. Auto will automatically detect your hard drive every time the computer boots. If required, a specific Hard Drive type may be selected.

Boot Sector Virus Protection

The options are either Enabled or Disabled.

Advanced CMOS Setup

Advanced CMOS Setup options are displayed by choosing the Advanced CMOS Setup option from the AMIBIOS Setup main menu. All Advanced CMOS Setup options are described in this section.

Event Log Capacity

Event Log Validity

View DMI Event Log

Press <enter> to select.

Clear All DMI Event Logs

Yes/No.

Event Logging

Enable/Disable.

Mark DMI Events Read

Yes/No.

Quick Boot

Set this option to Enabled to instruct AMIBIOS to boot quickly when the computer is powered on. This option replaces the old

Above 1 MB Memory Test Advanced Setup option. The settings are: Enabled and Disabled.

Pri Master ARMD Emulated as
Pri Slave ARMD Emulated as

If set to Auto, the default emulation depends on ARMD drive. The default emulation type is floppy for LS120, hard drive for MO and hard drive for ZIP drives.

1st Boot Device
2nd Boot Device
3rd Boot Device
4th Boot Device

These options set the drive boot sequence that Gator 550-G attempts to boot from after AMIBIOS POST completes. The settings are Disabled, 1st IDE, 2nd IDE, 3rd IDE, 4th IDE, Floppy, ARMD-FDD, ARMD-HDD, ATAPI-CDROM, SCSI, Network and I2O. The default is:

1st Boot Device - Floppy
2nd Boot Device - 1st IDE-HDD
3rd Boot Device - ATAPI-CDROM
4th Boot Device - Disabled

Try Other Boot Devices

Set this option to Yes (*default*) to instruct AMIBIOS to attempt to boot from any other drive in the system if it cannot find a boot drive among the drives specified in the 1st, 2nd, 3rd and 4th Boot Device options.

Initial Display Mode

Set this option to BIOS (*default*) to obtain the normal boot-up screen. Set to Silent to obtain the customized graphic boot-up screen.

Display Mode At

Add-On ROM Display Mode

Set this option to display add-on ROM (read-only memory) messages. The Optimal and Fail-Safe default setting is *Force BIOS*. An example of this is a SCSI BIOS or VGA BIOS.

Force BIOS Set this value to allow the computer system to force a third party BIOS to display during system boot. This is the default setting.

Keep Current Set this value to allow the computer system to display the ezPORT information during system boot.

Floppy Access Control

This option selects usage right from the floppy drive. The setting is either Read/Write (*default*) or Read-Only.

Hard Disk Access Control

This option selects usage right from the hard disk. The setting is either Read/Write (*default*) or Read-Only.

S.M.A.R.T. for Hard Disks

Set this option to Enabled to permit AMIBIOS to use the SMART (System Management and Reporting Technologies). The setting is either Enabled or Disabled (*default*).

Boot Up Num Lock

Set this option to Off to turn the Num Lock key off when the computer is booted so you can use the arrow keys on both the numeric keypad and the keyboard.

PS/2 Mouse Support

Set this option to Enabled (*default*) to enable AMIBIOS support for a PS/2-type mouse. Disabling mouse will also free up IRQ12.

System Keyboard

This option does not specify if a keyboard is attached to the computer. Rather, it specifies if an error message is displayed

when a keyboard is not attached. This option permits you to configure workstations with no keyboards.

Primary Display

This option configures the type of video card attached to the computer. The settings are Mono, CGA40x25, CGA80x25, VGA/EGA (*default*) and Absent. Use Absent for systems without video cards.

Password Check

This option enables password checking every time the system boots or when you run AMIBIOS Setup. If Always is chosen, a user password prompt appears every time the computer is turned on. If Setup is chosen, the password prompt appears if AMIBIOS is executed. See the Advanced Setup chapter for instructions on changing a password. The Optimal and Fail-Safe default is Setup.

Ask HDD Password on Every Boot

Yes/No.

BOOT to OS/2

Set this option to Enabled if running OS/2 operating system and using more than 64 MB of system memory on the motherboard. The setting is either Yes or No (*default*).

CPU Microcode Updation

Disable/Enable. Has no functionality at this time.

CPU Serial Number

N/A.

Internal Cache

This option enables (as WriteThrough or WriteBack) or disables the L1 internal Cache.

System BIOS Cacheable

When set to Enabled, the contents of the F0000h system memory segment can be read from or written to cache memory. The content of this memory segment is always copied from the BIOS ROM to system RAM for faster execution. The setting is either Enabled or Disabled.

C000,32K Shadow

These option specify how the 32 KB of video ROM at C0000h is treated. The settings are: Enabled, Disabled and Cached(*default*).

C800,16K Shadow
CC00,16K Shadow
D000,16K Shadow
D400,16K Shadow
D800, 16K Shadow
DC00,16K Shadow

These options enable shadowing of the contents of the ROM area named in the option. The ROM area not used by ISA adapter cards is allocated to PCI adapter cards. The settings are: Disabled (*default*), Cached and Enabled.

Advanced Chipset Setup

Cyrix MII Performance

Enabled (*default*) or Disabled.

CPU/DRAM Base Frequency

Several options available. The *default* for the 200MHz SoC and PC133 SDRAM is Host 100MHz memory 133MHz.

SiS550 Timing Settings

Several timing settings for memory management. Please, don't change the default settings unless necessary.

SiS550 VGA Settings

Graphic Win Size

4M, 8M, 16M, 32M, 64M(*default*).

Share Memory Size

Disabled, 4M, 8M, 16M (*default*), 32M and 64M.

CRT

On (*default*) and Off.

LCD

On and Off (*default*).

LCD Expanding

Expanding (*default*) and non-expanding.

VGA LCD Panel ID Select

Selects panel.

Power Management Setup

All Power Management Setup options are described in this section.

Power Switch Type

This option specifies how the power button mounted externally on the computer chassis is used. The settings are: On/Off and suspend. The default setting is On/Off.

ACPI Aware O/S

Set this value to allow the system to utilize the Intel ACPI (Advanced Configuration and Power Interface) specification. The Optimal and Fail-Safe default setting is *Yes*.
No This setting should be set if the operating system in use does not comply with the ACPI (Advanced Configuration and Power Interface) specification. DOS® , Windows 3.x® , and Windows NT® are examples of non-ACPI aware operating systems.
Yes This setting should be set if the operating system complies with the ACPI (Advanced Configuration and Power Interface) specification. This is the default setting. Windows 95® , Windows 98® and Windows 2000® are examples of ACPI aware operating systems.

ACPI Standby State

Only S1 is supported.

Power Management

Set this option to enable the power management. The settings for this option are: Enabled (*default*) and Disabled.

Suspend Timeout

This option specifies the length of the period of system inactivity when the computer is already in Standby mode before the computer is placed in Suspend mode. In Suspend mode, nearly all power use is curtailed. The settings are multiples of the standby suspend timer unit. The default setting is Disabled.

Hard Disk Timeout (Minute)

This option specifies the length of a period of hard disk inactivity. When this period expires, the hard disk drive enters the power-conserving mode specified in the ***Hard Disk Power Down Mode*** option described on the previous page. The settings

are Disabled, 1 Min (minutes) and all one-minute intervals up to and including 15 Min. The default setting is Disabled.

RTC Alarm Resume From Soft Off

Enable or Disable (*default*).

RTC Alarm Date

RTC Alarm Hour

RTC Alarm Minute

RTC Alarm Second

Resume Options: N/A

Restore on A/C Power Loss

Set this value to select how the CPU board will recover from an accidental A/C power failure – Mechanical off G3 State.
Power ON This setting will force the CPU board to turn ON as soon as A/C power is reestablished. This is the default setting.
Power OFF This setting will keep the CPU board OFF when A/C power is reestablished. To turn the board ON, the power button must be used.
Last State This setting will put the CPU board back to its state before the accidental power failure. It requires ACPI enabled and an ACPI capable OS. The board must be normally turned OFF through a controlled S5 (soft OFF/Power button) transition if it is not an accidental power failure.

PCI/Plug and Play Setup

PCI/PnP Setup options are displayed by choosing the PCI/PnP Setup from the AMIBIOS Setup main menu. All PCI/PnP Setup options are described in this section.

Plug and Play Aware OS

Set this option to Yes if the operating system installed in the computer is Plug and Play-aware. AMIBIOS only detects and enables PnP ISA adapter cards that are required for system boot. The Windows 95 and 98 operating systems detect and enable all other PnP-aware adapter cards. Windows 95 is PnP-aware. Set this option to No if the operating system (such as DOS, OS/2, Windows 3.x) does not use PnP. **You must set this option correctly or PnP-aware adapter cards installed in your computer will not be configured properly.** The setting is either No or Yes. The Optimal and Fail-Safe default setting is No.

PCI Latency Timer (PCI Clocks)

This option sets latency of all PCI devices on the PCI bus. The settings are in units equal to PCI clocks. The settings are 32, 64, 96, 128, 160, 192, 224 and 248. The Optimal and Fail-Safe default setting is 64.

Primary Graphics Adapter

Allocate IRQ to PCI VGA

This option determines if the BIOS should assign an IRQ to the VGA card. The settings are either Yes or No. The default setting is No.

PCI IDE Bus Master

Set this option to Enabled to specify that the IDE controller on the PCI local bus has bus mastering capability. The setting is either Disabled or Enabled. The default setting is Disabled.

Off-board PCI IDE Card

This option specifies if an off-board PCI IDE controller adapter card is used in the computer. You must also specify the PCI expansion slot on the motherboard where the off-board PCI IDE controller card is installed. If an off-board PCI IDE controller is used, the onboard IDE controller on the CPU board is automatically disabled. The settings are Auto (*default*), Slot1,

Slot2, Slot3, Slot4, Slot5 and Slot6. If Auto is selected, AMIBIOS automatically determines the correct setting for this option.

Off-board PCI IDE Primary IRQ

This option specifies the PCI interrupt used by the primary IDE channel on the off-board PCI IDE controller. The settings are: Disabled, INTA, INTB, INTC, INTD and Hardwired. The Optimal and Fail-Safe default setting is Disabled.

Off-board PCI IDE Secondary IRQ

This option specifies the PCI interrupt used by the secondary IDE channel on the off-board PCI IDE controller. The settings are Disabled, INTA, INTB, INTC, INTD and Hardwired. The Optimal and Fail-Safe default setting is Disabled.

DMA Channel 0
DMA Channel 1
DMA Channel 3
DMA Channel 5
DMA Channel 6
DMA Channel 7

These options allow you to specify the bus type used by each DMA channel. The setting is either PNP or ISA/EISA. The optimal and fail-safe default setting is PNP.

IRQ3
IRQ4
IRQ5
IRQ7
IRQ9
IRQ10
IRQ11
IRQ12
IRQ14
IRQ15

These options specify the bus that the specified IRQ line is used on. These options allow you to reserve IRQs for legacy ISA adapter cards. These options determine if AMIBIOS should

remove an IRQ from the pool of available IRQs passed to devices that are configurable by the system BIOS. If more IRQs must be removed from the pool, the end user can use these options to reserve the IRQ by assigning an ISA/EISA setting to it. Onboard I/O is configured as PCI/PNP. IRQ12 only appears if the mouse support option in advanced setup is set to disabled. IRQ14 and 15 will not be available if the onboard PCI IDEs are enabled. The optimal and fail-safe default setting is PCI/PNP.

Peripheral Setup

Peripheral Setup options are displayed by choosing Peripheral Setup from the AMIBIOS Setup main menu. All Peripheral Setup options are described here.

Audio Device

Set this option to Enable or Disable the on board Audio AC97 controller. If Audio is enabled, certain OSs will require a driver installation on every boot.

Enabled This setting will keep the onboard Audio Controller enabled. This is the default setting.

Disabled This setting will turn off the on board Audio controller.

USB Device

Set this option to Enable or Disable the on board USB 1.1 controller that controls USB Ports 0 and 1.

Enabled This setting will keep the onboard USB Controller enabled. This is the default setting.

Disabled This setting will turn off the on board USB controller.

USB Function

Legacy USB Support

Legacy USB Support refers to the USB mouse and USB keyboard support. Normally if this option is not enabled, any attached USB mouse or USB keyboard will not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there is no USB drivers loaded on the

system. Set this value to enable or disable the Legacy USB Support. The Optimal and Fail-Safe default setting is *Auto*.

Disabled Set this value to prevent the use of any USB device in DOS or during system boot.

Enabled Set this value to allow the use of USB devices during boot and while using DOS.

Auto This option auto detects USB Keyboards or Mice and if found, allows them to be utilized during boot and while using DOS.

Serial Port1 Address

This option specifies the base I/O port address of serial port 1. The settings are Disabled, 3F8h, 2F8h, 3E8h and 2E8h.

Serial Port1 IRQ

This option specifies the IRQ of serial port 1. The settings are 3, 4, 5 and 7.

Serial Port2 Address

This option specifies the base I/O port address of serial port 2. The settings are Disabled, 3F8h, 2F8h, 3E8h and 2E8h.

Serial Port2 IRQ

This option specifies the IRQ of serial port 2. The settings are 3, 4, 5 and 7.

Serial Port3 Address

This option specifies the base I/O port address of serial port 3. The settings are Disabled, 3F8h, 2F8h, 3E8h and 2E8h.

Serial Port3 IRQ

This option specifies the IRQ of serial port 3. The settings are 3, 4, 5 and 7.

Serial Port4 Address

This option specifies the base I/O port address of serial port 4. The settings are Disabled, 3F8h, 2F8h, 3E8h and 2E8h.

Serial Port4 IRQ

This option specifies the IRQ of serial port 4. The settings are 3, 4, 5 and 7.

IRQs cannot be shared among serial ports

Parallel Port Address

This option specifies the base I/O port address of the parallel port on the motherboard. The settings are Disabled, 378h, 278h and 3BCh.

Parallel Port IRQ

This option specifies the IRQ always used by the parallel port. When the port is set to a fixed address the settings are (IRQ) 5 and (IRQ) 7 (*default*).

Onboard PCI IDE

This option specifies the IDE channel used by the onboard IDE controller. The settings are Disabled and Enabled (*default*).

Primary Master Prefetch
Primary Slave Prefetch

Enabled (*default*) or Disabled.

Auto Detect Hard Disk

Choose this option to let AMIBIOS find the IDE hard disk drive parameters for all IDE drives connected to the primary IDE

channel installed in the system. AMIBIOS automatically configures the drive parameters after it has detected these parameters.

Change User Password

Select the Change User Password from the Security section of the AMIBIOS Setup main menu. Enter the password and press <Enter>. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press <Enter>. This option will be available only if Supervisor Passwords exists.

Change Supervisor Password

Select the Change Supervisor Password from the Security section of the AMIBIOS Setup main menu. Enter the password and press <Enter>. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press <Enter>.

Remember the Password *Keep a record of the new password when the password is changed. If you forget the password, you must erase the system configuration information in NVRAM (Non-Volatile Random Access Memory).*

Auto Configuration with Optimal Settings

You can load the optimal default settings for the AMIBIOS by selecting the Optimal option. The Optimal default settings are best-case values that should optimize system performance. If CMOS is corrupted, the Optimal settings are loaded automatically.

Auto Configuration with Fail-Safe Settings

You can load the Fail-Safe AMIBIOS Setup option settings by selecting the Fail-Safe option from the Default section of the AMIBIOS Setup main menu. The Fail-Safe settings provide far from optimal system performance, but are the most stable settings. Use this option as a diagnostic aid if the system is behaving erratically.

Save Settings and Exit

Exit AMIBIOS saving the changes.

Exit without Saving

Allows to exit AMIBIOS setup without saving.

Post Codes

Power On Self Test (POST) progress codes are written by the system BIOS to I/O port 80h, allowing the user to monitor the progress with a special monitor. A POST code is transmitted by the BIOS during the POST (Power On Self Test). It is a number that refers to the state or test condition of a circuit or group of circuits. Knowing the results of these tests (hence the POST code) can be very important in debugging a system.

POST Checkpoint Codes

When AMIBIOS performs the Power On Self Test, it writes diagnostic codes checkpoint codes to I/O port 0080h.

Table 2-1 Uncompressed Initialization Codes

The uncompressed initialization checkpoint codes are listed in order of execution:

Checkpoint Code	Description
D0h	The NMI is disabled. Power on delay is starting. Next, the initialization code checksum will be verified.
D1h	Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh, and entering 4 GB flat mode next.
D3h	Starting memory sizing next.
D4h	Returning to real mode. Executing any OEM patches and setting the stack next.
D5h	Passing control to the uncompressed code in shadow RAM at E000:0000h.The initialization code is copied to segment 0 and control will be transferred to segment 0.
D6h	Control is in segment 0. Next, checking if <Ctrl> <Home> was pressed and verifying the system BIOS checksum. If either <Ctrl> <Home> was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.
D7h	Main BIOS runtime code is to be decompressed and control to be passed to main BIOS in shadow RAM.

Table 2-2 Bootblock Recovery Codes

The bootblock recovery checkpoint codes are listed in order of execution:

Checkpoint Code	Description
E0h	The onboard floppy controller if available is initialized. Next, beginning the base 512 KB memory test.
E1h	Initializing the interrupt vector table next.
E2h	Initializing the DMA and Interrupt controllers next.
E6h	Enabling the floppy drive controller and Timer IRQs. Enabling internal cache memory.
EDh	Initializing the floppy drive.
EEh	Looking for a floppy diskette in drive A:. Reading the first sector of the diskette.
EFh	A read error occurred while reading the floppy drive in drive A:.

F0h	Next, searching for the AMIBOOT.ROM file in the root directory.
F1h	The AMIBOOT.ROM file is not in the root directory.
F2h	Next, reading and analyzing the floppy diskette FAT to find the clusters occupied by the AMIBOOT.ROM file.
F3h	Next, reading the AMIBOOT.ROM file, cluster by cluster.
F4h	The AMIBOOT.ROM file is not the correct size.
F5h	Next, disabling internal cache memory.
FBh	Next, detecting the type of flash ROM.
FCh	Next, erasing the flash ROM.
FDh	Next, programming the flash ROM.
FFh	Flash ROM programming was successful. Next, restarting the system BIOS.

Table 2-3 Uncompressed Initialization Codes

The following runtime checkpoint codes are listed in order of execution. These codes are uncompressed in F0000h shadow RAM.

Checkpoint Code	Description
03h	The NMI is disabled. Next, checking for a soft reset or a power on condition.
05h	The BIOS stack has been built. Next, disabling cache memory.
06h	Uncompressing the POST code next.
07h	Next, initializing the CPU and the CPU data area.
08h	The CMOS checksum calculation is done next.
0Ah	The CMOS checksum calculation is done. Initializing the CMOS status register for date and time next.
0Bh	The CMOS status register is initialized. Next, performing any required initialization before the keyboard BAT command is issued.
0Ch	The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller.
0Eh	The keyboard controller BAT command result has been verified. Next, performing any necessary initialization after the keyboard controller BAT command test.
0Fh	The initialization after the keyboard controller BAT command test is done. The keyboard command byte is written next.

10h	The keyboard controller command byte is written. Next, issuing the Pin 23 and 24 blocking and unblocking command.
11h	Next, checking if <End or <Ins> keys were pressed during power on. Initializing CMOS RAM if the *Initialize CMOS RAM in every boot* AMIBIOS POST option was set in AMIBCP or the <End> key was pressed.
12h	Next, disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2.
13h	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.
14h	The 8254 timer test will begin next.
19h	The 8254 timer test is over. Starting the memory refresh test next.
1Ah	The memory refresh line is toggling. Checking the 15 second on/off time next.
23h	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24h	The configuration required before interrupt vector initialization has completed. Interrupt vector initialization is about to begin.
25h	Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.
27h	Any initialization before setting video mode will be done next.
28h	Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.
2Ah	Bus initialization system, static, output devices will be done next, if present. See *Table D-7* for additional information.
2Bh	Passing control to the video ROM to perform any required configuration before the video ROM test.
2Ch	All necessary processing before passing control to the video ROM is done. Looking for the video ROM next and passing control to it.
2Dh	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control.

2Eh	Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2Fh	The EGA/VGA controller was not found. The display memory read/write test is about to begin.
30h	The display memory read/write test passed. Look for retrace checking next.
31h	The display memory read/write test or retrace checking failed. Performing the alternate display memory read/write test next.
32h	The alternate display memory read/write test passed. Looking for alternate display retrace checking next.
34h	Video display checking is over. Setting the display mode next.
37h	The display mode is set. Displaying the power on message next.
38h	Initializing the bus input, IPL, general devices next, if present. See *Table D-7* for additional information.
39h	Displaying bus initialization error messages. See *Table D-7* for additional information.
3Ah	The new cursor position has been read and saved. Displaying the *Hit <DEL>* message next.
3Bh	The *Hit <DEL>* message is displayed. The protected mode memory test is about to start.
40h	Preparing the descriptor tables next.
42h	The descriptor tables are prepared. Entering protected mode for the memory test next.
43h	Entered protected mode. Enabling interrupts for diagnostics mode next.
44h	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45h	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.
46h	The memory wraparound test is done. Memory size calculation has been done. Writing patterns to test memory next.
47h	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory next.
48h	Patterns written in base memory. Determining the amount of memory below 1 MB next.

49h	The amount of memory below 1 MB has been found and verified. Determining the amount of memory above 1 MB memory next.
4Bh	The amount of memory above 1 MB has been found and verified. Checking for a soft reset and clearing the memory below 1 MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.
4Ch	The memory below 1 MB has been cleared via a soft reset. Clearing the memory above 1 MB next.
4Dh	The memory above 1 MB has been cleared via a soft reset. Saving the memory size next. Going to checkpoint 52h next.
4Eh	The memory test started, but not as the result of a soft reset. Displaying the first 64 KB memory size next.
4Fh	The memory size display has started. The display is updated during the memory test. Performing the sequential and random memory test next.
50h	The memory below 1 MB has been tested and initialized. Adjusting the displayed memory size for relocation and shadowing next.
51h	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1 MB next.
52h	The memory above 1 MB has been tested and initialized. Saving the memory size information next.
53h	The memory size information and the CPU registers are saved. Entering real mode next.
54h	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57h	The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.
58h	The memory size was adjusted for relocation and shadowing. Clearing the *Hit <DEL>* message next.
59h	The *Hit <DEL>* message is cleared. The *<WAIT...>* message is displayed. Starting the DMA and interrupt controller test next.
60h	The DMA page register test passed. Performing the DMA Controller 1 base register test next.
62h	The DMA controller 1 base register test passed. Performing the DMA controller 2 base register test next.
65h	The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
66h	Completed programming DMA controllers 1 and 2. Initializing the 8259 interrupt controller next.

67h	Completed 8259 interrupt controller initialization.
7Fh	Extended NMI source enabling is in progress.
80h	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
81h	A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
82h	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83h	The command byte was written and global data initialization has completed. Checking for a locked key next.
84h	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85h	The memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next.
86h	The password was checked. Performing any required programming before WINBIOS Setup next.
87h	The programming before WINBIOS Setup has completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next.
88h	Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next.
89h	The programming after WINBIOS Setup has completed. Displaying the power on screen message next.
8Bh	The first screen message has been displayed. The <*WAIT...*> message is displayed. Performing the PS/2 mouse check and extended BIOS data area allocation check next.
8Ch	Programming the WINBIOS Setup options next.
8Dh	The WINBIOS Setup options are programmed. Resetting the hard diskcontroller next.
8Fh	The hard disk controller has been reset. Configuring the floppy drivecontroller next.
91h	The floppy drive controller has been configured. Configuring the hard disk drive controller next.
95h	Initializing the bus option ROMs from C800 next. See *Table D-7* for additional information.
96h	Initializing before passing control to the adaptor ROM at C800.

97h	Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next.
98h	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
99h	Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next.
9Ah	Set the timer and printer base addresses. Setting the RS-232 base address next.
9Bh	Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next.
9Ch	Required initialization before the Coprocessor test is over. Initializing the Coprocessor next.
9Dh	Coprocessor initialized. Performing any required initialization after the Coprocessor test next.
9Eh	Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.
A2h	Displaying any soft errors next.
A3h	The soft error display has completed. Setting the keyboard typematic rate next.
A4h	The keyboard typematic rate is set. Programming the memory wait states next.
A5h	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7h	NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.
A8h	Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next.
A9h	Returned from adaptor ROM at E000h control. Performing any initialization required after the E000 option ROM had control next.
AAh	Initialization after E000 option ROM control has completed. Displaying the system configuration next.
ABh	Uncompressing the DMI data and executing DMI POST initialization next.
B0h	The system configuration is displayed.
B1h	Copying any code to specific areas.

Checkpoint Code	Description
00h	Code copying to specific areas is done. Passing control to INT 19h boot loader next.

Table 2-4 Bus Checkpoint Codes

The system BIOS passes control to different buses at the following checkpoints:

Checkpoint Code	Description
2Ah	Initializing the different bus system, static, and output devices, if present.
38h	Initialized bus input, IPL, and general devices, if present.
39h	Displaying bus initialization error messages, if any.
95h	Initializing bus adaptor ROMs from C8000h through D8000h.

Table 2-5 Additional Bus Checkpoints

While control is inside the different bus routines, additional checkpoints are output to I/O port address 0080h as word to identify the routines being executed.

These are word checkpoints. The low byte of checkpoint is the system BIOS checkpoint where control is passed to the different bus routines.

The high byte of checkpoint indicates that the routine is being executed in different buses. This information will not be shown on POST code display because this device is 8-bit only. However, it can be seen in any equipment connected to I/O port address 0080h.

The system BIOS passes control to different buses at the following checkpoints:

High Byte The high byte of these checkpoints includes the following information:

Bits	Description
Bits 7-4	0000 Function 0. Disable all devices on the bus. 0001 Function 1. Initialize static devices on the bus. 0010 Function 2. Initialize output devices on the bus. 0011 Function 3. Initialize input devices on the bus. 0100 Function 4. Initialize IPL devices on the bus. 0101 Function 5. Initiate general devices on the bus. 0110 Function 6. Initialize error reporting on the bus. 0111 Function 7. Initialize add-on ROMs for all buses.
Bits 3-0	Specify the bus 0 Generic DIM Device Initialization Manager. 1 Onboard System devices. 2 ISA devices. 3 EISA devices. 4 ISA PnP devices. 5 PCI devices.

Table 2-7 AMIBIOS Beep Codes

Except for beep code #8, these codes are always fatal.

1 beep	Refresh failure.
2 beeps	Parity error.
3 beeps	Base 64K memory failure.
4 beeps	Timer not operational.
5 beeps	Processor error.
6 beeps	8042 - gate A20 failure.
7 beeps	Processor exception interrupt error.
8 beeps	Display memory read/write failure.
9 beeps	ROM checksum error.
10 beeps	CMOS shutdown register read/write error.
11 beeps	Cache memory bad.

Chapter 3 Upgrading

Upgrading the System Memory

The Gator 550-G allows an upgrade of the system memory.

The following describes the Integrated DRAM controller:

Supports 1 Double Sided μDIMM (2 Rows Memory)
Supports PC100/PC133 SDRAM Technology
Supports NEC Virtual Channel Memory (VC-SDRAM) Technology
System Memory Size up to 256 MB
Supports 16Mb, 64Mb, 128Mb, 256Mb, 512Mb SDRAM Technology
Relocatable System Management Memory Region
Programmable Buffer Strength for CS#, DQM[7:0], WE#, RAS#, CAS#, CKE,
MA[14:0] and MD[63:0]
Shadow RAM Size from 640KB to 1MB In 16KB Increments

User's Notes:

Appendix A Technical Specifications

Chipset

Core Logic

SiS550 SoC.

Integrated x86 Compatible CPU
x86 Instruction Set Compatible Processor
High Performance with Advanced Architectures
Superscalar Execution
Three Superpipelined Integer Units
Pipelined Floating Point Unit
Innovative Instruction Decode and Branch Prediction
Separate Code and Data Caches
Support for Bus Frequency up to 100MHz
Low Power Consumption Design
Software Compatibility with Microsoft Windows, Windows CE, MS-DOS, QNX and LINUX
Supports Host Bus Direct Access GUI Engine for Integrated A.G.P. VGA Controller

High Performance PCI Arbiter
Supports up to 3 external PCI Masters
Rotating Priority Arbitration Scheme
Advanced Arbitration Scheme Minimizing Arbitration Overhead
Guaranteed Minimum Access Time for CPU And PCI Masters

Integrated Host-To-PCI Bridge
Zero Wait State Burst Cycles
CPU-To-PCI Pipeline Access
256B to 4KB PCI Burst Length for PCI Masters
PCI Master Initiated Graphical Texture Write Cycles Re-Mapping
Reassembles PCI Burst Data Size into Optimized Block Size

Low Pin Count Interface
Forwards PCI I/O and Memory Cycles into LPC Bus
Translates 8-/16-Bit DMA Cycles into PCI Bus Cycles

Integrated DMA Controller
Two 8237A Compatible DMA Controllers

8/16- Bit DMA Data Transfer
Distributed DMA Support

Integrated Interrupt Controller
Two 8259A Compatible Interrupt Controllers
Level- Or Edge-Triggered Programmable Serial IRQ
Interrupt Sources Re-Routable to Any IRQ Channel

Three 8254 Compatible Programmable 16-Bit Counters
System Timer Interrupt
Generate Refresh Request
Speaker Tone Output

Bios

System BIOS

AMI Hiflex BIOS with Flash BIOS option.

Flash BIOS

Optional feature for System BIOS. Flash programming built into the BIOS. BIOS to be flashed is read from a floppy.

Embedded I/O

IDE

One PCI EIDE controllers. Supports up to 2 devices. Ultra DMA up to 100MB/sec. supported. ATAPI compatible. 44 pin header on-board. *ATA-66 and ATA-100 are faster timings and require a specialized cable (80-conductor) to reduce reflections, noise, and inductive coupling.*
The Parallel ATA IDE interfaces also support ATAPI devices (such as CD-ROM drives).

Fast PCI IDE Master/Slave Controller
Supports PCI Bus Mastering
Supports Native Mode and Compatibility Mode
Supports PIO Mode 0, 1, 2, 3, 4

Supports Multiword DMA Mode 0, 1, 2
Supports Ultra DMA 33/66/100

Floppy

One floppy disk drive. Sizes supported are: 5.25" 360K and 1.2MB; 3.5" 720K, 1.44MB and 2.88MB.

Serial Ports

Four high speed 16550 compatible UARTS. BIOS configurable as COM1 - 4. COM3 Optional RS422/485. COM2 optional RS-232 IrDA.

USB Interfaces

On-board dual USB.

Integrated Universal Serial Bus Host Controller
OpenHCI Host Controller with Root Hub
Two USB Ports
Supports Legacy Devices
Over Current Detection

Parallel Port

One bidirectional parallel port. SPP mode compatible.

Keyboard/Mouse Port

On-board Ethernet

On-board auto-sensing, bus mastering 10/100 Ethernet (SiS900).

Audio

Audio (AD1981B) AC97 compliant. Microphone In, Stereo Line In and Out(headphone), CD In.

Miscellaneous

CMOS/Battery

Integrated Real Time Clock (RTC) with 256B CMOS SRAM
Supports ACPI Day-Of-Month and Month-Of-Year Alarm
256 Bytes Of CMOS SRAM
Provides RTC H/W Year 2000 Solution

RTC with lithium battery. No external battery is required.

Form Factor

PC104 form factor.

PCB Construction

Six Layers, dry film mask.

Manufacturing Process

Automated surface mount.

Table A-1 Environmental

Environmental	Operating	Non-operating
Temperature	0° to +55° C	-40° to +65° C
Humidity	5 to 95% @ 40° C non-condensing	5 to 95% @ 40° C non-condensing
Shock	2.5G @ 10ms	10G @ 10ms
Vibration	0.25 @ 5-100Hz	5 @ 5-100Hz

Memory Map

Address Range Decimal	Address Range Hexadecimal	Size	Description
960K-1M	0F0000-0FFFFF	64 KB	Upper BIOS
896K-960K	0E0000-0EFFFF	64 KB	Lower BIOS
768K-896K	0C0000-0DFFFF	128 KB	Expansion Card BIOS and Buffer
640K-768K	0A0000-0BFFFF	128 KB	Standard PCI/ISA Video Memory
512K-640K	080000-09FFFF	128 KB	Ext. Conventional memory
0K- 512K	000000-07FFFF	512 KB	Conventional memory

DMA Channels

DMA #	Data Width	System Resource
0	8- or 16-bits	
1	8- or 16-bits	
2	8- or 16-bits	Floppy Drive
3	8- or 16-bits	
4	Reserved-	cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

I/O Map

Address (hex)	Description
0000-000F	DMA 1
0020-0021	Interrupt Controller 1
0040	Timer/Counter 0
0041	Timer/Counter 1
0042	Timer/Counter 2
0043	Timer Control Word
0060	Keyboard Controller Byte _ Reset IRQ
0061	NMI Status and Control
0070, bit 7	NMI enable
0070, bits 6:0	RTC Index
0071	RTC Data
0072	RTC Extended Index
0073	RTC Extended Data
0080-008F	DMA page registers / POST code display also located at 0080h
0092	Port 92
00A0-00A1	Interrupt Controller 2
00B2-00B3	APM control
00C0-00DE	DMA 2
00F0	Coprocessor Error
0110	Watch-Dog Timer (default)
0170 _ 0177	Secondary IDE channel
01F0 _ 01F7	Primary IDE channel
029x	LM79
0278-027F	LPT2 (if selected)
02E8-02EF	COM4 (if selected)
02F8-02FF	COM2 (default)
0310	Watch-Dog Timer (if selected)
0376	Secondary IDE channel command port
0377	Floppy channel 2 command
0377, bit 7	Floppy disk change, channel 2
0377, bits 6:0	Secondary IDE channel status port
0378-037F	LPT1 (default)
03B4-03B5	Video (VGA)
03BA	Video (VGA)
03BC-03CD	LPT3 (if selected)
03C0-03CA	Video (VGA)
03CC	Video (VGA)
03CE-03CF	Video (VGA)

Address (hex)	Description
03D4-03D5	Video (VGA)
03DA	Video (VGA)
03E8-03EF	COM3 (if selected)
03F0-03F5	Floppy Channel 1
03F6	Primary IDE channel command port
03F7	Floppy Channel 1 command
03F7, bit 7	Floppy disk change channel 1
03F7, bits 6:0	Primary IDE channel status report
03F8-03FF	COM1 (default)
04D0-04D1	INTC-1 Edge/Level Control
0CF8-0CFB - 4 bytes	PCI configuration address register
0CF9	Reset control register
0CFC-0CFF - 4 bytes	PCI configuration data register

PCI Configuration Space Map

Bus #	Device #	Function #	Description
00	00	00	North Bridge
00	00	01	PCI IDE
00	01	00	LPC
00	01	02	USB
00	01	04	Audio
00	02	00	PCI to PCI bridge
01	00	00	GUI
01	08	00	Ethernet
01	04	00	PC104+ IDSEL0
01	05	00	PC104+ IDSEL1
01	06	00	PC104+ IDSEL2
01	07	00	PC104+ IDSEL3

Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved (keyboard)
2	Reserved (cascade)
3	COM2*
4	COM1*
5	User Available
6	Floppy Drive
7	LPT1*
8	Real time clock
9	User Available
10	User Available
11	User Available
12	PS/2 mouse port (if present, else user available)
13	Reserved (math coprocessor)
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

**Default, but can be changed to another IRQ*

PCI Interrupt Routing Map

PCI Device	IDSEL	PIRQA	PIRQB	PIRQC	PIRQD
PC104+ ID0	AD20	INTA	INTB	INTC	INTD
PC104+ ID1	AD21	INTD	INTA	INTB	INTC
PC104+ ID2	AD22	INTC	INTD	INTA	INTB
PC104+ ID3	AD33	INTB	INTC	INTD	INTA
Ethernet	AD24	INTA			

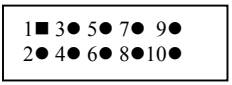
SMBUS

Device	Slave Address
DIMM0	01010000b
Clock Chip Write	11010010b
Clock Chip Read	11010011b

Connectors Pin-out

How to identify pin number 1: Looking to the solder side (The board side without components) of the PCB (Printed Circuit Board), pin number 1 will have a squared pad ■. Other pins will have a circular pad ●.

How to identify other pins: Header connectors are numbered alternately, i.e. pin number 2 is in the other row, but in the same column of pin number 1. Pin number 3 is in the same row of pin 1, but in the next column and so forth.



Header 10 pin connector
View from solder side of the PCB

Table A-9 J14 LCD Connector

Pin#	LCD Header – J14
1	LCDVCC
2	LCDVCC
3	LCDVCC
4	LCDVCC
5	VVBD7
6	VVBD6
7	VVBD5
8	VVBD4
9	GND
10	GND
11	VVBD3
12	VVBD2
13	VVBD1
14	VVBD0
15	VVBD11
16	VVBD10
17	VVBD9
18	VVBD8
19	GND
20	GND
21	LP/HSYNC
22	SHFCLK
23	ENBLT
24	FLM/VSYNC
25	NC
26	MOD/LDE
27	THSYNC
28	LLD0
29	TVSYNC
30	UUD4
31	UUD3
32	DEN
33	GND

Pin#	LCD Header – J14
34	XCLK
35	LLD5
36	LLD6
37	LLD7
38	LLD2
39	LLD3
40	LLD4
41	LLD1
42	GND
43	UUD5
44	UUD2
45	GND
46	UUD0
47	UUD1
48	UUD6
49	UUD7
50	GND

Table A-10 J27 Ethernet Header Connector

Pin#	Ethernet Header – J27
1	Termination
2	RX-
3	Shorted to pin 1
4	RX+
5	Termination
6	TX-
7	Shorted to pin 5
8	TX+
9	GND
10	GND
11	A+L VCC3
12	LED_LINK
13	SPEED VCC3
14	LED_SPEED

Table A-11 J30 VGA/KB/MS/LPT

Pin#	VGA/KB/MS/LPT Header – J30
1-26	**LPT**
1	-STROBE
2	AUTOFEED
3	+DATA BIT 0
4	ERROR
5	+DATA BIT 1
6	INIT
7	+DATA BIT 2
8	SLCT IN
9	+DATA BIT 3
10	GND
11	+DATA BIT 4
12	GND
13	+DATA BIT 5
14	GND
15	+DATA BIT 6
16	GND
17	+DATA BIT 7
18	GND
19	ACK1
20	GND
21	BUSY
22	GND
23	PAPER EMPTY
24	GND
25	SLCT
26	NC
27-38	**Keyboard and Mouse**
27	KBCLK
28	MSCLK
29	NC
30	MSDATA
31	VCC

Pin#	VGA/KB/MS/LPT Header – J30
32	VCC
33	NC
34	KBDATA
35	GND
36	NC
37	NC
38	NC
39-50	**VGA**
39	RED
40	GND
41	GREEN
42	GND
43	BLUE
44	GND
45	HSYNC
46	GND
47	VSYNC
48	DDC Power
49	DDC DATA
50	DDC CLK

Table A-12 LVDS Backlight, Power Button, Reset, Battery and Main Power.

Connector	Description		
J36	**LVDS Backlight**		
	1)+12Vcc	2)GND	3)Enable
J31	**Power Button**		
	1)GND	2)PWRBTN	
J11	**Reset**		
	1)GND	2)RESET	
J35	**Battery**		
	1)VBAT	2)GND	
J34	**Main Power +12Vcc**		
	1-Center)+12Vcc	2)GND	

Table A-13 J37 LPC

Pin#	LPC – J37
1	LAD0
2	SIRQ
3	LAD1
4	LFRAME
5	LAD2
6	GND
7	LAD3
8	PCI CLK
9	GND
10	GND
11	PCI RST
12	LDRQ1
13	NC
14	NC
15	PME
16	EXT SMI

Table A-14 J20 LVDS Connector (optional)

Pin#	LVDS Header – J20
1	LCDVCC
2	LCDVCC
3	GND
4	GND
5	NC
6	NC
7	GND
8	NC
9	NC
10	GND
11	TXCLK+
12	NC
13	GND
14	NC
15	TXCLK-
16	GND
17	TX2+
18	NC
19	GND
20	GND
21	LCDVCC
22	LCDVCC
23	GND
24	GND
25	TX2-
26	NC
27	GND
28	NC
29	TX1+
30	GND
31	TX1-
32	NC
33	GND

Pin#	LVDS Header – J20
34	NC
35	TX0+
36	GND
37	TX0-
38	NC
39	GND
40	GND

Table A-15 J26 COM1/COM2/COM3/Audio Connector

Pin#	COM1/COM2/COM3/Audio Header – J26
1-10	**COM1**
1	DCD
2	DSR
3	RX
4	RTS
5	TX
6	CTS
7	DTR
8	RI
9	GND
10	NC
11-20	**COM2**
11	DCD
12	DSR
13	RX
14	RTS
15	TX
16	CTS
17	DTR
18	RI
19	GND
20	NC

Pin#	COM1/COM2/COM3/Audio Header – J26
21-30	**COM3**
21	DCD - RS-422/485RXB(opt.)
22	DSR
23	RX - RS-422/485TXB(opt.)
24	RTS
25	TX - RS-422/485TXA(opt.)
26	CTS
27	DTR
28	RI – RS-422/485RXA(opt.)
29	GND
30-40	**AUDIO**
30	MIC IN
31	CD IN Left
32	CD IN Right
33	CD GND
34	MIC BIAS
35	GND
36	LINE IN Left
37	LINE IN Right
38	GND
39	Headphone OUT Left
40	Headphone OUT Right

Table A-16 J25 FDD/USB/COM4

Pin#	FDD/USB/COM4/IrDA Header – J25
1-20	**FDD**
1	NC
2	NC
3	LDRQ
4	DSKCHG
5	RDATA
6	GND
7	GND
8	WPRTCT
9	DRV S0
10	MTR0
11	TRK0
12	INDEX
13	GND
14	GND
15	SIDE1
16	WGATE
17	WDATA
18	STEP
19	DIR
20	DENSEL0
21-30	**USB**
21	VCC
22	VCC
23	DATA0-
24	DATA1-
25	DATA0+
26	DATA1+
27	GND
28	GND
29	GND
30	GND

Pin#	VGA/KB/MS/LPT Header – J30
31-39	**COM4**
31	DCD
32	DSR
33	RX
34	RTS
35	TX
36	CTS
37	DTR
38	RI
39	GND
40-50	**IrDA**
40	GND
41	IRMODE
42	IRRX
43	NC
44	IRTX
45	NC
46	NC
47	NC
48	NC
49	NC
50	NC

User's Notes:

Appendix B Flash BIOS programming

The Gator 550-G offers the optional FLASH BIOS. When installed, you will be able to update your BIOS without having to replace the EPROM. The AMIBIOS will read the new BIOS file from a floppy disk, replace the old BIOS and reboot your computer.

When updating your BIOS, make sure you have a disk with the correct BIOS file (its size should be 256K).

Rename the file to "AMIBOOT.ROM". Turn your computer off. Insert the disk in Drive A:, Turn the computer on while pressing <CTRL><HOME>. Your computer will show no screen, but will beep to indicate what is being done.

If the programming is successful, you should hear 4 beeps and your computer will reboot with the new BIOS.

Please never turn the power off while reprogramming a FLASH BIOS.

Refer to the table on the next page for beep errors.

Table B-1 Flash BIOS Beep Errors

Beeps	Description
1	Insert diskette in floppy A:
2	The AMIBOOT.ROM file was not found in the root directory of floppy drive A:
3	Base memory error
4	Flash program successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No FLASH EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash erase error
11	Flash program error
12	AMIBOOT.ROM file size error

Appendix C On-board Video

The Gator 550-G offers standard CRT and LCD connections and an optional LVDS interface.

For pin out descriptions of the CRT, LCD and LVDS interfaces, please check *appendix A*.

The following is a description of the video capabilities of SiS550:

Integrated A.G.P. Compliant Target Host-To-PCI Bridge

AGP V2.0 Compliant
Supports Graphic Window Size from 4Mbytes To 256Mbytes
Supports Pipelined Process in CPU-To-Integrated A.G.P. VGA Access
Supports 8 Way, 16 Entries Page Table Cache for GART to Enhance Integrated
A.G.P. VGA Controller Read/Write Performance
Supports PCI-To-PCI Bridge Function for Memory Write from 33Mhz PCI Bus to Integrated A.G.P. VGA

Integrated Ultra-AGPTM VGA for Hardware 2D/Video/Graphics Accelerators
Supports Tightly Coupled 64 Bits 100Mhz Host Interface to VGA to Speed Up GUI
Performance and the Video Playback Frame Rate
AGP Rev. 2.0 Compliant
Zero-Wait-State Post-Write Buffer with Write Combine Capability
Zero-Wait-State Read Ahead Cache Capability
Re-Locatable Memory-Mapped and I/O Address Decoding
Flexible Design Shared Frame Buffer Architecture for Display Memory
Shared System Memory Area up to 128 MB
128-Bit 2D Engine with a Full Instruction Set
Built-In 64x64x2 Bit-Mapped Hardware Cursor
Built-In 32x32x16, 32x32x32 Bit-Mapped Hardware Color Cursor and Alpha Cursor
MPEG-2 ISO/IEC 13818-2 MP@ML and MPEG-1 ISO/IEC 11172-2 Standards Compliant
Supports Advanced H/W DVD Accelerator
Built-in Video Processor to Support De-interlace Function and High Quality Multi-tap Video Scaling

Direct DVD to TV Playback
Supports Two Independent Video Windows with Overlay Function and Scaling Factors
Supports YUV-To-RGB Color Space Conversion
Supports Bi-Linear Video Interpolation with Integer Increments of Pixel Accuracy
Supports Graphic and Video Overlay Function
Supports VCD/DVD to TV Playback Mode
Simultaneous Graphic and TV Video Playback Overlay
Supports Current Scan Line Of Refresh Red-Back and Interrupt
Supports Tearing Free Double/Triple Buffer Flipping
Supports Input Video Vertical Blank or Line Interrupt
Supports RGB555, RGB565, YUV422 and YUV420 Video Playback Format
Supports Filtered Horizontal up and down Scaling Playback
Supports DVD Sub-Picture Playback Overlay
Supports DVD Playback Auto-Flipping
Built-In Two Video Playback Line Buffers
Supports DCI Drivers
Supports Direct Draw Drivers
Built-In Programmable 24-Bit True-Color RAMDAC up to 300 MHz Pixel Clock RAMDAC
Snoop Function
Built-In Reference Voltage Generator and Monitor Sense Circuit
Supports Down-Loadable RAMDAC for Gamma Correction In High Color and True Color Modes
Built-In Dual-Clock Generator
Supports Multiple Adapters and Multiple Monitors
Built-In Digital Interface for LVDS
Supports Digital Flat Panel Port for Digital Monitor (LCD Panel)
Supports VESA Standard Super High Resolution Graphic Modes
640x480 16/256/32K/64K/16M Colors 160 Hz NI
800x600 16/256/32K/64K/16M Colors 120 Hz NI
1024x768 256/32K/64K/16M Colors 120 Hz NI
1280x1024 256/32K/64K/16M Colors 85 Hz NI
1600x1200 256/32K/64K/16M Colors 85 Hz NI
1920x1440 256/32K/64K Colors 60 Hz NI
1920x1440 256 Colors 75 Hz NI
Low Resolution Modes
Supports Virtual Screen up to 4096x4096
Fully DirectX 8.0 Compliant
Efficient and Flexible Power Management with ACPI Compliance
Supports DDC1, DDC2B and DDC 3.0 Specifications

Appendix D On-Board Industrial Devices

The Gator 550-G features two industrial devices: A 10/100 Ethernet controller and four serial ports (one RS-422/485 optional).

On-board Ethernet

The Gator 550-G features a built-in 10/100 Ethernet controller (SiS900).

Features
Integrated Fast Ethernet controller and 10/100 megabit per second (Mbps) Physical Layer Transceivers for the PCI local bus

- PCI specification revision 2.1 compliant
- 32-bit glueless PCI host interface
- Plug and Play compatible
- Supports PCI clock frequency from DC to 33 MHz independent of network clock
- Supports network operation with PCI clock from 25Mhz to 33Mhz
- Supports both +3.3v and +5v PCI signaling
- High-performance 32-bit PCI bus master architecture with integrated Direct Memory Access (DMA) Controller for low CPU and bus utilization
- Supports an unlimited PCI burst length
- Supports big endian and little endian byte alignments
- Supports PCI Device ID, Vendor ID/Subsystem ID, Subsystem Vendor ID programming through the EEPROM interface
- Implements optional PCI 3.3v auxiliary power source 3.3Vaux pin and optional PCI power management event (PME#) pin
- IEEE 802.3 and 802.3u standard compatible
- IEEE 802.3u Auto Negotiation and Parallel detection for automatic speed selection
- Full duplex and half duplex mode for both 10 and 100 Mbps.
- Fully compliant ANSI X3.263 TP-PMD physical sub-layer which includes adaptive equalization and Baseline Wander compensation.

- Automatic Jam and IEEE 802.3x Auto-Negotiation for flow control
- Single access to complete PHY register set
- Built-in waveform shaping requires no external filters
- Single 25Mhz clock for 10 and 100 Mbps operation.
- Power down of 10Base-T/100Base-TX sections when not in use
- Jabber control and auto-polarity correction for 10Base-T.
- User programmable LED function mapping
- Supports software, enhanced software, and automatic polling schemes to internal PHY status monitor and interrupt
- Supports 10BASE-T, 100BASE-TX, and any future
- Supports PC97, PC98, and Net PC requirements – Green PC compatible
- Supports Advanced Configuration and Power Interface Specification (ACPI) Revision 1.0
- Supports PCI Bus Power Management Interface Specification Version 1.0a
- Supports Network Device Class Power Management Specification Version 1.0a
- Supports PCI Hot-Plug Specification Revision 1.0
- Implements IEEE 802.3x compliant Flow Control
- Internal 128-bit Multicast Hash Table address filter
- Serial EEPROM support
- Extensive programmable internal/external loopback capabilities
- +3.3V power supply with +5V tolerant I/Os
- 128pin PQFP package. Low-Power CMOS 0.35um Technology

Serial Ports

The Gator 550-G features four serial ports (one RS-422/485 optional).

TIA/EIA-232

RS is the abbreviation for recommended standard. Usually, it is based on or is identical to other standards, e.g., EIA/TIA-232-F. TIA/EIA-232, previously known as RS-232 was developed in the 1960's to interconnect layers of the interface (ITU–T V.11), but also the pignut of the appropriate connectors (25-pin D-type or 9-pin DB9S) (ISO 2210) and the protocol (ISSUED-T V.24). The interface standard specifies also handshake and control lines in addition to the 2 unidirectional receive data line (RD) and transmit data line (TD). The control lines data carrier detect (DCD), data set ready (DSR), request to send (RTS), clear to send (CTS), data terminal ready (DTR), and the ring indicator (RI) might be used, but do not necessarily have to be (for example, the PC-serial-mouse utilizes only RI, TD, RD and GND). Although the standard supports only low speed data rates and line length of approximately 20 m maximum, it is still widely used. This is due to its simplicity and low cost.

Electrical

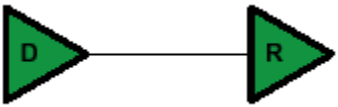
TIA/EIA-232 has high signal amplitudes of ±(5 V to 15 V) at the driver output. The triggering of the receiver depends on the sign of the input voltage: that is, it senses whether the input is above 3 V or less than –3 V. The line length is limited by the allowable capacitive load of less than 2500 pF. This results in a line length of approximately 20 m. The maximum slope of the signal is limited to 30 V/ms. The intention here is to limit any reflections that can occur to the rise-and fall-times of the signal. Therefore, transmission line theory does not need to be applied, so no impedance matching and termination measures are necessary.

Do not connect termination resistor when operating in RS-232 mode.

Protocol

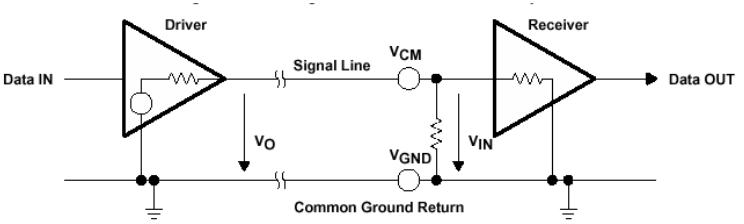
Different from other purely electrical-layer-standards, TIA/EIA-232 defines not only the physical layer of the interface (ITU-T V.11), but also the pinout of the appropriate connectors (25-pin D-type or 9-pin DB9S) (ISO 2210) and the protocol (ITU-T V.24). The interface standard specifies also handshake and control lines in addition to the 2 unidirectional receive data line (RD) and transmit data line (TD). The control lines might be used, but do not necessarily have to be.

RS-232 is Single-Ended Point-to-point Transmission



Single-Ended, Point-to-Point

Single-ended transmission is performed on one signal line, and the logical state is interpreted with respect to ground. For simple, low-speed interfaces, a common ground return path is sufficient; for more advanced interfaces featuring higher speeds and heavier loads, a single return path for each signaling line (twisted pair cable) is recommended. The figure below shows the electrical schematic diagram of a single-ended transmission system.



Advantages of Single-Ended Transmission

The advantages of single-ended transmission are simplicity and low cost of implementation. A single-ended system requires only one line per signal. It is therefore ideal for cabling, and connector costs are more important than the data transfer rate, e.g. PC, parallel printer port or serial communication with many handshaking lines, e.g. EIA-232. Cabling costs can be kept to a minimum with short distance communication, depending on data throughput, requiring no more than

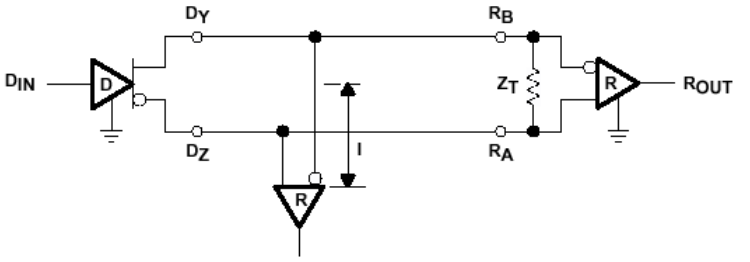
a low cost ribbon cable. For longer distances and/or noisy environments, shielding and additional ground lines are essential. Twisted pair cables are recommended for line lengths of more than 1 meter.

TIA/EIA-422

TIA/EIA-422 (RS-422) allows a multi-drop interconnection of one driver, transmitting unidirectionally to up to 10 receivers. Although it is not capable of bidirectional transfer, it is still applicable and used for talker-audience scenarios.

Electrical

TIA/EIA-422 (ITU-T V.11) is comparable to TIA/EIA-485. It is limited to unidirectional data traffic and is **terminated only at the line-end opposite to the driver**. The maximum line length is 1200m, the maximum data rate is determined by the signal rise- and fall-times at the receiver's side (requirement: <10% of bit duration). TIA/EIA-422 allows up to ten receivers (input impedance of 4 kΩ attached to one driver. The maximum load is limited to 80 Ω. Although any TIA/EIA-485 transceiver can be used in a TIA/EIA-422 system, dedicated TIA/EIA-422 circuits are not feasible for TIA/EIA-485, due to short circuit current limitations. The TIA/EIA-422 standard requires only short circuit limitation to 150 mA to ground, while TIA/EIA-485 additionally has to limit short circuit currents to 250 mA from the bus pins to –7 V and 12 V to address malfunctions in combination with ground shifts.

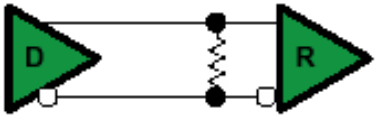


RS-422 is terminated only at the line-end opposite to the driver even if there is only one receiver.

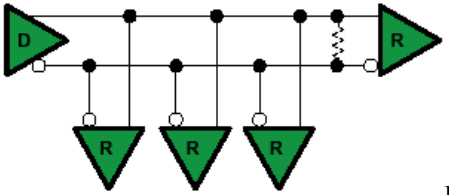
Protocol

Not applicable/none specified.

RS-422 is Differential and may be either Point-to-Point or Multi-Drop Connected



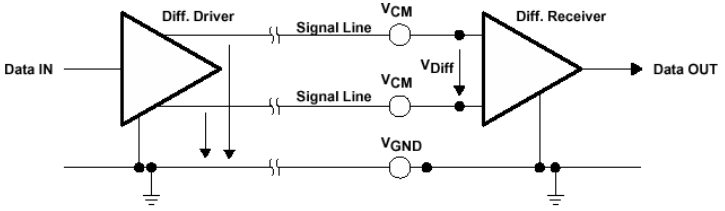
Differential, Point-to-Point



Differential, Multi-Drop

Differential Transmission

For balanced or differential transmission, a pair of signal lines is necessary for each channel. On one line, a true signal is transmitted, while on the second one, the inverted signal is transmitted. The receiver detects voltage difference between the inputs and switches the output depending on which input line is more positive. As shown below, there is additionally a ground return path.



Balanced interface circuits consist of a generator with differential outputs and a receiver with differential inputs. Better noise performance stems from the fact that noise is coupled into both wires of the signal pair in much the same way and is common to both signals.

Due to the common mode rejection capability of a differential amplifier, this noise will be rejected. Additionally, since the signal line emits the opposite signal like the adjacent signal return line, the emissions cancel each other. This is true in any case for crosstalk from and to neighboring signal lines. It is also true for noise from other sources as long as the common mode voltage does not go beyond the common mode range of the receiver. Since ground noise is also common to both signals, the receiver rejects this noise as well. The twisted pair cable used in these interfaces in combination with a correct line termination—to avoid line reflections—allows very high data rates and a cable length of up to 1200 m.

Advantages of Differential Transmission

Differential data transmission schemes are less susceptible to common-mode noise than single-ended schemes. Because this kind of transmission uses two wires with opposite current and voltage swings compared to only one wire for single-ended, any external noise is coupled onto the two wires as a common mode voltage and is rejected by the receivers. This two-wire approach with opposite current and voltage swings also radiates less electro-magnetic interference (EMI) noise than single-ended signals due to the canceling of magnetic fields.

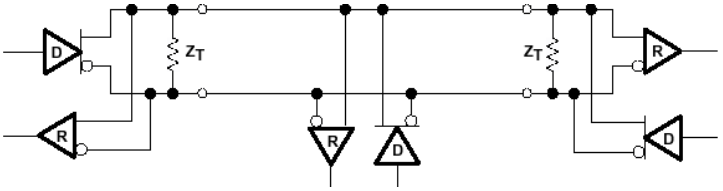
TIA/EIA-485

Historically, TIA/EIA-422 was on the market before TIA/EIA-485. Due to the lack of bi-directional capabilities, a new standard adding this feature was created: TIA/EIA-485 . The standard (TIA/EIA-485-A or ISO/IEC 8284) defines the electrical characteristics of the interconnection, including driver, line, and receiver. It allows data rates in the range of 35 Mbps and above and line lengths of up to 1200 m. Of course both limits can not be reached at the same time. Furthermore, recommendations are given regarding wiring and termination. The specification does not give any advice on the connector or any protocol requirements.

Electrical

TIA/EIA-485 describes a half-duplex, differential transmission on cable lengths of up to 1200 m and at data rates of typically up to 35 Mbps (requirement similar to TIA/EIA-422, but tr<30% of the bit duration, there are also faster devices available, suited for higher rates under certain load-conditions). The standard allows a maximum of 32

unit loads of 12 kΩ, equal to 32 standard nodes or even higher count with increased input impedance. The maximum total load should not drop below 52 Ω. The common-mode voltage levels on the bus have to maintain between –7 V and 12 V. The receivers have to be capable to detect a differential input signal as low as 200 mV.

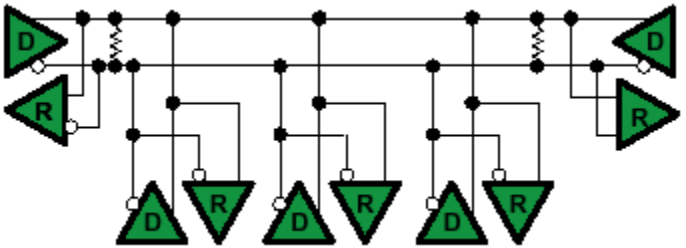


RS-485 is terminated at both sides of the common bus, even if only two stations are connected to the backbone.

Protocol

Not applicable/none specified; exceptions: SCSI systems and the DIN-Bus DIN66348.

RS-485 is Differential and Multi-Point Connected



Differential Transmission

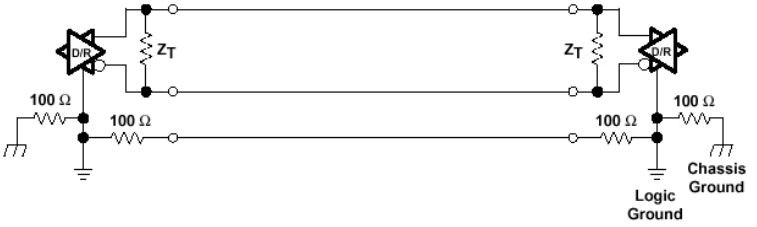
Please, read the Differential Transmission explanation in the previous RS-422 section.

Termination Resistors

Follow instructions in the previous RS-422 and RS-485 sections. The termination resistors available are rated to 120Ω.

Ground Connections

All 422- and 485-compliant system configurations shown up to this point do not have incorporated signal-return paths to ground. Obviously, having a solid ground connection so that both receivers and drivers can talk error free is imperative. The figure below shows how to make this connection and recommends adding some resistance between logic and chassis ground to avoid excess ground-loop currents. Logic ground does not have any resistance in its path from the driver or receiver. A potential problem might exist, especially during transients, when a high-voltage potential between the remote grounds could develop. Therefore, some resistance between them is recommended.



User's Notes:

MN-G55PC-01