Pentium PCI

Green M/B

USER'S GUIDE

PART NO.: MN-586S

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CHAPTER 1
Introduction

1.1 Introduction of the Pentium Processor

Intel's Pentium microprocessor introduces several new features and benefits not found in earlier Intel microprocessors. Following figure depicts the primary changes to the Pentium microprocessor over the i486 microprocessor. These changes fall into six major areas:

- Wider Data Bus (64 bits)
- Dedicated Instruction Cache
- Dedicated Data Cache
- Two Separate Execution Units (integer math)
- Enhanced Floating-Point Execution Unit
- New Instructions

The 64-bit Data Path

The Pentium processor has a 64-bit data bus that permits eight bytes (a quadword) of information to be transferred to and from system memory in a single bus cycle. This wider data path permits faster cache line fills from its two internal caches. This wider data path is supported by a new 64-bit addressing scheme that uses eight byte enable lines.

Intruction Cache

The Pentium microprocessor incorporates a dedicated 8 KB instruction cache that feeds its two integer execution units and a floating-point unit via a dual instruction pipeline. The instruction cache is a read-only cache and is organized as a 2-way set associative cache with 32-byte lines.

Data Cache

The data cache is an 8 KB cache that serves all three execution units. The data cache is a write-back cache, and like the code cache, is organized as a 2-way set associative cache with 32-byte lines. External pins are implemented to control the write-back feature, thus, ensuring cache coherency with other caches and main memory.

The Parallel Integer Execution Units

The instruction pipeline includes two parallel paths called the "u" pipeline and the "v" pipeline. The dual instruction pipeline and execution unit allows two instructions to be decoded and executed simultaneously, permitting two instructions to complete execution in a single processor clock; hence, its superscalar performance.

Another feature of the Pentium microprocessor is its branch target buffer

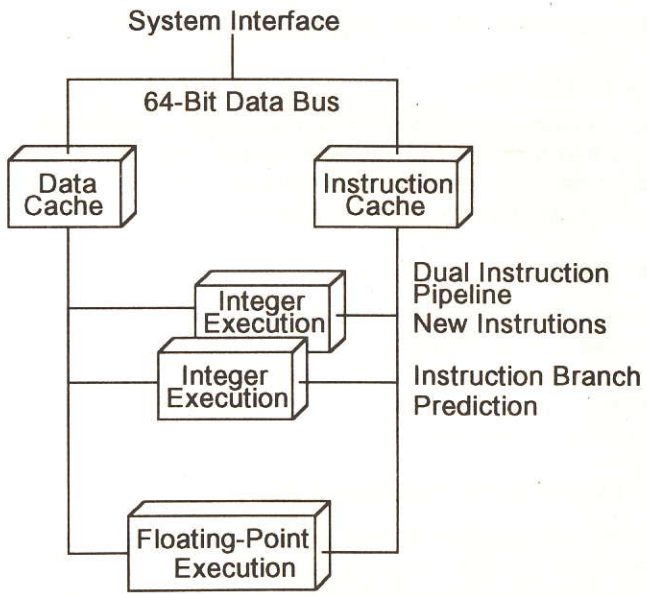
and branch predication algorithm. The branch target buffer keeps track of execution history to detemine when an instruction branch is likely to occur again. When a branch operation is predicted, the branch target buffer in conjunction with the prefetcher fetches the next instruction that is predicted, rather than continuing in a sequential fashion. This means that the execution pipelines do not always stall when a branch operation executes, as with earlier processors.

Floating-Point Unit

The floating-point unit employs a new design that provides substantial performance increases over the i486 design. The floating-point performance gains result mainly from pipelined execution of floating-point instructions.

New Instructions

Several new instructions have been added to the publicly documented instruction set in the Pentium processor.



The Pentium Microprocessor Enhancement

1.2 Introduction of PCI Bus

PCI stands for Peripheral Component Interconnect.

On 6/22/92 Intel released the specification of PCI Bus. It (PCI) is driving a new architecture for PC's - eliminating the I/O bottleneck of standard expansion busses. PCI provides a glueless interface for high performance peripherals such as LAN, SCSI, graphics and video to be placed onto a fast local bus. By utilizing this technology and incorporating read/write burst transfers, PCI bus can achieve a great throughput betten than VL-Bus.

All PCI data transfers are block data transfers and are accomplished using burst transfers. Each burst transfer consists of the following basic components.

- All PCI devices must support PCI operation within 0MHz ~ 33MHz.
- The address and transfer type are output during the address phase.
- A data object (32-bits) may then be transferred during each subsequent data phase.

When block 32-bits transfers are accomplished with no wait states inserted in each data phase, a transfer rate of 132M bytes/second may be achieved.

CHAPTER 2
Product Overview

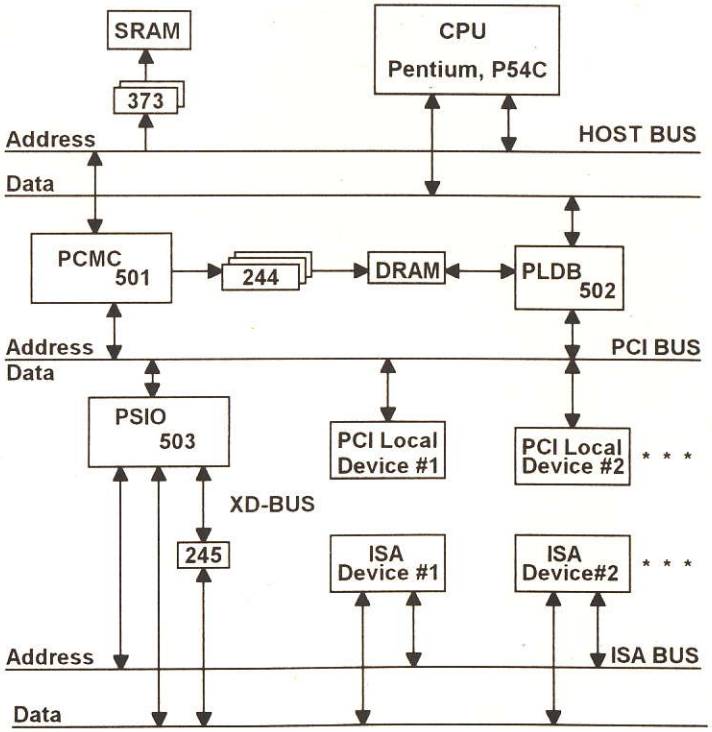
2.1 Pentium Board Specification

- Supports Intel Pentium 60/66 MHz CPU.
- Supports 256KB/512KB/1M 2nd Level Cache, Using 32Kx8/64Kx8/128Kx8 Asynchronous SRAM.
- Supports Single-Side plus 1 Double-Side DRAM Banks, or 2 Double-Side DRAM Banks. The Maximum Memory Size is upto 128MB.
- Supports 4 ISA Slots and 4 PCI Slots (4 PCI masters).
- Supports CPU SMM Mode.
- Supports CPU Clock Scaling Function (CPU Clock Down to 33 MHz).

2.2 SiS85C501/502/503 System Block Diagram

SiS85C501	PCI/ISA Cache Memory Controller (PCMC)
SiS85C502	PCI Local Data Buffer (PLDB)
SiS85C503	PCI System I/O (PSIO)

The SiS85C501, 85C502, and 85C503 chipset provides fully integrated support for the Pentium/P54C PCI/ISA system. The chipset was developed by using a very high level of function integration and system partitioning. With the SiS85C501, SiS85C502, and SiS85C503 chipset, only 13 TTLs (include 3 DRAM address buffer) are required to implement a low cost, high performance, Pentium/P54C PCI/ISA system. Following figure shows the system block diagram.



System Block Diagram

2.3 Feagures of SiS85C501/502/503

SiS85C501

- Supports the Pentium Processor at 60MHz or 66MHz Bus speed.
- Supports the P54C Processor at 50MHz, 60MHz or 66MHz Bus Speed.
- Supports the Pipelined Address Mode of the Pentium or the P54C Processor.
- Integrated Second Level (L2) Cache Controller.
  - Write Through and Write Back Cache Modes.
  - Direct Mapped Organization.
  - Supports Standard and Burst SRAMs.
  - Supports 64KBytes to 2MBytes Cache Sizes.
  - Cache Read/Write Cycle of 3-2-2-2 or 4-3-3-3 Using Standard SRAMs at 66MHz
  - Cahce Read/Write Cycle of 3-1-1-1 Using Burst SRAMs at 66MHz.
- Integrated DRAM Controller.
  - Supports 2MBytes to 128MBytes of Cacheable Main Memory.
  - Concurrent Write Back.
  - CAS#-before-RAS# Transparent DRAM Refresh.
  - 256K/1M/4M/16M x N 70ns Fast Page Mode DRAM Support.
  - Programmable DRAM Speed.
- Two Programmable Non-Cacheable Regions.
- Option to Disable Local Memory in Non-Cacheable Regions.
- Shadow RAM in Increments of 16KBytes.
- Supports Pentium/P54C SMM Mode.
- Supports CPU Stop Clock.
- Provides High Performance PCI Arbiter.
  - Supports Four PCI Masters.
  - Supports Rotating Priority Mechanism.
  - Hidden Arbitration Scheme Minimizes Arbitration Overhead.

- Integrated PCI Bridge.
  - Translates the CPU Cycles into the PCI Bus Cycles.
  - Provides CPU-to-PCI Read Assembly and Write Disassembly Mechanism.
  - Translates Sequential CPU-to-PCI Memory Write Cycles into PCI Burst Cycles.
  - PCI Burst Write in the Pace of X-2-2-2-....
  - PCI Burst Read L2 Cache in X-2-2-2-....
  - PCI Burst Read DRAM in X-3-2-3-2....
  - Cache Snoop Filters Ensure Data Coherency and Minimize Snoop Frequency.
- 208-Pin PQFP Package.
- 0.6um CMOS Technolgy.

SiS85C502

- Supports the Full 64-Bit Pentium Processor Data Bus.
- Provides a 64-Bit Interface to DRAM Memory.
- Provides a 32-Bit Interface to PCI.
- Three Integrated Posted Write Buffers and Two Read Buffers Increase System Performance.
  - 1 level CPU-to-Memory Posted Write Buffer (CTMPB) with 4 QuadWords (QWs) Deep.
  - 4 level CPU-to-PCI Posted Write Buffer (CTPPB) with 4 Double Words (DWs) Deep.
  - 1 level PCI-to-Memory Posted Write Buffer (PTMPB) with 1 QW Deep.
  - 1 level Memory-to-CPU Read Buffer (CRMB) with 1 QW Deep.
  - 1 level Memory-to-PCI Read Buffer (PRMB) with 1 QW Deep.
- Near Zero Wait State Performance on CPU-to-Memory and CPU-to-PCI Writes.
- Operates Synchronously to the 66.7 MHz CPU and 33.3 MHz PCI Clocks.
- Provides Parity Generation for Memory Writes.
- 208-Pin PQFP.
- 0.6um CMOS Technology.

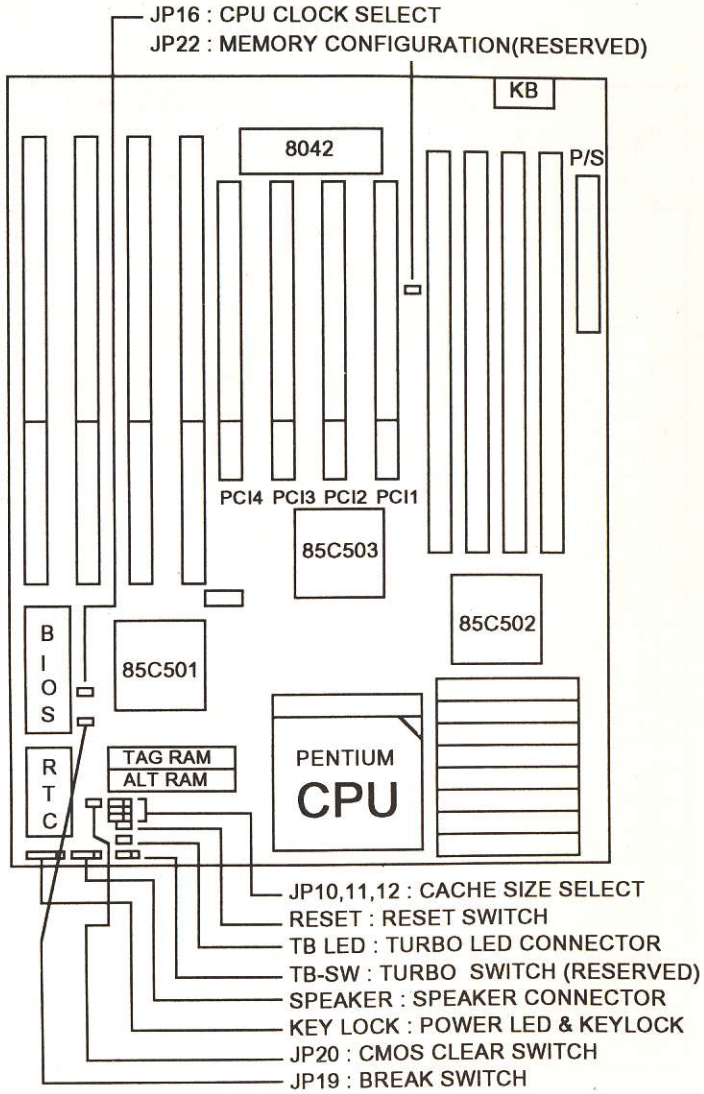
SiS85C503

- Integrated Bridge Between PCI Bus and ISA Bus.
  - Translates PCI Bus Cycles into ISA Bus Cycles.
  - Translates ISA Master or DMA Cycles into PCI Bus Cycles.
  - Provides PCI-to-ISA Memory one Double Word Posted Write Buffer.
- Integrated ISA Bus Compatible Logic.
  - ISA Bus Controller.
  - ISA Arbiter for ISA Master, DMA Devices, and Refresh.
  - Built-in Two 8237 Compatible DMA Controllers.
  - Built-in Two 8259A Compatible Interrupt Controllers.
  - Built-in One 8254 Timer.
- Supports Reroutibilty of Four PCI Interrupts to Any Unused IRQ Interrupt.
- Supports Flash ROM.
- 160-Pin PQFP.
- 0.6um CMOS Technology.

CHAPTER 3

Hardware Description

3.1 Board Outlines and Connectors

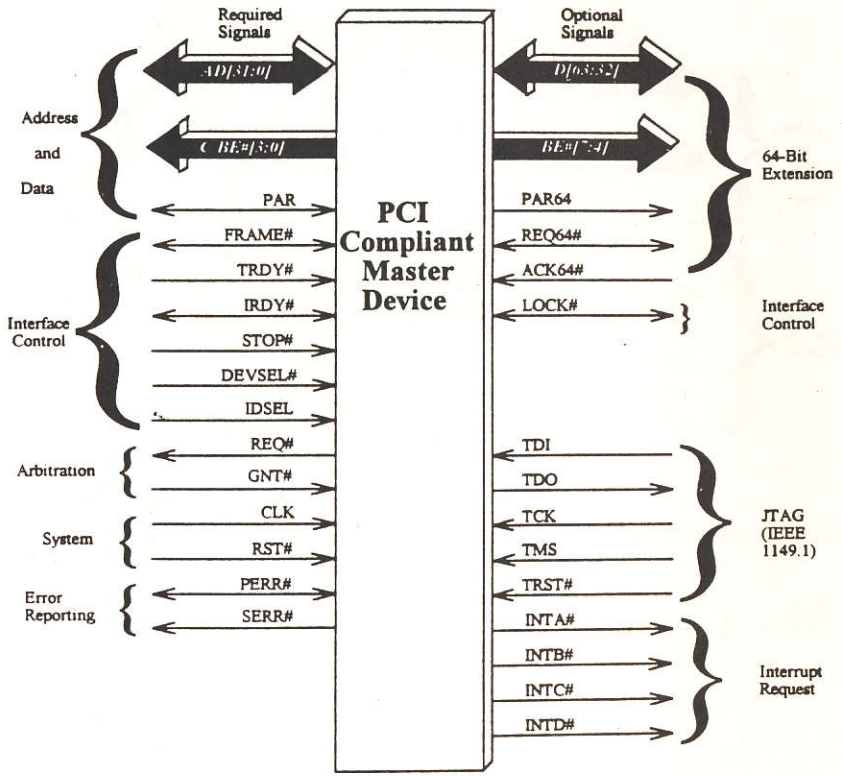


The following charts summarize pin assignments for the PCI slot.

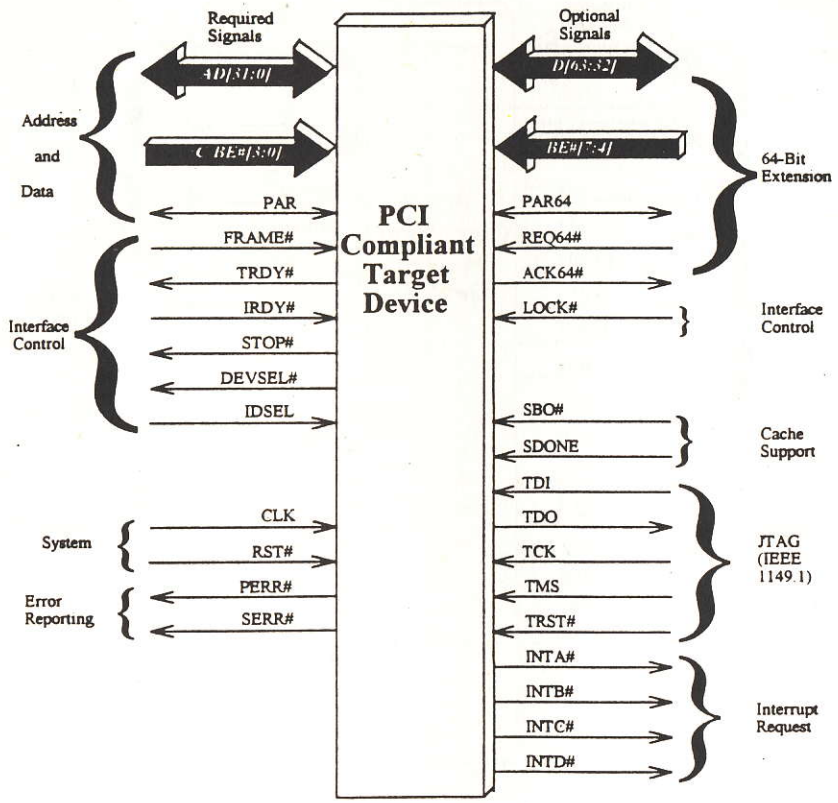
PCI SLOT

	5V Card			5V Card	
Pin	Side B	Side A	Pin	Side B	Side A
1	-12V	TRST#	32	AD[17]	AD[16]
2	TCK	+12V	33	C/BE#[2]	+3.3V
3	Ground	TMS	34	Ground	FRAME#
4	TDO	TDI	35	IRDY#	Ground
5	+5V	+5V	36	+3.3V	TRDY#
6	+5V	INTA#	37	DEVSEL#	Ground
7	INTB#	INTC#	38	Ground	STOP#
8	INTD#	+5V	39	LOCK#	+3.3V
9	PRSNT1#	Reserved	40	PERR#	SDONE
10	Reserved	+5V	41	+3.3V	SBO#
11	PRSNT2#	Reserved	42	SERR#	Ground
12	Ground	Ground	43	+3.3V	PAR
13	Ground	Ground	44	C/BE[1]#	AD[15]
14	Reserved	Reserved	45	AD[14]	+3.3V
15	Ground	RESET#	46	Ground	AD[13]
16	CLK	+5V	47	AD[12]	AD[11]
17	Ground	GNT#	48	AD[10]	Ground
18	REQ#	Ground	49	Ground	AD[09]
19	+5V	Reserved	50	Keyway	
20	AD[31]	AD[30]	51	Keyway	
21	AD[29]	+3.3V	52	AD[08]	C/BE#[0]
22	Ground	AD[28]	53	AD[07]	+3.3V
23	AD[27]	AD[26]	54	+3.3V	AD[06]
24	AD[25]	Ground	55	AD[05]	AD[04]
25	+3.3V	AD[24]	56	AD[03]	Ground
26	C/BE#[3]	IDSEL	57	Ground	AD[02]
27	AD[23]	+3.3V	58	AD[01]	AD[00]
28	Ground	AD[22]	59	+5V	+5V
29	AD[21]	AD[20]	60	ACK64#	REQ64#
30	AD[19]	Ground	61	+5V	+5V
31	+3.3V	AD[18]	62	+5V	+5V

PCI-Compliant Master Device Signals



PCI-Compliant Target Device Signals



The following charts summarize pin assignments for the I/O channel

ISA A-SIDE SLOT

I/O PIN	SIGNAL NAME	INPUT/OUTPUT
A1	I/O CHECK	I
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	I/O CH RDY	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA09	I/O
A23	SA08	I/O
A24	SA07	I/O
A25	SA06	I/O
A26	SA05	I/O
A27	SA04	I/O
A28	SA03	I/O
A29	SA02	I/O
A30	SA01	I/O
A31	SA00	I/O

ISA B-SIDE SLOT

I/O PIN	SIGNAL NAME	INPUT/OUTPUT
B1	GND	GROUND
B2	RESETDRV	I
B3	+5VDC	POWER
B4	IRQ9	I
B5	-5VDC	POWER
B6	DRQ2	I
B7	-12VDC	POWER
B8	OWS	I
B9	+12VDC	POWER
B10	GND	POWER
B11	SMEMW	O
B12	SMEMR	O
B13	IOW	I/O
B14	IOR	I/O
B15	DACK3	O
B16	DRQ3	I
B17	DACK1	O
B18	DRQ1	O
B19	REFRESH	I/O
B20	CLK	O
B21	IRQ7	I
B22	IRQ6	I
B23	IRQ5	I
B24	IRQ4	I
B25	IRQ3	I
B26	DACK2	O
B27	T/C	O
B28	BALE	O
B29	+5VDC	POWER
B30	OSC	O
B31	GND	GROUND

ISA C-SIDE SLOT

I/O PIN	SIGNAL NAME	INPUT/OUTPUT
C1	SBHE	I/O
C2	LA23	I/O
C3	LA22	I/O
C4	LA21	I/O
C5	LA20	I/O
C6	LA19	I/O
C7	LA18	I/O
C8	LA17	I/O
C9	MEMR	I/O
C10	MEMW	I/O
C11	SD08	I/O
C12	SD09	I/O
C13	SD10	I/O
C14	SD11	I/O
C15	SD12	I/O
C16	SD13	I/O
C17	SD14	I/O
C18	SD15	I/O

ISA D-SIDE SLOT

I/O PIN	SIGNAL NAME	INPUT/OUTPUT
D1	MEMCS 16	I
D2	IOCS 16	I
D3	IRQ10	I
D4	IRQ11	I
D5	IRQ12	I
D6	IRQ15	I
D7	IRQ14	I
D8	DACK0	O
D9	DRQ0	I
D10	DACK5	O
D11	DRQ5	I
D12	DACK6	O
D13	DRQ6	I
D14	DACK7	O
D15	DRQ7	I
D16	+5V	POWER
D17	MASTER	I
D18	GND	GROUND

3.2 Jumpers and Connectors Summary

Before installing your Pentium Board, the jumpers and connectors are set to the correct position.

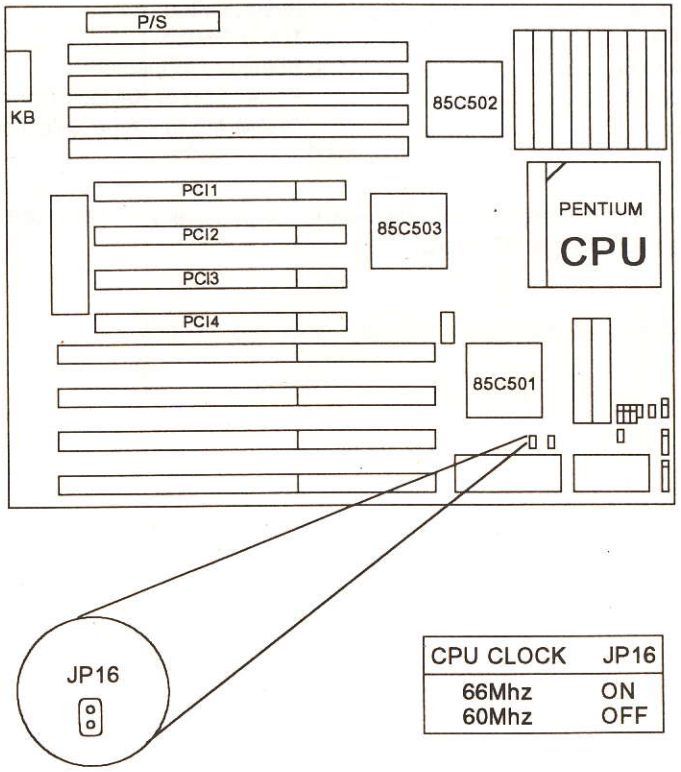
There are:

JP10,JP11,JP12.....Cache Size Selection
JP16.....Cache Size Selection
JP19.....Break Switch
JP20.....Clear CMOS
RESET.....Reset Switch
* TB SW.....Turbo Switch
SPEAKER.....Speaker Connector
KEYLOCK.....Power LED & Keylock Connector
• JP22.....DRAM Module type Selection

* TB SW :
This switch is reserved for "Revision C" or later version. User can identify the version on the PC board.

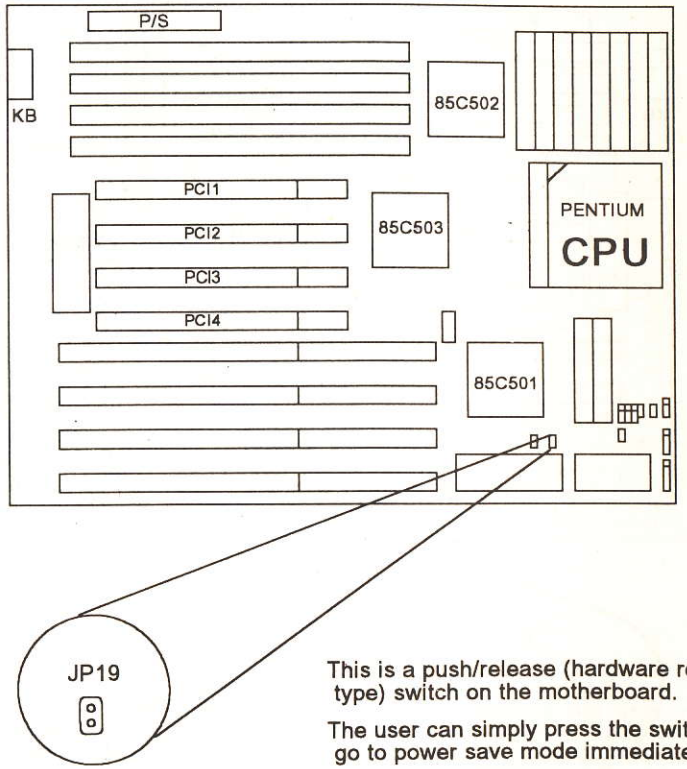
• JP22 :
This switch is reserved for "Revision B" or later version.

JP 16 : CPU CLOCK SELECTION



CPU CLOCK	JP16
66Mhz	ON
60Mhz	OFF

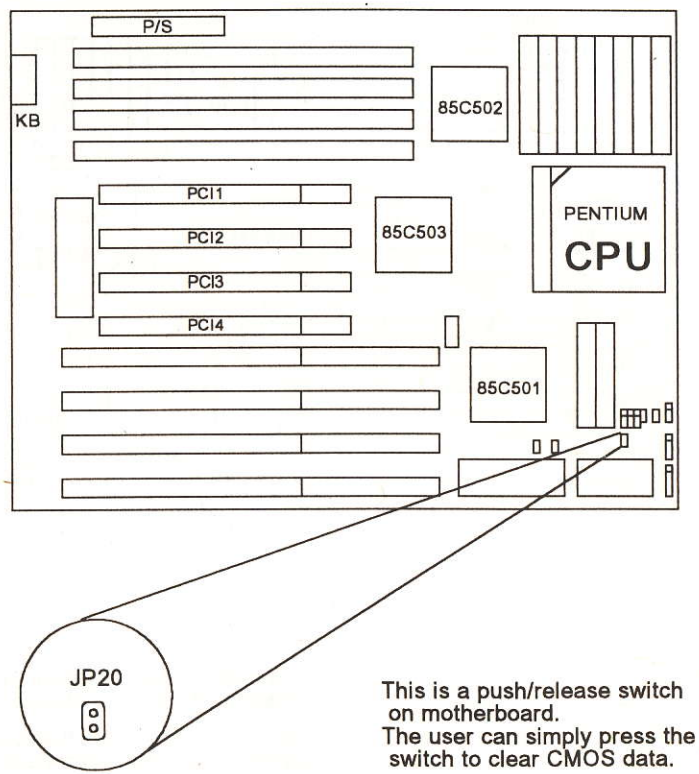
JP19 : BREAK SWITCH



This is a push/release (hardware reset type) switch on the motherboard.

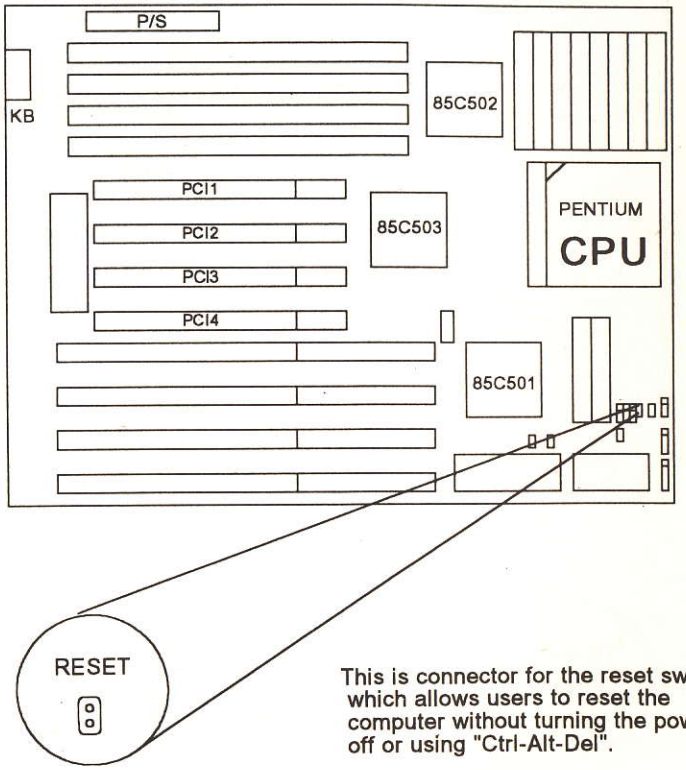
The user can simply press the switch to go to power save mode immediately.

JP20 : CMOS CLEAR SWITCH



This is a push/release switch on motherboard.
The user can simply press the switch to clear CMOS data.

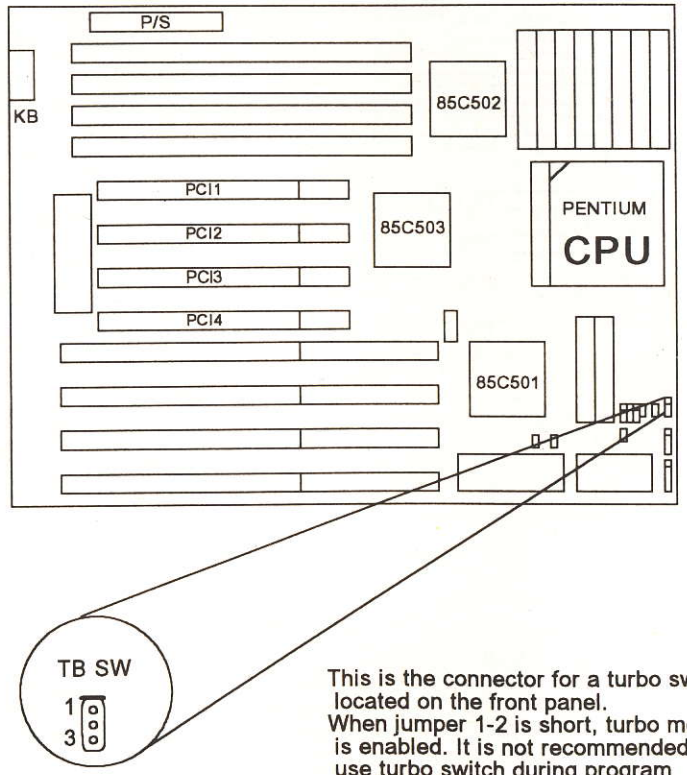
RESET : RESERT SWITCH



This is connector for the reset switch which allows users to reset the computer without turning the power off or using "Ctrl-Alt-Del".

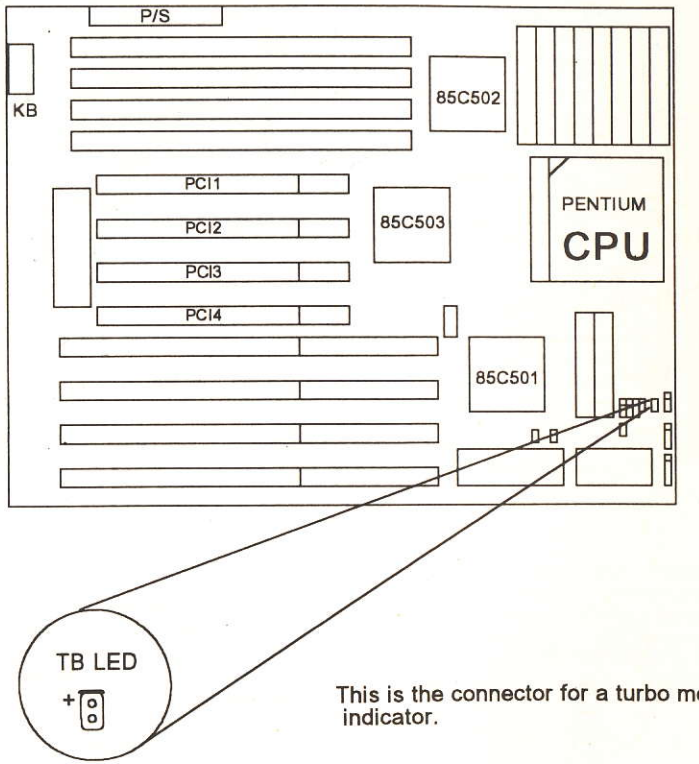
TB-SW : TURBO SWITCH CONNECTOR

This turbo switch function is reserved for "REV. C" or later version. Users can identify the version on PC board.



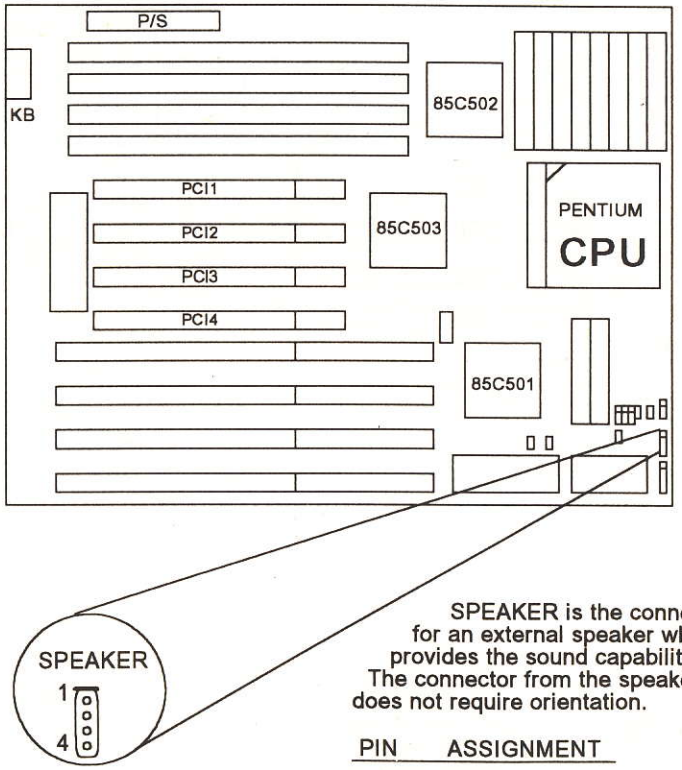
This is the connector for a turbo switch located on the front panel.
When jumper 1-2 is short, turbo mode is enabled. It is not recommended to use turbo switch during program execution.

TB-LED : TURBO LED CONNECTOR



This is the connector for a turbo mode indicator.

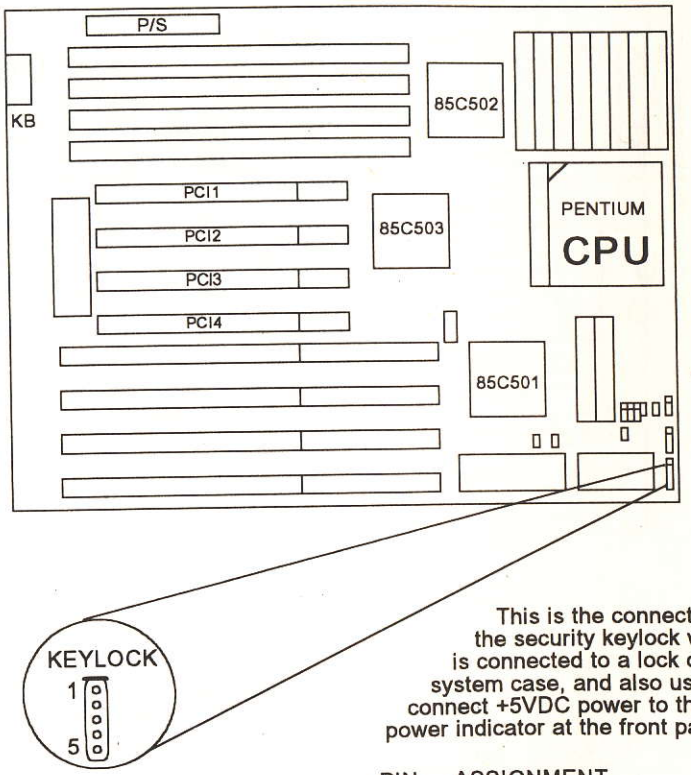
SPEAKER : SPEAKER CONNECTOR



SPEAKER is the connector for an external speaker whitch provides the sound capability. The connector from the speaker does not require orientation.

PIN	ASSIGNMENT
1	DATA
2	GROUND
3	GROUND
4	+5 VDC

KEYLOCK : POWER LED & KEYLOCK CONNECTOR

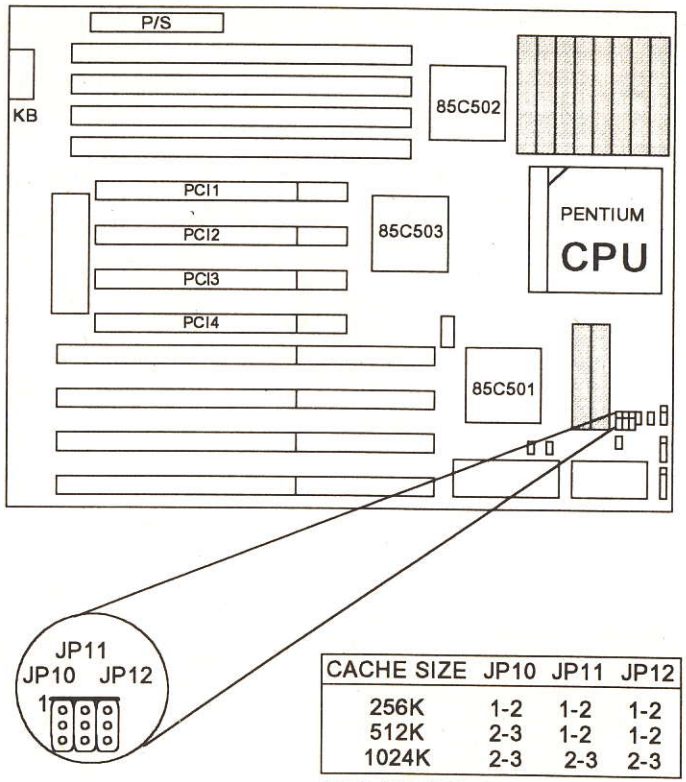


This is the connector for the security keylock which is connected to a lock on the system case, and also used to connect +5VDC power to the power indicator at the front panel.

PIN	ASSIGNMENT
1	POWER LED
2	KEY(N/C)
3	GROUND
4	KEYBOARD LOCK
5	GROUND

3.3 Cache Memory Installation

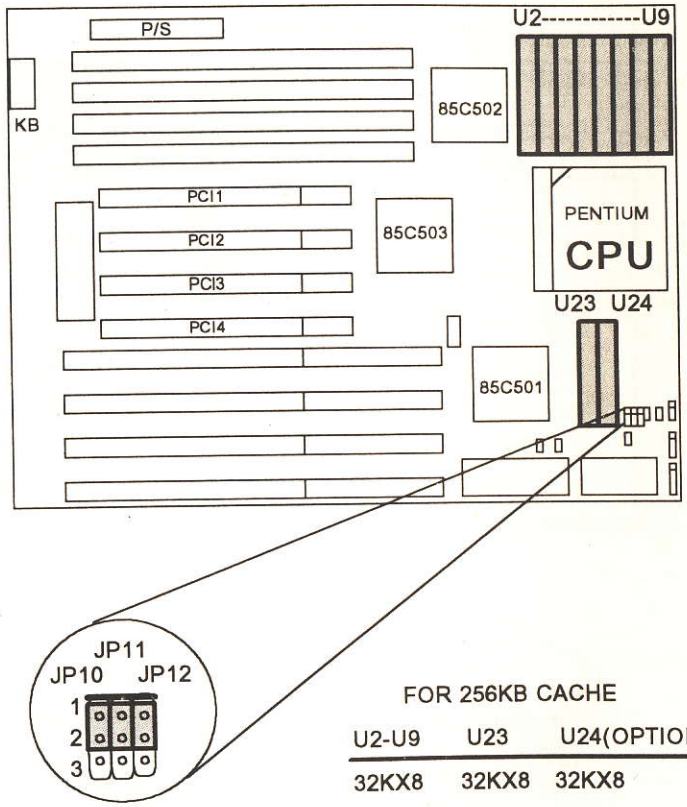
JP10,JP11,JP12 : CACHE MEMORY SIZE SELECT



CACHE SIZE	JP10	JP11	JP12
256K	1-2	1-2	1-2
512K	2-3	1-2	1-2
1024K	2-3	2-3	2-3

CACHE DATA RAM : U2-U9
CACHE TAG RAM : U23
CACHE ALT RAM : U24 (OPTIONAL)

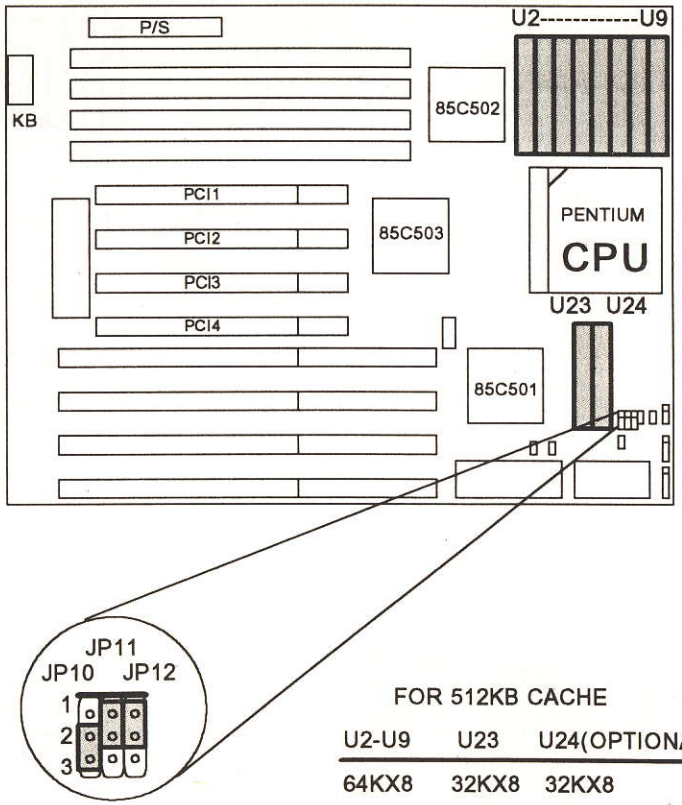
JP10,JP11,JP12 FOR 256KB CACHE



FOR 256KB CACHE

U2-U9	U23	U24(OPTIONAL)
32KX8	32KX8	32KX8

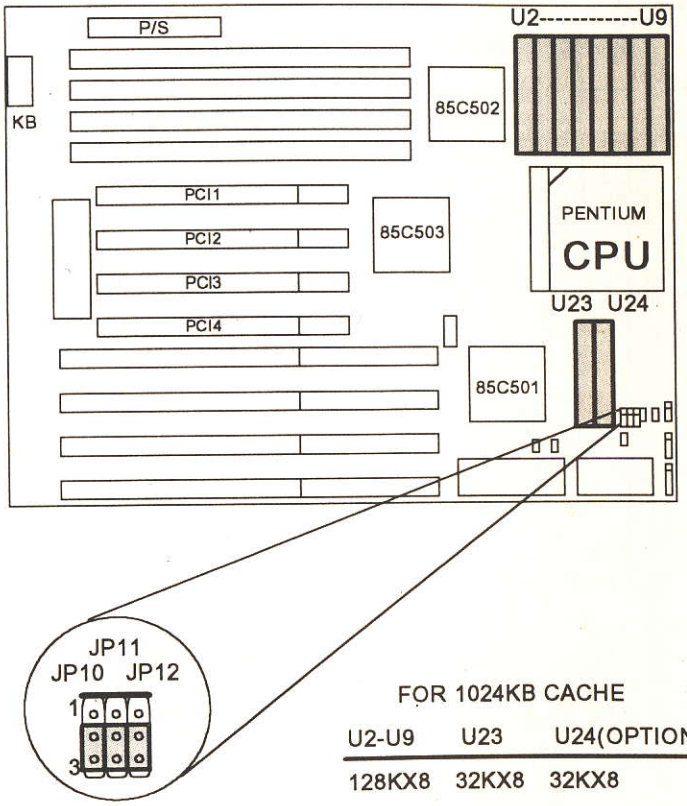
JP10,JP11,JP12 FOR 512KB CACHE



FOR 512KB CACHE

U2-U9	U23	U24(OPTIONAL)
64KX8	32KX8	32KX8

JP10,JP11,JP12 FOR 1024KB (1MB) CACHE



FOR 1024KB CACHE

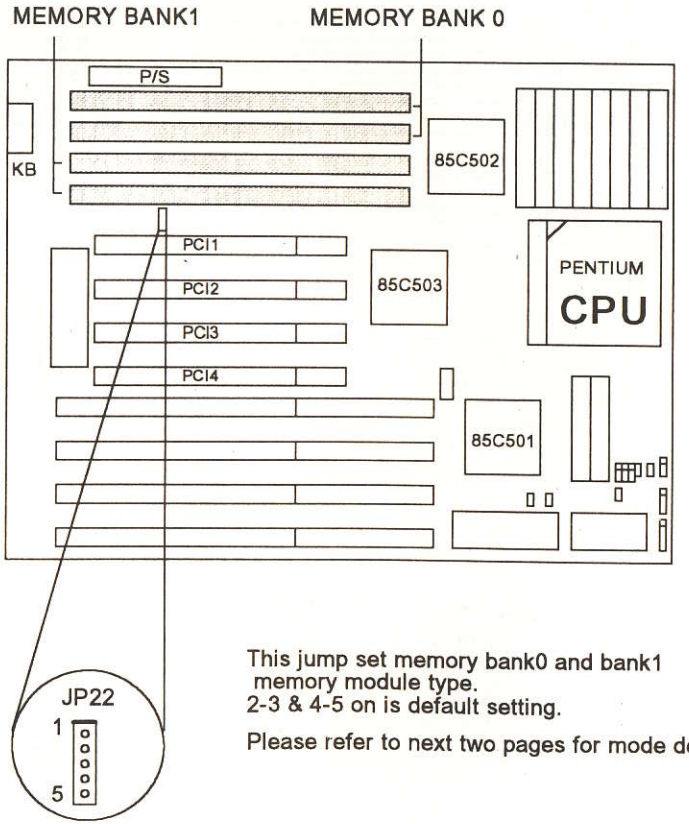
U2-U9	U23	U24(OPTIONAL)
128KX8	32KX8	32KX8

3.4 Memory Module Installation

The memory configuration for "REV. A" PC board is same as page 35.

JP22 : MEMORY CONFIGURATION SETTING

This jump is reserved for "REV. B" or later version PC board.



This jump set memory bank0 and bank1 memory module type.
2-3 & 4-5 on is default setting.

Please refer to next two pages for mode detail.

ird.

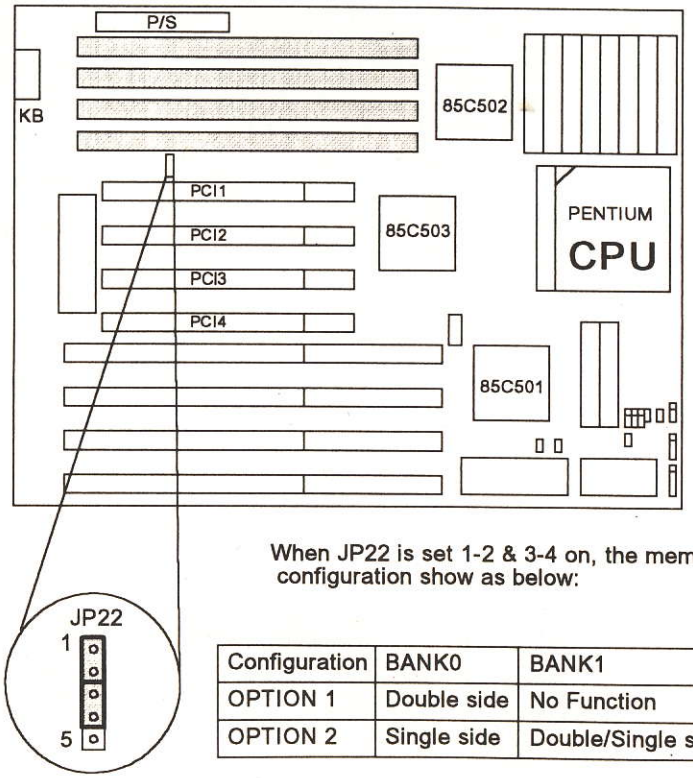
RE:SIMM MODULE FOR SUNTAC PENTIUM 60/66 MHZ MB
FOR THE SUNTAC PENTIUM 60/66 MHZ MBS VERSION-A USING THE FOLLOWING COMBINATION OF SIMM MODULES:

MEMORY	BANK0		BANK1	
SIZE	SIMM1	SIMM2	SIMM1	SIMM2
2MB	1MB-S	1MB-S	X	X
4MB	2MB-D	2MB-D	X	X
8MB	2MB-D	2MB-D	2MB-D	2MB-D
8MB	4MB-S	4MB-S	X	X
16MB	8MB-D	8MB-D	X	X
20MB	2MB-D	2MB-D	8MB-D	8MB-D
32MB	8MB-D	8MB-D	8MB-D	8MB-D
32MB	16MB-S	16MB-S	X	X
36MB	2MB-D	2MB-D	16MB-S	16MB-S
48MB	8MB-D	8MB-D	16MB-S	16MB-S
64MB	32MB-D	32MB-D	X	X
80MB	8MB-D	8MB-D	32MB-D	32MB-D
128MB	32MB-D	32MB-D	32MB-D	32MB-D
128MB	64MB-S	64MB-S	X	X

NOTE: "S" SINGLE SIDE DRAM MODULES
"D" DOUBLE SIDE DRAM MODULES

JP22 : MEMORY CONFIGURATION SETTING

This jump is reserved for "REV. B" or later version PC board.



When JP22 is set 1-2 & 3-4 on, the memory configuration show as below:

Configuration	BANK0	BANK1
OPTION 1	Double side	No Function
OPTION 2	Single side	Double/Single side

CHAPTER 4

System Setup

4.1 Award BIOS Setup Utility

Once you enter Award BIOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from ten setup functions and two exit choices. Use arrow keys to select among the items and press <Enter> to accept or enter the sub-menu.

ROM PCI/ISA BIOS (2A5IA000)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.

STANDARD CMOS SETUP	PASSWORD SETTING
BIOS FEATURES SETUP	IDE HDD AUTO DETECTION
CHIPSET FEATURES SETUP	HDD LOW LEVEL FORMAT
POWER MANAGEMENT SETUP	SAVE & EXIT SETUP
PCI CONFIGURATION SETUP	EXIT WITHOUT SAVING
LOAD BIOS DEFAULTS	
LOAD SETUP DEFAULTS	
ESC : Quit	PU/PD/+/- : Modify
F1 : Help	(Shift)F2 : Change Color
Time, Date, Hard Disk Type..	

Standard CMOS setup
This setup page includes all the items in a standard compatible BIOS. See page 40 for details.

BIOS features setup
This setup page includes all the items of Award special enhanced features. See page 42 to 43 for details.

Chipset features setup
This setup page includes all the items of chipset special features. See page 44 for details.

Powe Management Setup
This setup page includes all the power management features. Details refer to page 45.

PCI Configuration Setup
This setup page includes all the PCI features. Details refer to page 47.

Load BIOS defaults
BIOS defaults include the most appropriate value of the system parameter which the system would be in minimum performance. However, you may change the parameter value through the Option Page Setup Menu.

Load Setup defaults
Setup defaults indicates the values required by the system for the maximum performance. However, you may change the parameter through the Option Page Setup Menu.

Password setting
Change, set, or disable password. It allows you to limit access to the system and setup, or just to Setup. See page 48 for details.

IDE HDD auto detection
Automatically configure hard disk parameters.

HDD low level format
Hard disk low level format utility.

Save & exit setup
Save CMOS value changes to CMOS and exit setup.

Exit without save
Abandon all CMOS value changes and exit setup.

4.2 Standard CMOS Setup

This items in Standard CMOS Setup Menu are divided into 10 categories. Each category includes no, one or more than one setup items. Use the arrow keys to highlight the item and then use the <PgUp> or <PgDn> keys to select the value you want in each item.

ROM PCI/ISA BIOS (2A5IA000)
STANDARD CMOS SETUP
AWARD SOFTWARE, INC.

```
Date (mm:dd/yy) : Sat, Oct 22 1994
Time (hh:mm:ss) : 10 : 28 : 17

                        CYLS. HEADS  PRECOMP LANDZONE SECTORS  MODE
Drive C : User (521Mb)  1060    16    65535    1059      63   NORMAL
Drive D :  None(  0Mb)     0     0        0       0       0   -----

Drive A : 1.2M, 5.25 in.
Drive B : 1.44M, 3.5 in.

Video   : EGA/VGA
Halt On : All Errors

                        Base Memory  :  640K
                     Extended Memory : 15360K
                       Other Memory  :  384K

                        Total Memory : 16384K

ESC :  Quit          ↓→↑← : Select Item      PU/PD/+/- : Modify
F1  :  Help          (Shift)F2  : Change Color
```

Date
The date format is <day>, <date><month><year>. Press <F3> to show calendar.

Time
The time format is ur><minute><second>. The time is calculated base on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00.

Drive C type/Drive D type
The category identify the types of hard disk drive C or drive D that has been installed in the computer. There are 46 predefined types and a user definable type. Type 1 to Type 46 are predefined. Type User is user-definable.

Drive A type/Drive B type
The category identify the types of floppy disk drive A or drive B that has been installed in the computer. The options are 360KB 5 ¼ ", 1.2MB 5 ¼ ", 720KB 3 ½ ", 1.44MB 3 ½ ", 2.88MB 3 ½ ", and None.

Video
The category selects the type of adapter used for the primary system monitor that must matches your video display card and monitor. The options are EGA/VGA, CGA 40, CGA 80, MONO.

Error halt
The category determines whether the computer will stop if an error is detected during power up.

4.3 BIOS Features Setup

Virus Warning
This category flashes on the screen. During and after the system boots up any attempt to write to the boot sector or partition table of the hard disk drive will halt the system and the following error message will appear, in the mean time, you can run anti-virus program to locate the problem.

ROM PCI/ISA BIOS (2A5IA000)
BIOS FEATURES SETUP
AWARD SOFTWARE, INC.

Virus Warning	: Enabled	Video BIOS Shadow	: Enabled
CPU Internal Cache	: Enabled	C8000-CBFFF Shadow	: Disabled
External Cache	: Enabled	CC000-CFFFF Shadow	: Disabled
Quick Power On Self Test	: Enabled	D0000-D3FFF Shadow	: Disabled
Boot Sequence	: A, C	D4000-D7FFF Shadow	: Disabled
Swap Floppy Drive	: Disabled	D8000-DBFFF Shadow	: Disabled
Boot Up Floppy Seek	: Enabled	DC000-DFFFF Shadow	: Disabled
Boot Up NumLock Status	: On		
IDE HDD Block Mode	: Disabled		
Gate A20 Option	: Fast		
Security Option	: Setup		

ESC :Quit	↓→↑←: Select Item
F1 :Help	PU/PD/+/- :Modify
F5 :Old Values	(Shift)F2 :Color
F6 :Load BIOS Defaults	
F7 :Load BIOS Defaults	

CPU Internal Cache/External Cache
These two categories speed up memory access.

Quick Power On Self Test
This category speeds up Power On Self Test (POST) after you power on the computer. If it is set to Enable, BIOS will shorten or skip some check items during Power On Self Test.

Boot Sequence
This category determines which drive computer searches first for the disk operating system (i.e. DOS). Default value is A.C.

Boot Up Floopy Seek
During POST, BIOS will determine if the floopy disk drive installed is 40 or 80 tracks.

Boot Up NumLock Status
The default value is On. When "On" the keypad is mumber keys, otherwise the keypad is arrow keys.

Boot Up System Speed
It selects the default system speed - the speed that the system will run immediately after power up. The options are High or Low.

IDE HDD Block Mode
When enabled, the IDE hard disk allows data to be transferred to and from the IDE drive in multiple sector blocks at one time. There is an additional setup option to disable or enable this function.

Security Option
This category allows you to limit access to the system and setup, or just Setup.

Video BIOS Shadow
It determines whether video BIOS will be copied to RAM. Video BIOS Shadow will increase the video speed.

C8000 -CBFFF Shadow/EC000 - EFFFF Shadow
These categories detemine whether optional ROM will be copied to RAM by 16K byte.

4.4 Chipset Features Setup

This portion of the BIOS setup is entirly chipset specific and requires knowledge about the particular chip set in use. This option is used to change the register values for the chipset registers. These registers control most of the system options in the computer.

Auto Configuration

By enabling this option, system BIOS will automatically detect CPU speed and configure the DRAM speed. CACHE read/write timing and BUS frequency.

ROM PCI/ISA BIOS (2A5IA000)
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.

Auto Configuration	: Enabled	PCI Clock Frequency	: CPUCLK/2
		ISA Bus Clock Frequency	: PCICLK/4
Read CAS Pulse Width	: 4T		
DRAM Write CAS Width	: 2T	Non-Cacheable Block 1	: Disabled
L2 Cache Update Mode	: WB	Block 1 Start Address	: Disabled
L1 Cache Update Mode	: WB	Block 1 Size	: 64KB
L2 (WB) Tag Bit Length	: 8 bits		
SRAM Speed Option	: Slower		
SRAM Burst R/W Cycle	: 2T		
System BIOS Cacheable	: Disabled		
Video BIOS Cacheable	: Disabled		
		ESC :Quit	↓→↑←: Select Item
		F1 :Help	PU/PD/+/- :Modify
		F5 :Old Values	(Shift)F2 :Color
		F6 :Load BIOS Defaults	
		F7 :Load BIOS Defaults	

Note : All above values are default.

4.5 Power Management Setup

Power management

The options for Power Management is Disable, Enable, Minimum, Maximum and User define. When disable, the Power Management will inactive. Otherwise the HDD Power Down, System Doze, System Standby will active according to the PM (Power Management) timers.

ROM PCI/ISA BIOS (2A5IA000)
CMOS SETUP UTILITY
POWER MANAGEMENT SETUP

Power Management	: User Define	VGA Activity	: Enable
PM Control by APM	: Yes	IRQ3 (COM 2)	: Enable
Video Off Option	: Suspend -> Off	IRQ4 (COM 1)	: Enabled
Video Off Method	: V/H SYNC+Blank	IRQ5 (LPT 2)	: Enable
Suspend Switch	: Enable	IRQ6 (Floppy Disk)	: Enable
Doze Speed (div by)	: 2	IRQ7 (LPT 1)	: Enable
Sydby Speed(div by)	: 3	IRQ8 (RTC Alarm)	: Disable
** PM Tmiers **		IRQ9 (IRQ2 Redir)	: Enable
HDD Power Down	: Disable	IRQ10 (Reserved)	: Enable
Doze Mode	: 15 Min	IRQ11 (Reserved)	: Enable
Standby Mode	: 10 Min	IRQ12 (Reserved)	: Enable
Suspend Mode	: 20 Sec	IRQ13 (PS/2 Mouse)	: Enable
		IRQ14 (Hard Disk)	: Enable
** PM Events **		IRQ15 (Reserved)	: Enable
COM Ports Activity	: Enable	ESC :Quit	↓→↑←: Select Item
LPT Ports Activity	: Enable	F1 :Help	PU/PD/+/- :Modify
HDD Ports Activity	: Enalbe	F5 :Old Values	(Shift)F2 :Color
PCI/ISA Master Act.	: Enable	F6 :Load BIOS Defaults	
IRQ1-15 Activity	: Enable	F7 :Load BIOS Defaults	

PM Control by APM (Advanced Power Management)

When set YES, the Power Management will control by APM.

Video Off Option

Number of minutes after which the monitor's V-sync & H-sync will cut off. The options are Always On, Suspend Off, Susp/Stdby Off and All Modes Off.

Break Switch
This is a push/release (hareware reset type) switch. The user can simply press the switch to go to suspend mode immdeiately. The options are RC Pin, DeTurbo Pin and Diable.

PM Timers
The System Doze, Standby and Suspend modes will active step by step according to PM Times.

PM Events
The system will resume immediately by PM Events through Local Master, Local Device, Video, DMA, IRQ1 to IRQ14.

4.6 PCI Configuration Setup

This portion of the BIOS is requires knowledge about the hardware interrupt (IRQn) in use. This option is used to change the PCI's INT# & IRQ# for the PCI slot. The follow figure are default values. It is suitable for most of PCI Add-Ons.

ROM PCI/ISA BIOS (2A5IA000)
PCI CONFIGURATION SETUP
AWARD SOFTWARE, INC.

Slot 1 Using INT#	: AUTO
Slot 2 Using INT#	: AUTO
Slot 3 Using INT#	: AUTO
SLOT 4 Using INT#	: AUTO
1st Available IRQ	: 9
2nd Available IRQ	: 10
3rd Available IRQ	: 11
4th Available IRQ	: 12
PCI IRQ Actived By	: Edge
PCI IDE IRQ Map To	: PCI
Primary IDE INT#	: A
Secondary IDE INT#	: B

ESC:Quit ↓→↑←: Select Item
F1 :Help PU/PD/+/- :Modify
F5 :Old Values (Shift)F2 :Color
F6 :Load BIOS Defaults
F7 :Load BIOS Defaults

The options for "Slot X Using INT#" are : AUTO, A, B, C, and D.

The options for "Available IRQ" are : 3,4,5,7,9,10,11,12,14,15 and NA.

The options for "PCI IDE IRQ Map To" are : PCI and ISA, when it is set to "PCI" then the options for the "Primary IDE INT#" and "Secondary IDE INT#" are A, B, C and D.

4.7 Password Setting

When you select this function, the following message will appear at the center of the screen to assist you in creating password.

ENTER PASSWORD:

Type the password, up to eight characters, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password.

To disable password, just press <Enter> when you are prompted to enter password. A message will confirm the password being disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

PASSWORD DISABLED.

If you select System at Security Option of BIOS Features Setup Menu, you will be prompted for the password every time the system is rebooted or any time you try to enter Setup. If you select Setup at Security Option of BIOS Features Setup Menu, you will be prompted only when you try to enter Setup.

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