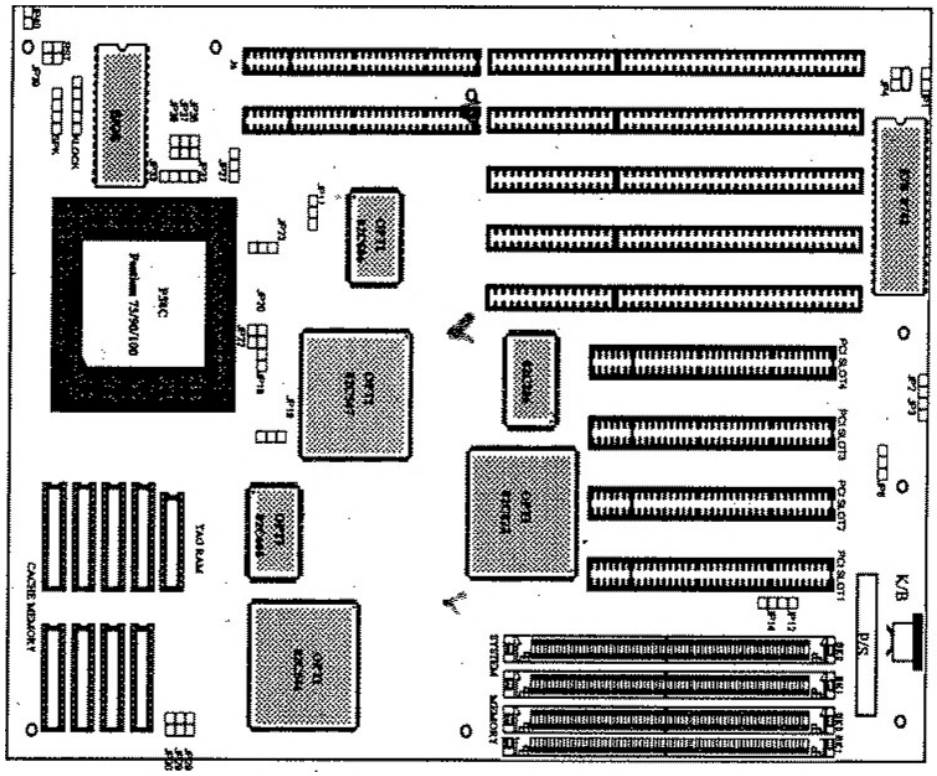
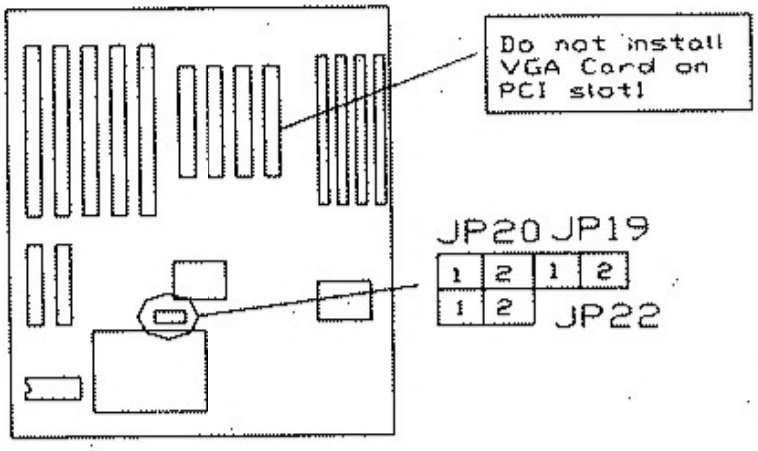
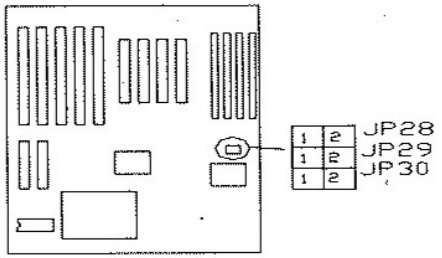




	JP19	JP20	JP22
100 MHz	▬	▬	▬
90 MHz	▬ ✔	▯▯ ✔	▬ ✔
75 MHz	▯▯	▯▯	▬



	JP28	JP29	JP30
256K			
512K			
1M			

	TAG RAM U38	DATA RAM U37, U39-U43, U47, U48
256K	8K*8	32K*8
512K	32K*8	64K*8
1M	32K*8	128k*8

TAG RAM uses 5V SRAM

DATA RAM uses 5V/3.3V *mixed mode SRAM

* mixed mode SRAM means VCC 5V, I/O 3.3V

Jumper Setting		Function
JP17		Always Invalidate Cache
		Invalidate Cache on Write
JP32		2/3 Bus/Core Ratio
		1/2 Bus/Core Ratio
JP27		128M DRAM on Board
		Memory Mapped I/O at Top of Memory
JP4		End of Last T2
		Beginning of Last T2
JP3		Disable Fast VESA Bus
		Enable Fast VESA Bus
JP12		3 AT Clock Added
		0 AT Clock Added
JP14		End of First T2
		End of Second T2
JP6		Clear CMOS Memory
		Normal Operation
JP36		VESA Bus 0 Wait
		VESA Bus 1 Wait