

54TPI

Pentium ISA/PCI System Board

User's Manual

Man-100
4/18/96

Quick Reference Section

Warning !!!

Cooling fan and heat sink must be placed on the Pentium CPU at all times. Manufacturers of motherboard and CPU are not responsible for any damages due to the absence of cooling fan and heat sink.

QUICK INTRODUCTION

CPU installation

The 54TPI supports Intel Pentium 75/90/100/120/133/150/166/180/200MHz microprocessors. Carefully install the Pentium processor into the ZIF socket at location U25. Make sure Pin One of the CPU corresponds to Pin One of the socket.

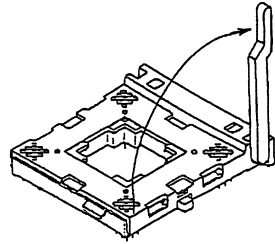
Power supply

The 54TPI system board has a built-in voltage regulator to convert the typical 5.0 Volt output from the regular PC/AT compatible power supply to the 3.3 Volts and VRE 3.45Volts required for the Pentium processor. You do not need to have a special power supply with 3.3 Volts and 3.45 Volts output for the system board.

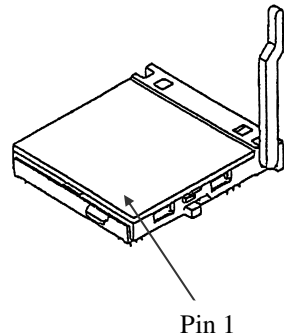
CPU INSTALLATION INSTRUCTIONS

54TPI uses a Single Lever ZIF (Zero Insertion Force) PGA (Pin Grid Array) socket for your CPU. To install your CPU, follow the steps below:

1. Rotate the actuator arm 90 degrees to its fully up right position.



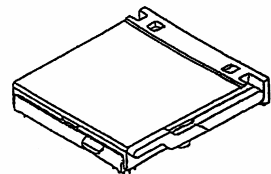
2. To insert the CPU, make sure the notched corner of the CPU is placed adjacent to the Pin One on the socket. The pins of CPU must be aligned with the holes of the sockets. **No force should be required to insert the CPU into the socket.**



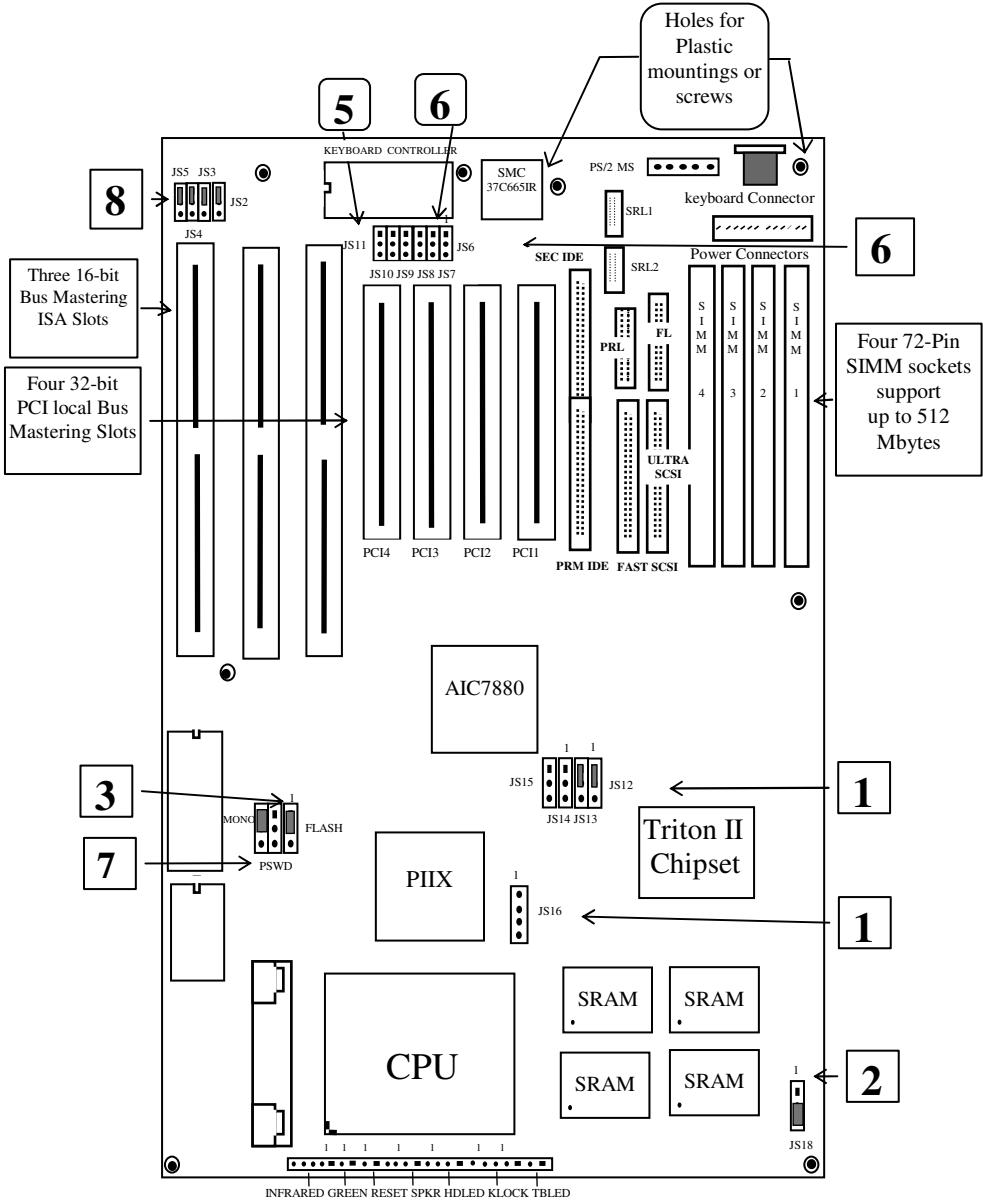
3. Rotate the actuator to a horizontal position, making sure it locks under the detent.

The CPU is now installed!

To remove the CPU, simply reverse the same procedure as shown and gently lift the CPU out of the socket.



Board Layout Quick Reference



Remark: The sample jumper setting shown above is set to Pentium-133MHz, 256K cache size.

JUMPER SETTING QUICK REFERENCE:

1) CPU clock Frequency Selection Jumper

CPU Speed	JS12	JS13	JS14	JS16
75 Mhz	1-2	2-3	2-3	Open
90 Mhz	1-2	1-2	1-2	Open
100 Mhz	2-3	2-3	1-2	Open
120 Mhz	1-2	1-2	1-2	3-4
133 Mhz	2-3	2-3	1-2	3-4
150 Mhz	1-2	1-2	1-2	1-2, 3-4
166 Mhz	2-3	2-3	1-2	1-2, 3-4
180 Mhz	1-2	1-2	1-2	1-2
200 Mhz	2-3	2-3	1-2	1-2

2) Jumper Setting for VRE CPU

CPU Voltage installed	JS18
3.30V	2-3
3.45 Volt	1-2

3) Peripheral Section

Floppy Port Select

Mode of Operation	JS6	JS7
Normal Mode	2-3	1-2
Enhanced Floppy Drive	1-2	2-3

Parallel Port Interrupt Select

Interrupt Select	JS8
Interrupt 7	1-2
Interrupt 5	2-3

ECP (Enhance Communication Port)

Mode of Operation	JS9	JS10	JS11
Normal Mode	2-3	Open	Open
Enhanced Mode 1 (DMA 1)	1-2	1-2	1-2
Enhanced Mode 2 (DMA 2)	1-2	2-3	2-3

4) SCSI data bus width

Mode of Operation	JS15
<i>Fast 8-bit</i>	2-3
Fast and Wide 16-bit	1-2

5) Monitor Type

Mode of Operation	Mono
Mono	2-3
<i>Color</i>	1-2

Clear Password Jumper

Mode	PSWD
<i>Normal Operation</i>	2-3
Clear Password	1-2

Flash EPROM Type Selection

Flash EPROM Type	FLASH
5V	2-3
12V	1-2

Note: Manufacturing setting jumper.

6) Clear Content of system CMOS Jumper

(To clear the content of the CMOS, install a jumper at JS2 pin 1-2 and quickly return back to position 2-3)

Mode	JS2
Normal	2-3
Clear	1-2

P/S2 Mouse enabled

Mode	JS3
<i>Enabled</i>	<i>1-2</i>
Disabled	2-3

Infrared Jumper (For 32C665IR Only)

Mode	JS4	JS5
<i>Serial Port 2</i>	<i>1-2</i>	<i>1-2</i>
Infrared Support	2-3	2-3

NOTE: Refer to chapter 2 “System Board Jumpers” Section for more detailed information.

CMOS SETUP QUICK REFERENCE

For Quick Setup (recommended)

1. Go to STANDARD CMOS SETUP to set Date, Time, Hard drive type, and Floppy drive type.
2. From main menu, use the TAB key or mouse to go to the DEFAULT SETUP menu. Select *Optimal* icon. Select Yes to load the Optimal values.

For manual setup (For advanced user who has high technical understanding)

3. Select ADVANCED CMOS SETUP, ADVANCED CHIPSET SETUP, and POWER MGMT SETUP menus to set each option individually.

I. STANDARD SETUP:

Primary Master	: Auto
Primary Slave	: Auto
Secondary Master	: Auto
Secondary Slave	: Auto
Date and Time	: Default
Floppy Drive A	: 1.44 MB 3.5"
Floppy Drive B	: Not Installed

II. ADVANCED CMOS SETUP

<u>Option Name</u>	<u>Optimal</u>	<u>Failsafe</u>
Quick Boot	Enabled	Disabled
BootUp Sequence	C:;A:;CDROM	A:;C:;CDROM
BootUp Num-Lock	On	On
Floppy Drive Swap	Disabled	Disabled
Floppy Drive Seek	Disabled	Disabled
Mouse Support	Disabled	Disabled
System Keyboard	Present	Present
Primary Display	VGA/EGA	VGA/EGA
Password Check	Setup	Setup
Parity Check	Disabled	Disabled
OS/2 Compatible Mode	Disabled	Disabled
Internal Cache	WriteBack	WriteBack
External Cache	Enabled	Disabled
System BIOS Cacheable	Enabled	Disabled
C000,16k Shadow	Enabled	Disabled
C400,16k Shadow	Enabled	Disabled
C800,16k Shadow	Disabled	Disabled
CC00,16k Shadow	Disabled	Disabled
D000,16k Shadow	Disabled	Disabled

D400,16k Shadow	Disabled	Disabled
D800,16k Shadow	Disabled	Disabled
DC00,16k Shadow	Disabled	Disabled

III. ADVANCED CHIPSET SETUP

<u>Option Name</u>	<u>Optimal</u>	<u>Failsafe</u>
Global Triton2 Enable	Enabled	Enabled
Memory Hole	Disabled	Disabled
8Bit I/O Recovery Time(Sysclk)	2	8
16Bit I/O Recovery Time(Sysclk)	1	4
DRAM Timings	60ns	70ns
Refresh Rate	60Mhz	60Mhz
Turbo Read Lead Off	Enabled	Disabled
Read Burst Timing	x333	x444
Write Burst Timing	x333	x444
Fast RAS to CAS Delay (Clocks)	2	3
Lead Off Timing	6/5/3/4	7/6/4/5
Turbo Read Pipelining	Disabled	Disabled
Speculative LeadOff	Disabled	Disabled
Turn-Around Insertion	Disabled	Disabled
Memory Address Drive Strength	8ma/8ma	8ma/8ma
Type F DMA Buffer Control 1	Disabled	Disabled
Type F DMA Buffer Control 2	Disabled	Disabled
Peer Concurrency	Enabled	Disabled
USB Function Enable	Enabled	Enabled

IV. POWER MANAGEMENT

<u>Option Name</u>	<u>Optimal</u>	<u>Failsafe</u>
Power Management/APM	Disabled	Disabled
Instant-On Timeout (Minute)	Disabled	Disabled
Green PC Monitor Power State	Standby	Standby
Video Power Down Mode	Disabled	Disabled
Hard Disk Power Down Mode	Disabled	Disabled
Hard Disk Time Out (Minute)	Disabled	Disabled
Standby Time Out (Minute)	Disabled	Disabled
Suspend Time Out (Minute)	Disabled	Disabled
Slow Clock Ratio	1:8	1:8
Display Activity	Ignore	Ignore
IRQ3	Monitor	Ignore
IRQ4	Monitor	Ignore
IRQ5	Monitor	Ignore
IRQ7	Monitor	Ignore
IRQ9	Monitor	Ignore
IRQ10	Monitor	Ignore
IRQ11	Monitor	Ignore

IRQ12	Monitor	Ignore
IRQ13	Ignore	Ignore
IRQ14	Monitor	Ignore
IRQ15	Monitor	Ignore

V. PCI/PnP SETUP DEFAULTS

<u>Option Name</u>	<u>Optimal</u>	<u>Failsafe</u>
Plug and Play Aware O/S	Yes	No
PCI Latency Timer (PCI Clocks)	32	32
PCI VGA Palette Snoop	Disabled	Disabled
PCI IDE BusMaster	Disabled	Disabled
OffBoard PCI IDE Card	Auto	Auto
OffBoard PCI IDE Primary IRQ	Disabled	Disabled
OffBoard PCI IDE Secondary IRQ	Disabled	Disabled
PCI Slot 1 IRQ Priority	Auto	Auto
PCI Slot 2 IRQ Priority	Auto	Auto
PCI Slot 3 IRQ Priority	Auto	Auto
PCI Slot 4 IRQ Priority	Auto	Auto
IRQ3	ISA/EISA	ISA/EISA
IRQ4	ISA/EISA	ISA/EISA
IRQ5	ISA/EISA	ISA/EISA
IRQ7	ISA/EISA	ISA/EISA
IRQ9	PCI/PnP	PCI/PnP
IRQ10	PCI/PnP	PCI/PnP
IRQ11	PCI/PnP	PCI/PnP
IRQ14	PCI/PnP	PCI/PnP
IRQ15	PCI/PnP	PCI/PnP
Reserved Memory Size	Disabled	Disabled
Reserved Memory Address	C8000	C8000

VI. Peripheral Setup

<u>Option Name</u>	<u>Optimal</u>	<u>Failsafe</u>
OnBoard SCSI	Enabled	Enabled
OnBoard FDC	Auto	Auto
OnBoard Serial Port1	Auto	Auto
OnBoard Serial Port2	Auto	Auto
OnBoard Parallel Port	Auto	Auto
Parallel Port Mode	Normal	Normal
Parallel Port DMA Channel	None	None
IRQ Active	High	High
OnBoard IDE	Primary	Primary

MEMORY CONFIGURATION QUICK REFERENCE

The 54TPI's on-board DRAM memory subsystem support EDO Memory DRAM, 1Mx36, 2Mx36, 4Mx36 8Mx36, 16Mx36, 32Mx36, Fast Page Mode, and None Parity DRAM Modules. DRAM speed must be 70ns or faster. The table below shows some of the variety of ways to configure the memory.

SIM1 & SIM2	SIM3 & SIM4	TOTAL
1Mx36	None	8 Mbyte
1Mx36	1Mx36	16 Mbyte
1Mx36	4Mx36	40 Mbyte
2Mx36	None	16 Mbyte
2Mx36	2Mx36	32 Mbyte
2Mx36	4Mx36	48 Mbyte
2Mx36	8Mx36	80 Mbyte
4Mx36	none	32 Mbytes
4Mx36	4Mx36	64 Mbyte
8Mx36	None	64 Mbyte
8Mx36	8Mx36	128 Mbyte
16Mx36	16Mx36	256 Mbyte
32Mx36	32Mx36	512 Mbyte

- Note:**
1. You can use 70ns or faster memory for 54TPI. Please see chapter 3, Hardware Installation, for more detailed information.
 2. SIMMs must be installed by groups of SIM1 & SIM2 or SIM3 & SIM4.

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PREFACE

Thank you for purchasing the 54TPI system board. This document will aid you to properly configure and install this system board into your computer system. The document is accurate to the best of our knowledge; however, we make no representation or warranty concerning the contents or use of this manual, and specifically disclaim any expressly implied warranties or merchantability or fitness for any particular purpose. The information in this document is subject to change without notice.

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Technical References

- . Pentium[™] Microprocessor Family User's Manual.
- . Intel PCIset 82439HX (TXC) Data Buffer
- . Intel PCIset 82371SB (PIIX3) ISA/PCI-IDE Controller
- . The Peripheral Component Interconnect (PCI) Specification

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<u>CHAPTER 1: INTRODUCTION</u>	

PRODUCT OVERVIEW

The 54TPI system board is a powerful combination of performance, quality, and innovation designed to address the needs of today's high performance systems. With Pentium 75/90/100/120/133/150/166/180/200MHz support, optional 256K/512K external Level 2 fast write-back Pipelined Burst Mode Fast Cache Memory, and 64-bit BURST bus DRAM Memory, the board brings exceptional processing power that could only be achieved by Mini-computers just a few years ago. Incorporating the emerging industry standard Peripheral Component Interconnect (PCI) Local Bus together with the standard 16-bit Industry Standard Architecture (ISA) bus, the board dramatically boosts system I/O throughput for even the most demanding applications in today's market.

Features

CPU Support

- 320-pin ZIF socket for P54C & P54CT(Intel Pentium 75/90/100/120/133/150/166/180/200MHz) with built-in 16KB of fast Cache Memory.

Cache Memory

- Supports 256K and 512K High speed Pipelined Burst Mode fast Cache SRAM

System Memory DRAM

- 2 Banks of Memory that support EDO or Fast Page Mode 72 pins SIMM, with capacity of 1MB, 2MB, 4MB, 8MB, 16MB, and 32MB, both x32 and x36 bits SIMM types can be used.
70ns or faster; 64-bits Interleaved. (Minimum 2 pieces of DRAM modules must be installed.)
- Up to 512 MBytes on-board memory.

System BIOS

- 1 Megabit of AMI BIOS with Built-in Window standard CMOS, Advanced CMOS, Advanced Chipset, Configuration Utilities, Password, Power Management Setup Menus.

System Chipset

- Intel Advanced Chipset 82490HX(Host-To-PCI), Intel Chip 82371SB(PCI-To-ISA), and SCSI controller 7880 Chipset on board. Provides excellence PCI/ISA compatibility.

PCI/ISA Bus

- Four 32-bit Bus Mastering PCI bus slots.
- Three ISA Bus Mastering slots.

Real Time Clock:

- Real Time Clock with built-in Battery to provide very accurate timer clock.

Board Form Factor

- Standard Baby AT form factor and mounting holes.

Product Specifications

Electrical

Power (System board only): 26 Watts @ 5VDC
0.06 Watts @ \pm 12VDC

Environmental

Operating temperature (ambient): 0⁰C to 55⁰C
Non-Operating temperature: -42⁰C to 70⁰C
Relative Humidity: 90% RH @ 36⁰C
MTBF 120,000 Hours
Airflow Requirement: 100LFM with on-board fan.

Dimensions

Width: 8.700 inches (221.98 mm)
Length: 12.000 inches (330.20 mm)

TECHNICAL OVERVIEW

Pentium™ Microprocessor

The 54TPI supports P54C and P54CT (75/90/100/120/133/150/166/180/200 Mhz). The microprocessor incorporates the following features:

- 16KB Internal Cache Memory in a 2-way 32-Byte Line Size. The Cache Memory is separated into two 8KB each for Data and Code for performance improvement.
- 32-bit Address and 64-bit Data interfaces
- 4 Gigabytes (Giga = 1,073,741,824) of physical address space
- 64 Terabytes (Tera = 2 to the power of 40) of virtual address space
- Binary Compatible with Large Software Base such as DOS, OS/2, UNIX, Windows, Windows95, WindowNT, Netware, etc.,
- Advanced Design Features such as Branch Prediction, Virtual Mode Extensions
- Built-in 80387 Compatible high performance Floating-point Instruction Execution Unit.

Cache Memory

The increase in speeds of DRAM over the last few years has not kept pace with the increase in microprocessor speeds. This requires very fast and unavailable DRAMs or many wait states have to be inserted to the CPU memory cycles. System performance decreases as the number of wait states increases.

Cache memory is small but can be accessed very fast. The code and data frequently accessed by the CPU normally is stored here. The Pentium Microprocessor has built-in 16KB that is separated

into two 8KB of Code and Data Cache. When the Pentium processor accesses memory, it checks if data is in the cache memory and, if the data is there, it will fetch that instead of going to much slower main system memory. This is a cache hit situation. It is possible that 95 to 99 memory accesses out of 100 memory accesses are cache hits depending on the application software.

An optional 256KB to 512KB external Pipelined Burst Mode cache memory is provided on the 54TPI system board to achieve an even higher performance. This external cache requires four pieces of 32Kx32 fast SRAM chips. With external cache memory, the memory hit rate of the system will be further improved so that the overall performance is higher. Please see Appendix C section for system memory mapping with cached and non-cached locations.

Main System Memory (DRAM)

The main memory subsystem of the 54TPI consists of 640K of DRAM memory below 1 Megabyte address space, 256K of I/O ROM BIOS, 128KB of system BIOS ROM, and up to 127MB (128MB - 1MB of Base and reserve mem) of extended system memory.

System ROM

The BIOS ROM is provided in a single 8-bit EPROM, which can hold up to 128KB of code and data. It is accessible at the top of the system's 4 GB memory address space and at the top of the first Megabyte of memory. The BIOS ROM supports all PCI/ISA compatible features. In addition, a Shadow RAM feature is provided to allow the BIOS code and VIDEO BIOS to be executed from 32-bit system DRAM resident at the same physical address.

The processor is reset when power is turned on or when the RESET switch is used. After RESET, the Pentium CPU is initialized to a known internal state and begins fetching instructions, out of the BIOS ROM, from the reset address FFFFFFF0. This address leads to the entry point of the power-on

system initialization procedure stored in BIOS ROM. The BIOS system initialization procedure consists of the following functions:

- Power-on self-tests such as BIOS Check Sum Test, system DRAM Test, Battery- Backed CMOS RAM Test.
- Initializing all the standard compatible I/O components such as Interrupt Controllers, DMA Controllers (Intel 8237A register compatible), Keyboard Controller (Intel 8742 register compatible), Video Controller (CGA, EGA, VGA, etc..), System Timers (Intel 8254 register compatible).
- Initializing all the PCI/ISA add-on cards based on the information stored in the CMOS.
- Built-in SETUP program, if allowed, is used for system configuration such as:
 - . Day/Time setting
 - . Selection for floppy disk and hard disk types
 - . Shadow RAM, Cache Memory Enable, Disable options.
 - . Auto Detect IDE Hard Drives
 - . Virus Protection and Password for Security

Besides initializing the system, the BIOS ROM also provides BIOS interrupt calls for such functions as video access, floppy disk access, printer access, etc..

DRAM control Logic

The DRAM control logic on the 54TPI system board is designed and optimized for the Pentium CPU. Unlike most other systems with a separate cache controller, the DRAM control logic is tightly coupled with the on-chip cache controller. When CPU address becomes available for a new memory cycle, both controllers operate in parallel. If the cycle is a read hit or a write hit, the cache controller will take control of the cycle while the DRAM controller stays in idle. If the cycle is a read miss, the DRAM controller will cooperate with the cache controller to generate appropriate cycles to write the data from the cache

memory back to the system memory. If the cache data line is dirty, the CPU read data from the system memory and update the cache memory. If the cycle is a write miss, the DRAM controller simply takes control to write the data to the system memory while the cache controller stays in idle. The DRAM controller and the system memory support the Pentium 128Byte-burst memory read cycles and fast-page mode cache write back cycles for the highest performance.

The on-board DRAM is configured in a 72-bit-wide arrangement consisting of 64 bits of data and 8 bits of parity. Each parity bit is directly associated with one of the 8 bytes in the 72-bit double long word. At least two SIMMs are required to have a system running at full 64-bit data path.

Shadow DRAM Feature

The 54TPI supports the Shadow DRAM feature which allows the BIOS ROM, VIDEO ROM, and I/O ROM codes to be executed from the system DRAM resident at the same physical address space. The Shadow DRAM feature significantly improves the system performance in BIOS-call intensive applications because executing code out of 64-bit DRAM is very much faster than from 8-bit EPROMs.

PCI/ISA Compatible Expansion Bus

The 54TPI system board has 4 slots 32-bit PCI Expansion Bus connectors and 3 16-bit ISA Expansion Bus connectors for interfacing with all PCI and ISA compatible I/O, memory, and bus mastering adapters.

Introduction to PCI Local Bus

PCI is an electrical specification and logic requirement for a local bus standard, i.e. a multiplexed extension of the CPU bus. PCI defines a standard I/O component level interface that permits all PCI Local Bus products to be totally interchangeable and directly connected without using any glue logic.

What PCI Accomplishes

PCI is a way to physically interconnect highly integrated peripheral components and processor/memory systems.

PCI Features

- Up to 4 PCI loads can be used in the same system on the PCI expansion slots, not including the PCI Controller and an expansion bus controller for ISA, or MCA. PCI de-couples the CPU from the expansion bus and works at 33 MHz but can use either a 32-bit or 64-bit data connection path to the CPU is processor-independent.
- Has a multiplexed address, command, and data bus and supports burst mode operation on reads and writes.
- Runs synchronous with the CPU at speeds up to 33 Mhz, has a maximum data transfer rate of 120 MBs (with a peak rate of 132 MBs on a 32-bit data path).
- Has an optional 64-bit data path that is transparently interoperable with the 32-bit data path.
- Has low latency random accesses (about 60ns write access latency) to slave registers from a PCI bus master on the PCI bus.
- Is capable of full concurrence with the processor and PCI bus masters.
- Has full multi-master capability, allowing any PCI Master peer-to-peer access to any PCI slave.
- Has hidden and overlapped central arbitration.
- Has a low pin count (master - 47; slave - 45),
- Has address and data parity, and uses three physical address spaces: 32-bit memory, 32-bit I/O, and a 256 byte-per-agent configuration space.

- The PCI Controller buffers reads and writes between the memory/CPU and PCI peripheral devices.
- The CPU in a PCI system runs concurrently with PCI bus mastering peripherals. Although bus mastering peripheral devices are arbitrated, significant data transfer rate improvements can be achieved without splitting resource utilization between the CPU and a bus mastering device. Peripheral devices can operate Up to 33 MHz in a PCI environment.
- PCI devices can be bus masters, slaves, or a combination of bus master and slave.
- The PCI specification also provides for burst mode of any length for both reads and writes.
- PCI is a multiplexed bus. Multiplexing allows more than one signal to be sent on the same electrical path. The control mechanisms have been modified and extended to optimize I/O support.

ISA BUS

The Industry Standard Architecture(ISA) is 16-bit data transfer, addressing capabilities to the AT Bus Architecture.

ISA Features

- 16-bit addressing and data transfers
- Data transfer rates up to 8MB/s.

Setup information writes to system board battery backed CMOS RAM and to special I/O ports.

ISA Compatible Peripherals

The 54TPI system board provides the following standard peripherals:

- Enhanced DMA functions with seven independently programmable channels.
- Two 82C59A compatible Interrupt Controllers.
- Four 82C54 compatible programmable interval timers.
- One keyboard controller.
- Real time Clock controller with 114Bytes of CMOS SRAM

CHAPTER 2: BOARD'S JUMPERS & CONNECTORS



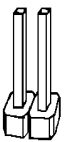
When working with the 54TPI, it is extremely important that you avoid Electrical Static Discharge (ESD). Always ground yourself by wearing a grounded wristband or ankle strap.

Figure 1 on the next page shows the component layout of the 54TPI system board with locations of the system board jumpers and connectors. Note that most jumpers and connectors on the system board are labeled with proper names with pin 1 marked as '1'. To avoid damaging the board and to have proper operation, caution should be taken when connecting these jumpers and connectors.

JUMPER DESCRIPTIONS

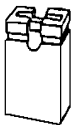
Jumpers are used to select between various operating modes. A jumper switch consists of two, three, or four gold pins projecting from the system board. Placing the plastic jumper cap over two pins connects those pins and makes a particular selection. Using the jumper cap to cover two pins in this way is referred to as shorting those pins. If the cap is not placed on any pins at all or placed on only one pin, this is referred to as leaving the pins open.

Note: When you open a jumper, leave the plastic jumper cap attached to one of the pins so you don't lose it.



OPEN

2-pin jumper

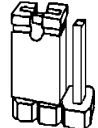


SHORTED



1 2 3

3-pin jumper



PINS 1-2
SHORTED

CPU Jumpers

CPU Clock Frequency Jumpers

The 54TPI supports 75/90/100/120/133/150/166/180/200MHz Pentiums. The jumpers should be set to the corresponding CPU speeds.

CPU Speed	JS12	JS13	JS14	JS16 Pin 1-2
75 Mhz	1-2	2-3	2-3	Open
90 Mhz	1-2	1-2	1-2	Open
100 Mhz	2-3	2-3	1-2	Open
120 Mhz	1-2	1-2	1-2	3-4
133 Mhz	2-3	2-3	1-2	3-4
150 Mhz	1-2	1-2	1-2	1-2, 3-4
166 Mhz	2-3	2-3	1-2	1-2, 3-4
180 Mhz	1-2	1-2	1-2	1-2
200 Mhz	2-3	2-3	1-2	1-2

Jumper Setting for VRE CPU

CPU Voltage installed	JS18
3.30V	2-3
3.45 Volt	1-2

Peripheral Section

Enhanced Floppy

Mode of Operation	JS6	JS7
Normal Mode	2-3	1-2
Enhanced Floppy Drive	1-2	2-3

Parallel Port Interrupt Select Jumper

Interrupt for Parallel Port can be optionally set to IRQ7 or IRQ5 by this jumper.

Interrupt Select	JS8
Interrupt 7	1-2
Interrupt 5	2-3

Extended Capabilities Port (ECP) Jumpers

The onboard Parallel Port Controller supports PC/AT Compatible Mode (Normal mode), High Speed HP and Microsoft Compatible Extended Capabilities Port mode (ECP). In Normal mode, system CPU will handle data transfer from the FIFO buffers of the Parallel Port Controller to system memory. In ECP mode, to improve data transfer rate, system DMA will be used to handle the data transfer. (For more information about ECP mode, please refer to Extended Capabilities Port Protocol and ISA Interface Standard specification that is available from Microsoft Corporation)

Mode of Operation	JS9	JS10	JS11
<i>Normal Mode</i>	2-3	Open	Open
Enhanced Mode 1 (DMA 1)	1-2	1-2	1-2
Enhanced Mode 2 (DMA 2)	1-2	2-3	2-3

SCSI Data Bus width

The 54TPI supports both 8-bit and 16-bit data bus SCSI ports. Both of the connectors can be used at the same time because the SCSI controller firmware can detect the Bus size of the devices connected to the SCSI bus and generate appropriate data bus size cycles. This is especially useful because you can concurrently operate SCSI Tape or CD-ROM devices that typically are 8-bit bus type and 16-bit hard drives.

Mode of Operation	JS15
-------------------	------

<i>Fast 8-bit</i>	2-3
Fast and Wide 16-bit	1-2

Monitor Type

Mode of Operation	Mono
Mono	2-3
<i>Color</i>	1-2

Clear password Jumper

The jumper PSWD is used to clear all information, including password, currently stored in the CMOS RAM. It is typically used when you forget the password that you selected previously and you cannot get into the CMOS setup menu.

Function	PSWD
<i>Normal Operation (Default)</i>	2-3
Clear Password	1-2

Flash Program

Intel 28F001BX-T & Intel 28F010 & SST 29EE010 Flash EEPROM can be used +12V to program the BIOS. For some other EEPROM +5V can be used to program

Flash EPROM Type Selection

Flash EPROM Type	FLASH
+5V	2-3
+12V	1-2

Note: Manufacturing jumper setting.

Clear Content os system CMOS

(To clear the content of the CMOS, install a jumper at JS2 pin 1-2 and quickly return back to position 2-3)

Mode	JS2
Normal	2-3
Clear	1-2

PS/2 Mouse enabled

Mode	JS3
<i>Enabled</i>	<i>1-2</i>
Disabled	2-3

Infrared Jumper (For 32C665IR Only)

Mode	JS4	JS5
<i>Serial Port 2</i>	<i>1-2</i>	<i>1-2</i>
Infrared Support	2-3	2-3

CONNECTOR DESCRIPTIONS

Following is the list of 54TPI system board connectors required to be installed for proper system operation. For detailed descriptions of these components, please refer to the next section. To avoid damaging the board and to have proper operation, caution should be taken when connecting these components.

- Power supply connectors (PS8 and PS9)
- Keyboard connector (KBCN)

- Reset connector (RESET)
- Power LED and keyboard lock connector (KEYLOCK)
- Speaker connector (SPKR)
- Turbo LED connector (TBLED)
- Hard Disk Activity LED connector (HDLED)

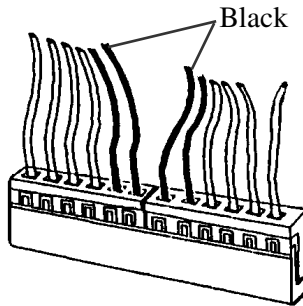
- Parallel Port connector (LPT1)
- Serial Port 1 & 2 connectors (SRL1, SRL2)
- Floppy Interface connector (FDC1)
- IDE Interface connectors (Primary, Secondary)
- Wide Ultra SCSI & Fast SCSI connector

PC/AT Standard Connectors

Power Supply Connectors (PS8 and PS9)

The two Power Supply connectors (PS8 and PS9) are 6-pin AT standard power connectors. Most power supplies have two six-wire connectors, two of the wires on each connector are black. Align the two six-wire connectors so that the two black wires on each connector are in the middle as shown below.

Pin	Connector PS8	Connector PS9
1	Power Good	Ground
2	+5 VDC	Ground
3	+12 VDC	-5 VDC
4	-12 VDC	+5 VDC
5	Ground	+5 VDC
6	Ground	+5 VDC



Keyboard Connector

The keyboard connector (KBCN) is a 5-pin, circular-type DIN socket. It is used to connect the system board keyboard interface to any standard AT-compatible keyboard. (84 or 101 -key type keyboards). The pin assignments are listed below:

Pin	Description
1	Keyboard Clock Signal
2	Keyboard Data Signal
3	Not Used
4	Ground
5	+5V Fused VDC

Reset Connector

The system RESET connector (RESET) is a 2-pin BERG strip. It is used to connect the push button reset switch located on the front panel to the system board. System reset can be done by shorting pin 1 to pin 2 with the same effect as turning the power off and then on again.

Pin	Description
1	Ground
2	Reset Input

Power LED and Keyboard Lock Connector

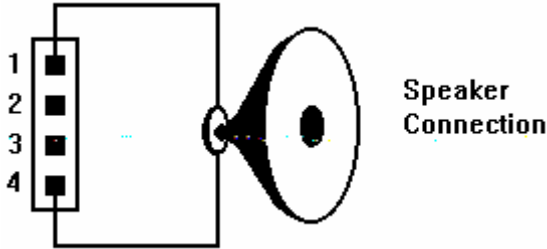
The Power LED and Keyboard Lock connector (KEYLOCK) is 5-pin keyed BERG strip. It is used to connect +5 VDC power to the power indicator LED at the front panel and connect security keyboard lock to the keyboard controller. This allows you to switch off the keyboard and so provide limited security against casual intruders. The pin assignments are indicated below:

Pin	Description
1	LED Power
2	Key (N/C)
3	Ground
4	Keyboard Lock
5	Ground

Speaker Connector

The Speaker connector (SPKR) is a 4-pin keyed BERG strip. It is used to connect an external 2-inch, 8-ohm speaker to the system board to provide sound capability. The pin assignments are defined below:

Pin	Description
1	Speaker Data Out
2	Key (N/C)
3	Ground
4	+5 VDC



Turbo LED Connector

The Turbo LED connector (TBLED) is a 2-pin BERG strip. It is used to connect a CPU operating frequency indicator LED from the front panel to the system board. The pin assignments are indicated below:

Pin	Description
1	LED Anode
2	LED Cathode

Hard disk Activity LED Connector

The hard disk activity LED connector (HDLED) is a 4-pin keyed BERG strip. It is used to connect to front pannel hard disk LED.

Pin	Description
1	LED Anode (+)
2	Key (N/C)
3	LED Cathode (-)
4	LED Anode (+)

Peripheral Connectors

Parallel Port Connector

The on-board parallel port connector (PARALLEL) is a 2x13-pin male header connector. The On-board Parallel Port can be disabled through the BIOS Setup. Please refer to Chapter 3 “Peripheral Management Setup” section for more detail information. The pin assignment is shown below:

Pin	Description	Pin	Description
1	STROBE	14	AUTO FEED XT
2	Data Bit 0	15	ERROR
3	Data Bit 1	16	INIT
4	Data Bit 2	17	SLCT IN
5	Data Bit 3	18	Ground
6	Data Bit 4	19	Ground
7	Data Bit 5	20	Ground
8	Data Bit 6	21	Ground
9	Data Bit 7	22	Ground
10	ACK	23	Ground
11	BUSY	24	Ground

Pin	Description	Pin	Description
12	PE	25	Ground
13	SLCT	26	Key (N/C)

The Integrated Parallel Port supports Extended Capabilities Port protocol (ECP) to provide a number of advantages for the parallel port as listed below:

- Use DMA channel 1 or 3 to transfer data across the Parallel port in both forward and reverse directions; therefore, processor time is saved for other tasks. This is especially important in multi-tasking operating systems such as the coming Windows Chicago.
- Peer-to-peer capability for networking.

Single byte run length encoded (RLE) compression for improved throughput (64:1.)

Serial Port 1 & 2 Connectors

The Serial Port 1 and 2 connectors are the 2x5-pin male headers SRL1 and SRL2. Users should use a flex cable with a 9 or 25 - pin male D-subminiature receptacle at one end and a 2x5-pin female header at the other end to provide RS-232 serial interface. The On-board Serial Ports can be disabled through BIOS setup. Please refer to Chapter 3 “Peripheral Management Setup” section for more detail information. The pin assignment is defined below:

Pin	Description	Pin	Description
1	Carrier Detect (CD)	6	Receive Data (RXD)
2	Transmit Data (TXD)	7	Data Terminal Ready (DTR)
3	Signal Ground	8	Data Set Ready (DSR)
4	Request To Send (RTS)	9	Clear To Send (CTS)
5	Ring Indicator (RI)	10	Key (N/C)

Floppy Interface Connector

The On-board Floppy Interface connector (FDC1) is 2x17-pin male headers. This interface supports two 5.25" or 3.5" floppy drives in any combination and also can be disabled if no floppy drives are present on the system. The On-board Floppy Port can be disabled through the BIOS setup. Please refer to Chapter 3 "Peripheral Management Setup" section for more detail information. Pin assignment is as follows:

Pin	Description	Pin	Description
2	RPM	1	Ground
4	No Connection	3	Ground
6	No Connection	5	Key (N/C)
8	Index	7	Ground
10	Motor 1	9	Ground
12	Drive 2	11	Ground
14	Drive 1	13	Ground
16	Motor 2	15	Ground
18	Direction	17	Ground
20	Step	19	Ground
22	Write Data	21	Ground
24	Write Enable	23	Ground
26	Track0	25	Ground
28	Write Protect	27	Ground
30	Read Data	29	Ground
32	Head Select	31	Ground
34	Disk Change	33	Ground

IDE Interface Connectors

The on-board IDE Interface connectors (Primary IDE and Secondary IDE) are 2x20-pin male headers. Each port supports up to two IDE devices. This interface can be disabled through BIOS setup. Please refer to Chapter 4 “Peripheral Management Setup” section for more detail information. Pin assignment of IDE is as follows:

Pin	Description	Pin	Description
2	Ground	1	IDE Reset/
4	Data 8	3	Data 7
6	Data 9	5	Data 6
8	Data 10	7	Data 5
10	Data 11	9	Data 4
12	Data 12	11	Data 3
14	Data 13	13	Data 2
16	Data 14	15	Data 1
18	Data 15	17	Data 0
20	Key (N/C)	19	Ground
22	Ground	21	No Connection
24	Ground	23	I/O Write/
26	Ground	25	I/O Read/
28	ALE	27	No Connection
30	Ground	29	No Connection
32	IOCS16/	31	IDE IRQ 14
34	No Connection	33	Address A1
36	Address A2	35	Address A0
38	IDE Chip Select 1/	37	IDE Chip Select 0/
40	Ground	39	IDE Active/

SCSI Interface Connectors

The 54TPI supports two SCSI Port connectors. The 2x25 pin header SCSI1 is for 8-bit Fast SCSI-2 interface. The 68-pin Female Miniature receptacle header SCSI2 is for 16-bit Fast and Wide SCSI-2 interface. The SCSI Ports can be disabled through BIOS setup. Please refer to Chapter 4 “Peripheral Management Setup” section for more detailed information. The pin assignment of SCSI1 is as follows:

Pin	Description	Pin	Description
2	Data 0	1	Ground
4	Data 1	3	Ground
6	Data 2	5	Ground
8	Data 3	7	Ground
10	Data 4	9	Ground
12	Data 5	11	Ground
14	Data 6	13	Ground
16	Data 7	15	Ground
18	Data Parity	17	Ground
20	Ground	19	Ground
22	Ground	21	Ground
24	Ground	23	Ground
26	Terminator Power	25	Key (N/C)
28	Ground	27	Ground
30	Ground	29	Ground
32	Attention	31	Ground
34	Ground	33	Ground
36	Busy	35	Ground
38	Acknowledge	37	Ground
40	Reset	39	Ground
42	Message	41	Ground
44	Select	43	Ground

Pin	Description	Pin	Description
46	Command/Data	45	Ground
48	Request	47	Ground
50	In/Out	49	Ground

The pin assignment for 68-pin receptacle header SCSI2 is as follows:

Pin	Description	Pin	Description
35	Data12	1	Ground
36	Data13	2	Ground
37	Data14	3	Ground
38	Data15	4	Ground
39	Data Parity(8-15)	5	Ground
40	Data0	6	Ground
41	Data 1	7	Ground
42	Data 2	8	Ground
43	Data 3	9	Ground
44	Data 4	10	Ground
45	Data 5	11	Ground
46	Data 6	12	Ground
47	Data 7	13	Open
48	Data Parity(0-7)	14	Ground
49	Ground	15	Ground
50	Ground	16	Ground
51	Terminator Power	17	Terminator Power
52	Terminator Power	18	Terminator Power
53	Reserved	19	Reserved
54	Ground	20	Ground
55	Attention	21	Ground
56	Ground	22	Ground
57	Busy	23	Ground
58	Acknowledge	24	Ground
59	Reset	25	Ground
60	Message	26	Ground

Pin	Description	Pin	Description
61	Select	27	Ground
62	Command/Data	28	Ground
63	Request	29	Ground
64	In/Out	30	Ground
65	Data8	31	Ground
66	Data9	32	Ground
67	Data10	33	Ground
68	Data11	34	Ground

CHAPTER 3: HARDWARE INSTALLATION

BUILDING A HIGH PERFORMANCE SYSTEM

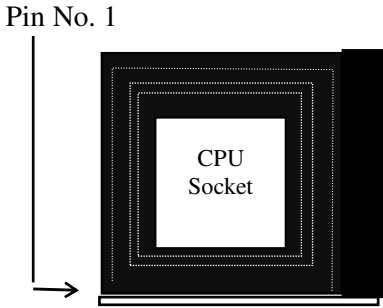
The dimensions of the 54TPI system board are designed to fit perfectly in a PC/AT standard case. To build a complete high performance system based on the 54TPI system board, the following equipment is needed:

1. A chassis (Case) with dimensions similar to PC/AT standard chassis. The chassis should have a front Panel with connectors for Reset, Power, Keylock, Turbo LED, Speaker, and Hard drive LED. AC Power cable is included with the chassis. The standard AT 200W power supply should be capable of providing a continuous power within a +4.75 VDC to +5.25 VDC range. A power line filter may be needed for areas with noisy transmission
2. One or two floppy drives (360K/1.2M/1.44M/2.88M).
3. A SCSI Hard disk drive or IDE hard disk drive with a hard drive controller.
4. A Video card (Monochrome, CGA, EGA, VGA). If the Video card is VGA, then it could be PCI interface type for the best display performance.
5. A video display monitor.
6. An AT-compatible keyboard (84 Or 101 Keyboard).
7. The following additional peripherals will be useful to enhance the system:
 - A bus or serial mouse.
 - A tape back up drive.
 - A CD-ROM drive.
8. Cables
 - A set of flat cables for floppy drive & hard disk drive.
9. Tools
 - Set of Screw drivers, Cutter, Pliers

CPU INSTALLATION

Care should be taken when installing the CPU into the Zero Insertion Force (ZIF) socket 7 on the system board. Lift the handle of ZIF socket

up. Place the Pentium processor into the ZIF socket. No force should be required to insert the CPU. On Pentium processors pin 1 is with the square base and it goes to particular hole on the socket. Match the hole and pin one first and then easily insert the processor into the socket. Press the handle gently down.



!! Important !!

Cooling fan installation

Mount the cooling kit with fan on top of the CPU. Connect power to fan from power supply. Make sure the cooling kit's bottom surface makes proper contact with top surface of CPU.

!! Warning !!

Manufacturer of the board or CPU is not responsible for damage to CPU because of improper handling during installation or cooling kit with fan is not used.

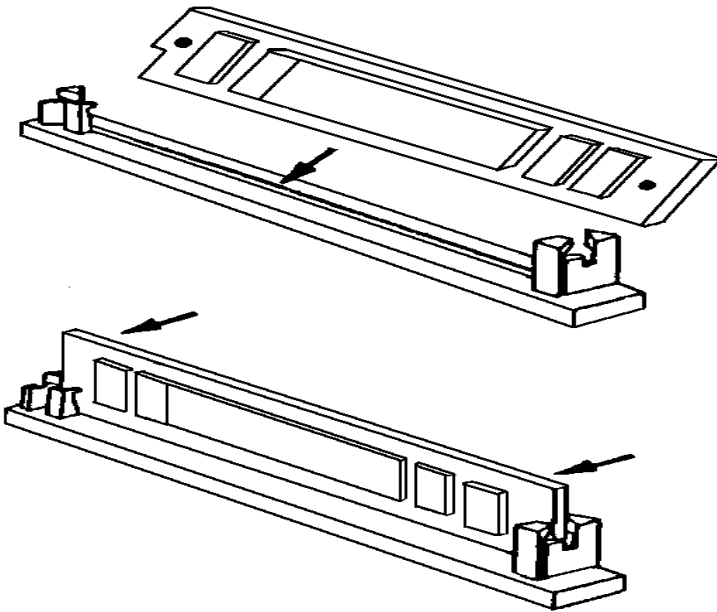
INSTALLING DRAM SIMMS



When working with DRAM SIMMs, it is extremely important that you avoid Electrical Static Discharge (ESD). Always ground yourself by wearing a grounded wristband or ankle strap.

1. Power must be off while installing SIMMs.
2. The SIMM module should face to the right with pin 72 next to the power supply connectors.
3. Insert the SIMM at a 45 degree angle, tilted towards ISA slots.
4. Gently push the SIMM to an upright position until it "snaps" into place.

Repeat above steps until the entire bank is filled.



DRAM SIMMs Configuration

The on-board DRAM memory sub-system has four module mounting sockets which are divided into “banks” of two sockets each. Sockets labeled SIM1 and SIM2 constitute bank 0. Sockets labeled SIM3 and SIM4 constitute bank 1. They support 1MB, 2MB, 4MB, 8MB, 16MB, and 32MB x32 or x36 DRAM SIMMs. DRAM speed must be 70ns or faster. Both EDO or Fast Page Mode DRAMs are supported.

Memory Configuration

SIM1 & SIM2	SIM3 & SIM4	TOTAL
1Mx36	None	8 Mbyte
1Mx36	1Mx36	16 Mbyte
1Mx36	4Mx36	40 Mbyte
2Mx36	None	16 Mbyte
2Mx36	2Mx36	32 Mbyte
2Mx36	4Mx36	48 Mbyte
2Mx36	8Mx36	80 Mbyte
4Mx36	none	32 Mbytes
4Mx36	4Mx36	64 Mbyte
8Mx36	None	64 Mbyte
8Mx36	8Mx36	128 Mbyte
16Mx36	16Mx36	256 Mbyte
32Mx36	32Mx36	512 Mbyte

Peripheral Add-on Card installation

The 54TPI supports both PCI slots and ISA slots. You can install the corresponding add-on cards into any of these slots. Make sure these add-on cards' interrupts or DMA channels do not conflict with each other. The best way to remember is to write down the information of all the installed cards into the back of this manual for later reference.

- . PCI Add-on cards are normally automatically configured by system BIOS during boot up. However, some PCI add-on cards do have jumper settings for INTA or INTB. Write down the information if it is available for later reference.

ISA add-on cards can be installed in provided ISA slots. Since there is no specific software that can automatically configure the ISA add-on cards, special care should be taken when setting Interrupt and DMA channels of ISA cards.

Please refer to the manuals shipped with the add-on cards for more information. Care should be taken when inserting the cards into the slots to make sure the connectors slots are not damaged.

CHAPTER 4: SYSTEM SETUP

SYSTEM CMOS

You need to setup the system CMOS every time:

- You start a new and un-configured system
- You receive a start-up error message indicating the configuration information stored in the non-volatile CMOS RAM has somehow become corrupted.
- You add, remove, or change peripherals from your system.
- * You add, remove, or change DRAM from your system.

The first time you power up the system, the configuration information stored in the battery-backed CMOS RAM may not be correct. The BIOS detects this condition and prompts the user to go through the SETUP section. This chapter explains how to use the BIOS SETUP program and make the appropriate entries.



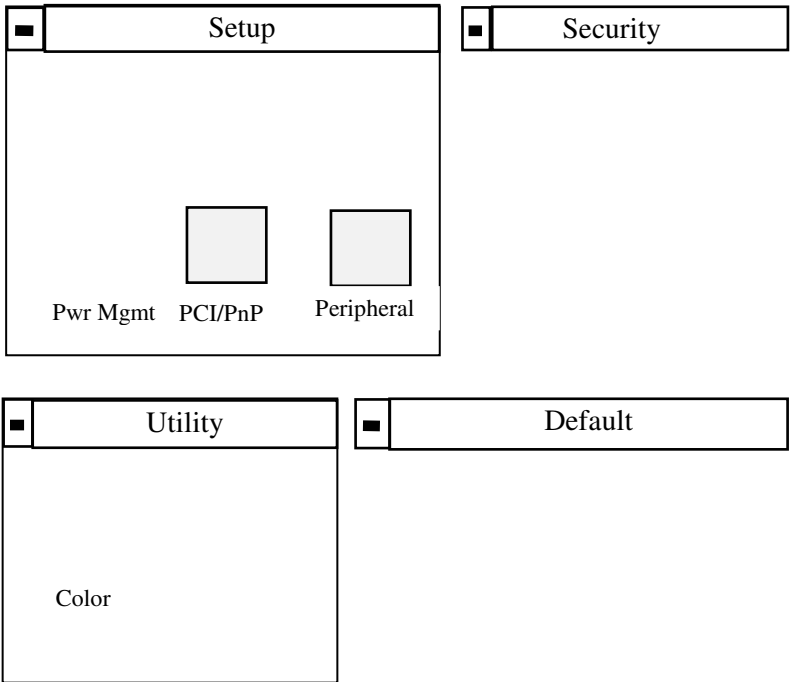
Some of the parameters are already factory preset and do not need to be changed. Please read the instructions carefully and only change the settings if necessary.

Entering CMOS Setup

The System BIOS provides a Built-in Setup Utility that can be accessed by pressing < Del > key at the appropriate time during system boot up. Setup configuration data is stored in the system CMOS RAM.

The Following window will appear in the AMIBIOS Setup main screen. Details of setup options in each window is given in the following section:





Setup Window

Types of Setup	Description
Standard Setup	Sets date & time, hard disk type, types of floppy drives, display type, and if Keyboard is installed.
Advanced Setup	Quick Boot ,BootUp Sequence , BootUp Num-Lock Floppy Drive Swap, Mouse Support, Primary Display, Password Check, OS/2 Compatible Mode, Internal Cache, External Cache, System BIOS Cacheable, C000 to DC00 Shadow.
Chipset Setup	Sets chipset-specific options and features.
Power Mgmt	Controls I/O Controller-related options.
PCI/PnP Setup	Sets options related to the PCI bus and Plug and Play features.

Peripheral Setup	Controlles I/O Controller-related options.

Standard Setup

Standard Setup options are displayed by choosing the Standard icon from the WINBIOS Setup menu. All Standard Setup options are described below.

Pri Master

Pri Slave

Sec Master

Sec Slave

To select **Auto** for hard drives, that allow the system automatic detect the hard drives.

Date/Time

Select the Date/Time option to change the date or time. The current date and time are displayed. Enter new values through the displayed window.

Floppy Drive A, B

Choose the Floppy Drive A or B icon to specify the floppy drive type. The settings are *360 KB 5¼"*, *1.2 MB 5¼"*, *720 KB 3½"*, *1.44 MB 3½"*, or *2.88 MB 3½"*.

Configuring IDE Drives

Select the appropriate drive icon (Primary Master, Primary Slave, Secondary Master, and Secondary Slave). Choose the TYPE parameter and select auto. If using Master & Slave drives select the drive id that provide by drive's Manufacturing.

Configuring a CD-ROM Drive

Select the appropriate drive icon (Pri Master, Pri Slave, Sec Master, or Sec Slave). Choose the **Type** parameter and select CDROM. You can boot the computer from a CD-ROM drive.

Advanced Setup

Advanced Setup options are displayed by choosing the Advanced icon from the WINBIOS Setup main menu. All Advanced Setup options are described in this section.

Quick Boot

Set this option to *Enabled* to instruct AMIBIOS to boot quickly when the computer is powered on. This option replaces the old **Above 1 MB Memory Test** Advanced Setup option. The settings are:

Setting	Description
<i>Disabled</i>	AMIBIOS test all system memory. AMIBIOS waits up to 40 seconds for a READY signal from the IDE hard disk drive. AMIBIOS waits for .5 seconds after sending a RESET signal to the IDE drive to allow the IDE drive time to get ready again. AMIBIOS checks for a key press and runs WINBIOS Setup if the key has been pressed.
<i>Enabled</i>	AMIBIOS does not test system memory above 1 MB. AMIBIOS does not wait up to 40 seconds for a READY signal from the IDE hard disk drive. If a READY signal is not received immediately from the IDE drive, AMIBIOS does not configure that drive. AMIBIOS does not wait for .5 seconds after sending a RESET signal to the IDE drive to allow the IDE drive time to get ready again. You cannot run WINBIOS Setup at system boot, because there is no delay for the <i>Hit to run Setup</i> message.

The Optimal and Fail-Safe default settings are *Enabled*.

BootUp Sequence

This option sets the sequence of boot drives (floppy drive A:, hard disk drive C:, or a CD-ROM drive) that the AMIBIOS attempts to boot from after AMIBIOS POST completes. The settings are *C:,A:,CDROM*, *CDROM,C:,A:*, or *A:,C:, CDROM*. The default settings are *C:,A:,CDROM*.

BootUp NumLock

Set this option to *Off* to turn the Num Lock key off when the computer is booted so you can use the arrow keys on both the numeric keypad and the keyboard. The settings are *On* or *Off*. The default settings are *On*.

Floppy Drive Swap Set this option to *Enabled* to permit drives A: and B: to be swapped. The settings are *Enabled* or *Disabled*. The default settings are *Disabled*.

Mouse Support

When this option is set to *Enabled*, AMIBIOS supports a PS/2-type mouse. The settings are *Enabled* or *Disabled*. The default settings are *Enabled*.

Primary Display This option specifies the type of display monitor and adapter in the computer. The settings are *Mono*, *CGA40*, *CGA80*, *EGA/VGA*, or *Absent*. The Optimal and Fail-Safe default settings are *EGA/VGA*.

Password Check

This option enables password checking every time the computer is powered on or every time WINBIOS Setup is executed. If *Always* is chosen, a user password prompt appears every time the computer is turned on. If *Setup* is chosen, the password prompt appears if WINBIOS is executed.

The Optimal and Power-On defaults are *Setup*.

OS/2 Compatible Mode

Set this option to *Enabled* to permit AMIBIOS to run with IBM OS/2. The settings are *Enabled* or *Disabled*. The default settings are *Disabled*.

Internal Cache

This option specifies the caching algorithm used for L1 internal cache memory. The Advanced Chipset Setup

Setting	Description
<i>Disabled</i>	Neither L1 internal cache memory on the CPU or L2 secondary cache memory is enabled.
<i>WriteBack</i> (default)	Use the write-back caching algorithm.

External Cache

External Cache This option specifies the caching algorithm used for L2 secondary (external) cache memory. The settings are:

Setting	Description
<i>Disabled</i>	Neither L1 internal cache memory on the CPU or L2 secondary cache memory is enabled.
<i>Enabled</i> (default)	Use the write-back caching algorithm.

System BIOS Shadow Cacheable

When this option is set to *Enabled*, the contents of the F0000h system memory segment can be read from or written to L2 secondary cache memory. The contents of the F0000h memory segment are always copied from the BIOS ROM to system RAM for faster execution.

The settings are *Enabled* or *Disabled*. The Optimal default setting is *Enabled*. The Fail-Safe default setting is *Disabled*.

C000,16K Shadow

C400,16K Shadow
C800,16K Shadow
CC00,16K Shadow
D000,16K Shadow
D400,16K Shadow
D800,16K Shadow
C000,16K Shadow

These options control the location of the contents of the 16KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

Setting	Description
<i>Shadow</i>	The contents of C0000h - C3FFFh are written to the same address in system memory (RAM) for faster execution.
<i>Cache</i>	The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adaptor ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory.
<i>Disabled</i>	The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory.

The default setting is *Cached*.

In the AMIBIOS for the Intel 82490HX chipset, the E000h page is used as ROM during POST, but shadowing is disabled and the ROM CS# signal is disabled to make the E000h page available on the local bus.

Advanced Chipset Setup

Global Triton2 Enable

This setup question provides a method to enable or disable all of the additional features provided by the Intel Advanced Chipset 82490HX controller.

Memory Hole

This option allows the enabling of a memory hole at either address 512K - 640K or at address 15M - 16M.

IRQ12/M Mouse Function

Set this option to *Enabled* to specify that IRQ12 will be used for the mouse. The settings are *Disabled* or *Enabled*. The Optimal and Fail-Safe default settings are *Enabled*.

DRAM Timings

This setup question allows the system to be set to either optimal settings for 60ns or 70ns DRAM, or to be set to manual. In this mode the next nine options are made available for customizing the memory timings.

Refresh Rate

Allows the refresh rate to be set according to the memory bus clock (50mhz, 60mhz or 66mhz).

Turbo Read LeadOff

A feature to enable the skipping of the first input register in the DRAM data pipeline. This results in a 1 HCLK savings of all READ leadoff timings.

Read Burst Timing

Allows customizing of the read timings in the memory design.

Write Burst Timings

Allows customizing of the write timings in the memory design.

Fast RAS to CAS Delay (Clocks)

If enabled, the row miss leadoff timing delay is set to 2 clocks, otherwise it is set to 3 clocks.

LeadOff Timing

These bit control additional DRAM timings. This includes: Read LeadOff, Write LeadOff, RAS# Precharge, and Refresh RAS assertion.

Turbo Read Pipelining

This bit affects the Read timings.

Speculative Lead Off

In this mode the DRAM controller read request is presented before the final memory target (main memory, cache, or PCI) is decoded. This results in a 1 HCLK increase in DRAM read leadoff latencies.

Turn-Around Insertion

When enabled the chipset inserts 1 extra clock of turnaround on the MD lines after asserting memory write enable (MWE#).

USB Function Enable

This option is the global disable for the USB functionality of the PIIX3. In addition to disabling USB circuitry, this also disables response by the PIIX3 to PCI configuration accesses to function 2 of the PIIX3 device.

Power Management Setup

Power Management Setup options are displayed by choosing the Power Mgmt icon from the WINBIOS Setup main menu. All Power Management Setup options are described in this section.

Power Management/APM

Set this option to *Enabled* to enable the power management and APM (Advanced Power Management) features.

The settings are *Enabled* or *Disabled*. The default settings are *Disabled*.

Instant On Support

Set this option to *Enabled* to allow the computer to go to full power on mode when leaving a power-conserving state. *This option is only available if supported by the computer hardware.* AMIBIOS uses the RTC Alarm function to wake the computer at a prespecified time. The settings are *Enabled* or *Disabled*. The default settings are *Disabled*.

Green PC Monitor Power State

This option specifies the power management state that the Green PC-compliant video monitor enters after the specified period of display inactivity has expired. The settings are *Disabled*, *Off*, *Standby*, or *Suspend*. The default settings are *Standby*.

Video Power Down Mode

This option specifies the power management state that the video subsystem enters after the specified period of display inactivity has expired. The settings are *Disabled*, *Standby*, or *Suspend*. The default settings are *Disabled*.

Hard Disk Power Down Mode

This option specifies the power management state that the hard disk drive enters after the specified period of display inactivity has expired. The settings are *Disabled*, *Standby*, or *Suspend*. The default settings are *Disabled*.

Hard Disk Time-out (Min.)

This option specifies the length of a period of hard disk inactivity. When this period expires, the hard disk drive enters the power-conserving mode specified in the **Hard Disk Power Down Mode** option described on the previous page. The settings are *Disabled*, *1 Min (minutes)*, and all one minute intervals up to and including *15 Min*. The default settings are *Disabled*.

Standby Time-out

This option specifies the length of the period of system inactivity when the computer is in Full-On mode before the computer is placed in Standby mode. In Standby mode, some power use is curtailed. The settings are *Disabled*, *1 Min*, *2 Min.*, and all one minute intervals up to and including *15 Min*. The default settings are *Disabled*.

Suspend Time-out

This option specifies the length of the period of system inactivity when the computer is already in Standby mode before the computer is placed in Suspend mode. In Suspend mode, nearly all power use is curtailed. The settings are *Disabled*, *1 Min.*, *2 Min.*, and all one minute intervals up to and including *15 Min*. The default settings are *Disabled*.

Slow Clock Ratio

This option specifies the speed at which the system clock runs in power saving modes. The settings are expressed as a ratio between the normal clock speed and the power down clock speed. The settings are *1:1*, *1:2* (half as fast as normal), *1:4* ((the normal clock speed), *1:8*, *1:16*, *1:32*, *1:64*, or *1:128*. The default setting is *1:1*.

Display Activity

This option specifies if AMIBIOS is to monitor activity on the display monitor for power conservation purposes. When this options set to *Monitor* and there is no display activity for the length of time specified in the value in **the Full-On to Standby Timeout (Min)** option, the computer enters a power saving state. The settings are *Monitor* or *Ignore*. The default settings are *Ignore*.

IRQ 3

IRQ 4

IRQ 5

IRQ 7

IRQ 9

IRQ 10

IRQ 11

IRQ 12

IRQ 13

IRQ 14

IRQ 15

These options enable event monitoring. When the computer is in a power saving mode, activity on the named interrupt request line is monitored by AMIBIOS. When any activity occurs, the computer enters Full On mode.

Each of these options can be set to *Monitor* or *Ignore*. The default setting for all options is *Ignore*.

PCI/PnP Setup

PCI/PnP Setup options are displayed by choosing the PCI/PnP Setup icon from the WINBIOS Setup main menu. All PCI/PnP Setup options are described in this section

Plug and Play Aware OS

Set this option to *Yes* if the operating system installed in the computer is Plug and Play-aware. AMIBIOS only detects and enables PnP ISA adapter cards that are required for system boot. The Windows 95 operating system detects and enables all other PnP-aware adapter cards. Windows 95 is PnP-aware. Set this option to *No* if the operating system (such as DOS, OS/2, Windows 3.x) does not use PnP. *You must set this option correctly or PnP-aware adapter cards installed in your computer will not be configured properly.* The settings are *No* or *Yes*. The Optimal and Fail-Safe default settings are *No*.

PCI Latency Timer (in PCI Clocks)

This option sets latency of all PCI devices on the PCI bus. The settings are in units equal to PCI clocks. The settings are *32, 64, 96, 128, 160, 192, 224, or 248*. The Optimal and Fail-Safe default settings are *32*.

PCI VGA Palette Snoop

This option must be set to *Enabled* if any ISA adapter card installed in the computer requires VGA palette snooping. The settings are *Disabled* or *Enabled*. The Optimal and Fail-Safe default settings are *Disabled*.

PCI IDE Bus Master

Set this option to *Enabled* to specify that the IDE controller on the local bus has bus mastering capability. The settings are *Disabled* or *Enabled*. The Optimal and Fail-Safe default settings are *Disabled*.

Offboard PCI IDE Card

This option specifies if an offboard PCI IDE controller adapter card is used in the computer. You must also specify the PCI expansion slot on the motherboard where the offboard PCI IDE controller card is installed. If an offboard PCI IDE controller is used, the onboard IDE controller on the motherboard is automatically disabled. The settings are *Disabled*, *Auto*, *Slot1*, *Slot2*, *Slot3*, or *Slot4*.

If *Auto* is selected, AMIBIOS automatically determines the correct setting for this option. The Optimal and Fail-Safe default settings are *Auto*.

In the AMIBIOS for the Intel Triton chipset, this option forces IRQ 14 and 15 to a PCI slot on the PCI local bus. This is necessary to support non-compliant PCI IDE adapter cards.

Offboard PCI IDE Primary IRQ

This option specifies the PCI interrupt used by the primary IDE channel on the offboard PCI IDE controller. The settings are *Disabled*, *INTA*, *INTB*, *INTC*, or *INTD*. The Optimal and Fail-Safe default settings are *Disabled*.

Offboard PCI IDE Secondary IRQ

This option specifies the PCI interrupt used by the secondary IDE channel on the offboard PCI IDE controller. The settings are *Disabled*, *INTA*, *INTB*, *INTC*, or *INTD*. The Optimal and Fail-Safe default settings are *Disabled*.

IRQ3
IRQ4

IRQ5
IRQ7
IRQ9
IRQ10
IRQ11
IRQ14
IRQ15

Reserved Memory Size

Reserved Memory Address

These options specify the bus that the named interrupt request lines (IRQs) are used on. These options allow you to specify IRQs for use by legacy ISA adapter cards.

These options determine if AMIBIOS should remove an IRQ from the pool of available IRQs passed to BIOS configurable devices. The available IRQ pool is determined by reading the ESCD NVRAM. If more IRQs must be removed from the pool, the end user can use these PCI/PnP Setup options to remove the IRQ by assigning the option to the *ISA/EISA* setting. Onboard I/O is configurable by AMIBIOS. The IRQs used by onboard I/O are configured as *PCI/PnP*.

The settings are *PCI/PnP* or *ISA/EISA*. The Optimal and Fail-Safe default settings are *PCI/PnP*.

Peripheral Setup

Peripheral Setup options are displayed by choosing the Peripheral Setup icon from the WINBIOS Setup main menu. All Peripheral Setup options are described in this section.

Onboard FDC

This option enables the floppy drive controller on the motherboard. The settings are *Auto*, *Enabled* or *Disabled*. The Optimal default setting is *Enabled*. The Fail-Safe default setting is *Auto*.

Onboard Serial Port1

This option enables serial port 1 on the motherboard and specifies the base I/O port address for serial port 1. The settings are *2F8h*, *2E8h*, *3F8h*, *3E8h*, *Auto* or *Disabled*. The Optimal default setting is *3F8h*. The Fail-Safe default setting is *Auto*.

Onboard Serial Port2

This option enables serial port 2 on the motherboard and specifies the base I/O port address for serial port 2. The settings are *2F8h*, *2E8h*, *3F8h*, *3E8h*, *Auto* or *Disabled*. The Optimal default setting is *3F8h*. The Fail-Safe default setting is *Auto*.

Onboard Parallel Port

This option enables the parallel port on the motherboard and specifies the parallel port base I/O port address. The settings are *378h*, *278h*, *3Bch*, *Auto* or *Disabled*. The Optimal default setting is *378h*. The Fail-Safe default setting is *Auto*.

Parallel Port Mode

This option specifies the parallel port mode. ECP and EPP are both bidirectional data transfer schemes that adhere to the IEEE P1284 specifications. The settings are:

Setting	Description
<i>Normal</i>	The normal parallel port mode is used. This is the default setting.
<i>EPP</i>	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.
<i>ECP</i>	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve transfer rates of approximately 2.5 Mbs. ECP provides symmetric bidirectional communications.

Parallel Port DMA

This option is only available if the setting for the **Parallel Port Mode** option is *ECP*.

The settings are *Disabled*, *DMA CH (channel) 0*, *DMA CH 1*, or *DMA CH 3*. The default setting is 0.

Onboard IDE

This option specifies the onboard IDE controller channels that will be used. The settings are *Primary*, *Secondary*, *Both*, or *Disabled*. The Optimal and Fail-Safe default settings are *Primary*.

Onboard SCSI

This option specifies the onboard SCSI Controller. The settings are *Enabled & Disabled*. The Default setting is *Enabled*.

SYSTEM BOARD CONFIGURATION

Programming Flash BIOS

To support FLASH BIOS, the component at location U18 must be a FLASH EPROM. Follow these steps to reprogram FLASH BIOS:

1. Prepare a diskette for BIOS ROM file with the file name should be 54TPI.ROM.
2. Insert a diskette into drive A.
3. Press the keys CTRL + HOME down and turn the system power on. Release the keys during the system searching the floppy and system will flash the BIOS ROM file into EPROM.

Note: a. If the system is beep two time that indicate the ROM file is wrong name.

b. If the system is beep continous that indicate no diskette in floppy drive.

c. If no beep during search that indicate the system gets the right file to flash. The system will give four beeps when it is done the flashing

Process and boot up system.

4. Now you can enter into the CMOS setup by following the procedure in the manual.
5. If the system crash during flash or corruption cause by BIOS. Just insert the BIOS ROM file into floppy and turn on the power. The system will automatic flash BIOS ROM file into EPROM.

APPENDIX A: AMI BIOS HARD DISK TYPE

Type	Cylinder	Heads	Write Precomp	Landing Zone	Sectors	Size
1	306	4	128	305	17	10MB
2	615	4	300	615	17	20MB
3	615	6	300	615	17	31MB
4	940	8	512	940	17	62MB
5	940	6	512	940	17	47MB
6	615	4	65535	615	17	20MB
7	462	8	256	511	17	31MB
8	733	5	65535	733	17	30MB
9	900	15	65535	901	17	112MB
10	820	3	65535	820	17	20MB
11	855	5	65535	855	17	35MB
12	855	7	65535	855	17	50MB
13	306	8	128	319	17	20MB
14	733	7	65535	733	17	43MB
16	612	4	0	663	17	20MB
17	977	5	300	977	17	41MB
18	977	7	65535	977	17	57MB
19	1024	7	512	1023	17	60MB
20	733	5	300	732	17	30MB
21	733	7	300	732	17	43MB
22	733	5	300	733	17	30MB
23	306	4	0	336	17	10MB
24	925	7	0	925	17	54MB
25	925	9	65535	925	17	69MB
26	754	7	754	754	17	44MB
27	754	11	65535	754	17	69MB
28	699	7	256	699	17	41MB

Type	Cylinder	Heads	Write Precomp	Landing Zone	Sectors	Size
29	823	10	65535	823	17	68MB
30	918	7	918	918	17	53MB
31	1024	11	65535	1024	17	94MB
32	1024	15	65535	1024	17	128MB
33	1024	5	1024	1024	17	43MB
34	612	2	128	612	17	10MB
35	1024	9	65535	1024	17	77MB
36	1024	8	512	1024	17	68MB
37	615	8	128	615	17	41MB
38	987	3	987	987	17	25MB
39	987	7	987	987	17	57MB
40	820	6	820	820	17	41MB
41	977	5	977	977	17	41MB
42	981	5	981	981	17	41MB
43	830	7	512	830	17	48MB
44	830	10	65535	830	17	69MB
45	917	15	65535	918	17	114MB
46	1224	15	65535	1223	17	152MB
47	USER'S	TYPE				

APPENDIX B: ISA I/O ADDRESS MAP

I/O ADDRESS (HEX)	I/O DEVICE
000 - 01F	DMA Controller 1, 8237A-5
020 - 03F	Interrupt Controller 1, 8259A
040 - 05F	System Timer, 8254-2
060 - 06F	8742 Keyboard Controller
070 - 07F	Real-Time Clock/CMOS and NMI Mask
080 - 09F	DMA Page Register, 74LS612
0A0 - 0BF	Interrupt Controller 2, 8259A
0C0 - 0DF	DMA Controller 2, 8237A-5
0F0 - 0FF	i486 Math Coprocessor
1F0 - 1F8	Fixed Disk Drive Adapter
200 - 207	Game I/O
20C - 20D	Reserved
21F	Reserved
278 - 27F	Parallel Printer Port 2
2B0 - 2DF	Alternate Enhanced Graphic Adapter
2E1	GPIO Adapter 0
2E2 - 2E3	Data Acquisition Adapter 0
2F8 - 2FF	Serial Port 2 (RS-232-C)
300 - 31F	Prototype Card
360 - 363	PC Network (Low Address)
364 - 367	Reserved
368 - 36B	PC Network (High Address)
36C - 36F	Reserved
378 - 37F	Parallel Printer Port 1
380 - 38F	SDLC, Bisynchronous 2
390 - 393	Cluster
3A0 - 3AF	Bisynchronous 1
3B0 - 3BF	Monochrome Display and Printer Adapter

I/O ADDRESS (HEX)	I/O DEVICE
3C0 - 3CF	Enhanced Graphics Adapter
3D0 - 3DF	Color/Graphics Monitor Adapter
3F0 - 3F7	Diskette Drive Controller
3F8 - 3FF	Serial Port 1 (RS-232-C)
6E2 - 6E3	Data Acquisition Adapter 1
790 - 793	Cluster Adapter 1
AE2 - AE3	Data Acquisition Adapter 2
B90 - B93	Cluster Adapter 2
EE2 - EE3	Data Acquisition Adapter 3
1390 - 1393	Cluster Adapter 3
22E1	GPIB Adapter 1
2390 - 2393	Cluster Adapter 4
42E1	GPIB Adapter 2
62E1	GPIB Adapter 3
82E1	GPIB Adapter 4
A2E1	GPIB Adapter 5
C2E1	GPIB Adapter 6
E2E1	GPIB Adapter 7

APPENDIX C: MEMORY MAPPING

Address (hex)	Function	Comments
00000000-0007FFFF	512K System RAM	Cached
00080000-0009FFFF	128K System RAM	Cached
000A0000-000BFFFF	128K Video RAM	Not Cached
000C0000-000C7FFF	32K Video BIOS	Cached
000C8000-000CFFFF	32K I/O ROM	Not Cached
000D0000-000DFFFF	64K I/O ROM	Not Cached
000E0000-000EFFFF	64K Extended BIOS	Not Cached
000F0000-000FFFFFFF	64K On-Board BIOS ROM	Cached
00100000-00BFFFFFFF	System Memory (RAM)	Cached
00C00000-00FFFFFFF	System Memory (RAM)	Cached
01000000-BFFFFFFF	System Memory (RAM)	Cached
C0000000-C1FFFFFF	System Memory (RAM)	Cached
C2000000-FFDFDFFF	System Memory	Cached
FFFE0000-FFFFFFF	128K On-Board BIOS ROM	Not cached

APPENDIX D: INTERRUPT LEVEL ASSIGNMENTS

LEVEL on SYSTEM	LEVEL on IO BUS	TYPICAL INTERRUPT SOURCE
NMI	None	Parity, ISA/EISA Channel Check, Bus Time Out, Fail Safe Timer Timeout
IRQ0	None	Interval Timer 1, Counter 0 Out
IRQ1	None	Keyboard Controller
IRQ2	None	Cascade Interrupts from IRQ8 to IRQ15
IRQ3	IRQ3	Serial Port 2
IRQ4	IRQ4	Serial Port 1
IRQ5	IRQ5	Parallel Port 2
IRQ6	IRQ6	Diskette Controller
IRQ7	IRQ7	Parallel Port 1
IRQ8	None	Real Time Clock
IRQ9	IRQ2	Expansion Bus Pin
IRQ10	IRQ10	Expansion Bus Pin
IRQ11	IRQ11	Expansion Bus Pin
IRQ12	IRQ12	Expansion Bus Pin
IRQ13	None	Coprocessor Error, DMA Chaining
IRQ14	IRQ14	Fixed Disk Drive Controller Expansion Bus Pin
IRQ15	IRQ15	Expansion Bus Pin

PRODUCT INFORMATION RECORD

Record all the information as you receive the product and provide to your supplier in writing in the event that you should need technical support assistance. This will help to speed up the response and get your problem solved.

System Board

Date Purchased or Received: _____

Purchased From: _____

Product Name: _____ PCB Ver: _____ Rev: _____

Serial Number: _____

CPU Processor Speed: _____ Memory Size: _____

BIOS Version: _____ Software Driver Rel #: _____

PCI Add-on Cards:

Model # _____ Interrupt: _____ Slot #: _____

Model # _____ Interrupt: _____ Slot #: _____

Model # _____ Interrupt: _____ Slot #: _____

ISA Add-on Cards:

Model # _____ Interrupt: _____ DMA: _____ Slot #: _____

Model # _____ Interrupt: _____ DMA: _____ Slot #: _____

Model # _____ Interrupt: _____ DMA: _____ Slot #: _____

Model # _____ Interrupt: _____ DMA: _____ Slot #: _____

For More Information .
