LOCAL BUS-486C/50

User's Manual

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CHAPTER 1
INTRODUCTION

Overview

The Local Bus-B486C board is a high-performance and high-enhanced function board that provides the primary elements for building more advanced system. This board is functionally compatible with the system board in the IBM PC/AT, and vastly exceeds it in function, capability, and processing power. This board also offers the highest performance for DOS, OS/2, Windows, and UNIX System V/386 applications.

Features

Major features of the Local Bus-B486C board include:

- Intel 80486DX-25/33/50, 486SX-20/25, or 487SX-20/25 CPUs.
- Socket for Weitek 4167 floating point accelerator.
- Dual speeds 8 MHZ or 20/25/33/50 MHZ, switchable by either hardware switch or software control.
- 32 bit memory expandable from 1 M Byte to 64 M Bytes on system board.
- Optional 32/64/128/256KB secondary level cache memory.
- Mixed or matched DRAM size from 256KB, 1MB, or 4MB density.
- Caching shadow RAM function from C0000H to FFFFFH, and supporting 32 KB blocks selection in the add-on card ROM ranging from C0000H to DFFFFH.

. Three 32-bit Local Bus (compatible 16-bit ISA) and five 16-bit ISA expansion slots.
. Baby AT size and tooling hold, fit desk-top and tower cabinet.
. Three-channel timer, sixteen interrupt, and seven direct memory access (DMA) channels.
. Fast CPU reset and fast GATE A20 for OS/2 optimization.
. Hardware reset switch capability.

Benchmark

The following shows the system performance benchmark.

Benchmark	CPU	
	486DX	486SX/487SX
Landmark V1.14 (MHz)	114.1 (25) 150.7 (33) >200 (50)	90.8 (20)
Power Meter V1.5 (MIPS)	11.136 (25) 21.653 (50)	8.838 (20)

CHAPTER 2
FEATURES OF THE LOCAL BUS-B486C BOARD

Overview

This chapter briefly describes every major features of the Local Bus-B486C main board. It covers the following topics:

(a) Microprocessor
(b) Coprocessor
(c) RAM Module
(d) CACHE Module
(e) ROM Module
(f) Real-Time Clock
(g) Shadow RAM

Microprocessor

The CPU option for Local Bus-B486C can be Intel 80486DX, 486SX, or 487SX microprocessor. The 80486 combines three firmly separate chips into one : an 80386 processor, a math coprocessor, and an 8 KB memory cache. A new burst mode allows 32 bits of data to be transferred in one clock cycle - twice the speed of the 80386DX. Intel's 486SX is a slow-down 80486 with its built-in FPU deliberately disabled. Except for slightly difference in pin assignment, 487SX CPU is fully functional

compatible with 486DX CPU. Those are fully software compatible with earlier Intel processors. The Local Bus-B486C board is designed to build a system as network or database servers, applications development workstations, or high-end CAD/CAM workstations.

For those applications that require slower operation, the Local Bus-B486C board offers a Jumper that enables the board to simulate the performance of 8 MHZ PC/AT. The Jumper is switchable between 8 MHZ and 20/25/33/50 MHZ with either a hardware or a software switch.

Coprocessor

The coprocessor socket is an 144-pin PGA socket for Weitek 4167 floating point accelerator. The 4167 is upwardly compatible with Weitek 3167 chip, which is used to increase the numeric performance of 386-based systems.

RAM Module

The Local Bus-B486C board has a 32-bit DRAM subsystem that provides up to 64 Megabyte memory. The mother board accepts 256KB, 1MB, or 4MB of 80 nanosecond page-mode Single In Line Memory Modules (SIMMS). You can expand the system board memory from 1MB to a total of 64MB. Since the Local Bus-B486C is able to house all 64MB system RAM on the mother board, user does not need any proprietary memory board. Therefore, it would be easier for upgrading the system memory.

CACHE Module

Although the Microprocessor has an internal 8KB cache memory, it is just enough for DOS applications. When you run memory-hungry software (such as UNIX, XENIX), the benefits of an external cache are clear. The Local Bus-B486C board provides 32KB, 64KB, 128KB, or 256KB external cache options.

ROM Module

The system board contains 64K or 128K bytes of ROM, which comprises the system BIOS. This memory resides at the upper 64K or 128K bytes of address space in the first 1MB and is also mapped to the upper 64K or 128K bytes of the last 1MB of the 4GB space when the processor switches into protected mode.

Real-Time Clock

A Real-Time Clock (RTC) is for maintaining the time and date. This subsystem also contains 64 bytes of RAM in addition to the clock/calender. The clock/calendar information and RAM are kept active by connecting the device to an external battery when system power is turned off.

Shadow RAM

The shadow RAM is a technology that loads system BIOS and adapter BIOS directly into fast RAM on boot-up of the computer, offering enhanced speed at the cost of 384KB memory from the first 1MB of system RAM.

Local Bus

This bus, also an ISA compatible, is defined for high speed peripherals. The following table shows its signal definition based upon an EISA connector.

PIN	ROW F	PIN	ROW B	PIN	ROW E	PIN	ROW A
1	CA2	1	GND	1	GND	1	IOCHK#
2	CA4	2	RESETDRV	2	CA3	2	SD7
3	CA6	3	+5V	3	CA5	3	SD6
4	CA8	4	IRQ9	4	CA7	4	SD5
5	+5V	5	-5V	5	CA9	5	SD4
6	ACCESS KEY	6	DRQ2	6	ACCESS KEY	6	SD3
7	CA10	7	-12V	7	GND	7	SD2
8	CA12	8	NOWS#	8	CA11	8	SD1
9	CA14	9	+12V	9	CA13	9	SD0
10	CA16	10	GND	10	CA15	10	CHRDY
11	+5V	11	SMWTC#	11	CA17	11	AEN#
12	CA18	12	SMRDC#	12	GND	12	SA19
13	CA20	13	IOWC#	13	CA19	13	SA18
14	CA22	14	IORC#	14	CA21	14	SA17
15	CA24	15	DAK3#	15	CA23	15	SA16
16	ACCESS KEY	16	DRQ3	16	ACCESS KEY	16	SA15
17	+5V	17	DAK1#	17	CA25	17	SA14
18	DRAWS#	18	DRQ1	18	GND	18	SA13
19	RST#	19	REFRESH#	19	GND	19	SA12
20	+5V	20	BCLK	20	RDY#	20	SA11
21	BE2#	21	IRQ7	21	BE3#	21	SA10
22	BE0#	22	IRQ6	22	BE1#	22	SA9
23	HRQ0	23	IRQ5	23	GND	23	SA8
24	M/IO#	24	IRQ4	24	HLDA1	24	SA7
25	ACCESS KEY	25	IRQ3	25	ACCESS KEY	25	SA6
26	W/R#	26	DAK2#	26	ADS#	26	SA9
27	+5V	27	T/C	27	D/C#	27	SA8
28	SCLK	28	BALE	28	RDY0#	28	SA7
29	LDEV#	29	+5V	29	GND	29	SA6
30	CD31	30	OSC	30	CD30	30	SA7
31	CD29	31	GND	31	CD28	31	SA6

PIN	ROW H	PIN	ROW D	PIN	ROW G	PIN	ROW C
1	CD27	1	M16#	1	GND	1	SBHE#
2	+5V	2	IO16#	2	CD26	2	LA23
3	CD25	3	IRQ10	3	CD24	3	LA22
4	CD23	4	IRQ11	4	CD22	4	LA21
5	CD21	5	IRQ12	5	CD20	5	LA20
6	ACCESS KEY	6	IRQ13	6	ACCESS KEY	6	LA19
7	CD19	7	IRQ14	7	CD18	7	LA18
8	CD17	8	DAK0#	8	CD16	8	LA17
9	CD15	9	DRQ0	9	GND	9	MRDC#
10	+5V	10	DAK5#	10	CD14	10	MWTC#
11	CD13	11	DRQ5	11	CD12	11	SD8
12	CD11	12	DAK6#	12	CD10	12	SD9
13	CD9	13	DRQ6	13	CD8	13	SD10
14	CD7	14	DAK7#	14	GND	14	SD11
15	ACCESS KEY	15	DRQ7	15	ACCESS KEY	15	SD12
16	+5V	16	+5V	16	CD6	16	SD13
17	CD5	17	MASTER#	17	CD4	17	SD14
18	CD3	18	GND	18	CD2	18	SD15
19	CD1			19	CD0		

CHAPTER 3
JUMPER SETTING

Overview

A jumper is a kind of switch which is used to enable/disable a feature, or to make a selection between two features. A jumper has either two or three pins. Placing a plastic cap over both pins means short. Removing a Plastic cap from both pins means open. The Local Bus-B486C board has several jumper switches that are used to configure the system board. Figure 3-1 tabulates the function of all jumpers. And, Figure 3-2 shows the locations of all jumper blocks on the Local Bus-B486C board.

Jumper	Function
JP2	Video Selection
ZIP1 ZIP2	Cache Size Selection
SW1 JP20 JP21	CPU Type Selection

Figure 3-1 Jumper Function

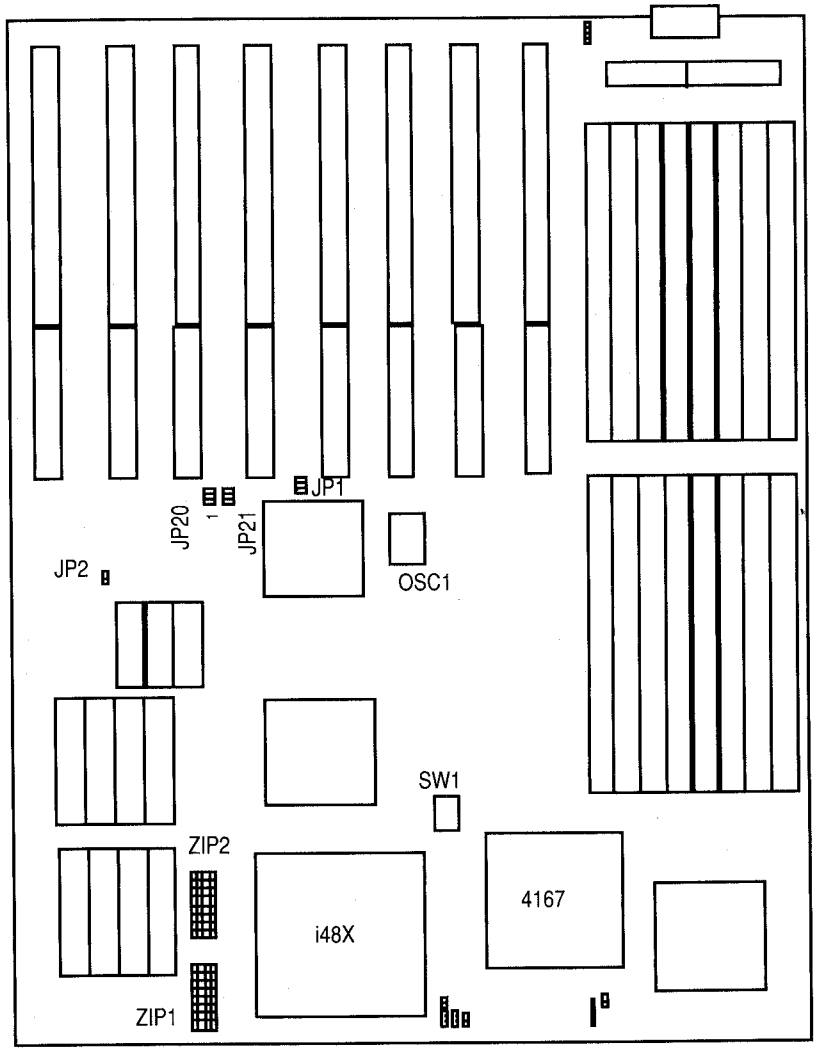


Figure 3-2 Jumper Locations

Battery Discharge Jumper (JP1)

JP1 is able to discharge the content saved in the real time clock, i.e. 82C206. This is quite useful, especailly when password is forgetten.

JP1	Pin	Function
	1	Battery
	2	82C206 VDD
	3	GND
1, 2 Short: Battery on supply power		
2, 3 short: Discharging 82C206		

Video Selection Jumper (JP2)

JP2 should be set to choose either color or monochrome monitor is being in use. The video selection jumper is an 1x2 header whose pin assignment is shown as follows:

JP2	Pin	Function
	1	GND
	2	Select Pin
	1, 2 Short	Monochrome
	1, 2 Open	Color

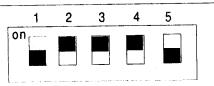
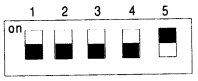
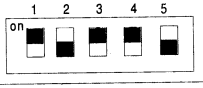
Cache Size Seclection (ZIP1 & ZIP2)

ZIP1 and ZIP2 are for choosing the cache size, 32KB, 64KB, 128KB, or 256KB.

CPU Type Selection (SW1)

SW1 is for defining the CPU type, with different pin assignments corresponding to each CPU, 80486DX, 486SX, or 487SX.

The following figure shows the relationship between CPU type and Oscillator value. This jumper will be adjusted to their proper settings when shipped out by the manufacturer and should not be handled by the user.

SW1							
CPU Type	486DX(2)			486SX		487SX	
CPU SPEED	486DX/25 486DX2/50	486DX/33 486DX2/66	486DX/50	486SX/20	486SX/25	487SX/20	487SX/25
OSC1(MHZ)	25	33	50	20	25	20	25
JP20 JP21							
DRAM speed option (*) (MHz)	25.0	33.0	50.0	Slow CPU (**)	25.0	Slow CPU (**)	25.0
Bus clock frequency select (*)	1/3 ACLK	1/4 ACLK	1/6 ACLK	1/3 ACLK	1/3 ACLK	1/3 ACLK	1/3 ACLK

(*) : "DRAM speed option" & "Bus clock frequency select" are options in the ADVANCED CHIPSET SETUP of CMOS BIOS, and should be set as the proper values indicated in the above table.

(**): "Slow CPU (below 25MHz)" is another option in the ADVANCED CHIPSET SETUP and should be set as "ebabled" when system is below 25MHz.

Connectors

The Local Bus-B486C main board has several connectors, which are used for computer chassis and power supply to connect to the main board. Figure 3-3 tabulates the function of all connectors. Also, Figure 3-4 illustrates the locations of all the connectors on this main board.

Connector	Function
CN1	Keyboard
CN2	External Battery
CN3	Power Supply
CN4	Keyboard Lock
CN5	Turbo LED
CN6	Turbo Switch
CN7	Speaker
CN8	Hardware Reset

Figure 3-3 Connector Functions

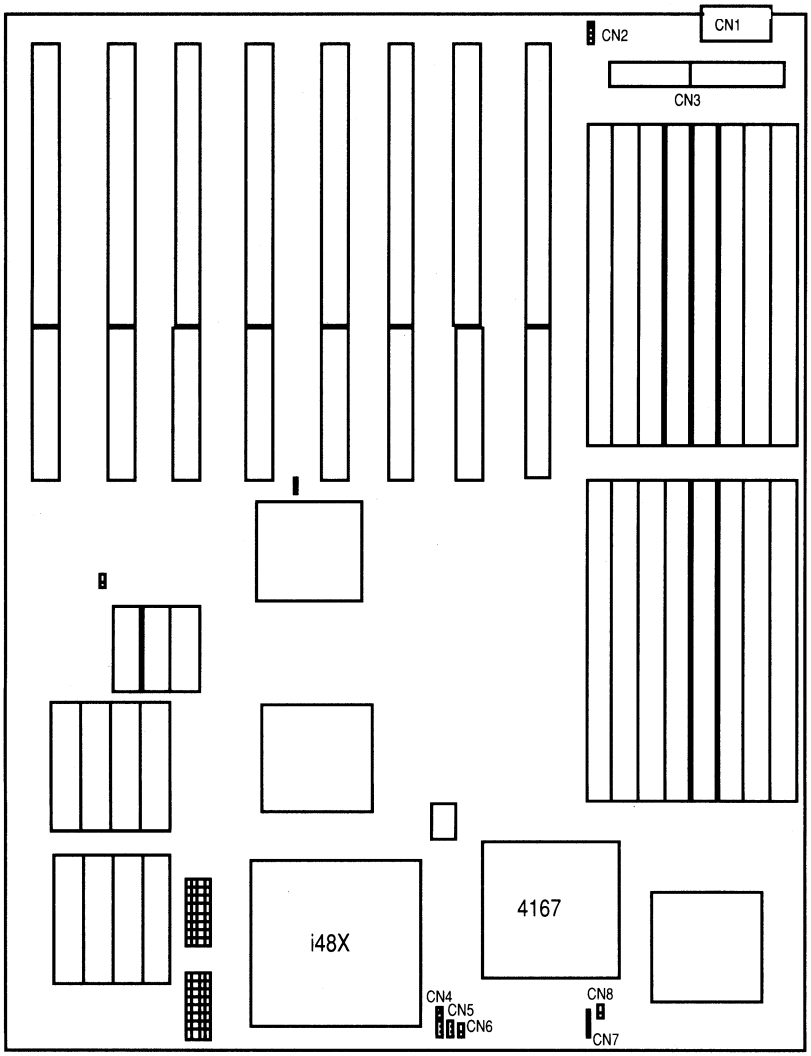


Fig 3-4 Connector Locations

Keyboard Connector (CN1)

CN1 is a 5-pin 90-degree printed circuit board mounting and DIN connector. Its pin assignment is shown in the following table:

	Pin	Function
CN1	1	Clock
	2	Data
	3	NC
	4	GND
	5	Vcc

External Battery (CN2)

CN2 is for External Battery.

	Pin	Function
CN2	1	Battery (V+)
	2	NC
	3	GND
	4	GND

Power Connector (CN3)

There are two power supply connectors on all AT-compatible power supply, PS8 and PS9. Be aware the ground signals for PS8 and PS9 always stick with each other when hooked up to the connector CN3.

The following figure shows the pin assignment of the two power supply output connectors.

	Pin	Function
CN3	1	Power Good
	2	+ 5 VDC
	3	+12 VDC
	4	-12 VDC
	5	GND
	6	GND
	7	GND
	8	GND
	9	-5 VDC
	10	+5 VDC
	11	+5 VDC
	12	+5 VDC

Keyboard Lock Connector (CN4)

CN4 provides an interface to the key switch which can enable/ disable the keyboard operation. To operate the keyboard, a right key to turn the key-switch to "ENABLE" is needed in advance. Power LED indicates whether the power is on. Keyboard Lock Connector is an 1x5 header whose pin assignment is shown as follows:

	Pin	Function
CN4	1	Power for LED
	2	N.C
	3	Ground
	4	Keyboard inhibit
	5	Ground

Turbo LED Connector (CN5)

CN5 is for the connection to turbo LED, which is normally installed on the front panel of the chassis. When the system is working in turbo mode, the LED is turned on. Turbo LED Jumper is an 1x2 header whose pin assignment is shown as follows:

	Pin	Function
CN5	1	Signal power
	2	Turbo LED

Turbo Switch (Hardware Switch) Connector (CN6)

CN6 allows you to select the operating speed for the microprocessor, 8 MHZ or 25/33/50 MHZ. Turbo Switch is an 1x2 header whose pin assignment is shown as follows:

	Pin	Function
CN6	1	GND
	2	Select

Speaker Connector (CN7)

CN7 provides you to enable/disable the connection to a speaker for audible tone generation. Speaker Connector is an 1x4 header whose pin assignment is shown as follows:

	Pin	Function
CN7	1	speaker Ou
	2	NC
	3	ND
	4	VCC

Hardware Reset Connector (CN8)

CN8 can help you reboot the system without turning off the power. To reboot the system, touch the button once. Hardware Reset Connector is an 1x2 header whose pin assignment is shown as follows.

	Pin	Function
CN8	1	GND
	2	Select
1, 2 Short: Hardware reset		

CHAPTER 4
INSTALLATION

Overview

This chapter provides the information for installing a system with the Local Bus-B486C board. It also describes how to install memory and coprocessor onto the system board.

Static Precautions

Static electricity is a constant danger to a computer system. The charge is usually high enough to damage integrated circuits on the Local Bus-B486C board. To avoid damaging your equipment from electrostatic discharge, observe the following precautions:

(1) Do not remove Local Bus-B486C board from anti-static packaging until you are ready to install it.

(2) Discharge any static electric charge that may have built-up in your body by touching a grounded, anti-static surface, or an unpainted portion of the system unit chassis for a few seconds, before installing or removing components from your Local Bus-B486C board.

(3) When handling an individual card, boards or modules, becareful to avoid contact with the components and golden fingers on them. It is best to handle them by their edges or mounting bracket.

When you follow the above procedures, there should be no static discharge problems.

Mounting Holes

The Local Bus-B486C has nine mounting holes drilled in the printed circuit board. These will line up with some or all of the mounting points on any PC/AT cabinet or tower cabinet. Some forms of mounting hardware are used to fasten the board to the cabinet. In some cabinets, the long inside edge of the board fits under metal flanges in the cabinet frame instead of being screwed to the cabinet.

Installing the Coprocessor

There is a socket provided by the Local Bus-B486C for a Weitek 4167 numeric coprocessor to speed up the floating-point-intensive applications. When adding this chip, please follow the procedures:

1. The corner, with a notch located at the inner side of the coprocessor socket, points to pin 1 position of 4167. And, a corner of a coprocessor with a dot usually means the position for pin 1 (this corresponding corner of 4167 is also slightly cut off). The dot on the coprocessor should be oriented to the same direction with the notch of the coprocessor socket.

2. When the coprocessor's pins are properly seated in the pinholes, smoothly press the coprocessor to firmly install the chip into the socket.

3. The frequency of the coprocessor should match the specification of the system's microprocessor.

Installing the SIMM Modules

The Local Bus-B486C board provides 16 sockets for SIMM modules. These 16 sockets are divided into four banks and each bank can accommodate four SIMM sockets. Every bank can accept 256 KB, 1MB or 4MB SIMM modules, but all of the four SIMM modules used in the same bank must be with the same size. This ability for mixing assorted SIMM modules on the four banks allows the system to be shipped with minimal memory and upgraded without sacrificing the memory already on board.

The following figure shows the arrangement of the memory socket on the system board.

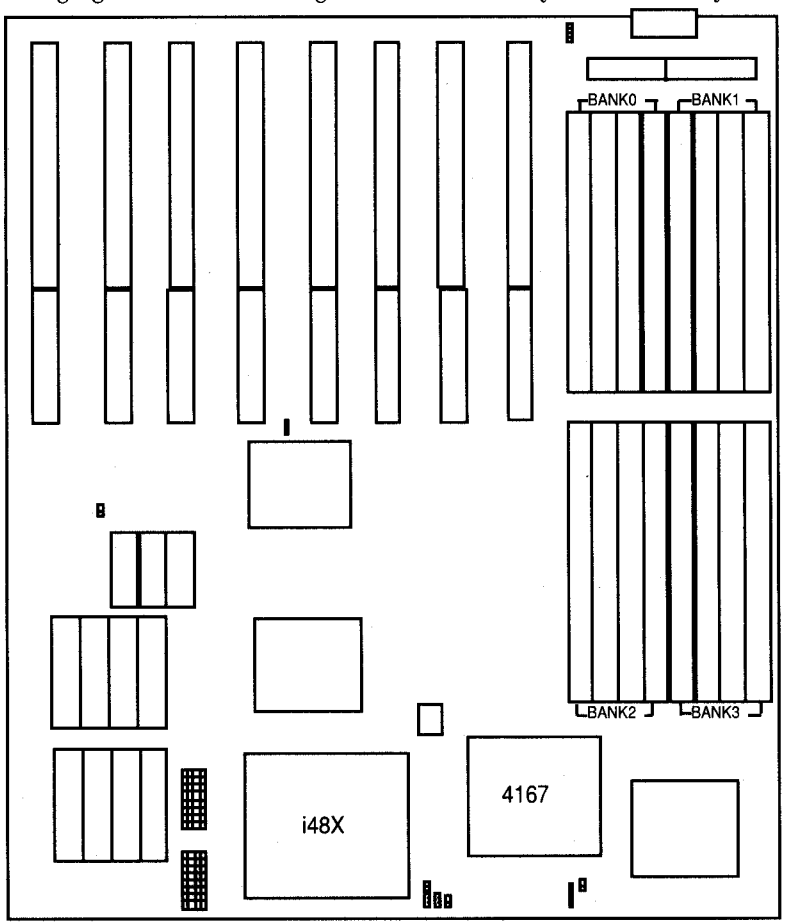


Figure 4-1. SIMM Socket Layout

System RAM Specification

To optimize accessing to the on-board memory, the Local Bus-B486C main board must be employed the fast page mode SIMM modules. The access time of a SIMM is normally specified by the RAS access time (tRAC). And, the CAS access time (tCAC) is usually for reference only. The following shows the timing specification for the fast page mode DRAM SIMM for this motherboard:

1. 80486DX 25/33/50MHZ

. tRAC (RAS access time): 80ns or less.
. tCAC (CAS access time): 30ns or less.

The following also shows some options, which should be chosen with respect to each CPU operating speed when doing the CMOS BIOS setup (please also reference to Appendix A for more detail):

CPU (MHz)speed	50	40	33	25	20
DRAM speed	slowest	slower	faster	fastest	fastest
Write Pulse	2T	2T	1T	1T	1T

Adding Memory Modules to a SIMM Socket

It is recommended that you install the memory from Bank0 to Bank3. A card retainer holds a SIMM with a securing lip on the solder side and a stud through a hole in the card on each end. Slip a SIMM straight down into the first empty slot, with the component side facing to the power supply. You may need to guide the SIMM down with both hands to have it straight in. Gently press the SIMM back against the lips and studs into the holes on the SIMM. Be sure the SIMM is securely seated in its slot and both ends are engaged by the card retainer.

Figure 4-2 shows all the memory configurations.

BANK 0	BANK 1	BANK 3	BANK 4	TOTAL MEMORY
256K SIMM				1MB
256K SIMM	256K SIMM			2MB
256K SIMM	256K SIMM	1M SIMM		6MB
256K SIMM	256K SIMM	1M SIMM	1M SIMM	10MB
256K SIMM	256K SIMM	4M SIMM		18MB
1M SIMM				4MB
1M SIMM	1M SIMM			8MB
1M SIMM	1M SIMM	1M SIMM		12MB
1M SIMM	1M SIMM	1M SIMM	1M SIMM	16MB
1M SIMM	4M SIMM			20MB
1M SIMM	1M SIMM	4M SIMM		24MB
1M SIMM	4M SIMM	4M SIMM		36MB
1M SIMM	1M SIMM	4M SIMM	4M SIMM	40MB
4M SIMM				16MB
4M SIMM	4M SIMM			32MB
4M SIMM	4M SIMM	4M SIMM		48MB
4M SIMM	4M SIMM	4M SIMM	4M SIMM	64MB

Figure 4-2 Memory Configuration

Installing the Cache Memory

The Local Bus-B486C board supports 64K,or 256K of Cache RAM sizes. There are 8 sockets for installing the optional secondary cache. After completing the SRAM insertion, the jumper should be placed at the corresponding position for its proper operation. The following figure illustrates the locations of the cache memory on the Local Bus-B486C board.

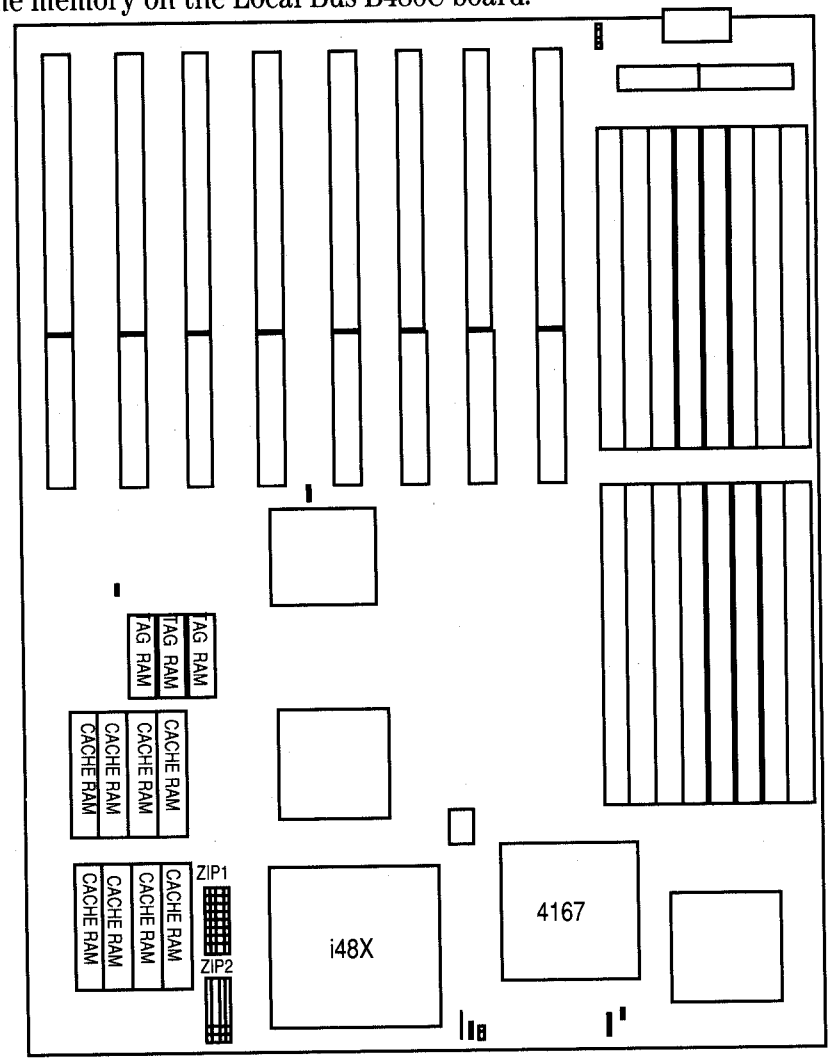


Figure 4-3 Cache Memory Position

Cache Specification

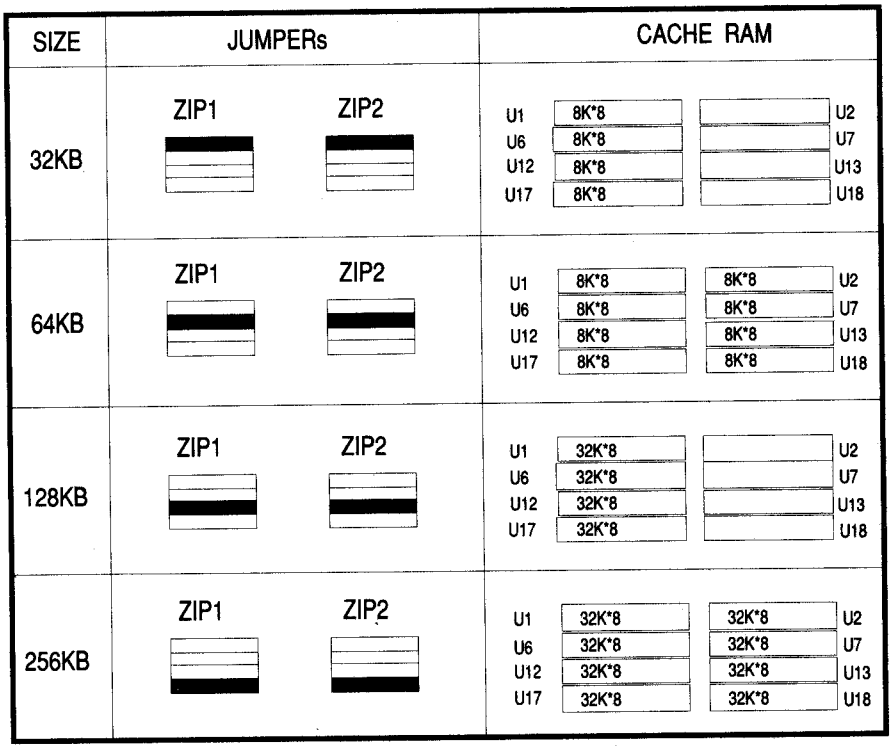
A Cache is a fast and relatively small memory which resides between the processor and the main memory. An SRAM Cache system makes all of the large main memory (typically DRAM) appear to respond as fast as the high-speed SRAMs in the Cache, thereby providing the performance of high-speed SRAMs at a cost approaching that of lower-speed DRAMs.(Please also reference to Appendix A-4 for more datails)

CPU Clock Frequency (MHz)	20	25/33/50
Cache SRAM Speed Required	35ns	25ns
Tea (Address access Time)	35ns	25ns
Tace (chip enable access time)	35ns	25ns
Thzoe(Output disable time)	15ns	10ns

Cache SRAM Speed Required

Cache Memory Configuration

Figure 4-4 shows the relationship among cache size, jumper, tag RAM, and cache RAM.



Note: ▬ insert resistor array to this jumper for selecting proper cache size.

Figure 4-4 Cache Size, Jumper, Tag RAM, and Cache RAM

CHAPTER 5
BIOS SETUP

Overview

The Local Bus-B486C board offers AMI BIOS. The SETUP program is resident in the BIOS and used to configure the system. Those system options are stored in the CMOS. If the CMOS is good, the system is configured with the values stored in the CMOS. If the CMOS is bad, the system is configured with the default values stored in the ROM file.

The AMI BIOS has a password feature in it. The user is asked for the password either in every boot or for entering into the SETUP program or never. If the CMOS is good, the user is asked for the password stored in the CMOS, else he is asked for the ROM password. The different options in the BIOS Setup program are shown as Figure. 5-1. The user is given a warning message before he is allowed to change any of the setup parameters. The warning message is shown in Figure. 5-2.

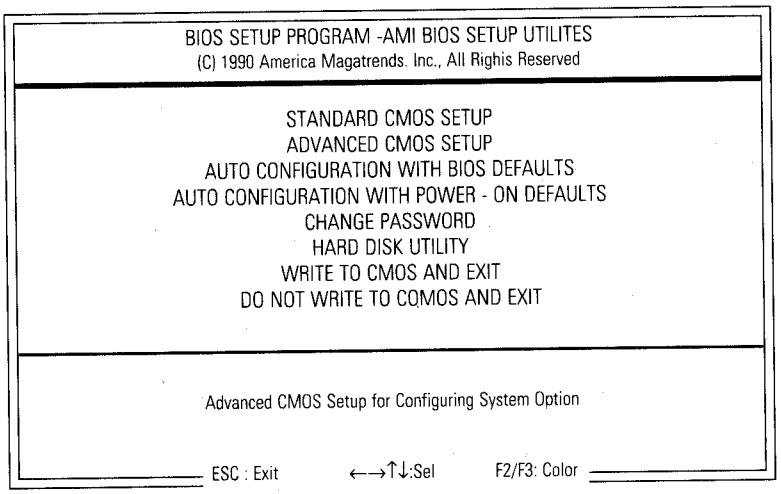


Figure 5-1 BIOS Setup Options

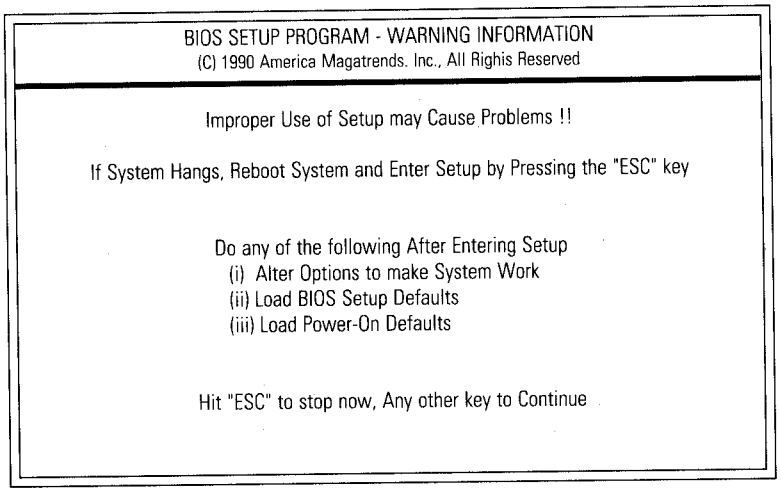


Figure 5-2 BIOS Setup Warning Message

Standard CMOS Setup

This option is used to configure the following options:

- Date: Month, Date and Year
- Time: Hour, Minute and Second
- Daylight Saving: Disabled or Enabled
- Hard Disk C: and Hard Disk D: The user can choose any of the standard hard disk types from 1 to 46. The user also can choose type 47 which is the user definable type. The user must enter the hard disk parameters if he wants to choose the user-definable hard disk type per drive, i.e., type 47 may be different for drive C: and for drive D:
- Floppy drive a: and Floppy drive B: 360 KB 5 1/4", 1.2 MB 5 1/4", 720KB 3 1/2", 1.44 MB 3 1/2", Not Installed
- Primary Display: Monochrome, Color 40x25, VGA/PGA/EGA, Color 80x25, Not Installed
- Keyboard: Installed or Not Installed

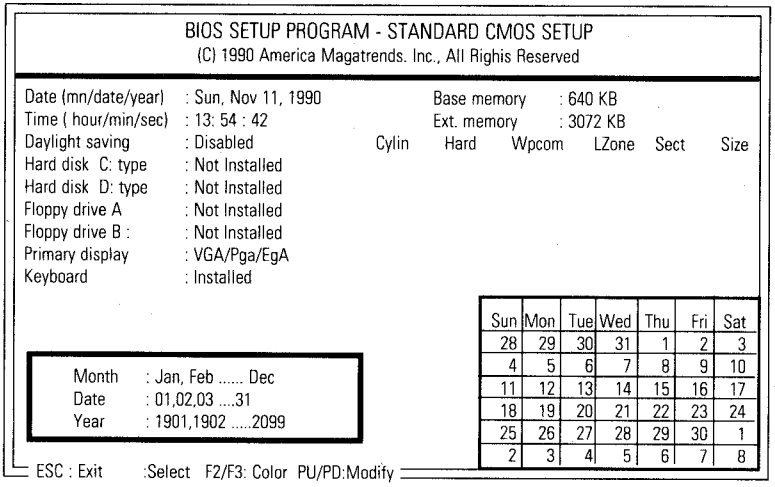


Figure 5-3 Standard CMOS Setup Screen

Advanced CMOS Setup

The ADVANCED CMOS SETUP option is used to set the various system options for the user. The user can have various options, some of which are listed below:

- Typematic Rate Delay
- Typematic Rate
- Password checking for Setup
- Above IMB memory test
- Memory test tick sound
- Memory parity error check
- Co-processor detection
- Scratch RAM area for BIOS
- Wait for <F1> if there is any error
- Power-On num lock status
- CPU Speed at system boot
- Video ROM Shadow
- Adaptor ROM Shadow
- Main ROM Shadow

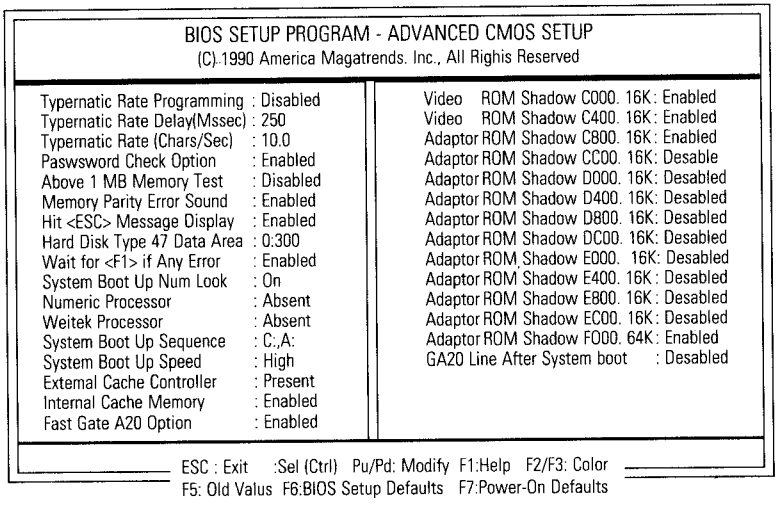


Figure 5-4 Advanced CMOS Setup Screen

Change Password

This option can be used to change the password (of the user). The password can be named as long as six characters. The password is stored in the CMOS. If the CMOS is bad, there is a default password (AMI) which is stored in the ROM.

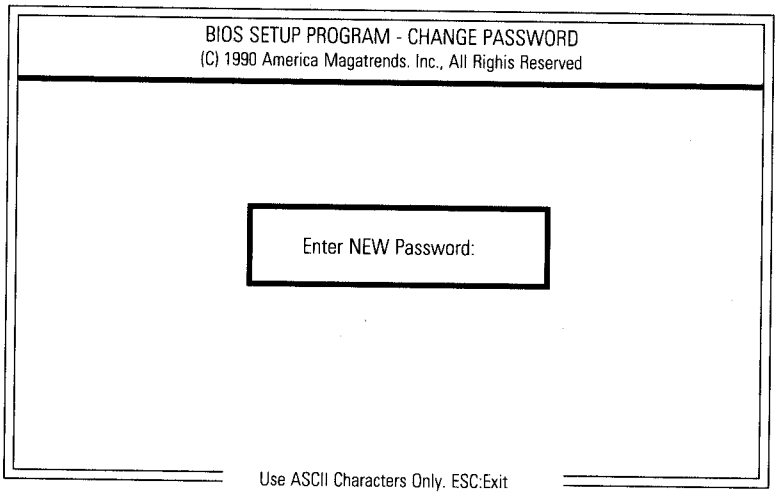


Figure 5-5 Change Password Screen

Hard Disk Diagnostics

This option is used to format the hard disk. The disk drive information is taken from the Standard CMOS Setup information. To change the Disk Drive types, the user must go to the Standard CMOS Setup and change it. The user will be asked for the Disk Drive (C/D) if 2 disks have been installed. The type for the hard disk is same as that shown in Standard CMOS Setup.

The various sub-options are:

(1) Hard Disk Format: For formatting the hard disk. The user will be asked for the Interleave Factor. The user can also enter the Bad Track List.

(2) Auto Interleave: For automatically deleting the best interleave factor and formatting the disk. The user can enter the Bad Track List.

(3) Media analysis: The user is asked for the Interleave Factor. The Bad Tracks List will be generated for the hard disk. The user can update the Bad Track List if wanted.

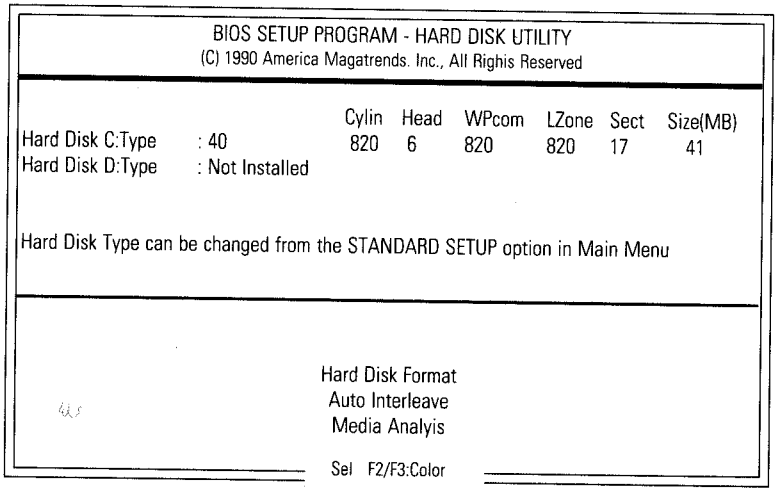


Figure 5-6 Hard Disk Utility Setup Screen

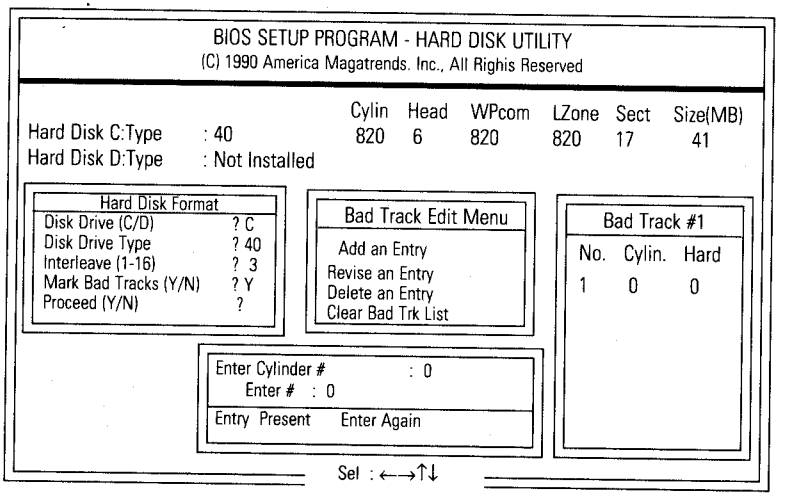


Figure 5-7 Hard Disk Utility Options

Write To CMOS and Exit

The options set in the standard setup, Advanced Setup, Advanced Chipset Setup and the New Password (if changed) are stored in the CMOS. The CMOS checksum is calculated and written into the CMOS. After that, control right will be switched back to the BIOS.

Do Not Write To CMOS and Exit

By doing so, control right will be just switched back to the BIOS without writing the updated data into the CMOS.

Changing The Processing Speed

The AMI BIOS allows you to change system speeds through the keyboard at any time. Normally you will always want to use the high speed mode unless you have software compatibility problems. These problems occurs when software uses CPU instruction as a delay values.

Following are the key combinations and their meanings.

	Key Combinations	Meanings
1.	<Ctrl> <Alt> <+>	Switch to High Speed
2.	<Ctrl> <Alt> <->	Switch to Low Speed

Appendix A
SiS/ISA 486 SiS85C401

FUNCTIONAL DESCRIPTION
Cache Controller
Direct Mapped Cache

Cache is a good means to de-couple fast processor from slow main memory and get the best performance of the processor. Direct mapped cache is the most suaightforward, flexible, easyto-implement, and cost-effective cache structure. A 2/4-way set associative cache has better performance than the direct mapped cache, but the delta is negligible when the cache size is large enough (e.g. 64KB). The SiS85C401 provides a fast 8-bit tag comparator and all the control logic for a secondary cache of the 80486 processor. To implement a cache, user just needs to add SRAMs for the tag and data memories. The maximum cache size in the configuration register is 256KB but larger (512KB, IMB, etc.) size is still applicable.

Write-Back vs. Write-Through

When the contents of the cache data are modified (i.e. written) by the processor, the same changes should be made in the main memory as well. Failing to do so will raise an inconsistency problem when the stale data in the main memory are accessed. There are two general approaches to update the main memory. The first is the write-through method and the second is the writeback (also called "copy-back") method.

In a write-through cache system, data are written to the main memory immediately while or after they are wntten into the cache. So the main memory always contains valid data. All the memory writes will only be as fast as the DRAM write and do not take the speed advantage of the cache. To improve the write speed, a write buffer (queue) can be used to store the written data, so the processor can do other things before the data are actually written into the main memory. Since there is already a four-level wnte buffer built-in in the 80486, the DRAM access penalty coming from the write cycles is reduced significantly.

In a write-back cache system, there is an "alter" bit per data LINE (data line means the data block referenced to a specific tag). When a write hit happens on the *cache, the* corresponding alter bit will be set. The written data are transferred to the main memory when they are to be over-written by a cache line fill. In this case, the cache controller checks the corresponding alter bit. If the alter bit is set, the cache data will then be written to the main memory before the cache line fill starts.

A write-back cache can offer higher performance than a write-through cache if writes to the main memory are much,slower than writes to the cache. The write-back cache is also favored when a memory location is written several times in the cache before written into the main memory. The performance advantage of the write-back cache over write-through cache is software dependent.

The SiS85C401 can be configured to provide a write-back or write-through cache scheme. Besides tag and data RAM, a write-back cache needs an SRAM for the alter bits. So a writeback cache may have better performance, but costs more, than a write-through cache does. It is up to the indivisual user to judge if the extra cost of the write-back cache is justified.

80486 Burst Cache Line Fill

The internal cache of the 80486 has a 16-byte line size. When a read miss happens in the internal cache, the 80486 initiates off-chip memory read cycles to update current cache line. The 80486 will read 16 continuous bytes (4 doublewords). To increase the bus throughput, the 80486 provides a burst mode transfer, four doublewords can be read sequentially in 5 processor clocks (2-1-1-1) at the fastest.

The secondary cache provided by the SiS85C401 also has a 16-byte line size. It supports the 80486 burst read cycles to get the fastest cache line fill. When both the 80486 intemal and secondary caches encounter a read miss, they are updated with the data read from DRAM simultaneously.

Cache Update Policy

For CPU cycles, the content of the cache memory is renewed when either the cache read miss or write hit occurs. Tag and data RAMs are both updated in the cache read miss cycles. In the cache write hit cycles, the SiS85C401 updates only the data RAM.

In the cache write miss cycles, the 80486 writes data into the main memory (DRAM), while the cache memory remains unchanged. The alter bits in the write-back cache are reset in the cache update (read miss) *cycles* and *set* in the write hit cycles.

When the cache is disabled, all the CPU reads to the cacheable memory, are treated as cachc read miss, so both tag and data RAMs are updated. This feature is used tO initialize the cache memory before enabling it.

In DMA/master cycles, the cache data RAM is written when a write hit occurs, to assure the cache coherency. Cache memory is not accessed in DMA/master write miss or read cycles for the write-through cache. For the write-back cache, DMA/master read hit cycles are conducted to the cache, not to the DRAM.

Cache Size Options(16 * 4 -20)

Cache Size	Tac RAM	Data RAM	Alter RAM	Cacheable Size
32KB	2Kx8	8Kx8 x4	2Kxl	8MB
64KB	4Kx8	8Kx8 x8	4Kxl	16MB
128KB	8Kx8	32Kx8 x4	8Kxl	32MB
256KB	16Kx8	32Kx8 x8	16Kxl	64MB
51 2KB	32Kx8	1 28Kx8 x4	32Kxl	64MB

The cacheable DRAM size is determined by the cache size because the tag address field is always 8-bit wide. The on-board DRAM beyond the cacheable size is not cacheable for the secondary cache. It is still cacheable for the 80486 internal cache, however.

Cache Speed Options

· *The* secondary cache can be configurated to non-interleave or two-bank interleave. Two-bank interleaved *cache can* use slower *cache data* RAM but needs more data RAM chips.

The SiS85C401 provides four cache read speed options: 2-1-1-1, 3-1-1-1, 2-2-2-2 and 3-2-2-2, and two options of cache write cycle: 2T or 3T. The cache read speed x-y-y-y is selected via the bit 7 of configuration register 60 (x) and the bit 0 of configuration register 61 (y). The 2T cache write is applicable only when the first cache read of a burst is also set to 2T (2-1-1-1 or 2-2-2-2).

To reduce the propagation delay of the chip output buffer, the SiS85C401 employs an "advanced clock" instead of CPU clock to clock the cache read control signals. The adv;mced clock should lead CPU clock by 3 to 7 ns. It will increase the margin of data RAM access time. For 16/20 MHZ systems, the ACLK can be connected to CPUCLK to simplify the clock circuit.

The following is a table of cache configurations and suggested speed ratings of the SRAM for implementing the cache data RAM for various speeds of the 80486 CPU.

Cache Confiauration	25MHz CPU	33MHz CPU	40MHz CPU	5OMHz CPU
2-1-2 Interleave (*1)	35 (*2)	-20	-12	---
2-1-2 Non-interleave	-25	-15	---	---
2-1-3 Interleave .	-40	-25	-20	---
2-1-3 Non-interleave	-25	- 15	---	---
3-1-3 Interleave	-55	-35	-25	-15
3-1-3 Non-interleave	-25	-15	---	---
2-2-2 Non-interleave	-35	-20	-12	---
2-2-3 Non-interleave	-40	-25	-20	---
3-2-3 Non-interleave	-65	-45	-35	-25

Note: * 1. x-y-z means x-y-y-y burst read and zT write cycle
* 2. -m means the access speed of SRAM in ns.

The following is a table of cache configurations and suggested speed ratings of the SRAM for implementing the cache tag and alter RAM for various speeds of the 80486 CPU.

Cache ConfiauraUon	25MHz CPU	33MHz CPU	40MHz CPU	50MHz CPU
2-X-2	-25	-20	-1 2	-----
2-X-3	-35	-25	-15	-----
3-X-3	-45	-35	-25	-20

· **Note: X presents elther 1T or 2T cycles.**

Non-Cacheable Regions

In some applications, users desire a block of memory not to be cached. The SiS85C401 provides two programmable non-cacheable regions to serve this function. Besides, the cacheability of the shadow RAM can be programmed in 32KB granularity.

Only the on-board DRAM directly controlled by the SiS85C401 is cacheable. The memory residing on the AT add-ons is non-cacheable. When a memory space is mapped by both the on-board DRAM and AT add-on memory, CPU access will be conducted to the on-board DRAM. If users desire the AT add-on memory to be accessed instead of the on-board DRAM at the overlapped memory space, the two non-cacheable regions can be used to disable the on-board DRAM in the programmed space.

The size and starting address of two non-cacheable regions are programmable in configuration register 64, 65, 66 and 67. The validity of the starting address bits depends on the size of related non-cacheable region.

Size	A23	A22	A21	A20	A19	A18	A17	A16
64K	V	V	V	V	V	V	V	V
128K	V	V	V	V	V	V	V	X
256K	V	V	V	V	V	V	X	X
512K	V	V	V	V	V	X	X	X
IM	V	V	V	V	X	X	X	X
2M	V	V	V	X	X	X	X	X
4M	V	V	X	X	X	X	X	X

V =Valid
X = Don't Care

Cache Initialization

The secondary cache supported by the SiS85C401 does NOT provide the validation flag (bit) for the data lines. All the cache data are assumed valid once the cache is enabled. So the whole cache must be filled by valid data before the cache enable bit is turned on. The cache initialization can be done via sequential reads to a block of on-board DRAM which is equal to or larger than the cache in size.

DRAM Controller

Because the 80486 already has an 8K bytes internal cache, the-performance contribution of a secondary cache in the 80486 systems is not as significant as that in the 80386 systems. Many 80486 systems may therefore be built without the secondary cache. The performance of the DRAM access becomes important in these systems. The SiS85C401 povides a high performance DRAM controller for the 80486 system.

Burst Read for Cache Line Fill

Both the 80486 internal cache and the secondary cache provided by the SiS85C401 have a 16-byte line size. When the read miss happens in both caches memories, the SiS85C401 offers a DRAM burst of 4 doubleword-reads to fill the cache lines in the 80486 and the secondary cache.

Bank (Double-word) Interleave

The 80486 burst read is so fast that wait states are needed for DRAM accesses even in page hit burst cycles. Because Ihe burst cycles are sequential – in even-odd-even-odd sequence, the word interleave scheme is adaptive to hide pre-charge overhead in the burst read cycles. When even bank (doubleword) is accessed, the odd bank does the pre-charge, and vice versa. The commonly used "page interleave" scheme does not take the advantage of the sequential burst because all of the four reads will access the same bank.

The SiS85C401 knows if the DRAM interleave is applicable to current DRAM size configu˙ ration or not. So the DRAM interleave enable bit in configuration regisler 61 can be always set to ON. DRAM interleave will not be tumed on if the size setting is not interleave applicable.

DRAM Speed Options

The SiS85C401 provides 5 read and 2 write speed options in the configuration register. A table of page hit cycle time of all the possible speed configurations is listed as follows:

	Interleave Read	Non-interleave Read	Write
Supper Fast	3 -1-1-1	3-2-2-2	2
Fastest	4 -1-1-1	4-2-2-2	2
Faster	5-2-2-2	5-3-3-3	2/3
Slower	6-2-2-2	6-4-4-4	3/4
Slowest	7-3-3-3	7-5-5-5	4

Note: The unit of the above table is in T cycles.

There will be plenty of timing margin if the user adopt Super Fast for 16/20MHz 80486, Fastest for 25MHz, Faster for 33MHz, Slower for 40MHZ, and Slowest for 50MHz, even when 100ns DRAMs are used.

DRAM Access Timing

	Fastest	Faster	Slower	Slowest	Slow-CPU	
Trcd	2T	2T	3T	3T	1 T	RAS-to-CAS delay
Tcas	1T	2T	2T	3T	1T	Read CAS pulse width
Trp	3T	3T	4T	5T	2T	RAS precharge
Tcp	1 T	1 T	2T	2T	1 T	CAS precharge

DRAM Size Configuration

The SiS85C401 supports 32 different DRAM configurations in 4 banks. Besides the traditional 256K/IM/4M xN DRAMs, the new 512K xN and future 2M xN DRAMs are also supported. The doubleword interleave scheme is applicable when bank 0/1 and bank 2/3 are implemented with same DRAM types, respectively.

Transparent Refresh

In the original PC/AT design, the CPU is held off (i.e. can not do anything) during the DRAM refresh cycles. It happens once per 16us and takes at least 0.Sus each time.

Recently the speed of DRAM is becoming faster so the time needed per refresh cycle is getting shorter. The refresh cycle time for the 100ns DRAM is 200ns minimum, for example. In a system with cache, most of the CPU accesses are referred to the cache so that the DRAM usage (percent of time the DRAM is accessed by the CPU) is significantly reduced.

In the SiS85C401, the main memory refresh is independent to the AT-bus refresh so the cycle time is shorter (need not follow the standard AT-bus timing). When the main memory is refreshed, the CPU is NOT held off so it may execute the program stored in the cache at the same tirne. If the CPU accesses the main memory while it is being refreshed, this access will be pending (i.e. the CPU must wait) until the refresh is finished.

'Ihe following table lists the refresh-related RAS timings of the on-board DRAM:

	Fastest	Faster	Slower	Slowest	Slow-CPU
RAS pre-charge	3T	3T	4T	5T	2T
RA.Ci ctive	3T	4T	5T	6T	3T

On the other hand, the AT bus refresh cycles are issued by the SiS85C401 once per 16us when there is no access from the (CPU, the DMA controller, or the bus master on the AT bus. The 80486 CPU will not feel the existing of the AT bus refresh unless it issues an AT cycle coincidentaly. The SiS85C401 arbitrates among the CPU AT cycle, DMA/master request, and bus refresh so that they can be executed one after another when more than one of them intend to use the AT bus at the same time.

The SiS85C401 has a slow refresh feature to cut the refresh frequency down to 1/4. It should be selected only when the system is equipped with slow-refresh DRAM.

The refresh scheme of local DRAM is the CAS-before-RAS refresh. The CASs go active at least one- T before RASs in local refresh. To reduce the power noise caused by refresh, the RASs of odd banks go active one T aher that of even banks. It is called "staggered refresh".

Shadow RAM

Memory space OAOOOO-OFFFFFh is reserved for the video RAM, 1/0 and system BIOS ROM. Access to this area should not be conducted to the main memory in standard PC/AT. Since the speed of the DRAM is significantly faster than that of the ROM, if contents of the BIOS ROM are copied to the unused DRAM (OAOOOO- OFFFFFh), the DRAM can work as fast BIOS ROM and raise the overall system performance. This is called the "Shadow RAM".

The SiS85C401 provides shadow to OCOOOO-OEFFFFh in 32KB granularity and shadow to OFOOOO-OFFFFFh. Because many 1/0 related codes cannot be executed too fast, the cacheability of each shadow block is also programmable.

256KB Relocation

The SiS85C401 provides the 256KB DRAM relocation from OAOOOO-OBFFFFh and ODOOOOOEFFFFh to the top of configurated DRAM size.

This function works for the DRAM sizes of IMB, 2MB, 4MB, 6MB and 8MB when the shadowing of segments D and E is disabled.

ROM Support

The SiS85C401 provides a chip select signal for the system BIOS ROM. The memory space assigned to the ROM is the highest 64/128KB of the real (IMB) and the protected (4GB) address modes of the 80486.

The system BIOS ROM can be shadowed by the DRAM to improve performance. When the shadow RAM is turned on, the access to system BIOS with address below lOOOOOh will be channeled to the DRAM.

Fast A20GATE And CPU Reset

In the original PC/AT design, the A20GATE and CPU Reset (RC) are controlled by the 8042 keyboard controller to switch the 80286 CPU between the real and protected address modes. The operation of 8042 is quite slow so if the address mode switching happens frequently, the program execution speed will be affected.

The SiS85C401 provides a 8042 emulation to generate the A20GATE and CPU reset in hardware ,This feature is software transparent.

Local Bus Support

The SiS85C401 uses LBD# and LRDYI# pins to support local bus devices suchas Weitek 4167. The interface protocol is very straightforward.

When a local bus device decodes the bus definition/address from 486 CPU and finds this is its cycle at the start of a CPU bus cycle, it should assert LBD# to inform the SiS85C401 this is a local bus device cycle. The SiS85C401 will not send ATCYC# to the SiS85C402 but will wait for LRDYI# to terminate current cycle. When the local bus device want to finish its bus cycle, it should send a LRDYI# pulse to the SiS85C401. The SiS85C401 will synchronize LRDYI# with CPUCLK then send a RDY# to CPU. The local bus device should monitor the RDY# to know when the bus cycle is exactly finished.

When there are more than one local bus devices, their LBD# and LRDYI# signals should be ANDed together then sent to the SiS85C401.

T he SiS85C40 1 samples the LBD# input at the end of T2 when DRAM speed is set to FASTEST or FASTER, and at the end of T3 when DRAM speed is SLOWER or SLOWEST. LBD# should be asserted before the sampling point and kept active till RDY# is asserted.

Turbo Switch

The 80486 can run over 10 times faster than the original PC/AT. But some old applications may get into trouble if the system speed is too fast. The SiS85C401 offer a de-turbo function that can be controlled through a hardware switch or software

programming. When the deturbo function is turned on, the SiS85C401 disables both the 80486 internal and secondary caches, which decreases the system speed to approximately 1/4 of that of the normal speed.

Configuration Registers

There are eight configuration registers inside the SiS85C401. An indexing scheme is used to access all the registers. Port 22h is the index register and port 23h is the data register. T he conhguration registers are accessed by hrst writing the index to port 22h and immediately followed by a read or a write to port 23h. The index is reset aher data access. Every data access to port 23h must be preceded by an index write to port 22h, even if the same register is being accessed. All the reserved bits should be set to zero for future compatibility purpose. The contents of the registers are listed as follows.

SiS85C401 **Conflguration Registers**

Reglster 60 (index 60) Defaull = 00

bit 7,6 DRAM Speed
00: Slowest (50MHz)
01: Slower (40MHz)
10: Faster (33MHz)
11: Fastest (25MHz)

Bit 7 also defines the first cache read cycle time of a burst: 0/1: 3T/2T

bit 5 DRAMWrite CAS PulseWidth
0:2T (~40.50)
1: 1T (33,25,20)

bit 4 -0 DRAM Size Configuration

	Bank-0	Bank-1	Bank-2	Bank-3	Total Main Memory
00000	1 M				1 MB
·00001	1 M	1 M			2MB
00010	1M	1M	2M		4MB
00011	1 M	1 M	4M		6MB
00100	1M	1M	2M	4M	8MB
·00101	1M	1M	4M	4M	10MB
00110	1M	1M	16M		18MB
00111	2M				2MB
0100	2NI	2M			4MB
01001	2M	4M			6MB
01010	2M	2M	4M		8MB
·01011	2M	2M	4M	4M	12MB
01100	2M	16M			18MB
01101	2M	2M	16M		20MB
01110	2M	2M	4M	16M	24MB
·01111	2M	2M	1 6M	1 6M	36MB
10000	4M				4MB
·10001	4M	4M			8MB
10010	4M	4M	4M		12MB
·10011	4M	4M	4M	4M	16MB
10100	4M	16M			20MB
10101	4M	4M	16M		24MB
10110	4M	16M	16M		36MB
·10111	4M	4M	16M	16M	40MB
11000	8M				8MB
·11001	8M	8M			16MB
11010	8M	8M	8M		24MB
·11011	8M	8M	8M	8M	32MB
11100	1 6M				1 6MB
·11101	16M	16M			32MB
11110	16M	16M	16M		48MB
·11111	16M	16M	16M	16M	64MB

Note:
1 MB= 256K x 36bits
2MB= 512K x 36bits
4MB= 1 M x 36bits
8MB= 2M x 36bits
1 6MB= 4M x 36bits

· DRAM InterleaveApplicable

Reglster 61 (index 61) Default = 00

bit 7 Cache Enable
0: Disable
1: Enable

bit 6 Wrlte Back Enable
0: Disable (Write Through)
1: Enable (Write Back)

bit 5,4 Cache Size
00: 32KB
0 1: 64KB
10: 1 28KB
11: 256KB and above

bit 3 Cache Interleave Enable
0: Disable
1: Enable

bit 2 DRAM Interleave Enable (for 2/4 banks only)
0: Disable
1: Enable
bit 1 Reserved
bit 0 Reserved

Register 62 (index 62) Default = 00

bit 7 Shadow RAM Read Enable
0: Disable
1: Enable
bit 6 Shadow RAMWrite Protection Enable
0: Disable
1: Enable
bit 5 E8000h-EFFFFh Shadow RAM Enable
bit 4 E0000h-E7FFFh Shadow RAM Enable
bit 3 D8000h-DFFFFh Shadow RAM Enable
bit 2 D0000h-D7FFFh Shadow RAM Enable
bit 1 C8000h-CFFFFh Shadow RAM Enable
bit 0 C0000h-C7FFFh Shadow RAM Enable

Reglster 63 (index 63) Defaulat = 00

bit 7 System BIOS ROM Size
0: 64K
1: 128K

bit 6 F0000h-FFFFFh Shadow RAM Cacheable

bit 5 E8000h-EFFFFh Shadow RAM Cacheable

bit 4 E0000h-E7FFFh Shadow RAM Cacheable

bit 3 D8000h-DFFFFh Shadow RAM Cacheable

bit 2 D0000h-D7FFFhShadow RAM Cacheable

bit 1 C8000h-CFFFFh Shadow RAM Cacheable

bit 0 C0000h-C7FFFh Shadow RAMCacheable

Register 64 (index 64) Default=00

bit 7 Allocation of Non-Cacheable Area#1
0. Local DRAM
1 AT Bus, local DRAM is disabled

bit 6 4 Size of Non-Cacheable Area #1 (within 16 MB)
000: 0KB disabled)
001: 64KE
010: 1 28KB
011: 256KB
100: 51 2KB
101: 1 MB
110: 2MB
111:4MB

bit 3 Allocation of Non-CacheableArea#2
0: Local DRAM
1: AT Bus, local DRAM is disabled

bit 2-0 Size of Non-Cacheable Area #2 (within 64 MB)
000: OKB (disabled)
001: 64KB
010: 1 28KB
011 . 256KB
100 512KB
101: 1MB
11 0. 2MB
111 4MB

Register 65 (index 65) Default = 00

bit 7-0 A23-Al 6 of Non-Cacheable Area #1 (within 16 **MB)**

Register 66 (index 66) Default=00

bit 7-0 A23-A16 of Non-Cacheable Area #2 (within 64 **MB)**

Reglster 67 (index 67) Default=00

bit 7, 6 A25 and A24 of Non-Cacheable Area #2

bit 5 GATE A20 Emulation Enable
0: Disable
1: Enable
bit 4 Fast Reset Emulation Enable
0: Disable
1: Enabl

bit 3 Fast Reset Latency Control
0: 2us
1: 6us

bit 2 Slow Refresh Enabled (1:4)
0: Normal Refresh
1: Slow Refresh

bit 1 De-Turbo ON/OFF
0: Turbo
1: De-Turbo

bit 0 TurboSwitch Enable
0: Always Turbo, ignores the status of Turbo switch
1: Turbo Switch enable

Register 68 (index 68) Default = 00

bit 7 Super Fast DRAM Access Enable
0: Disable 1: Enable
This function is valid only when
a. DRAM speed is set onto FASTEST and
b. 2nd cache is disabled.

bit 6 Slow CPU (below 25MHz) Enable
0: Disable 1: Enable
This function is valid only when
DRAM speed is set onto FASTEST
This bit optimizes DRAM timing for <25MHz system.
Trcd 2T –> 1T (RAS-to-CAS delay)
Trp 3T –> 2T (RAS precharge time)

bit 5,4 Proprietary Chip Select (pin 149)
00: Port E8 - EFh
01 : Port C8 - CFh
10 : Port 28 - 2Fh
11: Turbo Indicator

blt 3,2,1,0 reservd and should be written with zero.