Little Board™/486*i*

Technical Manual

P/N: 5000941

Revision: E

Ampro Computers, Incorporated
4757 Hellyer Avenue ■ San Jose, CA 95138
Tel (408) 360-0200 ■ FAX (408) 360-0220
WEBSITE: www.ampro.com

WARNING

The Female PC/104 Bus Headers supplied on this Third Generation Little Board CPU are not compatible with backplanes and cable adapters intended for use with First and Second Generation Little Boards. Damage to the Little Board will occur if used with these components. Use only Bus Expansion components intended for use with Third Generation products.

NOTICE

DISCLAIMER

Ampro Computers, Incorporated makes no representations or warranties with respect to the contents of this manual or of the associated Ampro products, and specifically disclaims any implied warranties of merchantability or fitness for any particular purpose. Ampro shall under no circumstances be liable for incidental or consequential damages or related expenses resulting from the use of this product, even if it has been notified of the possibility of such damages. Ampro reserves the right to revise this publication from time to time without obligation to notify any person of such revisions. If errors are found, please contact Ampro at the address listed on the title page of this document.

TRADEMARKS

The Ampro logo is a registered trademark, and Ampro, Little Board, StackPlane, MiniBackplane, MiniModule, and CoreModule are trademarks of Ampro Computers, Inc. All other marks are the property of their respective companies.

TECHNICAL SUPPORT

Technical support is available from 8:00 AM to 5:00 PM, Pacific time.

- **Technical support telephone number: 800 966-5200. (Please have the product you wish to discuss at hand when you call.)**
- **E-mail address: techsupport@ampro.com**

Revision History

Revision	Reason for Change	Date
A	Production Release	10/95
B	Update	12/95
C	Update	2/96
D	Update Fig. 1-1	4/96
E/A	Update	6/96
B	Jumper Update and CPU	8/97
C	66/100/133 MHZ Versions	11/97
D	EPROM S0 Jumpers	6/99
E	Errata Update	8/00

PREFACE

This manual is for integrators and programmers of systems based on the Ampro Little Board™/486*i* single board system. It contains information about hardware specifications, jumpering and installation, details about system setup, and how to configure peripheral drivers.

There are three chapters and an Appendix, organized as follows:

- **Chapter 1**—Introduction. General information pertaining to the Little Board/486*i*, its features, and specifications.
- **Chapter 2**—Hardware Configuration. A description of how to configure and connect the Little Board/486*i* for use with a variety of onboard and external devices. Included are tables listing the pinouts of each of the board's connectors, details about jumper options, installation and mounting instructions, and descriptions and specifications regarding peripheral interfaces provided on the board.
- **Chapter 3**—Software Configuration. An overview of the system features, configuration options, SETUP guidelines, utilities, and peripheral drivers that are available under DOS, Windows, and other operating systems.
- **Appendix A**—Cable diagrams for flat panel displays that are supported in the board's ROM BIOS.

TABLE OF CONTENTS

CHAPTER 1—INTRODUCTION

CHAPTER 2—HARDWARE CONFIGURATION

CHAPTER 3—SOFTWARE CONFIGURATION

APPENDIX A—FLAT PANEL CABLES

FIGURES

TABLES

CHAPTER 1

INTRODUCTION

1.1 GENERAL DESCRIPTION

The Little Board/486*i* is an exceptionally high integration, high performance 486DX-based PC/AT compatible system in the footprint of a 5 1/4 inch disk drive. This rugged and high quality single-board system contains all the component subsystems of a PC/AT motherboard plus the equivalent of six PC/AT expansion boards.

Key functions included on the Little Board/486*i* are CPU, RAM, embedded-PC BIOS, keyboard and speaker interfaces, four buffered serial ports, a multimode IEEE-1284-compliant parallel port, floppy and local-bus IDE drive controllers, a flat panel/CRT display interface, a SCSI-II controller, and an Ethernet LAN interface. In addition, the Little Board/486*i* includes a comprehensive set of system extensions and enhancements that are specifically designed for embedded systems. Furthermore, it is designed to meet the size, power consumption, temperature range, quality, and reliability demands of embedded applications.

Among the many embedded-PC enhancements that ensure fail-safe embedded system operation are a watchdog timer, a powerfail NMI generator, and an onboard bootable "solid state disk" (SSD) capability. System operation requires a single +5 Volt power source and offers "green PC" power-saving modes under support of advanced power management (APM) BIOS functions.

1.2 FEATURES

CPU/Motherboard

The Little Board/486*i* has a fully PC-compatible motherboard architecture. Versions with CPUs running 66 Mhz, 100 Mhz, and 133 Mhz are available. The 486 CPU has an 16K byte on-chip cache memory which can be configured as ‘Write-Back’ or ‘Write-Through’.

The board uses standard 72-pin Single In-line Memory Module (SIMM™) memory modules, and supports memory from 4M bytes to 64M bytes.

It has a full complement of standard PC/AT architectural features, including DMA channels, interrupt controllers, real-time clock, and timer counters.

Enhanced Embedded-PC BIOS

One of the most valuable features of the Little Board/486*i* is its enhanced embedded-PC BIOS, which includes an extensive set of functions that meet the unique requirements of embedded system applications. These enhancements include:

- Solid State Disk (SSD) support (see below)
- SCSI services—full SCSI BIOS services are integrated with hard disk support
- Watchdog timer—monitors boot process; provides function call for applications
- Fast boot operation—normal or accelerated POST
- Fail-safe boot support—intelligently retries boot devices until successful
- Battery-free boot support—saves system SETUP information in non-volatile EEPROM
- Serial console option—lets you use a serial device as console

- Serial loader option—supports loading boot code from an external serial source
- EEPROM access function—512 bits of EEPROM storage available to user; useful for serialization, copy protection, security, etc.
- OEM customization hooks—can execute custom code prior to system boot via ROM extensions; allows sophisticated system customization without BIOS modification

Modular PC/104 Expansion Bus

The Little Board/486*i* provides a PC/104-compatible expansion bus for additional system functions. This bus offers compact, self-stacking, modular expandability. The growing list of PC/104 modules available from Ampro and hundreds of other PC/104 vendors includes such functions as communications interfaces, video framegrabbers, field bus interfaces, digital signal processors (DSPs), data acquisition and control functions, and many specialized interfaces and controllers. In addition, custom application-specific logic boards can also be stacked directly on top of the Little Board/486*i* using its PC/104 expansion bus interface as a rugged and reliable interconnect. The PC/104 bus is an embedded system version of the signal set provided on a desktop PC's ISA bus.

Byte-Wide Sockets and Solid State Disk (SSD)

An important feature of the Little Board/486*i* is its pair of byte-wide memory sockets, in which you can install a bootable "solid state disk" (SSD). The SSD substitutes EPROMs, Flash EPROMs, or battery-backed SRAMs for conventional rotating-media drives. Using Ampro's SSD Support Software, any DOS-based application, including the operating system, utilities, drivers, and application programs, can easily be run from SSD without modification. SSD operation is also supported by a growing number of real-time operating systems.

Two 32-pin byte-wide sockets are configurable for nearly every available 28-pin and 32-pin byte-wide memory device. The sockets support all varieties of devices, CMOS SRAM, SRAM non-volatile modules, EPROM, Flash EPROM, from 32K bytes to 1M byte and larger.

Serial Ports

The board provides four PC-compatible RS232C serial ports, implemented using 16C550-type UARTs. These UARTs are equipped with 16-byte FIFO buffers to improve throughput.

Parallel port

A new enhanced bi-directional parallel port interface conforms to the IEEE-1284 standard. It provides new features attractive to embedded system designers, including an internal FIFO buffer and DMA transfer capability.

Fast IDE Interface

An onboard fast IDE provides high speed hard disk access. The interface supports up to two hard disk drives.

SCSI-II Interface

An onboard SCSI-II controller is implemented using the Adaptec AIC 6360 SCSI-II controller. A high speed controller clock improves the performance over earlier Ampro models. The board's SCSI-BIOS is included as a part of the Ampro enhanced ROM-BIOS. The SCSI-II interface is compatible with current SCSI-II standards. It is also ASPI-compatible.

Local-Bus Flat Panel/CRT Display Controller

A powerful and flexible local bus video display controller interfaces with both flat panels and CRTs, and offers full software compatibility with five popular video standards, VESA (Super-VGA), VGA, EGA,

CGA, and MDA. Resolutions up to 1280 x 1024 pixels and up to 16 million colors are supported (refer to Tables 1–2 through 1–7 for video specifications). The display controller features:

- **High-speed Local Bus Architecture.** The video controller provides an optimized 32-bit path between the CPU and video memory.
- **Graphical User Interface (GUI) Accelerator.** Can dramatically boost the performance of Windows® and many other graphics-intensive applications.
- **Color Flat Panel Support.** Up to 16 M colors can be displayed on color TFT LCD flat panels and up to 226,981 colors on color STN LCD panels.
- **Color Simulation/Reduction.** Color is automatically converted to gray-scale on monochrome LCD panels, using a 61-level Frame Rate Modulation (FRM) technique and dithering.
- **Automatic Power Controls.** The video controller provides the signals to safely control the power and data signals to a flat panel. Advanced power management features are implemented in the power control logic.
- **PC Video Support.** The video controller allows up to 18 bits of external RGB video data to be input and merged with the internal VGA data stream. The controller supports two forms of video windowing, color key input and X-Y window keying.
- **Standard Panel Support in the ROM BIOS.** The ROM BIOS supports a number of standard flat panel displays, selectable from SETUP.

Ethernet LAN Interface

The Ethernet LAN interface uses Carrier Sense, Multiple Access/Collision Detect (CSMA/CD) for node access and operates at a 10 Mbits/second data rate. The Ethernet interface contains the logic necessary to send and receive data packets and to control the CSMA/CD network access technology, and meets the IEEE 802.3 (ANSI 8802-3) Ethernet standard. The interface supports the Ethernet twisted-pair standard (10BaseT) and the AUI interface (Adapter Unit Interface), allowing for maximum versatility in connecting to different types of LAN media.

Ethernet is preferred in many applications because of its high data rate and broad level of compatibility. Ampro supplies the Little Board/486*i* with drivers and utilities to ensure compatibility with a wide range of popular operating systems and network operating systems. The Ethernet interface is based on the SMC9000-series single-chip Ethernet controller. DOS software drivers for ODI, NDIS, packet, and TCP/IP are supplied with the Little Board/486*i* Development Kit. OS support includes QNX, UNIX, OS2, Windows®95, Windows NT™, and Windows/DOS.

The Ethernet interface provides boot PROM capability. When implemented, the embedded system boots directly from the network, eliminating the need for a local floppy, hard drive, or SSD.

1.2.1 Enhanced Reliability

Reliability is especially important in embedded computer systems. Ampro, specializing in embedded system computers and peripherals, knows that embedded systems must be able to run reliably in rugged, hostile, and mission-critical environments without operator intervention. Over the years, Ampro has evolved system designs and a comprehensive testing program to ensure a reliable and stable system in harsh and demanding applications.

ISO 9001 Manufacturing. Ampro is a certified ISO 9001 vendor.

EMC testing. Knowing that many embedded systems must qualify under regulatory compliance testing, Ampro designs boards with careful attention to EMI issues. Boards are tested in standard enclosures to ensure that they can pass C E mark testing.

Wide-range temperature testing. Ampro engineering qualifies its designs by extensive thermal and voltage margin testing.

3.3V CPU for greater high temperature tolerance. The board uses the latest low-voltage CPU technology to extend its temperature range and reduce cooling requirements.

Holes for tie-wraps for socketed components. Provision is made to tie down socketed components and other attachments so that they are able to withstand high-vibration environments.

Shrouded latching headers for cables. Onboard shrouded headers make assembly easier and less error-prone. Clips hold cables firmly to enhance reliability in high-vibration environments.

1.3 Little Board/486*i* SPECIFICATIONS

The following section provides technical specifications for the Little Board/486*i*.

1.3.1 CPU/Motherboard

- CPU: 3.3 V 80846 100 Mhz, 66 Mhz, or 133 Mhz. (133 Mhz may be jumpered for 100 Mhz.)
- System RAM:
  - Sockets for one or two 72-pin SIMMs
  - Supports up to 64M bytes total RAM
- Shadow RAM support provides fast system and video BIOS execution
- 15 interrupt channels (8237-equivalent)
- 7 DMA channels (8259-equivalent)
- 3 programmable counter/timers (8253-equivalent)
- Standard PC/AT keyboard port
- Standard PC speaker port with .1 watt output drive
- Battery-backed real-time clock and CMOS RAM:
  - Up to 10 year battery life
  - Supports battery-free operation
- Award ROM BIOS with Ampro extensions

1.3.2 Embedded-PC System Enhancements

- Two 32-pin byte-wide memory sockets:
  - Usable with 32K to 1M byte EPROMs, 32K to 512K byte Flash EPROMs, 32K to 512K byte SRAMs, or 32K to 512K byte NOVRAMs (Non-volatile RAMs)
  - Onboard battery converts SRAM in one socket (S0) to NOVRAM

- Onboard programming of 5 V and 12 V Flash EPROMs
- Onboard +12 Volt power supply for Flash EPROM programming
- Configurable as 64K or 128K byte window, addressed in the range of D0000h to EFFFFh
- Supports PCMCIA memory card connection via Ampro Memory Card Adapter
- Supported by Ampro SSD Support Software and many third-party operating systems

- 2K-bit configuration EEPROM:
  - Stores system SETUP parameters
  - Supports battery-free boot capability
  - 512 bits available for OEM use
- Watchdog Timer
  - Utilizes the onboard real-time clock alarm function
  - Timeout triggers hardware reset
- Powerfail NMI triggers when +5 Volt power drops below +4.7 Volts.

1.3.3 Onboard Peripherals

This section describes standard peripherals found on every Little Board/486*i*.

- Four buffered serial ports with full handshaking
  - Implemented with 16550-equivalent controllers with built-in 16-byte FIFO buffers
  - Onboard generation of ±9 Volts for RS232C signal levels
  - Each channel supports either RS232C (direct connection) or RS485 (via Ampro RS485 Adapter)
  - Logged as COM1, COM2, COM3, and COM4 by DOS
- Multimode Parallel Port
  - Superset of standard LPT printer port
  - Bidirectional data lines
  - IEEE-1284 (EPP/ECP) compliant
  - Standard hardware supports all four IEEE-1284 protocol modes
  - Internal 16-byte FIFO buffer
  - Can use DMA for data transfers
- Floppy Disk Controller
  - Supports one or two drives
  - Reliable digital phase-locked loop circuit
  - BIOS supports all standard PC/AT formats: 360K, 1.2M, 720K, 1.44M
- Fast IDE Disk Controller
  - A high-speed implementation of a standard IDE hard disk controller
  - Supports up to two hard disk drives.

- SCSI-II Interface
  - ANSI X3.131-compliant
  - Uses the Adaptec AIC 6360 controller
  - Synchronous or asynchronous data transfer
  - Supports SCSI-II data transfers (10MB/sec)
  - Onboard active terminators for low current drain
  - Built-in SCSI-BIOS in Ampro enhanced ROM-BIOS
  - Compatible with standard SCSI driver products that are ASPI compatible
- Flat Panel/CRT Video Controller
  - Supports CRT, LCD, and EL displays
  - Uses the C&T 65545 High Performance Flat Panel/CRT VGA Controller
  - Onboard display RAM 512K bytes standard, 1M byte special order
  - Modes, resolutions, and memory requirements: See Table 1-2.
  - Supports interlaced or non-interlaced displays in up to 1280 x 1024 resolution modes
  - Supports 24-bit True Color
  - GUI accelerator for enhanced performance
  - Video BIOS supports VESA super VGA modes. See Table 1-2.
  - Software programmable flat panel interface. Signal timing contained in an onboard Flash EPROM device for easy customization
  - Optional LCD Bias Supply. Circuit board plugs on to connector on the Little Board/486i
    - Supplies 15 V < Vee < 30 V DC, positive or negative polarity, at 30 mA (max)
    - Voltage level (LCD contrast control) adjustable with an onboard or external potentiometer
    - Sequences LCD power supplies to protect display
    - Implements advanced power management functions
- Ethernet LAN Interface
  - Complies with IEEE 802.3 (ANSI 8802-3)
  - Controller: SMC9000-series
  - Topology: Ethernet bus, using CSMA/CD
  - Media interface options:
    - 10BaseT (twisted pair), via an onboard RJ45 connector
    - AUI, via an onboard header connector, DB15F (transition cable available from Ampro)
    - 10Base2 (thin coax), via external MAU
  - Data rate: 10M bits per second
  - Data buffer: 4608 byte RAM, accessed via I/O ports

- I/O base address options: 300h, 320h, 360h, or 380h
- Interrupt options: IRQ3, IRQ9 (default), IRQ10, IRQ11
- DMA: not used
- Boot ROM image can be installed in system using a Flash programming utility (provided)

1.3.4 Support Software

- Enhanced Embedded-PC BIOS Features:
  - Solid State Disk (SSD) support
  - SCSI services
  - Watchdog timer (WDT) support
  - Fast boot options
  - Fail-safe boot logic
  - Battery-free boot
  - Serial console option
  - Serial loader option
  - EEPROM access function
  - Advanced Power Management (APM) support
  - OEM customization hooks

  See the Ampro Embedded-PC BIOS data sheet for additional details about these features.
- Software Utilities Included
  - Watchdog timer support
  - Power management support
  - Serial access and development support
  - SCSI support, including ASPI manager
  - Display controller support
  - Ethernet controller support

1.3.5 Mechanical and Environmental Specifications

- 8.0 x 5.75 x 1.2 inches (146 x 203 x 30 mm). Refer to Figure 1–1 for mounting dimensions.
- Provision for system expansion with one or more Ampro MiniModule products or other PC/104 expansion modules.
- Power requirements (typical, with 8M byte DRAM):
  - 66 MHz 80486DX2 CPU version: 2.0 Amps at +5V ±5%
  - 100 MHz 80486DX4 CPU version: 2.3 Amps at +5V ±5%
  - 133 Mhz 80486DX5 CPU version: 2.4 Amps at +5V ±5% (2.3 amps when jumpered for 100 Mhz)

- Operating environment:
  - Standard: 0° to 70° C (with adequate airflow); Extended temperature range can be tested by special order
  - 5 to 95% relative humidity (non-condensing)
- Storage temperature: -55° to +85° C
- Weight: 10.1 oz. (290 gm) with 4 M byte DRAM installed
- PC/104 expansion bus
  - Female (non-stackthrough) 16-bit bus connectors, for expansion via PC/104 Version 2 "double-stackthrough" (DST) modules
  - Four mounting holes
- 8-layer PCB using latest surface mount technology

Note

Contact Ampro regarding custom configurations and special order options.

Video Standard	Maximum Resolution	Maximum Colors Displayed	Video RAM Requirement* (Bytes)
CGA Graphics	320 x 200 640 x 200	4 2	512K 512K
CGA Text	640 x 200	16	512K
MDA	720 x 350	Mono	512K
EGA	640 x 350	16	512K
VGA	320 x 200 640 x 480	256 16	512K 512K
VESA (Standard SuperVGA)	640 x 480 800 x 600 1024 x 768 640 x 480 640 x 480 640 x 480 1024 x 768 1280 x 1084	256 256 16 32K 64K 16 M 256 16	512K 512K 512K 1M 1M 1M 1M 1M
* NOTE: All video RAM is factory-installed; 512K is standard, 1M is available by special order			

Table 1-1 Summary of Video Modes and DRAM Requirements

Flat Panel Displays

The Little Board/486*i* display controller supports all flat panel display technologies including plasma, electroluminescent (EL), and LCD. LCD panel types include single panel-single drive (SS), and dual panel-dual drive (DD) configurations. The following table lists the flat panel displays supported by the Little Board/486*i* ROM BIOS. You can also install a custom video BIOS in the board's Flash EPROM to support a panel not on this list.

Model	Type	Resolution	Size (Diagonal)
Sharp LM64P839	Passive Monochrome	640 x 480	9.4 in.
Sharp LJ64ZU51	Gray Scale EL	640 x 480	9.4 in.
Sharp LM64C35P	STN Color	640 x 480	10.4 in.
Sharp LQ10D131	TFT Color	640 x 480	10.4 in.
Sharp LQ64D142	TFT Color	640 x 480	6 in.
Flat Panel Display Co. LDH102T	TFT Color	640 x 480	10.4 in.
Flat panel technology changes rapidly. Contact Ampro Technical Support for the list of currently supported panels. Ampro provides a Flat Panel BIOS Customization Kit that allows OEMs to configure a video BIOS for panels not currently supported. Contact your Ampro sales representative for details.			

Table 1-2 Flat Panel Support

Note

Panel technology is changing rapidly. Flat panel support in the Little Board/486i ROM BIOS will change from time to time to maintain compatibility with current panel technology. Contact Ampro Technical Support for a list of currently supported panels.

Resolution	CRT Colors	Mono LCD Gray Scales	DD STN LCD Colors	9-bit TFT LCD Color	Video Memory	Simul-taneous Display?
320 x 200	256/256K	61/61	256/226,981	256/185,193	512K	Yes
640 x 480	16/256K	16/61	16/226,981	16/185,193	512K	Yes
640 x 480	256/256K	61/61	256/226,981	256/185,193	512K	Yes
800 x 600	16/256K	16/61	16/226,981	16/185,193	512K	Requires 1M
800 x 600	256/256K	61/61	256/226,981	256/185,193	512K	Requires 1M
1024 x 768	16/256K	16/61	16/226,981	16/185,193	512K	Requires 1M
1024 x 768	256/256K	61/61	256/226,981	256/185,193	1M	Yes
NOTE: Availability of colors and palette capacity depends on internal settings controlled by the video BIOS. A customized version of the BIOS is required for some displays.						

Table 1-3 Flat Panel Controller Display Capabilities

Mode	Display Mode	Colors	Text	Font	Pixels	Clock (MHz)	Horiz (KHz)	Vert (Hz)
0+, 1+	Text	16	40x25 40x25 40x25	9x16 8x14 8x8	360x400 320x350 320x200	28.322 25.175 25.175	31.5	70
2+, 3+	Text	16	80x25 80x25 80x25	9x16 8x14 8x8	720x400 640x350 640x200	28.322 25.175 25.175	31.5	70
4	Graphics	4	40x25	8x8	320x200	25.175	31.5	70
5	Graphics	4	40x25	8x8	320x200	25.175	31.5	70
6	Graphics	2	80x25	8x8	640x200	25.175	31.5	70
7+	Text	Mono	80x25 80x25 80x25	9x16 9x14 9x8	720x400 720x350 720x350	28.322	31.5	70
D	Planar	16	40x25	8x8	320x200	25.175	31.5	70
E	Planar	16	80x25	8x8	640x200	25.175	31.5	70
F	Planar	Mono	80x25	8x14	640x350	25.175	31.5	70
10	Planar	16	80x25	8x14	640x350	25.175	31.5	70
11	Planar	2	80x30	8x16	640x480	25.175	31.5	60
12	Planar	16	80x30	8x16	640x480	25.175	31.5	60
13	Packed Pixel	256	40x25	8x8	320x200	25.175	31.5	70

Table 1-4 Supported CRT Video Modes—Standard VGA

CRT Support for Standard Video Modes:

- PS/2 fixed frequency analog CRT monitor or equivalent. 31.5/35.5 KHz horizontal frequency specification.
- Multi-frequency CRT monitor. 37.5 KHz minimum horizontal frequency specification (NEC MultiSync 3D or equivalent).
- Multi-frequency High-Performance CRT monitor. 48.5 KHz minimum horizontal frequency specification (Nanao Flexscan 9070s, MultiSync 5D, or equivalent).

Mode	Display Mode	Colors	Text	Font	Pixels	Clock (MHz)	Horiz (KHz)	Vert (Hz)	Memory	CRT*
20	4-bit Linear	16	80x30	8x16	640x480	25.175	31.5	60	512K	a, b, c
22	4-bit Linear	16	100x37	8x16	800x600	40.000	37.5	60	512K	b,c
24	4-bit Linear	16	128x48	8x16	1024x768	65.000	48.5	60	512K	c
24I						44.900	35.5	43	512K	b,c
30	8-bit Linear	256	80x30	8x16	640x480	25.175	31.5	60	512K	a,b,c
32	8-bit Linear	256	100x37	8x16	800x600	40.000	37.5	60	512K	b,c
34	8-bit Linear	256	128x48	8x16	1024x768	65.000	48.5	60	1M	c
34I						44.900	35.5	43	1M	b,c
40	15-bit Linear	32K	80x30	8x16	640x480	50.350	31.5	60	1M	a,b,c
41	16-bit Linear	64K	80x30	8x16	640x480	50.350	31.5	60	1M	a,b,c
50	24-bit Linear	16M	80x30	8x16	640x480	65.000	27.1	51.6	1M	b,c
60	Text	16	132x25	8x16	1056x400	40.000	30.5	68	256K	a,b,c
61	Text	16	132x50	8x16	1056x400	40.000	30.5	68	256K	a,b,c
6A,70	Planar	16	100x37	8x16	800x600	40.000	38.0	60	256K	b,c
72,75	Planar	16	128x48	8x16	1024x768	65.000	48.5	60	512K	c
72I,75I						44.900	35.5	43	512K	b,c
78	Packed Pixel	16	80x25	8x16	640x400	25.175	31.5	70	256K	a,b,c
79	Packed Pixel	256	80x30	8x16	640x480	25.175	31.5	60	512K	a,b,c
7C	Packed Pixel	256	100x37	8x16	800x600	40.000	37.5	60	512K	b,c
7E	Packed Pixel	256	128x48	8x16	1024x768	65.000	48.5	60	1M	c
7EI						44.900	35.5	43	1M	b,c

Table 1-5 Supported CRT Video Modes—Extended Resolution

Mode	Display Mode	Colors	Text	Font	Pixels	Clock (MHz)	Horiz (KHz)	Vert (Hz)	Memory	CRT*
12**	Planar	16	80x30	8x16	640x480	31.500	37.5	75	256K	b, c
30	8-bit Linear	256	80x30	8x16	640x480	31.500	37.5	75	256K	c
79	Packed Pixel	256	80x30	8x16	640x480	31.500	37.5	75	512K	c
6A,70	Planar	16	100x37	8x16	800x600	49.500	46.9	75	512K	c
32	8-bit Linear	256	100x37	8x16	800x600	49.500	46.9	75	1M	c
7C	Packed Pixel	256	100x37	8x16	800x600	49.500	46.9	75	1M	c

Table 1-6 Supported CRT Video Modes—High Refresh

*** CRT Support for Extended Resolution Modes:**

a PS/2 fixed frequency analog CRT monitor or equivalent (31.5/35.5 KHz horizontal frequency specification).

b Multi-frequency CRT monitor. 37.5 KHz minimum horizontal frequency specification (NEC MultiSync 3D or equivalent).

c Multi-frequency High-Performance CRT monitor. 48.5 KHz minimum horizontal frequency specification (Nanao Flexscan 9070s, MultiSync 5D, or equivalent).

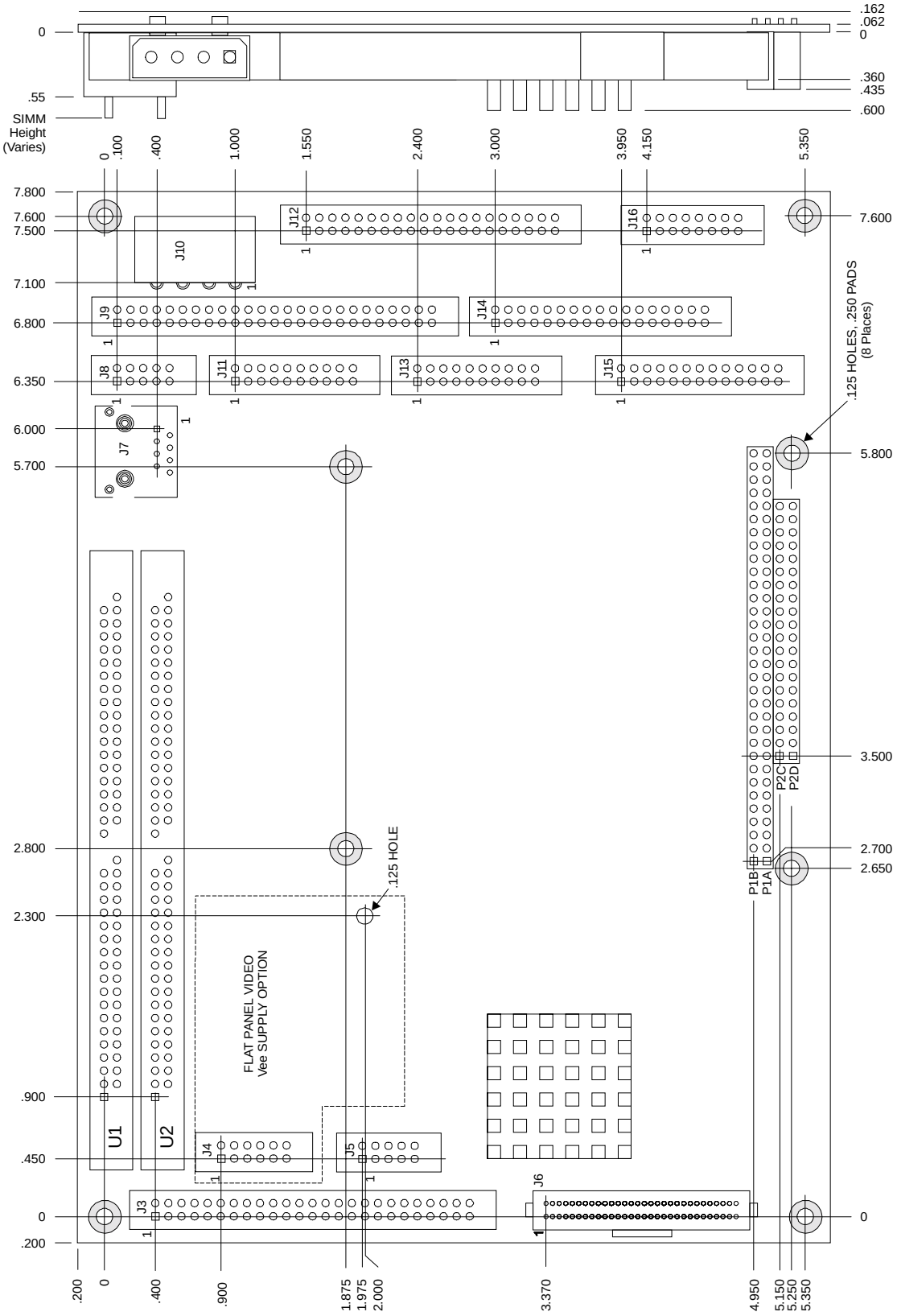


Figure 1-1 Mechanical Dimensions

CHAPTER 2

HARDWARE CONFIGURATION

2.1 INTRODUCTION

This chapter covers configuring the Little Board/486*i* and using on-board and peripheral devices. The topics covered in this chapter are:

- Power and the power fail monitor
- DRAM memory
- Four RS232C serial ports
- Enhanced parallel port
- Floppy disk interface
- IDE hard disk interface
- Two 32-pin byte-wide sockets
- SCSI-II hard disk interface
- Flat-panel/CRT video interface
- Ethernet local area network interface
- Utility connector (Keyboard, PC speaker, reset button, external battery)
- Watchdog timer
- Battery-backed clock
- PC/104-compatible expansion bus

This chapter includes data on the board's connector signals and pinouts, external device requirements, interconnection cable wiring, and board configuration.

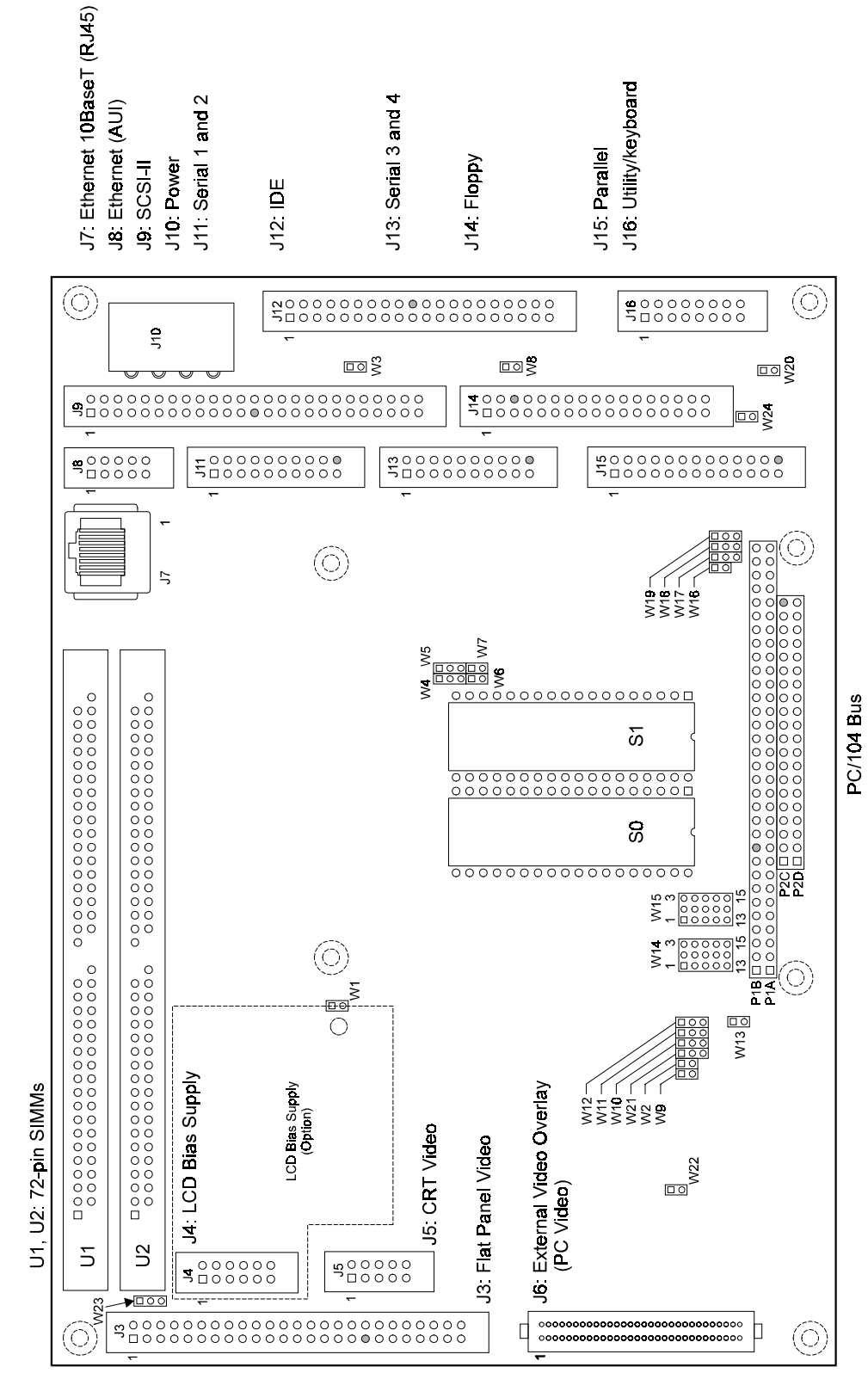
2.1.1 Interface Connector Summary

Refer to Figure 2-1 for the locations of the connectors (J1-J16) and configuration jumpers (W1–W24). Table 2-1 summarizes the use of the I/O connectors and Table 2-2 summarizes use of the configuration jumpers. Each interface is described in its own section, showing connector pinouts, signal definitions, required mating connectors, and configuration jumper options.

Many of the connectors have a key pin removed. This allows you to block the corresponding cable connector socket to help prevent improper assembly. Table 2-1 indicates which pins are key pins, and Figure 2-1 shows their locations.

Connector	Function	Size	Key Pin
P1A/B	PC/104 Expansion Bus	64-Pin	B10
P2C/D	PC/104 Expansion Bus	40-pin	C19
J1-J2	Designations not used	N/A	N/A
J3	Flat Panel Video	50-pin	35
J4	LCD Bias Supply Connector	12-pin	None
J5	CRT Video	10-pin	None
J6	Video External Overlay	60-pin .050 in.	None
J7	Ethernet Twisted Pair	RJ45	None
J8	Ethernet AUI	10-pin	None
J9	SCSI Interface	50-pin	25
J10	Power, +5V and +12V	4-pin Molex	None
J11	Serial 1 and Serial 2	20-pin	20
J12	IDE Hard Disk	40-pin	20
J13	Serial 3 and Serial 4	20-pin	20
J14	Floppy Interface	34-pin	6
J15	Parallel Port	26-pin	26
J16	Utility/Keyboard	16-pin	None

Table 2-1 Connector Usage Summary



(Shaded connector pins indicate key pins.)

Figure 2-1 Connector and Jumper Locations

Connectors

The I/O connectors are shrouded dual-row headers for use with flat ribbon (IDC) connectors and ribbon cable. Ampro recommends that you use "center-bump polarized" connectors to prevent accidentally installing cables backwards. Use non-strain-relief connectors to stay within the vertical height envelope shown in Figure 1–1.

Many of the connectors have "key pins". Install a blocking key in the corresponding connector socket on the mating ribbon cable to prevent misalignment.

You can install a retaining clip to secure the cable to its connector. This is especially useful in high-vibration environments. You can also design a PC board assembly, made with female connectors in the same relative positions as the Little Board's connectors, to eliminate cables, meet packaging requirements, add EMI filtering, or customize your installation in other ways.

The PC/104-compatible expansion bus appears on two connectors (P1 and P2). You can expand the system with on-board MiniModule™ products or other PC/104-compliant expansion modules. These modules stack directly on the connectors, or use conventional or custom expansion hardware, including solutions available from Ampro.

If you plan to use the on-board video controller with a flat-panel LCD screen, you can install Ampro's optional LCD Bias Supply board on connector J4, as shown in Figure 2-1. This board can be jumpered to supply positive or negative Vee from ±15V to ±35V (adjustable).

2.1.2 Jumper Configuration Options

Ampro installs option jumpers in default positions so that in most cases the Little Board/486*i* requires no special jumpering for standard AT operation. You can connect the power and peripherals and operate it immediately. The only jumpers of concern are those that configure the byte-wide sockets for the devices you install.

Jumper-pin arrays are designated W1, W2, and so forth. Jumper pins are spaced 2 mm apart. A square solder pad identifies pin 1 of each jumper array. Table 2-2 is a summary of jumper use. In the Default column, two numbers separated by a slash (for example, 1/2) means that the pins are shorted with a 2 mm jumper block.

Jumper Group	Function	Default
W1	Video Controller Enable	ON
W2	Byte-wide S0 Battery Back-up Power	OFF
W3	SCSI Termination Power	OFF
W4	Serial 3 IRQ Select (IRQ4, IRQ12)	2/3 (IRQ12)
W5	Serial 4 IRQ Select (IRQ3, IRQ10)	2/3 (IRQ10)
W6	Serial 1 IRQ4 Sharing Pull-down	ON
W7	Serial 2 IRQ3 Sharing Pull-down	ON
W8	+5V Supply for External RS-485 Interface (Serial 4)	OFF
W9	BIOS Programming Disable	ON
W10	Write-back Cache Enable	1/2 (enabled)
W11	Watchdog Timer Output Select (IOCHCK, Reset)	OFF
W12	SCSI IRQ11 Select	2/3
W13	BIOS Flash EPROM Programming Power (+12V)	OFF
W14	Byte-wide S0 Configuration (default is 128K SRAM)	7/10, 8/9, 11,12, 14/15
W15	Byte-wide S1 Configuration (default is 29C512 FLASH device)	4/5, 7/8, 10/11, 13/14, 9/12
W16	Floppy Controller DRQ2 Enable	ON
W17	Parallel Port IRQ Selection (IRQ5, IRQ7)	1/2 (IRQ7)
W18	-DACK for ECP (Parallel Port)	OFF
W19	DRQ for ECP (Parallel Port)	OFF
W20	Power Fail Monitor NMI Enable	OFF
W21	Byte-wide Backup Battery	2/3
W22	CPU Clock Speed (133MHz version only)	ON (133MHz)
W23		1/2
W24	SCSI Hardware I/O Address Select	OFF
W25	SCSI Enable/Disable	ON

Table 2-2 Configuration Jumper Summary

2.2 DC POWER

The pinout of the power connector J10 is identical with the power connectors on 5-1/4 inch floppy disk drives. Refer to Table 2-3 for power connections, Table 2-4 for mating connector information, and Figure 2-2 for typical connector wiring.

Caution

Be sure the power plug is wired correctly before applying power to the board! See Figure 2-2.

Pin	Signal Name	Function
1	+12VDC	+12VDC ±5% input
2, 3	Ground	Ground return
4	+5VDC	+5VDC ±5% input

Table 2-3 Power Connector (J10)

Connector Type	Mating Connector
DISCRETE WIRE	AMP HOUSING 1-480424-0 AMP PIN 60619-1

Table 2-4 J10 Mating Connector

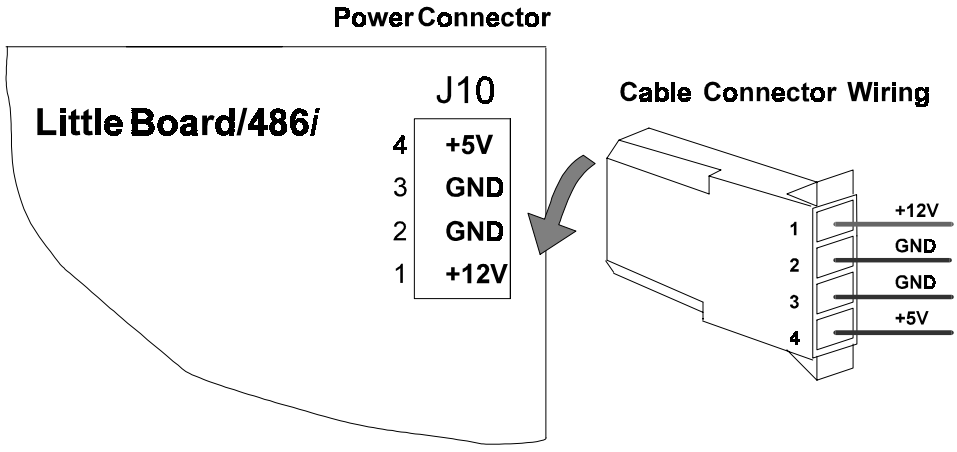


Figure 2-2 Power Connector Wiring

2.2.1 Power Requirements

The Little Board/486*i* requires only +5VDC (±5%) for operation. The ±9 volts for the RS232 ports is generated on-board from the +5VDC supply. An onboard +5V to +12V converter supplies power for

programming Flash EPROMs. (There may be a requirement for an external +12 volt supply, depending on what peripherals you connect to the Little Board system. For instance, +12V is required for most flat panel backlight power supplies and for an external Ethernet LAN MAU device connected to the Ethernet controller AUI interface.)

The exact power requirement of the Little Board/486*i* system depends on several factors, including the quantity of DRAM, installed byte-wide memory devices, SCSI bus termination, CPU speed, the peripheral connections, and which, if any, MiniModule products or other expansion boards are attached to the PC/104 bus. For example, AT keyboards draw their power from the board, and there can be some loading from the serial and parallel ports. Consult the specifications in Chapter 1 for the basic power requirements of your model.

If you use a switching power supply, be sure it regulates properly with the load your system draws. Some switching power supplies do not regulate properly unless they are loaded to some minimum value. If this is the case with your supply, consult the manufacturer about additional loading, or use another supply or another type of power source (such as a linear supply, batteries, etc.). The minimum power for the Little Board/486*i* appears in the power specifications in Chapter 1.

2.2.2 Powerfail Options

The Little Board/486*i* includes a circuit that can sense a power failure. If the +5V power supply falls below 4.7 V, the powerfail logic produces a non-maskable interrupt (NMI). If it falls below 4.5V, it generates a hard reset.

To enable the powerfail circuitry, short W20 with a jumper.

Non-maskable interrupt (NMI): When the supply voltage falls below (approximately) 4.7 volts, the powerfail logic sends an NMI to the CPU. When the BIOS detects the NMI, it displays the message "Power Fail NMI" on the screen. You have two options at this point (made by keyboard selections). One is to mask the NMI and continue. The other is to reboot the system. This, of course, requires operator intervention. If you want an automatic response to the NMI, you can provide an NMI handler in your application, and patch the NMI interrupt vector address to point to your routine. See Chapter 3 for additional information about writing an NMI handler for the powerfail interrupt.

If you have configured the byte-wide socket S0 for battery backup, it will be write protected while power is below 4.7 volts. (Its chip select is held to a logic 1.) This is to prevent writing bad data to an SRAM in S0 when the voltage is low.

Hardware reset: If the supply voltage falls below (approximately) 4.5V, the powerfail logic initiates a hardware reset (like pressing the RESET button). A "clean" reset during a low voltage period prevents erratic operation or crashes. Reset is asserted for the duration of the low-voltage period plus 100 mS after the voltage returns to above 4.5V.

2.2.3 Backup Battery

With only the real-time clock drawing current, the backup battery on the Little Board/486*i* should last 10 years. If it supplies only the clock, replace the battery every 10 years as a routine maintenance procedure.

If the battery is also used to back up an SRAM in byte-wide socket S0, calculate the battery life using the formula below. To calculate battery life, add the SRAM current and the clock current (1 uA) and divide 165 milliamp-hours by the sum. Then, multiply that result by the duty cycle of the battery. That is, estimate the percentage of time the battery supplies power (while the system is off).

(To connect the on-board battery to byte-wide socket S0 to back up an SRAM, install jumpers on W2 and W21-1/2. If you use another type of memory device in S0, you must remove W2 and install a jumper on W21-2/3.)

Here is the formula for calculating battery life (in hours):

Battery life = (165 milliamp-hours ÷ (1 uA + SRAM backup current)) × Duty Cycle

If the memory device you select draws too much current from the onboard battery, you can add an external 3.6 volt lithium battery to J16. Connect the positive terminal to J16-15 and the negative terminal to J16-16. (To conform to UL recommendations, internal and external batteries are connected by Schottky diodes using a circuit in which two blocking devices are in series with the batteries.)

2.2.4 Cooling Requirements

The 486 CPU, DRAM, video controller, and core logic chip draw most of the power and generate most of the heat. The board uses a 3.3 volt version of the 486 CPU chip to minimize power drain. In addition, a heat sink is provided for the CPU. However, you must provide additional air flow to keep the board's 486DX within its specified case temperature of 85°C when the ambient temperature is high.

2.3 CPU CLOCK AND CACHE CONFIGURATION

The LB/486i is factory configured to run at the maximum speed allowed by the CPU option. CPUs with internal clock rates of 66 MHz and 100 MHz can only be used at those speeds. The 133 MHz version can be jumpered to run at 100 MHz using W22. The slower clock rate can be used to reduce power requirements and improve thermal characteristics. The CPU manufacturer's datasheet gives a guideline of 7 mA / MHz for maximum current requirements. Table 2-5 indicates the function of W22 in setting the internal clock speed. The shaded field indicates factory default.

W22 ON	W22 OFF
133 MHz	100 MHz

Table 2-5 CPU Speed Settings (W22)

Another jumper, W10, is used to control the configuration of the CPU's internal Cache. This 16 Kbyte Cache is factory configured to 'Write-Back'. This setting can be changed to 'Write-Through' by moving the shunt on W10 to pin 2/3.

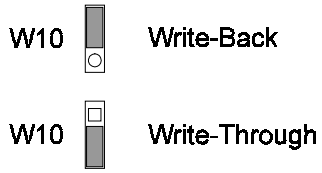


Figure 2-3 Write-Back Cache Configuration (W10)

2.4 DRAM

The board has positions for two 72-pin Single In-line Memory Modules (SIMMs), U1 and U2. 72-pin SIMMs are organized as a 32-bit data bus, so you can use either one or two modules, depending on your memory needs. 72-pin SIMMs come in 1M byte, 4M byte, 8M byte, 16M byte, and 32M byte versions. Any mix of SIMMs can be accommodated. The ROM BIOS automatically detects the memory modules that are installed and configures accordingly.

Specify page mode DRAMs with access times of 70 nS or less. 4M byte, 16M byte, and 32M byte versions have been tested and qualified by Ampro. 4M bytes is the minimum configuration. Since the quality of commercial DRAM modules can vary, test the Little Board/486*i* with the memory you select.

Note

Some memory modules are "taller" than others. The tall SIMMs will increase the thickness dimension of the Little Board/486*i* to 1.35 inches or more.

On-board memory is allocated as follows (standard for the PC architecture):

- The first 640K bytes of DRAM are assigned to the DOS region 00000h to 9FFFFh.
- DRAM in the top 384K bytes of the first 1M byte is not available for user programs. DRAM is mapped into the top 64K to shadow the ROM BIOS. DRAM can also be mapped into a portion of this region to *shadow* a video BIOS (a SETUP option). (Shadowing is described in the following section.)
- The remaining memory is mapped to extended memory starting at the 1M byte boundary.

A more detailed memory map is provided in Chapter 3.

When the system boots, the BIOS measures the amount of memory installed and configures the internal memory controller for that amount. (No jumpering or manual configuration is required.) The amount it measured can be displayed by running SETUP. Saving SETUP automatically stores this figure in the Configuration Memory.

Note

If you change the amount of memory installed, you must run SETUP again to save the new value in the Configuration Memory.

2.4.1 Shadowing

One way to improve system performance is to "shadow" the ROM BIOS and video BIOS. When the system operates directly from ROM code, it accesses an 8-bit memory device. When the ROM contents are shadowed, the contents are copied into system DRAM where they are accessed as 32-bit wide data. Shadowing a BIOS ROM substantially enhances system performance, especially when an application or operating system repeatedly accesses the ROM. ROM BIOS shadowing is built into the Ampro Extended BIOS. There is no user setting. Shadowing the video BIOS is a SETUP option. For information about how to set the video BIOS shadowing option, refer to the SETUP section in Chapter 3.

2.4.2 Expanded Memory and Extended Memory

Memory above the 1 megabyte boundary is called "extended" memory. It is a contiguous linear block of memory. Some programs require that memory be available as EMS memory. The EMS memory standard makes memory available as pages rather than as a contiguous block. The exact manner for accessing EMS memory is defined in the LIM 4.0 specification.

You can convert the board's extended memory into expanded memory using DOS EMS emulation utilities. Current versions of DOS provide EMS emulation utilities that conform to the LIM 4.0 specification. Refer to your DOS technical documentation for instructions for using their EMS emulation utility.

2.5 MATH COPROCESSOR

The 80486 CPU contains a built-in floating point math coprocessor. There are no configuration jumpers or options for the math coprocessor.

2.6 SERIAL PORTS (J11, J13)

The Little Board/486*i* provides four standard RS232C serial ports at J11 and J13. You can use the serial ports for printers, modems, terminals, remote hosts, or other RS232C serial devices. Many devices, such as printers and modems, require handshaking in one or both directions. Consult the documentation for the device(s) you use for information about handshaking and other interface considerations.

All ports support software selectable standard baud rates up to 115.2.2K bits/second, 5-8 data bits, and 1, 1.5, or 2 stop bits. Note that the IEEE RS232C specification limits the serial port to 19.2K bits/second on cables up to 50 feet in length.

2.6.1 I/O Addresses

The serial ports appear at the standard port addresses as shown in Table 2-6. These are fixed assignments and cannot be changed. Each serial port, however, can be independently disabled using the SETUP function, freeing its I/O addresses for use by other devices installed on the PC/104 expansion bus. For information about serial port configuration using SETUP, see Chapter 3.

Port	I/O Address	Interrupt
Serial 1	3F8h - 3FFh	4
Serial 2	2F8h - 2FFh	3
Serial 3	3E8h - 3EFh	4 or 12
Serial 4	2E8h - 2EFh	3 or 10

Table 2-6 Serial Port I/O Addresses and Interrupts

2.6.2 Interrupt Assignments

As shown in Table 2-6, interrupt 4 (IRQ4) is assigned to Serial 1 and Interrupt 3 (IRQ3) to Serial 2. These assignments can be disabled, but they cannot be changed. Serial 3 and Serial 4 can share these same interrupts, using a "wired-or" configuration, they can use independent IRQs, or they can be disabled and use no interrupt at all. Jumper options are provided to independently select the wired-or configuration or independent interrupts for Serial 3 and Serial 4.

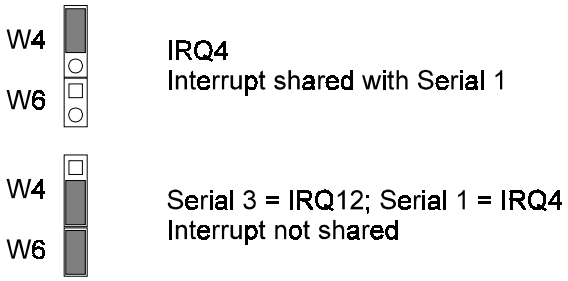


Figure 2-4 Serial 3 Interrupt Configuration (W4, W6)

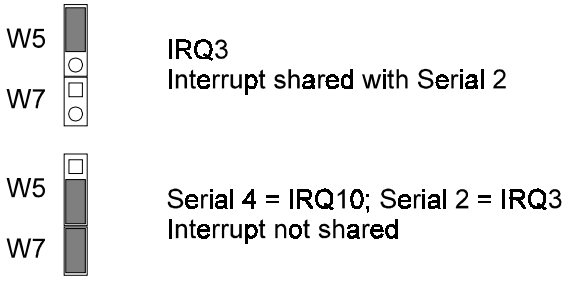


Figure 2-5 Serial 4 Interrupt Configuration (W5, W7)

When a serial port is disabled, leave its jumpers off to make its IRQ available to other peripherals installed on the PC/104 expansion bus. For information about disabling the serial ports using SETUP, see Chapter 3.

2.6.3 ROM-BIOS Installation of the Serial Ports

Normally, the ROM BIOS supports Serial 1 as the DOS COM1 device, Serial 2 as the DOS COM2 device, and so on. If you disable a serial port, and there is no substitute serial port in the system, then the ROM-BIOS assigns the COMn designations as it finds the serial ports, starting from the primary

serial port and searching to the last one, Serial 4. Thus, for example, if Serial 1 and Serial 3 are disabled, the ROM-BIOS assigns COM1 to Serial 2 and COM2 to Serial 4. .

2.6.4 Serial Port Connectors (J11, J13)

Serial 1 and Serial 2 appear on connector J11; Serial 3 and Serial 4 appear on connector J13. Table 2-7 gives the connector pinout and signal definitions for J11 and J13. Both connectors are wired the same, J11 for serial 1 and 2, and J13 for serial 3 and 4.

In addition, the table indicates the pins to which each signal must be wired for compatibility with DB25 and DB9 connectors. The serial port pinout is arranged so that you can use a flat ribbon cable between the header and a standard DB9 connector. Split a 20-wire ribbon cable into two 10-wire sections, each one going to a DB9 connector. Normally PC serial ports use male DB connectors. Table 2-8 shows the manufacturer's part number for mating connectors.

Ports	Pin	Signal Name	Function	In/Out	DB25 Pin	DB9 Pin
Serial 1 (J11) or Serial 3 (J13)	1	DCD	Data Carrier Detect	IN	8	1
	2	DSR	Data Set Ready	IN	6	6
	3	RXD	Receive Data	IN	3	2
	4	RTS	Request To Send	OUT	4	7
	5	TXD	Transmit Data	OUT	2	3
	6	CTS	Clear to Send	IN	5	8
	7	DTR	Data Terminal Ready	OUT	20	4
	8	RI	Ring Indicator	IN	22	9
	9	GND	Signal Ground	-	7	5
	10	N/A	No Connection	-	-	-
Serial 2 (J11) or Serial 4 (J13)	11	DCD*	Data Carrier Detect*	IN	8	1
	12	DSR	Data Set Ready	IN	6	6
	13	RXD	Receive Data	IN	3	2
	14	RTS	Request To Send	OUT	4	7
	15	TXD	Transmit Data	OUT	2	3
	16	CTS	Clear to Send	IN	5	8
	17	DTR	Data Terminal Ready	OUT	20	4
	18	RI	Ring Indicator	IN	22	9
	19	GND	Signal Ground	-	7	5
	20	N/A	Key Pin	-	-	-

* For Serial 4, W8 jumper OFF = DCD; W8 jumper ON = +5V for powering an Ampro RS485 Adapter board.

Table 2-7 Serial Port Connectors (J11, J13)

Connector Type	Mating Connector
RIBBON	3M 3421-7600
DISCRETE WIRE	MOLEX HOUSING 22-55-2202 PIN 16-02-0103

Table 2-8 J11 and J13 Mating Connector

2.6.5 Serial Console

Unique to Ampro is ROM BIOS support for using a serial console (keyboard and display) in place of the conventional video controller, monitor, and keyboard. See Chapter 3 for an explanation of the serial console option.

2.6.6 Serial Downloader

Also unique to Ampro is ROM BIOS support for downloading a program from a host computer via a serial port. The program is then run as if it had been loaded from disk. See Chapter 3 for an explanation of the serial download option.

2.7 MULTIMODE PARALLEL PORT (J15)

The Little Board/486*i* incorporates a multimode parallel port. This port supports four modes of operation:

- Standard PC/AT printer port (output only)
- PS/2-compatible bi-directional parallel port (SPP)
- Enhanced Parallel Port (EPP)
- Extended Capabilities Port (ECP)

See “Multimode Parallel Port” in Chapter 3 for a description of the parallel ports modes.

This section lists the pinout of the parallel port connector and describes how to configure it for its I/O port and interrupt assignments, and how to assign a DMA channel to the port when operating in ECP mode. Refer to Chapter 3 for programming information, including how to use the port for bi-directional I/O.

2.7.1 I/O Addresses

The parallel port functions are controlled by eight I/O ports and their associated register and control functionality. By selecting the base I/O address, you can configure the parallel port as the primary port (typically LPT1) or the secondary port (typically LPT2), or you may disable the port to free the hardware resources for other peripherals.

Table 2-9 lists the parallel port addresses you can select. Use the SETUP function described in Chapter 3 to select the parallel port I/O addresses.

Selection	I/O Address
Primary	378h - 37Fh
Secondary	278h - 27Fh
Disable	None

Table 2-9 Parallel Printer Port Address Configuration

For details about the parallel port I/O addresses and the data, status, control, EPP, and ECP port bit definitions, refer to the parallel port section in Chapter 3.

2.7.2 ROM-BIOS Installation of Parallel Ports

Normally, the BIOS assigns the name LPT1 to the primary parallel port, and LPT2 to the secondary parallel port (if present), and so on. However, the BIOS scans the standard addresses for parallel ports and if it only finds a secondary port, it assigns LPT1 to that one. Configure the parallel port for the primary assignment shown in Table 2-9, unless you have added another parallel port that occupies the primary parallel port's I/O addresses. In that case, make the Little Board/486*i*'s parallel port the secondary port.

2.7.3 Interrupts

The parallel port can be configured to generate an interrupt request upon a variety of conditions, depending on the mode the port is in. (These are described in Chapter 3.) In most applications, the interrupt is not used. The standard parallel port interrupts are:

- Primary port IRQ7
- Secondary port IRQ5

A jumper is used to select the parallel port interrupt. To select the interrupt, set jumper W17 as shown in the following figure:

Figure 2-6 Parallel Port IRQ Selection (W17)

2.7.4 DMA Channels

In ECP enhancement mode, the parallel port can send and receive data under control of an on-board DMA controller. DMA channels operate with a request/acknowledge hardware handshake protocol between an internal DMA controller and the parallel port logic. On the Little Board/486*i*, select the DMA request (DRQ) and DMA acknowledge (DACK) assignments using jumpers. You can configure the parallel port to use either DMA channel 1 or DMA channel 3. To select a DMA channel for the parallel port, set jumpers W18 and W19 as shown in the following figure:

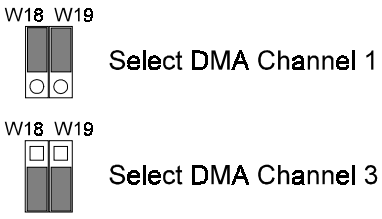


Figure 2-7 Parallel Port DMA Selection (W18, W19)

If you will not be using DMA with the parallel port, leave the jumpers off. This makes the DMA controls available to other peripherals installed on the expansion bus.

2.7.5 Parallel Port Connector (J15)

Connection to the parallel port is through connector J15. Table 2-10 gives this connector's pinout and signal definitions. You can use a flat ribbon cable between J15 and a female DB25 connector. The table also gives the connections from the header pins to the DB25 connector. Table 2-11 gives manufacturer's part numbers for mating connectors.

J15 Pin	Signal Name	Function	In/Out	DB25 Pin
1	-STROBE	Output data strobe	OUT	1
3	Data 0	LSB of printer data	I/O	2
5	Data 1		I/O	3
7	Data 2		I/O	4
9	Data 3		I/O	5
11	Data 4		I/O	6
13	Data 5		I/O	7
15	Data 6		I/O	8
17	Data 7	MSB of printer data	I/O	9
19	-ACK	Character accepted	IN	10
21	BUSY	Cannot receive data	IN	11
23	PAPER OUT	Out of paper	IN	12
25	SEL OUT	Printer selected	IN	13
2	-AUTOFD	Autofeed	OUT	14
4	ERROR	Printer error	IN	15
6	-INIT	Initialize printer	OUT	16
8	SEL IN	Selects printer	OUT	17
26	N/A	Key pin		
10,12, 14,16 18,20 22,24	GROUND	Signal ground	N/A	18-25
Data lines: 24 mA sink (.4 V max.), 12 mA source (2.4 V min.). Control lines: 24 mA sink (.4 V max.), open collector with 4.7K pull-ups.				

Table 2-10 Parallel Port Connector (J15)

Connector Type	Mating Connector
RIBBON	3M 3399-7600
DISCRETE WIRE	MOLEX HOUSING 22-55-2262 PIN 16-02-0103

Table 2-11 J15 Mating Connector

Note

For maximum reliability, keep the cable between the board and the device it drives to 10 feet or less in length.

The parallel port incorporates chip protection circuitry on some inputs, designed to minimize the possibility of CMOS "latch up" due to printer or other peripheral being powered up while the Little Board/486*i* is turned off.

2.8 FLOPPY DISK INTERFACE

The on-board floppy disk controller and ROM BIOS support one or two floppy disk drives in any of the standard DOS formats shown in Table 2-12.

Capacity	Drive Size	Tracks	Data Rate
360K	5-1/4 inch	40	250 KHz
1.2M	5-1/4 inch	80	500 KHz
720K	3-1/2 inch	80	250 KHz
1.44M	3-1/2 inch	80	500 KHz

Table 2-12 Supported Floppy Formats

2.8.1 Floppy Drive Considerations

Nearly any type of soft-sectored, single or double-sided, 40 or 80 track, 5-1/4 inch or 3-1/2 inch floppy disk drive is usable with this interface. Using higher quality drives improves system reliability. Here are some considerations about the selection, configuration, and connection of floppy drives to the Little Board/486*i*.

- **Drive Interface**—The drives must be compatible with the board's floppy disk connector signal interface, as described below. Ampro recommends any standard PC-or AT-compatible 5-1/4 inch or 3-1/2 inch floppy drive.
- **Drive Quality**—Use high quality, DC servo, direct drive motor floppy disk drives.
- **Drive Select Jumpering**—Both drives must be jumpered to the second drive select.
- **Floppy Cable**—For systems with two drives, use a floppy cable with conductors 10-16 twisted between the two drives. This is standard practice for PC-compatible systems. If you want to use a standard dual-drive cable with a combination floppy drive (with both 3.5 inch and 5.25 inch drives on the same connector), connect the drive to the non-twisted connector to configure the 3.5 inch drive to be A:.
- **Drive Termination**—Resistive terminations should be installed only on the drive connected to the last interface cable connector (farthest from the board). Near-end cable termination is provided on the Little Board/486*i*.
- **Head Load Jumpering**—When using drives with a Head Load option, jumper the drive for head load with motor on rather than head load with drive select. This is the default for PC-compatible drives.

- **Drive Mounting**—If you mount a floppy drive very close to the Little Board or another source of EMI, you may need to place a thin metal shield between the disk drive and the device to reduce the possibility of electromagnetic interference.

2.8.2 Floppy Interface Configuration

The floppy interface is configured using SETUP to set the number and type of floppy drives connected to the system. Refer to the SETUP section in Chapter 3 for details.

If you don't use the floppy interface, disable it in SETUP, and remove the jumper from W16. This frees DMA channel 2 for use by other peripherals installed on the PC/104 bus.

2.8.3 Floppy Interface Connector (J14)

Table 2-13 shows the pinout and signal definitions of the floppy disk interface connector, J14. The pinout of J14 meets the AT standard for floppy drive cables. Table 2-14 shows the manufacturer's part numbers for mating connectors.

Pin	Signal Name	Function	In/Out
2	RPM/-RWC	Speed/Precomp	OUT
4	N/A	(Not used)	N/A
6	N/A	Key pin	N/A
8	-IDX	Index Pulse	IN
10	-MO1	Motor On 1	OUT
12	-DS2	Drive Select 2	OUT
14	-DS1	Drive Select 1	OUT
16	-MO2	Motor On 2	OUT
18	-DIRC	Direction Select	OUT
20	-STEP	Step	OUT
22	-WD	Write Data	OUT
24	-WE	Write Enable	OUT
26	-TRKO	Track 0	IN
28	-WP	Write Protect	IN
30	-RDD	Read Data	IN
32	-HS	Head Select	OUT
34	-DCHG	Disk Change	IN
1-33	(all odd)	Signal grounds	N/A

Table 2-13 Floppy Disk Interface Connector (J14)

Connector Type	Mating Connector
RIBBON	3M 3414-7600
DISCRETE WIRE	MOLEX HOUSING 22-55-2342 PIN 16-02-0103

Table 2-14 J14 Mating Connector

2.9 IDE HARD DISK INTERFACE (J12)

The Little Board/486*i* provides an interface for one or two Integrated Device Electronics (IDE) hard disk drives. IDE drives, the most popular and cost-effective type of hard drive currently available, have a standard PC hard disk controller.

A standard IDE interface appears at connector J12, a 40-pin, dual-row connector. Table 2-15 shows the interface signals and pin outs for the IDE interface connector. Table 2-16 shows manufacturer's part numbers for mating connectors.

Note

For maximum reliability, keep IDE drive cables less than 18 inches long.

Pin	Signal Name	Function	In/Out
1	-HOST RESET	Reset signal from host	OUT
2	GND	Ground	OUT
3	HOST D7	Data bit 7	I/O
4	HOST D8	Data bit 8	I/O
5	HOST D6	Data bit 6	I/O
6	HOST D9	Data bit 9	I/O
7	HOST D5	Data bit 5	I/O
8	HOST D10	Data bit 10	I/O
9	HOST D4	Data bit 4	I/O
10	HOST D11	Data bit 11	I/O
11	HOST D3	Data bit 3	I/O
12	HOST D12	Data bit 12	I/O
13	HOST D2	Data bit 2	I/O
14	HOST D13	Data bit 13	I/O
15	HOST D1	Data bit 1	I/O
16	HOST D14	Data bit 14	I/O
17	HOST D0	Data bit 0	I/O
18	HOST D15	Data bit 15	I/O
19	GND	Ground	OUT
20	KEY	Keyed pin	N/C
21	RSVD	Reserved	N/C
22	GND	Ground	OUT
23	-HOST IOW	Write strobe	OUT
24	GND	Ground	OUT
25	-HOST IOR	Read strobe	OUT
26	GND	Ground	OUT
27	RSVD	Reserved	N/C
28	RSVD	Reserved	N/C
29	RSVD	Reserved	N/C
30	GND	Ground	OUT
31	HOST IRQ14	Drive interrupt request	IN

Table 2-15 IDE Drive Interface Connector (J12)

Pin	Signal Name	Function	In/Out
32	RSVD	Reserved	N/C
33	HOST A1	Drive address 1	OUT
34	RSVD	Reserved	N/C
35	HOST AD0	Drive address 0	OUT
36	HOST AD2	Drive address 2	OUT
37	-HOST CS0	Chip select	OUT
38	-HOST CS1	Chip select	OUT
39	-HOST SLV/ACT	Drive active/drive slave	10K Pull-up
40	GND	Ground	OUT

Table 2-15 IDE Drive Interface Connector (J12) (cont.)

Connector Type	Mating Connector
RIBBON	3M 3417-7600
DISCRETE WIRE	MOLEX HOUSING 22-55-2402 PIN 16-02-0103

Table 2-16 J12 Mating Connector

2.9.1 IDE Interface Configuration

Use SETUP to specify your IDE hard disk drive type. If you do not find a drive type whose displayed parameters match the drive you are using, use drive type 48 or 49. These two "pseudo-types" allow you to manually enter the drive's parameters. The drive manufacturer provides the drive parameters—check the drive's documentation for the proper values to enter. See the section on SETUP in Chapter 3 for additional information.

If you use an IDE drive in your system, you can still add SCSI drives or other SCSI peripherals. The Ampro ROM BIOS provides a means for allowing both IDE and SCSI drives on the same system. See the SETUP description in Chapter 3 for details.

2.10 SCSI INTERFACE

The Little Board/486*i* features a 16-bit Small Computer System Interface (SCSI) controller compatible with SCSI-II software and peripherals. The SCSI port uses a 50-pin male header connector (J9) to interface with peripherals. This connector provides an 8-bit path to the peripheral device, standard for most peripherals. The controller subsystem has a 16-bit path to the CPU. Table 2-17 shows the pinout and signal definitions of this interface. Refer to your SCSI device documentation, or the ANSI X3.131 SCSI specification for detailed information on the signal functions.

The recommended maximum SCSI bus cable length, from the board to the most distant SCSI peripheral, is 18 feet.

Table 2-18 shows manufacturer's part numbers for mating connectors.

Pin	Signal	Function
2	-DB0	Data Bit 0 (LSB
4	-DB1	Data Bit 1
6	-DB2	Data Bit 2
8	-DB3	Data Bit 3
10	-DB4	Data Bit 4
12	-DB5	Data Bit 5
14	-DB6	Data Bit 6
16	- DB7	Data Bit 7
18	-DBP	Data Parity
26	TERM PWR	Termination +5VDC
32	-ATN	Attention
34	GROUND	Signal Ground
36	-BSY	Busy
38	-ACK	Transfer Acknowledge
40	-RST	Reset
42	-MSG	Message
44	-SEL	Select
46	-C/D	Control/Data
48	-REQ	Transfer Request
50	-I/O	Data direction
25	N/A	Key pin
1-49(odd) 20,22,24 28,30	GROUND	Signal Grounds

Table 2-17 SCSI Interface Connector (J9)

Connector Type	Mating Connector
RIBBON	3M 3425-7600
DISCRETE WIRE	MOLEX HOUSING 22-55-2502 PIN 16-02-0103

Table 2-18 J9 Mating Connector

2.10.1 SCSI Interface Configuration

Configure the SCSI interface according to your system's needs. This is covered in the following paragraphs.

I/O Address Assignment

The base I/O address of the SCSI hardware is set to 340h at the factory. Addresses between 340h and 35Fh are used. If this address space is required for another purpose, the SCSI hardware I/O range can

be re-mapped to 140h-15Fh by installing a shunt on W24. The SCSI BIOS extensions of the ROM BIOS do not support the alternate I/O address range.

Interrupt Request Assignment

The SCSI interface, supported by the SCSI BIOS extensions of the ROM BIOS does not use an interrupt. However, some operating systems, such as OS/2 and Windows95, and Adaptec ASPI drivers require IRQ11. This is the default assignment, implemented on jumper W12. A shorting block installed on W12 connects the SCSI interface to IRQ11. If you use DOS and the internal SCSI support firmware, you can remove the jumper and use IRQ11 for another peripheral.

Active Terminators

The SCSI interface uses "active terminators" for the SCSI bus. Active terminators draw less current than 330/220 ohm terminators (the normal method of SCSI line termination), and are less susceptible to noise.

Only the SCSI devices on each end of the SCSI bus should be terminated. Enable or disable the SCSI terminators on the Little Board/486*i* using SETUP. Refer to the section describing SETUP in Chapter 3 for details.

External Termination Power Option

You can power external SCSI terminations from the Little Board/486*i*. A jumper option (W3), connects power (+5V) to the SCSI bus TERMPWR signal (J9, pin 26). The board includes a Schottky protection diode to prevent damage to the board by current flowing *from* the SCSI bus.

The default jumpering of W3 is open; that is, termination power is not normally supplied by the Little Board/486*i*.

SCSI ID

Every SCSI device must be configured for a specific SCSI bus ID, between 0 and 7. Normally, set the SCSI initiator ID to 7. Set disk drive and other SCSI target device IDs to 0 – 6. Set the SCSI initiator ID using SETUP. Details are provided in the SETUP section of Chapter 3.

Enabling or Disabling the SCSI Disk Interface

To enable the SCSI hardware, install W25. Removing W25 disables the SCSI sub-system. Using SETUP, disable or enable the SCSI BIOS disk drive services. Note that this SETUP option disables access to the SCSI BIOS disk drive services only. The SCSI hardware can still function normally and BIOS calls are still serviced. For instance, a CD ROM drive (with its driver) would still function normally. Disabling the SCSI BIOS might be desirable for several reasons:

- To speed system booting when you don't use SCSI. Otherwise, there is a delay while the system waits for a non-existent SCSI device to respond to initialization commands.
- To disable SCSI BIOS control of the SCSI hardware, when you have a non-standard use for the interface, implemented by a device driver.

Details about the SCSI interface, installing a SCSI hard disk, and using SETUP to configure the SCSI interface are provided in Chapter 3.

2.11 BYTE-WIDE SOCKETS

The Little Board/486*i* has two 32-pin on-board byte-wide memory sockets, designated S0 and S1. These sockets can accept a wide variety of EPROM, Flash EPROM, SRAM, and nonvolatile RAM

(NOVRAM) devices. Battery backup power can be connected to S0 using a jumper option to make an SRAM "non-volatile."

You can use devices installed in the byte-wide sockets for a variety of purposes:

- Simple program storage
- BIOS extensions
- Solid State Disk (SSD) drives

Table 2-19 shows some representative byte-wide memory devices that can be installed in the byte-wide sockets. The table gives examples of generic part numbers, the size of the device (K bytes), and the DIP package pin count. It also lists the SSD device type, used by the Ampro Solid State Disk (SSD) Support Software to identify memory devices.

SSD Device Type	Size	Package Pins	Generic Part Number
EPROMs			
EPROM32	32K byte	28	27C256
EPROM64	64K byte	28	27C512
EPROM128	128K byte	32	27C010
EPROM256	256K byte	32	27C020
EPROM512	512K byte	32	27C040
EPROM1024	1024K byte	32	27C080
Flash EPROMs			
EPROM128	128K bytes	32	28F010
EPROM256	256K bytes	32	28F020
EPROM512	512K bytes	32	29F040
SRAMs			
SRAM32	32K bytes	28	43256
SRAM128	128K bytes	32	62204
SRAM512	512K bytes	32	434000

Table 2-19 Typical Byte-wide Devices

The 32-pin socket is wired to accommodate a wide variety of byte-wide memory devices. The pinout of the 32-pin socket complies with the 28-pin and 32-pin JEDEC standards.

Install devices with pin 1 oriented to the appropriate shaded square, as indicated in Figure 2-7.

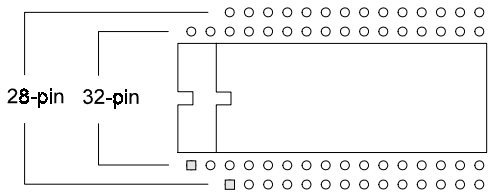


Figure 2-8 Using 28- and 32- pin Devices in 32-pin Sockets

2.11.1 Addressing the Byte-wide Sockets

Use the CPU SETUP program to specify the size and starting address of each socket, and which socket the BIOS enables upon system initialization. Table 2-20 lists the possible settings for sizes and address ranges of the byte-wide sockets.

Note

When a byte-wide socket is enabled, the memory address space it uses is unavailable for other devices, even if no memory device is installed in the socket. You must disable the byte-wide sockets in SETUP before you can use the memory space for other purposes.

Window	Address
DISABLE	N/A
64K	D0000-DFFFFh
64K	E0000-EFFFFh
128K	D0000-EFFFFh

Table 2-20 Window Size and Address Selection

The size of the device installed in a byte-wide socket is not limited to 128K bytes. Using a page addressing scheme, devices (or modules) up to 1M bytes can be used. Higher address lines (A16-A19) are synthesized and can be set by software. A description and examples of byte-wide page control are provided in Chapter 3.

2.11.2 Direct Program Access

Application software can access the memory devices in S0 and S1 if the program knows about them. To access a byte-wide socket, you must enable it. You must enable and disable the sockets in your application program to prevent a conflict. S0 and S1 can not be enabled at the same time.

If devices larger than 64K bytes are installed, you must select which page is visible in the address window assigned to the device. If the size is set to 64K bytes, a page is 64K bytes. If the size is set to 128K bytes, a page is 128K bytes. The Ampro Extended BIOS provides convenient software calls to manage enabling/disabling the sockets and selecting pages. Refer to Chapter 3 for details about the byte-wide extended ROM-BIOS calls.

If you install a device that is smaller than the selected window size, the contents of the device are duplicated in the byte-wide socket's memory space. For instance, the software will see two copies of a 32K device in a 64K window, and 4 copies in a 128K window.

ROM-BIOS Extensions

The system can run its entire application from memories in the byte-wide sockets, instead of loading it into DRAM from a disk drive. This technique, known as a ROM BIOS extension, directly executes the application at the end of the Power On Self Test (POST) instead of booting from floppy or hard disk. The ROM-BIOS extension concept, and its practical implementation, is discussed in Ampro Application Notes AAN-8702 and AAN-9003.

Performance Issues

Note that executing programs directly from the byte-wide sockets can adversely affect system performance. There are a number of factors that can contribute to the performance impact:

- Byte-wide devices are substantially slower than DRAM, as they are 8-bit devices instead of 32-bit.
- They are accessed from the PC expansion bus, which is much slower than the high-speed processor memory bus.
- Both sockets can share the same memory address space. If this is the case, you must enable the one you want to execute from and disable the other. (This is done with a BIOS call, described in Chapter 3.)

You can improve performance substantially by copying the contents of byte-wide devices into RAM and executing the RAM copy.

2.11.3 Solid State Disk (SSD) Drives

Using the Ampro Solid State Disk (SSD) Support Software, you can configure EPROM, Flash EPROM, or SRAM solid-state devices, installed in the byte-wide sockets, to act as one or more disk drives. No custom programming is required. Regular DOS-compliant programs, including standard DOS utilities, can be used without modification.

Ampro's SSD support software creates data image files, based on your application programs and operating system, which can be programmed into the devices you install in the byte-wide sockets. The Ampro ROM-BIOS treats these devices like one or more disk drives, loading the programs into DRAM for execution. The sockets can be combined to serve as a single drive, or each socket can be used as a separate drive. You can use SSD drives in addition to, or instead of, normal floppy and hard disk drives.

You can increase system SSD capacity by adding one or more of Ampro's SSD expansion modules.

2.11.4 Jumpering the Byte-Wide Sockets

You must jumper the byte-wide sockets for the devices you install in them. Jumper array W14 configures S0 for a particular device type. W15 configures S1. Figure 2-8 to Figure 2-10 show how

to install jumpers for supported memory devices. Table 3-12 describes the byte-wide socket signals that correspond to each jumper pin.

2.11.5 Using EPROMs

If you install an EPROM in socket S0, make sure the jumper on W2 is removed and the jumper on W21 is on 2/3 to prevent premature discharge of the on-board backup battery. Some EPROMs draw current through their chip select lines (or other pins) when powered down.

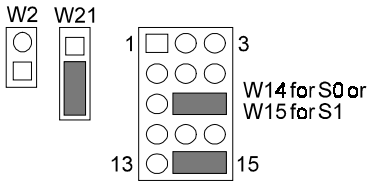
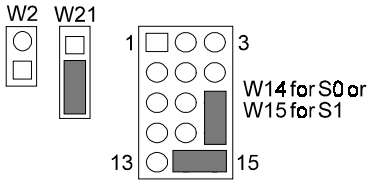
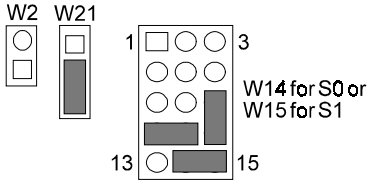
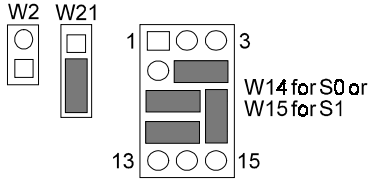
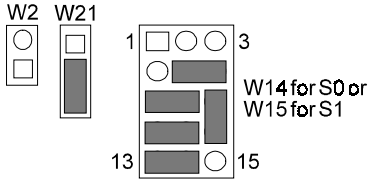
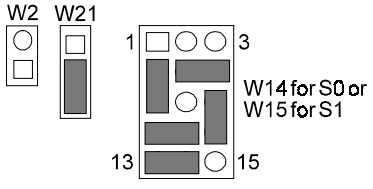
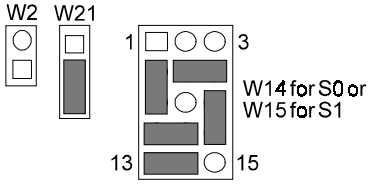
EPROM (Typical Devices)	Pins	Jumper Diagram
8K EPROM 27C64 16K EPROM 27C128 8K EEPROM 28C64	28	
32K EPROM 27C256	28	
64K EPROM 27C512	28	
128K EPROM 27C010	32	
256K EPROM 27C020	32	
512K EPROM 27C040	32	
1M EPROM 27C080	32	
NOTE: W2 and W21 configure S0 only.		

Figure 2-9 EPROM Jumpering for S0 and S1

2.11.6 Using Flash EPROMs

Flash programming power for +12V Flash devices is provided by an on-board power supply. You do not need to connect an external +12V power supply to program Flash devices. Programming power is switched under software control so that it is applied only during the actual programming process (to prevent accidental corruption of the data). A utility for programming supported Flash devices is included on the utility disk that is provided with the Little Board/486*i* Development Kit.

Some Flash EPROMs draw current through their chip select lines (or other pins) when powered down. If you install a Flash EPROM in socket S0, make sure the jumper on W2 is removed and the jumper on W21 is on 2/3 to prevent premature discharge of the on-board backup battery.

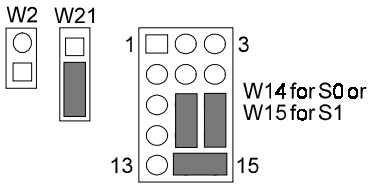
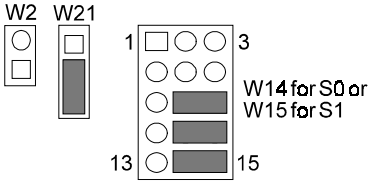
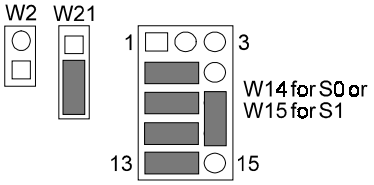
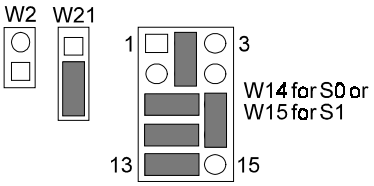
Flash EPROM Typical Devices	Pins	Jumper Diagram
32K 5V Flash EPROM 29C256	28	
32K 5V Flash EPROM 28C256	28	
64K 5V Flash EPROM 29F512 128K 5V Flash EPROM 29F010 256K 5V Flash EPROM 29F020 512K 5V Flash EPROM 29F040	32	
32K 12V Flash EPROM 28F256 64K 12V Flash EPROM 28F512 128K 12V Flash EPROM 28F010 256K 12V Flash EPROM 28F020	32	
NOTE: W2 and W21 configure S0 only.		

Figure 2-10 Flash EPROM Jumpering for S0 and S1

2.11.7 Using SRAMs

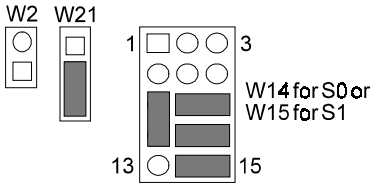
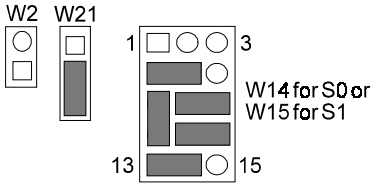
If you install an SRAM in socket S0, you can provide backup power from the battery when power is off by shorting W2 and W21-1/2.

Battery backup is provided for S0 only (not S1).

The external battery power is combined with the internal battery using low forward voltage drop Schottky diodes. The 165 milliamp-hour battery provides sufficient current for the onboard real-time clock for a 10 year life, but if you are going to battery-back-up a device in S0, Ampro recommends a larger battery, connected through the utility connector.

Note

Some byte-wide devices draw battery backup current through their chip select lines when power is off. When using memory devices that do not require battery backup power, remove the jumper on W2 and set W21 to 2/3. This prevents the backup battery from being drained prematurely.

SRAM Typical Devices			Pins	Jumper Diagram
32K SRAM	43256		28	
128K SRAM	628128		32	
32K NOVRAM	Dallas	DS1235Y		
	Benchmarq	BQ4013Y		
512K SRAM	628512		32	
512K NOVRAM	Dallas	DS1650Y		
	Benchmarq	BQ4015Y		

NOTE: W2 and W21 are show configured for NOVRAMs. To configure W2 and W21 for SRAM battery backup (on S0), install a jumper on W2 and move the jumper on W21 to 1/2. See text for details.

Figure 2-11 SRAM and NOVRAM Jumpering for S0 and S1

2.12 FLAT PANEL/CRT VIDEO CONTROLLER

The Little Board/486*i* provides an integrated high-performance super VGA video controller. The video controller supports both CRT and flat panel displays. It uses four connectors to interface with external devices. These connectors are summarized in the table below. Complete hardware details about each connector and the features they support are provided in sections that follow.

Name	Connector	Pins/Type	Description
Flat Panel	J3	50-pin Shrouded .100 Header	Provides connections for a broad array of standard flat panel displays. Intended for standard 50-wire ribbon cable.
LCD Bias Supply Option	J4	12-pin Shrouded .100 Header	Ampro provides a small add-on board that will supply the Vee voltage for most common LCD flat panel displays. It mounts to this connector. For details about the Vee Supply Option, refer to its section, below.
CRT	J5	10-pin Shrouded .100 Header	Provides connections for a CRT display. To connect to a standard CRT cable, use a short “transition cable” to a DB-15 connector.
External Video Overlay	J6	60-pin .050 Header	Not currently supported.

Table 2-21 Video Connector Summary

2.12.1 Connecting a CRT (J5)

Analog video signals from the video controller appear on a 10-pin dual-row header, J5. These signals are compatible with the standard video monitors commonly used with desktop PCs. Specifications for compatible monitors are provided in Chapter 1.

Normally, signals from J5 are connected to a standard DB-15 video connector by a “transition cable” made from a ribbon cable connector and a short length of 10-wire ribbon cable. A transition cable can connect the video signals to a bulkhead-mounted DB-15 or DB-9 connector, allowing any standard CRT to be easily connected using a standard monitor video cable. The following table gives the signal pinout of J5 and pin connections for a DB-15 connector. Pin connections for a DB-9 connector, used for some monitors, are also provided.

J5 Pin	Signal Name	DB-15	DB-9
1	Red	1	1
2	Ground	6	6
3	Green	2	2
4	Ground	7	7
5	Blue	3	3
6	Ground	8	8
7	Horizontal Sync.	13	4
8	Ground	10	9
9	Vertical Sync.	14	5
10	Ground	4, 5, 9, 11, 12, 15	-

Table 2-22 CRT Interface Connector (J5)

Connector Type	Mating Connector
RIBBON	3M 3473-7600
DISCRETE WIRE	MOLEX HOUSING 22-55-2102 PIN 16-02-0103

Table 2-23 J5 Mating Connectors

2.12.2 Connecting a Flat Panel (J3)

Signals for a wide range of flat display panels, both color and gray scale, appear on connector J3. Although flat panels of a similar type use similar sets of signals from the video controller, they do not share a standardized interface connector pin configuration. Note, also, that the names of panel control signals vary from manufacturer to manufacturer. Read the description of each signal carefully to determine how each signal is to be used for the display you choose. Refer to the panel manufacturer's technical literature to determine how to wire a cable for the panel you choose for your application.

Cable tables for the standard flat panels that are supported in the ROM BIOS are given in Appendix A.

The following table lists the signals available on connector J3.

J3 Pin	Signal Name	Description
2, 34, 37	+5V	+5 Volt supply from Little Board/486*i*
3	+12V	+12 Volt supply (from J10)
5	ShfClk	Shift Clock. Pixel clock for flat panel data. Sometimes called Video Clock. Jumper selectable polarity (W23).
7	M	M signal for panel AC drive control. Sometimes called ACDCLK or AC Drive. May also be configured to be -BLANK or as Display Enable (DE) for TFT panels.
9	LP	Latch Pulse. Sometimes called Load Clock, Line Load, or Input Data Latch. It's the flat panel equivalent of HSYNC. Active high.
10	FLM	First Line Marker. Also called Frame Sync or Scan Start-up. Flat panel equivalent to VSYNC. Active high.
12–31	VD0-VD19	Panel video data 0 through 19 (in order). For 8-, 9-, 12-, or 16-bit flat panels.
32	B1A18	Ampro reserved
36	ENABKL	Enable backlight. Power control for panel backlight. Active low, open collector.
38	ENAVEE	Enable Vee. Power sequencing control for panel bias voltage. Active high.
39	ENAVDD	Enable Vdd. Power sequencing control for panel driver electronics Vdd. Active high.
41	VD20	Video data 20
42	VD21	Video data 21
43	VD22	Video data 22
44	VDDSAFE	Switched +5V supply to panel
45	VD23	Video data 23
46	VEE	Switched Vee supply to panel (from LCD Bias Supply)
47	EXTCONT	External contrast adjustment (from LCD Bias Supply)
50	+12VSAFE	Switched +12V supply to panel
1, 4, 6, 8, 40, 48, 49	Ground	Ground
11, 33, 35	N/C	No connection

Table 2-24 Flat Panel Video Connector (J3)

Connector Type	Mating Connector
RIBBON	3M 4325-7600
DISCRETE WIRE	MOLEX HOUSING 22-55-2502 PIN 16-02-0103

Table 2-25 J3 Mating Connectors

Flat Panel Shift Clock Polarity

Some flat panels require an inverted shift clock. A jumper, W23 is provided for this purpose. Set the jumper block on W23 as shown in the following diagram.

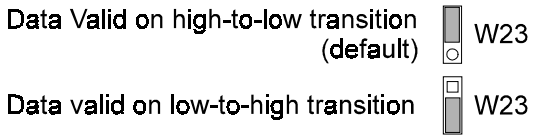


Figure 2-12 Flat Panel Shift Clock Polarity Jumper (W23)

Power Sequencing

LCD flat panel displays can be damaged when the Vee bias supply is applied to the LCD substrate without first enabling the control and data lines. This can result in damage to the panel or reduction of its operational life. The video controller provides signals for sequencing the power in the proper order to protect the panel from these effects. The Little Board/486*i* supports automatic sequencing of Vdd (+5V) and +12V (for an external backlight power inverter). The Ampro LCD Bias Supply board supports automatic power sequencing of Vee. If you use your own supply, you must enable the power using the special enable signals provided on connector J3, ENAVEE, ENAVDD, and ENABKL. The Ampro LCD Bias Supply board and circuits on the Little Board/486*i*, implement the power sequencing feature using these signals. For more information, see the section "The LCD Bias Supply Option."

Advanced Power Management

Note that the same signals that support power sequencing are also used to provide the power management feature. In "panel off mode" both the CRT and flat-panel interface are turned off, but the VGA subsystem (registers and display memory) remain powered. In "standby mode", the CRT and flat-panel interfaces are turned off, and in addition, the VGA subsystem is turned off. The screen DRAM is placed in a low-power mode in which only the DRAM is refreshed. To take advantage of the power savings modes, you must implement the power switches using the special enable signals on connector J3. The Ampro LCD Bias Supply option fully implements the advanced power management features.

BIOS Support of Non-Standard Panels

Ampro supplies flat panel BIOS images for several popular LCD panels. You select the panel BIOS using SETUP (see Chapter 3). If you select an unsupported panel, you must modify the standard BIOS to support the panel. Ampro can provide a BIOS modification kit to do this. Contact your Ampro sales representative or Ampro Technical Support for information about the Little Board/486*i* Flat Panel BIOS Modification Kit.

2.12.3 The LCD Bias Supply Option

The LCD Bias Supply Option is a small circuit board that supplies Vee power to an LCD display. The board converts the +5V from the Little Board/486*i* to the Vee voltage (between 15V and 35V) required by most LCD panels, and makes this voltage available on the flat panel connector J3.

LCD displays are sensitive to the sequence (order) and timing that power supply and control signals are applied to the display during power up and removed during power down cycles. LCD manufacturers warn OEMs that violating the sequence and timing specifications of these signals can damage the display or reduce its service life. The LCD Bias Supply option, in conjunction with control signals from the Little Board/486*i* video controller option, automatically sequences the appropriate signals to meet the requirements of virtually any LCD display.

The Ampro LCD Bias Supply option mounts parallel to the Little Board/486*i*, connected to the board via a 12-pin connector, J4. You secure the board to the Little Board/486*i* using a .6 inch standoff. The table below shows the connector pinout for J4, with a description of each signal. Note that some signals also appear on the flat panel connector, J3.

J4 Pin	J3 Pin	Description
1		Ground
2		+5V to the Vee Supply Option board
4		Ground
6	38	Enable Vee TTL control signal, driven by the VGA controller chip
8		Ground
11	46	Vee Output, to panel
12	47	Contrast adjustment Analog control signal

Table 2-26 LCD Bias Supply Option Connector (J4)

Selecting Vee Polarity

Most LCD displays require a Vee supply of between 15V and 35V. Some panels need a negative supply, and some a positive supply. The LCD Bias Supply Option provides a jumper for selecting the Vee output polarity. To select the polarity for the panel you will be using, set the jumper on W1 (on the LCD Bias Supply board, not on the Little Board/486*i*) as shown in the following figure.

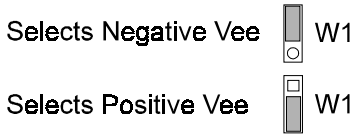


Figure 2-13 Vee Polarity Selection Jumper

Note

Incorrect Vee polarity or voltage can damage an LCD panel. Set the polarity and voltage on the Vee supply before connecting the LCD panel.

Attaching an External Contrast Control

Vee controls the contrast of the LCD display. (Do not confuse this with a backlight, which illuminates the screen using one or more fluorescent tubes. Backlights generally require a high voltage AC supply.)

An onboard control (R1) allows you to set the precise Vee voltage for the contrast you require. However, you may want to provide a more accessible Vee control so that a user can set the display contrast to accommodate various ambient lighting conditions. The board provides a jumper and control signal to allow the attachment of a remote potentiometer.

To use the contrast potentiometer on the LCD Bias Supply board, install a jumper on W2 (on the LCD Bias Supply board).

To use an external potentiometer, remove the jumper from W2, and attach the circuit shown below between J3-47 and ground.

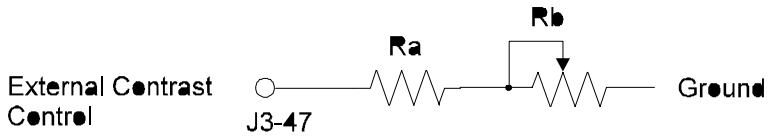


Figure 2-14 External Contrast Adjustment for LCD panels

Select Ra and Rb to provide the appropriate voltage range adjustment for the LCD panel you are using. Consult your panel's technical literature for the range of voltages you need to supply for the contrast adjustment. Use the following formulae to calculate the resistor values (in K Ohms).

$$Ra = \frac{270}{(Vee\ max/1.5) - 1} - 12$$

$$Rb = \frac{270}{(Vee\ min/1.5) - 1} - 12 - Ra$$

Example:

Suppose the following values are shown in the panel's data sheet:

Vee max = 24 V
Vee min = 20 V

Calculate the required resistor values as follows:

Ra = (270 / ((24 / 1.5) - 1)) -12

Ra = 6K Ω

Rb = (270 / ((20 / 1.5) - 1)) -12 - 6

Rb = 3.9K Ω

2.12.4 External Video Overlay Connector (J6)

This section describes the External Video Overlay Connector (J6). The interface at this connector is used to overlay externally-generated RGB video over the internal VGA data stream. It uses either color keying or X-Y window keying. For further information about the external video overlay function, see the explanation in Chapter 3.

J6 is a high density latching connector with .1 in. x .05 in pins. The following table lists the signals and pin numbers of J6:

J6 Pin	Name	Function
19	VSYNC	Vertical Sync (output)
21	HSYNC	Horizontal Sync (output)
29	PCLK	Pixel Clock (output)
31	KEY	Color Key (Input)
33	PCVR2	Video Data 0 (Input)
34	PCVR3	Video Data 1 (Input)
36	PCVR4	Video Data 2 (Input)
37	PCVR5	Video Data 3 (Input)
57	PCVR6	Video Data 4 (Input)
58	PCVR7	Video Data 5 (Input)
39	PCVG2	Video Data 6 (Input)
40	PCVG3	Video Data 7 (Input)
42	PCVG4	Video Data 8 (Input)
43	PCVG5	Video Data 9 (Input)
45	PCVG6	Video Data 10 (Input)
46	PCVG7	Video Data 11 (Input)
48	PCVB2	Video Data 12 (Input)
49	PCVB3	Video Data 13 (Input)
51	PCVB4	Video Data 14 (Input)
52	PCVB5	Video Data 15 (Input)
54	PCVB6	Video Data 16 (Input)
55	PCVB7	Video Data 17 (Input)
2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 35, 38, 41, 44, 47, 50, 53, 56	Ground	Ground
1, 3, 5, 7, 9, 11, 13, 15, 17, 23, 25, 27, 59, 60	No Connection	

Table 2-27 External Video Overlay Connector (J6)

Mating Connector
AMP 1-111196-1 (latching connector)

Table 2-28 J6 Mating Connector

2.13 ETHERNET NETWORK INTERFACE

This section describes how to configure and connect the Ethernet LAN interface.

There are no jumpers to set on the Ethernet interface, and no hardware configuration, other than connecting the network cable to an appropriate connector. Software configuration of the Ethernet interface includes the following steps (mentioned briefly here, and covered in detail in Chapter 3):

- In SETUP, enable the Ethernet interface.
- In SETUP, select the I/O address block. The interface uses a 16-byte block of I/O addresses starting at 300h, 320h (the default), 360h, or 380h.
- In SETUP, select the Ethernet media you will be using. Select the twisted pair interface if you want to connect a twisted pair cable to the RJ45 connector. Select the AUI interface if you want to attach an external transceiver or Media Attachment Unit (MAU) and run on a different medium, such as thick coax or thin coax.
- In SETUP, select an IRQ. The interface can use either IRQ3, IRQ9 (the default), IRQ10, or IRQ11. Choose an unused interrupt, as interrupt sharing is not implemented for this interface.

Note

IRQ11 is the default interrupt selection for the SCSI-II interface. Only select IRQ11 if you do not have it enabled for the SCSI interface using jumper W12.

Note

IRQ3 is the default interrupt for serial 2 and an option for serial 4. Only select IRQ3 if these serial ports are not using it.

- If you plan to boot from the network (that is, if you plan to use the Little Board/486*i* as a diskless peripheral or workstation), set up the boot PROM. See the section, “Setting up a Boot PROM”, below, for details.
- Install the proper driver for the network operating system you will be running. Normally this is done by adding a **DEVICE=** entry in the CONFIG.SYS file. This is covered in detail in Chapter 3.

2.13.1 Setting up a Boot PROM

If you plan to boot from the network, you must provide a boot ROM program compatible with your network operating system. You install this program in the Expansion BIOS ROM, a Flash EPROM device provided on the board. Complete details are provided in Chapter 3. Briefly, these are the steps you take:

- In SETUP, enable the expansion BIOS ROM at CC000h. (If you do not use a boot PROM, this option should be disabled.)
- Remove W9 and install W13.
- Program the PROM with your boot PROM code using a utility called PGMIBIOS.COM, supplied by Ampro on the utility disk that comes with the Little Board/486i Development Kit.
- Enable “Boot from Floppy” in SETUP. (SETUP is described in Chapter 3.)

2.13.2 Connecting to the Ethernet Cable

The Ethernet interface supports two Ethernet media, 10BaseT (twisted pair) and the AUI interface. The interface connectors are described in this section.

Ampro supplies an optional transition cable assembly that plugs into the AUI connector. The AUI interface cable provides a female DB-15 connector. Contact Ampro for information on ordering this cable.

Twisted Pair Interface (J7)

The twisted pair interface (10BaseT) appears on connector J7. It is a standard RJ45 telephone-type modular connector, which is the normal connector used with standard twisted-pair cables. If you are using the twisted-pair interface, you must select it using SETUP. Details are provided in Chapter 3.

The following table lists the signals and pin numbers of J7:

J7 Pin	Function
1	+ Transmit Data
2	- Transmit Data
3	+ Receive Data
4	N/C
5	N/C
6	- Receive Data

Table 2-29 RJ45 Twisted Pair Connector (J7)

AUI Interface (J8)

You can connect the Ethernet interface to a LAN through the standard Adapter Unit Interface (AUI) connection. The AUI connects to an external transceiver or MAU which, in turn, connects to the LAN cable. The AUI enables you to connect your node to fiber optic, thick net cable, or other Ethernet media, with the appropriate MAU. Connect the AUI adapter cable to J8. Ampro offers an optional AUI adapter cable to connect between J8 and a standard MAU adapter cable. Length of the MAU cable should be less than 24 inches.

If you use the AUI interface, you must supply +12V, via the PC Expansion Bus connector, J1A/B, or power connector, J10.

Note

This is the only Little Board/486i interface that requires an external +12V supply.

If you use the AUI interface, you must select it in SETUP. You cannot use the RJ45 interface and the AUI interfaces simultaneously.

The following table lists the signals and pin numbers of J8 and a MAU-compatible DB-15:

J8 Pin	AUI DB-15 Pin	Function
1	9	- Collision Detect
2	2	+ Collision Detect
3	10	- Transmit Data
4	3	+ Transmit Data
7	12	- Receive Data
8	5	+ Receive Data
9	13	+12V Power
5, 6, 10	4, 11, 6	Ground
	1, 7, 8, 14, 15	N/C
Twisted pairs: 1/2, 3/4, 7/8		

Table 2-30 AUI Connector (J8)

Connector Type	Mating Connector
RIBBON	3M 3473-7600
DISCRETE WIRE	MOLEX HOUSING 22-55-2102 Pin 16-02-0103

Table 2-31 J8 Mating Connector

2.14 BATTERY-BACKED CLOCK

An AT-compatible battery-backed real-time clock (with CMOS RAM) is standard on the Little Board/486*i*. The clock is powered by a 3.6 volt Lithium battery soldered to the board. Battery drain for the clock is less than 1 uA. This battery will support the clock for about 10 years. (This assumes that the battery is not also used to supply backup power to SRAM devices in the byte-wide sockets.)

The factory initializes the real-time clock and various parameters in the configuration memory for a standard configuration. The factory sets the date and time, but it may not be set for your time zone. Use the Ampro SETUP utility to change these values as needed.

The contents of the configuration memory are also stored in an onboard EEPROM. The ROM BIOS reads the EEPROM to get configuration information if the CMOS RAM data is lost. This means that the board will function without the battery. Note that without a battery, the real-time clock date and time will not be correct.

2.15 WATCHDOG TIMER

A unique feature of the on-board clock circuitry is a watchdog timer. You can program this timer to generate an interrupt or reset signal if the programmed time interval expires before the timer is reinitialized. Use SETUP to select the time interval. The options are: Disable, 30 seconds, 60 seconds, and 90 seconds.

The watchdog timer uses the standard alarm feature of the real-time clock. In a standard AT, the alarm output is connected to IRQ8. On the Little Board/486*i* you can also jumper the alarm output to I/O Channel Check (-IOCHCK) or Reset with W11. I/O Channel Check is the bus signal that triggers a non-maskable interrupt (NMI). Reset is a hard reset signal, the same as pressing the Reset button. For the watchdog timer to generate I/O Channel Check, short W11-1/2. For Reset, short W11-2/3. To disable the watchdog timer, leave W11 open, and select Watchdog Timer Disable in SETUP.

If you enable the watchdog timer in SETUP, but do not install a jumper on W11, IRQ8 will turn off the interrupt and the system will continue, unaffected. If you select I/O Channel Check, the watchdog timer will generate a message on the screen. If you select Reset, no interrupt handler is required.

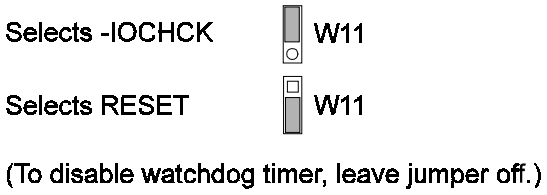


Figure 2-15 Watchdog Timer Response Jumper (W11)

2.16 UTILITY CONNECTOR (J16)

Seven functions appear on the 16-pin connector at J16. These are:

- Auxiliary power connections
- Power indicator LED
- PC speaker
- Push-button reset switch

- Security key switch
- Keyboard interface
- External back-up battery

Table 2-32 shows the pinout and signal definitions of the Utility Connector. Since there are connections for diverse features on this single connector, you would usually choose a discrete-wire connector rather than a ribbon cable connector, though this is not a requirement. Table 2-33 shows manufacturer's part numbers for both types of mating connectors.

Pin	Signal Name	Function
1	-12V power	Connect external -12V supply here for distribution to expansion cards needing this voltage.
2	Ground	Ground return
3	-5V power	Connect external -5V supply here for distribution to expansion cards needing this voltage.
4	Ground	Ground return
5	LED Anode	LED current source (+5V through 330 ohms)
6	KEY	No connection. Use for keying the connector.
7	Speaker +	PC audio signal output
8	Ground	Ground
9	Reset	To one side of manual reset button.
10	Kbd SW	To one side of the keyboard security switch.
11	Kbd Data	Keyboard serial data
12	Kbd Clk	Keyboard clock
13	Ground	Keyboard ground
14	Kbd Power	Keyboard +5V power
15	BATV+	External battery +
16	BATV-	External battery -

Table 2-32 Utility Connector (J16)

Connector Type	Mating Connector
RIBBON	3M 3452-7600
DISCRETE WIRE	MOLEX Housing 22-55-2162 Pin 16-02-0103

Table 2-33 J16 Mating Connector

2.16.1 LED Connection

To connect an external LED power-on indication lamp, connect the LED anode (-) to J16-5 and the cathode (+) to ground. J16-5 provides +5V through a 300 ohm resistor.

2.16.2 Speaker Connections

The board supplies about 100 milliwatts for a speaker on J16-7. Connect the other side of the speaker to ground (J16-8). A transistor amplifier buffers the speaker signal. Use a small general purpose 2 or 3 inch permanent magnet speaker with an 8 ohm voice coil. Refer to Chapter 3 for an explanation of the PC speaker circuit architecture.

2.16.3 Push-button Reset Connection

J16-9 provides a connection for an external normally-open momentary switch to manually reset the system. Connect the other side of the switch to ground. The reset signal is “de-bounced” on the board.

2.16.4 Security Switch Connection

Connect a security switch between J16-10 and ground. The security switch can be a key switch (as provided on desktop PCs) or other mechanical switch, or a digital signal that you provide. The security switch locks out keyboard entry.

2.16.5 Keyboard Connections

You can connect an AT (not PC) keyboard to the keyboard port. J16-11 through J16-14 provide this function. Normally, AT keyboards include a cable that terminates in a male 5-pin DIN plug for connection to an AT. Table 2-34 gives the keyboard connector pinout and signal definitions, and includes corresponding pin numbers of a normal AT DIN keyboard connector.

J16 Pin	Signal Name	DIN Pin
12	Keyboard Clock	1
11	Keyboard Data	2
N/C	N/C	3
13	Ground	4
14	Keyboard power	5

Table 2-34 Keyboard Connector (J16)

2.16.6 External Battery Connections

To connect an external battery in parallel to the onboard battery, connect its positive terminal to J16-15 and its negative terminal to J16-16. Use a 3.6 volt lithium cell.

The two batteries are connected by low-drop Schottky diodes. Two blocking devices are in series with the batteries, complying with UL recommendations for lithium batteries.

2.17 AT EXPANSION BUS

The PC/AT expansion bus appears on a pair of header connectors at P1 and P2. P1 is a 64-pin female dual-row header. P2 is a 40-pin female dual-row header. The PC-bus subset of the expansion bus connects to the first 62 positions of P1; the two additional positions of P1 (A32 and B32) are added grounds to enhance system reliability. Connector P2 replaces the 32-pin edgecard connector of a conventional AT expansion bus. It has extra ground positions at each end of the connector (C0, D0, D19). (C19 is a key pin.) The layout of signals on P1 and P2 is compliant with the PC/104 bus specification. PC/104-compatible expansion modules can be installed on the Little Board/486*i* expansion bus.

The buffered output signals to the expansion bus are standard TTL level signals. All inputs to the Little Board/486*i* operate at TTL levels and present a typical CMOS load to the expansion bus. The current ratings for most output signals driving the AT expansion bus are shown in Tables 2-35 through 2-38, and indicate how the signals are terminated on the Little Board/486*i*.

2.17.1 On-board MiniModule Expansion

You can install one or more Ampro MiniModule products or other PC/104 modules on the Little Board/486*i* expansion connectors. When installed on P1 and P2, the expansion modules fit within the Little Board/486*i*'s outline dimensions. Most Ampro MiniModule products have stackthrough connectors compatible with the PC/104 Version 2.1 specification. You can stack several modules on the Little Board/486*i* headers. Each additional module increases the thickness of the package by 0.66 inches (17 mm). See Figure 2-15.

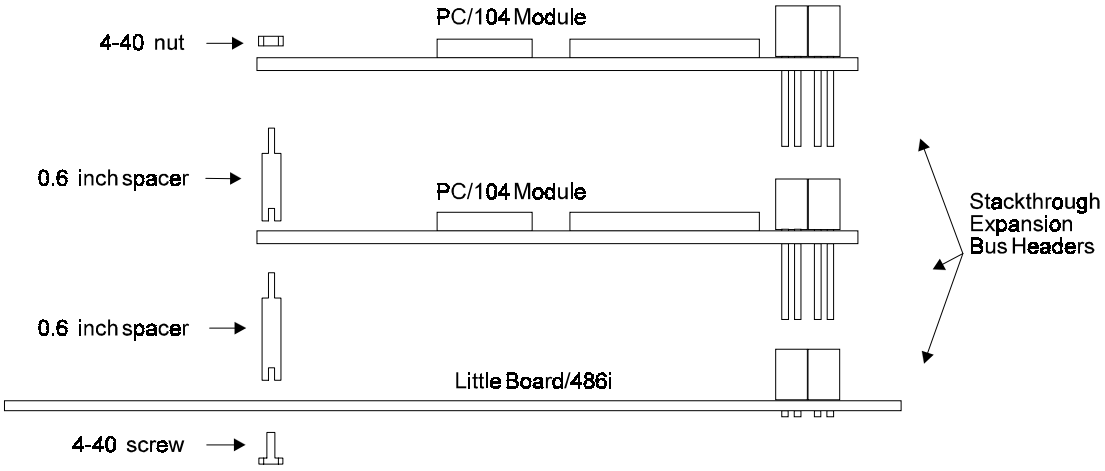


Figure 2-16 Stacking PC/104 Modules on the Little Board/486*i*

2.17.2 Using Standard PC and AT Bus Cards

Ampro offers several options that allow you to add conventional 8-bit and 16-bit ISA expansion cards to the Little Board/486*i* system. Contact Ampro for further information about optional bus expansion products.

2.17.3 Bus Expansion Guidelines

One way to expand a Little Board/486*i* is by connecting short cables to the header connectors. Ampro makes a small ribbon cable connector assembly that you can use to connect standard ribbon cable connectors to the female expansion bus connectors on the Little Board/486*i*. Contact your Ampro sales representative for more information about the ribbon cable adapter.

There are restrictions when attaching peripherals to the expansion bus with ribbon cables. If cables are too long or improperly terminated, noise and cross-talk introduced by the ribbon cables can cause errors. Ampro strongly recommends that you follow these guidelines.

- **Cable Length and Quality**—In general, keep the bus expansion cable as short as possible. Long cables reduce system reliability.
  - For cables up to 6 inches, use a high quality standard cable, such as 3M 3365/64 (64 conductor) and 3365/40 (40 conductor).
  - For cables between 6 to 12 inches long, use a high quality ground plane cable, such as 3M part number 3476/64 (64 conductor) and 3476/40 (40 conductor).
  - Do not use cables over 12 inches long.

WARNING

When using ground plane cable on P1, use a single drain cable with the drain wire on pin 64 of the cable. If the drain wire is on pin 1, IOCHK is shorted to GND, and the board will not function.

- **Backplane Quality**—If you connect a backplane to the Little Board/486i, be sure to use a high quality backplane that minimizes signal crosstalk. Use a backplane that has power and ground planes between trace layers, and run guard traces between sensitive bus signals.
- **Eliminating Reset and TC Noise**—Many cards have asynchronous TTL logic inputs that are susceptible to noise and crosstalk. The active high RESET and TC bus lines are especially vulnerable. You can make these signals more reliable by adding a 200 pF to 500 pF capacitor between the signal and ground to prevent false triggering by filtering noise on the signals. These RESET and TC filters are included on most Ampro backplane expansion products.

Bus Termination—Some backplanes include bus termination to improve system reliability by matching backplane impedance to the rest of the system. The IEEE-P996 draft specification for the AT expansion bus recommends the use of AC termination (sometimes called “snubbers”) rather than resistive termination. The recommended AC termination is a 50 to 100 pF capacitor, in series with a 50 to 100 ohm resistor, from each signal to ground. Ampro provides positions for OEM addition of AC termination on most bus expansion products. These positions are designed to accommodate 9-pin 8-terminator Single Inline Package (SIP) terminators.

Here are some manufacturer part numbers for 9-pin, eight-terminator devices with 100 pF capacitors in series with 100 ohm resistors:

- Dale CSRC-09C30-101J-101M
- Bourns 4609H-701-101/101

CAUTION

Do not use resistive bus termination! If the signal requires termination, use AC termination only.

The actual requirements for signal termination depend on system configuration, interconnecting bus cable, and on the number and type of expansion modules used. It is the system engineer's responsibility to determine the need for termination.

2.17.4 Expansion Bus Connector Pinouts

Tables 2-35 through 2-38 show the pinout and signal functions on the PC/104-compatible expansion bus connectors.

The Little Board/486*i* does not generate ±12VDC or -5VDC for the expansion bus. If devices on the bus require these voltages, -12V and -5V can be supplied to the bus connector from the utility connector (J16). +12V can be supplied through J10-1.

You do not need to add a +12V supply to program Flash EPROMs installed in the byte-wide sockets, or for the onboard Flash device that stores the ROM BIOS, video BIOS, and optional Ethernet boot PROM code. An onboard supply provides the programming voltage. This supply does not provide power to the expansion bus. Most Ampro expansion products provide onboard DC-to-DC converters to convert the +5V supply to other voltages they require.

The expansion bus pin numbers shown in the following tables correspond to the scheme normally used on ISA expansion bus card sockets. Rather than numerical designations (1, 2, 3) they have alpha-numeric designations (A1, A2…, B1, B2…, etc.) .

Pin	Signal Name	Function	In/Out	Current	PU/PD/Ser*
A1	-IOCHCK	bus NMI input	IN	N/A	
A2	SD7	Data bit 7	I/O	8 mA	10K PU
A3	SD6	Data bit 6	I/O	8 mA	10K PU
A4	SD5	Data bit 5	I/O	8 mA	10K PU
A5	SD4	Data bit 4	I/O	8 mA	10K PU
A6	SD3	Data bit 3	I/O	8 mA	10K PU
A7	SD2	Data bit 2	I/O	8 mA	10K PU
A8	SD1	Data bit 1	I/O	8 mA	10K PU
A9	SD0	Data bit 0	I/O	8 mA	10K PU
A10	IOCHRDY	Processor Ready Ctrl	IN	N/A	1K PU
A11	AEN	Address Enable	I/O	8 mA	
A12	SA19	Address bit 19	I/O	24 mA	
A13	SA18	Address bit 18	I/O	24 mA	
A14	SA17	Address bit 17	I/O	24 mA	
A15	SA16	Address bit 16	I/O	24 mA	
A16	SA15	Address bit 15	I/O	24 mA	
A17	SA14	Address bit 14	I/O	24 mA	
A18	SA13	Address bit 13	I/O	24 mA	
A19	SA12	Address bit 12	I/O	24 mA	
A20	SA11	Address bit 11	I/O	24 mA	
A21	SA10	Address bit 10	I/O	24 mA	
A22	SA9	Address bit 9	I/O	24 mA	
A23	SA8	Address bit 8	I/O	24 mA	
A24	SA7	Address bit 7	I/O	24 mA	
A25	SA6	Address bit 6	I/O	24 mA	
A26	SA5	Address bit 5	I/O	24 mA	
A27	SA4	Address bit 4	I/O	24 mA	
A28	SA3	Address bit 3	I/O	24 mA	
A29	SA2	Address bit 2	I/O	24 mA	
A30	SA1	Address bit 1	I/O	8 mA	
A31	SA0	Address bit 0	I/O	8 mA	10K PU
A32	GND (**)	Ground	N/A	N/A	

* PU=pull up; PD=pull down; S=resistance in series. All values in ohms.

** Added ground. Not needed with conventional expansion cards.

Table 2-35 AT Expansion Bus Connector, A1-A32 (P1)

Pin	Signal Name	Function	In/Out	Current	PU/PD/Ser*
B1	GND	Ground	N/A	N/A	
B2	RESETDRV	System reset signal	OUT	12 mA	
B3	+5V	+5 Volt power	N/A	N/A	
B4	IRQ9	Interrupt request 9	IN	N/A	10K PU
B5	-5V	To J16-3	N/A	N/A	
B6	DRQ2	DMA request 2	IN	N/A	10K PU
B7	-12V	To J16-1	N/A	N/A	
B8	-ENDXFR	Zero wait state	IN	N/A	
B9	+12V	To J10-1	N/A	N/A	
B10	N/A	Keyed pin	N/A	N/A	
B11	-SMEMW	Mem Write(lwr 1MB)	I/O	24 mA	33 S, 10K PU
B12	-SMEMR	Mem Read(lwr 1MB)	I/O	24 mA	33 S, 10K PU
B13	-IOW	I/O Write	I/O	8 mA	33 S, 10K PU
B14	-IOR	I/O Read	I/O	8 mA	33 S, 10K PU
B15	-DACK3	DMA Acknowledge 3	OUT	6 mA	
B16	DRQ3	DMA Request 3	IN	N/A	10K PU
B17	-DACK1	DMA Acknowledge 1	OUT	6 mA	
B18	DRQ1	DMA Request 1	IN	N/A	10K PU
B19	-REFRESH	Memory Refresh	I/O	24 mA	33 S,4.7K PU
B20	SYSCLK	Sys Clock	OUT	12 mA	
B21	IRQ7	Interrupt Request 7	IN	N/A	27K PU
B22	IRQ6	Interrupt Request 6	IN	N/A	27K PU
B23	IRQ5	Interrupt Request 5	IN	N/A	27K PU
B24	IRQ4	Interrupt Request 4	IN	N/A	27K PU
B25	IRQ3	Interrupt Request 3	IN	N/A	27K PU
B26	-DACK2	DMA Acknowledge 2	OUT	6 mA	
B27	TC	DMA Terminal Count	OUT	4 mA	
B28	BALE	Address latch enable	OUT	12 mA	33 S
B29	+5V	+5V power	N/A	N/A	
B30	OSC	14.3 Mhz clock	OUT	6 mA	33 S
B31	GND	Ground	N/A	N/A	
B32	GND**	Ground	N/A	N/A	

* PU=pull up; PD=pull down; S=resistance in series. All values in ohms.

** Added ground. Not needed with conventional expansion cards.

Table 2-36 AT Expansion Bus Connector, B1-B32 (P1)

Pin	Signal Name	Function	In/Out	Current	PU/PD/Ser*
C0	GND**	Ground	N/A	N/A	
C1	-SBHE	Bus High Enable	I/O	8 mA	10K PU
C2	LA23	Address bit 23	I/O	24 mA	
C3	LA22	Address bit 22	I/O	24 mA	
C4	LA21	Address bit 21	I/O	24 mA	
C5	LA20	Address bit 20	I/O	24 mA	
C6	LA19	Address bit 19	I/O	24 mA	
C7	LA18	Address bit 18	I/O	24 mA	
C8	LA17	Address bit 17	I/O	24 mA	
C9	-MEMR	Memory Read	I/O	8 mA	33 S, 27K PU
C10	-MEMW	Memory Write	I/O	8 mA	33 S, 27K PU
C11	SD8	Data Bit 8	I/O	8 mA	10K PU
C12	SD9	Data Bit 9	I/O	8 mA	10K PU
C13	SD10	Data Bit 10	I/O	8 mA	10K PU
C14	SD11	Data Bit 11	I/O	8 mA	10K PU
C15	SD12	Data Bit 12	I/O	8 mA	10K PU
C16	SD13	Data Bit 13	I/O	8 mA	10K PU
C17	SD14	Data Bit 14	I/O	8 mA	10K PU
C18	SD15	Data Bit 15	I/O	8 mA	27K PU
C19	Key	Key Pin	N/A	N/A	

* PU=pull up; PD=pull down; S=resistance in series. All values in ohms.

** Added ground. Not needed with conventional expansion cards.

Table 2-37 AT Expansion Bus Connector, C0-C19 (P2)

Pin	Signal Name	Function	In/Out	Current	PU/PD/Ser *
D0	GND**	Ground	N/A	N/A	
D1	-MEMCS16	16-bit Mem Access	IN	N/A	330 PU
D2	-IOCS16	16-bit I/O Access	IN	N/A	330 PU
D3	IRQ10	Interrupt Request 10	IN	N/A	10K PU
D4	IRQ11	Interrupt Request 11	IN	N/A	10K PU
D5	IRQ12	Interrupt Request 12	IN	N/A	10K PU
D6	IRQ15	Interrupt Request 15	IN	N/A	10K PU
D7	IRQ14	Interrupt Request 14	IN	N/A	10K PU
D8	-DACK0	DMA Acknowledge 0	OUT	6mA	
D9	DRQ0	DMA Request 0	IN	N/A	10K PU
D10	-DACK5	DMA Acknowledge 5	OUT	6mA	
D11	DRQ5	DMA Request 5	IN	N/A	10K PU
D12	-DACK6	DMA Acknowledge 6	OUT	6mA	
D13	DRQ6	DMA Request 6	IN	N/A	10K PU
D14	-DACK7	DMA Acknowledge 7	OUT	6mA	
D15	DRQ7	DMA Request 7	IN	N/A	10K PU
D16	+5V	+5 Volt Power	N/A	N/A	
D17	-MASTER	Bus Master Assert	IN	N/A	330 PU
D18	GND	Ground	N/A	N/A	
D19	GND**	Ground	N/A	N/A	

* PU=pull up; PD=pull down; SER=resistance in series. All values in ohms.

** Added ground. Not needed with conventional expansion cards.

Table 2-38 AT Expansion Bus Connector, D0-D19 (P2)

2.17.5 Interrupt and DMA Channel Usage

The AT bus provides several interrupt and DMA control signals. When you expand the system with MiniModule products or plug-in cards that require either interrupt or DMA support, you must select which interrupt or DMA channel to use. Typically this involves switches or jumpers on the module. In most cases, these are not shared resources. It is important that you configure the new module to use an interrupt or DMA channel not already in use. For your convenience, Tables 2-39 and 2-40 provide a summary of the normal interrupt and DMA channel assignments on the Little Board/486*i*.

Interrupt	Function
IRQ0*	ROM BIOS clock tick function, from Timer 0
IRQ1*	Keyboard interrupt
IRQ2*	Cascade input for IRQ8-15
IRQ3	Serial 2
IRQ4	Serial 1
IRQ5	Available
IRQ6	Floppy controller
IRQ7	Parallel port (option)
IRQ8*	Reserved for battery-backed clock alarm
IRQ9**	Ethernet interface default
IRQ10	Serial 4 (option)
IRQ11	SCSI interface default
IRQ12	Serial 3 (option)
IRQ13*	Reserved for coprocessor
IRQ14	IDE hard disk controller
IRQ15	Available

* Unavailable on PC/AT bus.
** Corresponds to IRQ2 on a PC's expansion bus.

Table 2-39 Interrupt Channel Assignments

Channel	Function
0	Available for 8-bit transfers
1	Available for 8-bit transfers (Multimode Parallel port)
2	Floppy controller
3	Available for 8-bit transfers
4	Cascade for channels 0-3
5	Available for 16-bit transfers
6	Available for 16-bit transfers
7	Available for 16-bit transfers

Table 2-40 DMA Channel Assignments

The following table summarizes the available interrupt assignments for all subsystems on the Little Board/486*i*. Use the table to plan which interrupts to use in your system. Factory defaults are shown in gray.

	IRQ										
Function	**3**	**4**	**5**	**6**	**7**	**9**	**10**	**11**	**12**	**14**	**15**
Serial 1		✓									
Serial 2	✓										
Serial 3		✓							✓		
Serial 4	✓						✓				
Parallel			✓		✓						
Floppy				✓							
IDE										✓	
SCSI								✓			
Ethernet	✓					✓	✓	✓			
Video	(None)										

Table 2-41 Summary of IRQ Options

CHAPTER 3

SOFTWARE CONFIGURATION

3.1 INTRODUCTION

This chapter provides the information you will need to configure your Little Board/486*i* from a software or firmware point-of-view. The first section describes the SETUP function. It describes how to configure onboard options. Additional sections cover each major functional block of the board.

Note

The SETUP descriptions in the following section also contain much useful information about each SETUP topic. Review these sections even if you already know how to set the SETUP parameters.

This chapter presumes you have some familiarity with DOS (PC-DOS, MS-DOS, or DR DOS). It does not attempt to describe the standard DOS and ROM BIOS functions. Refer to the appropriate DOS and PC reference manuals for further information about DOS, its drivers, and its utilities. Where Ampro has added to or modified standard functions, these will be described. The Ampro Common Utilities manual contains detailed descriptions of the Ampro utility programs.

3.2 SETUP

Many options provided on the Little Board/486*i* are controlled by the SETUP function. The parameters are displayed on four screens. To configure the board, you modify the fields in these screens and save the results in the onboard *configuration memory*. The configuration memory consists of portions of the CMOS RAM in the battery-backed real-time clock chip and an Ampro-unique configuration EEPROM. To enhance embedded-system reliability, the contents of the EEPROM mirror the contents of the CMOS memory. The EEPROM retains your configuration information even if the clock's backup battery should fail.

The SETUP information is retrieved from configuration memory when the board is powered up or when it is rebooted with a CTL-ALT-DEL key pattern. Changes made to the SETUP parameters (with the exception of the real-time clock time and date settings) do not take effect until the board is rebooted.

The SETUP function is located in the ROM BIOS. It can be accessed using CTRL-ALT-ESC while the computer is in the Power On Self Test (POST), just prior to booting up. This is called *hot key* access. The screen will display a message indicating when you can enter CTRL-ALT-ESC. You may also enter the SETUP function from the DOS command line using the SETUP.COM program provided on the Ampro Common Utilities diskette .

Table 3-1 summarizes the choices found on each SETUP page.

Page	Menu Name	Functions
1	Standard (CMOS/EEPROM) Configuration	Set date and time Define floppy drives Define IDE hard disks Select video type Display DRAM quantity Set error halt conditions Enable/disable video shadow RAM Set POST display option
2	Options/Peripheral Configuration	Enable/disable extended BIOS functions Enable/disable serial ports Enable/disable parallel port Enable/disable floppy interface Enable/disable IDE interface Enable/disable hot key access to SETUP Set video display state Select POST display option Configure byte-wide sockets Enable/disable expansion BIOS ROM Enable/disable serial boot loader Enable/disable watchdog timer Configure Ethernet LAN interface Configure video display Enable/Disable SCSI terminators
3	Extended SCSI and Hard Disk configuration	Set SCSI controller parameters Configure SCSI disk map Select floppy or hard disk boot Configure DOS disk map
4	Extended Serial Console Configuration	Configure serial port parameters for serial console output Configure serial port output handshake option Configure serial port parameters for serial console input Delete/include console port from DOS COM table
* SETUP pages 3 and 4 are available when you enable Extended BIOS from SETUP		

Table 3-1 Functions on Each SETUP Page

Note

Some SETUP options can put your system into an unrecoverable state. For instance, you might set a display option that prevents you from seeing the SETUP screens. Installing a jumper between J11-7 and J11-8 (Serial 1 DTR and RI) temporarily defeats the SETUP parameters stored in the configuration memory so that you can reenter SETUP and correct the problem.

3.3 SETUP PAGE 1—STANDARD (CMOS) SETUP

The first SETUP page contains the parameters normally saved in CMOS RAM plus some additional parameters unique to the Little Board/486*i*. The only parameters not also saved in the EEPROM memory are the real-time clock date and time. If no battery is used or if the battery fails, the date and time will not be accurate. All other parameters are saved in the EEPROM.

The following figure shows what can be configured from SETUP page 1. Sections following the figure describe each option.

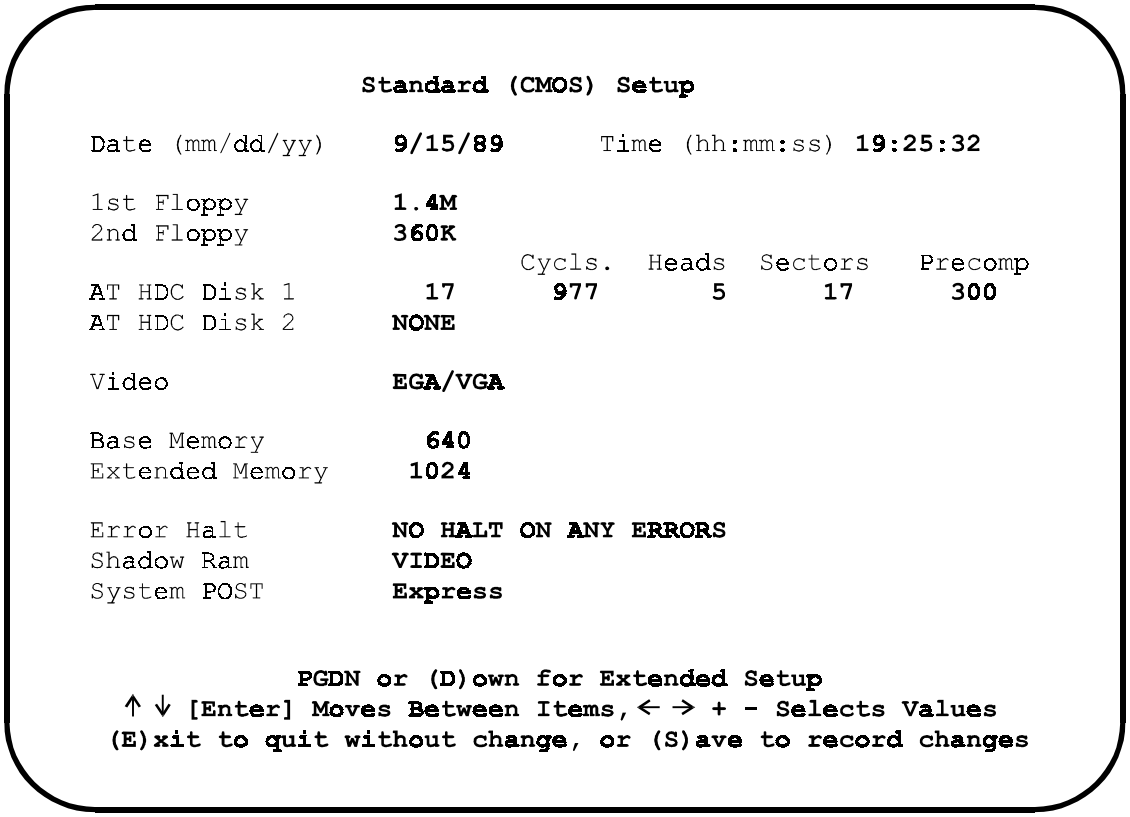


Figure 3-1 SETUP Page 1

3.3.1 Date and Time

The time shown on the screen is continuously updated by the SETUP function and reflects the current state of the hardware real-time clock. The new time that you enter is immediately written to the device. Enter the date in the form *mm/dd/yy*. Enter the time in 24-hour format, in the form *hh:mm:ss*.

The ROM BIOS maintains the *system* real-time clock. It is incremented approximately 18.2 times per second by an interrupt from timer/counter 0. The ROM BIOS automatically initializes the *system* real-time clock from the *hardware* real-time clock upon system reset or powerup.

3.3.2 Floppy Drives

The ROM BIOS supports all of the popular DOS-compatible floppy disk formats. This includes all the 5-1/4 inch and 3-1/2 inch floppy formats—360K, 720K, 1.2M, and 1.44M. (Note that some formats are not supported by early versions of DOS.) In addition, the ROM BIOS supports dual capacity use of high

density floppy drives. That is, you can read and boot from 360K floppies in a 1.2M 5-1/4 inch drive, and from 720K floppies in a 1.44M 3-1/2 inch drive.

Drive Parameter Setup

Enter the number and type of floppy drives in the system. If the drives connected to the system do not match the parameters in the configuration memory, POST displays an error message. To eliminate the error message, set the drive parameters to match your floppy drives.

3.3.3 IDE Hard Disk Drives

The ROM BIOS supports one or two hard disk drives connected to the IDE interface. The BIOS allows you to mix IDE drives in combination with SCSI hard disk drives.

Physical drives can have one or more logical partitions. You can install up to eight logical drives or drive partitions. (Older versions of DOS may limit the number of logical drives you can install.)

To configure the system for one or two IDE drives, set the drive parameters with SETUP, as outlined here:

- **Drive Types**—The configuration memory contains a default list of parameters that specify the physical format of each drive. Each *type* specifies the total number of cylinders, number of heads, cylinder to begin precompensation, landing zone cylinder number, and the number of sectors per cylinder. The drive manufacturer supplies these parameters. The list contains "legacy values", standard for PCs—a number of older (smaller) drives are defined. Two special drive types, 48 and 49 let you enter drive parameters manually. If no built-in drive type matches your drive, select drive type 48 or 49 and enter the drive parameters in the fields provided.
- **Drive Selection**—Besides specifying the physical characteristics of each IDE drive, you also must specify how they are to be used by the ROM BIOS. Two factors control how they are used, drive number jumper(s) and the DOS disk map.

    1. The IDE drive can be jumpered as a master or slave. Each manufacturer's drive is different, so refer to the drive's technical literature to find out how to jumper your drive. Drives default to **master** from the factory, so if you only have one IDE drive in a system it is generally already set up properly.
    2. Use the SETUP Extended SCSI and Hard Disk Configuration menu (SETUP page 3) to enter your IDE drive(s) in the DOS disk map. Disk 1 in the map will be logged by DOS to be drive C:, Disk 2 as drive D:, and so on. See the description of SETUP page 3 for details.

Once you have set the system's configuration memory, the IDE drive(s) can be formatted and otherwise prepared normally. Refer to your operating system and disk drive documentation for specific procedures and requirements.

3.3.4 Video

Specify the initial video mode. Select Mono, CGA, or EGA/VGA. If your video display card is VGA, super VGA, or any other high resolution standard, specify **EGA/VGA** no matter how it is configured to come up. If you are using the onboard flat panel/CRT video controller, specify **EGA/VGA**.

3.3.5 DRAM Memory

The ROM BIOS automatically sets the amount of memory during Power-On Self-Test (POST) and stores the result when you save the configuration values when exiting SETUP. If you change the amount of memory installed on the board, however, you must run SETUP and do a **save** when you exit. This updates

the configuration memory to the new memory size. Until you do this, an error message will appear during POST.

3.3.6 Error Halt

Select which kinds of errors will halt the POST. If you plan to use the module without a keyboard, be sure to set this option to *not* halt on keyboard error.

3.3.7 Video Shadow RAM

This option, when enabled, allows the ROM BIOS to copy the contents of a video BIOS into DRAM. The actual video BIOS ROM on the video controller is disabled, and DRAM is mapped into the address space it occupied. This speeds up video BIOS accesses. You can use this feature with either the onboard video controller or with an external video controller.

3.3.8 System POST

Set the System POST option to control how fast the computer powers up or to control what the user sees at power up time. The choices are:

- **Normal**—Displays the results of all tests
- **Fast**—Faster than Normal POST because it uses a shorter memory test
- **Express**—Skips most tests and does not display POST test results on the screen

3.4 SETUP PAGE 2—OPTIONS/PERIPHERAL CONFIGURATION

Use SETUP page 2 to enable or disable many of the functions and peripherals provided on the Little Board/486*i*. Figure 3-2 shows what can be configured on SETUP page 2, and the sections that follow describe each parameter.

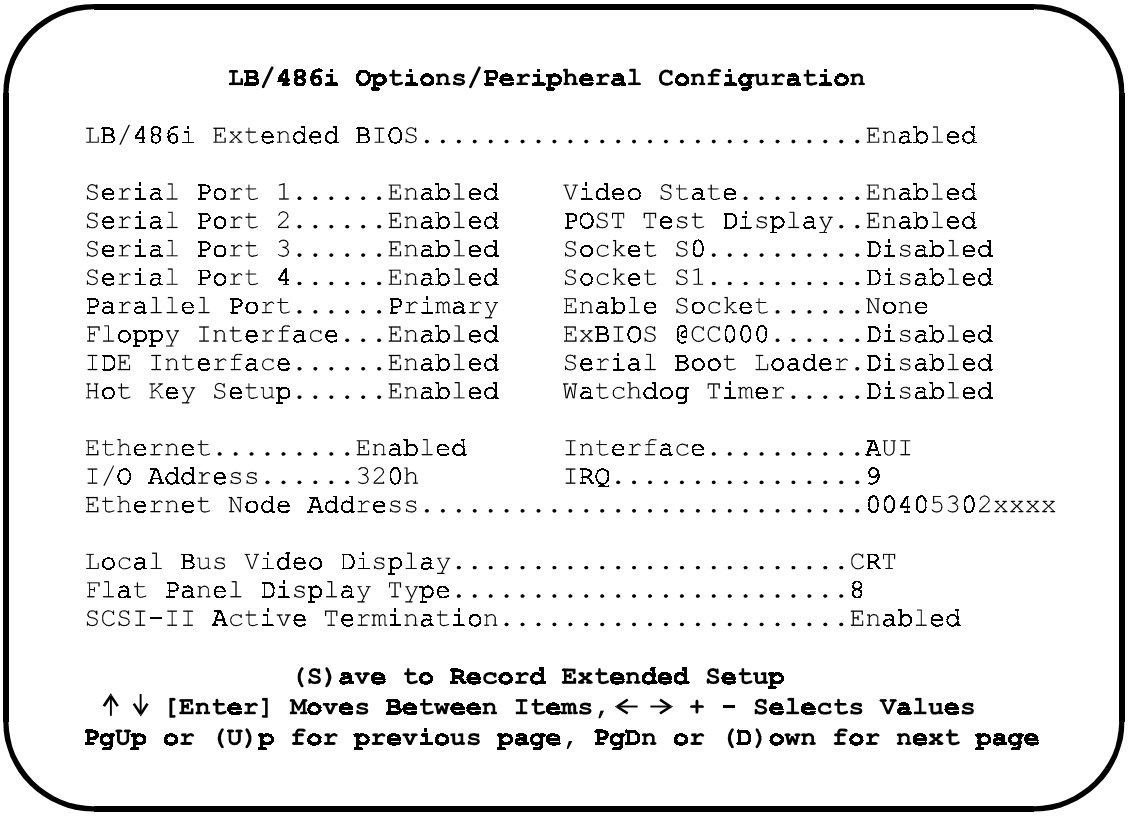


Figure 3-2 SETUP Page 2

3.4.1 Extended BIOS

Normally, the Ampro Extended BIOS is enabled. This allows access to SETUP pages three and four and the features they define. If you do not want to use the BIOS extensions, you can disable them using this parameter. (Sometimes UNIX or other operating systems may require disabling the extended portion of the BIOS.) Ampro Application Note AAN-9210 documents the features in the extended BIOS, including the application program interface specifications.

3.4.2 Serial Ports

Use SETUP to either enable or disable any of the four serial ports on the board. (When you use SETUP to enable or disable a port, the change does not take effect until you reboot the system.)

The I/O addresses for the serial ports cannot be changed. The following table lists the I/O addresses of each port (when enabled).

Port	Address
Serial 1	3F8h – 3FFh
Serial 2	2F8h – 2FFh
Serial 3	3E8h – 3EFh
Serial 4	2E8h – 2EFh

Table 3-2 Serial Port I/O Addresses

COM*n* is a logical designation, not a physical value. When the system boots, the ROM BIOS scans the standard serial port addresses and installs the first port it finds as COM1. If it finds a second port, it installs that one as COM2, and so on. If you disable a serial port, the COM*n* designations change.

3.4.3 Parallel Port

No special configuration is required to use the system with a PC-compatible parallel printer. SETUP allows you to enable the parallel port as the primary, or secondary port, or to disable it entirely.

The ROM BIOS assigns a logical designation (LPT1 or 2) to the parallel port, based on a scan at boot time. Changing the port's designation to **Secondary** with SETUP does not necessarily change it from LPT1 to LPT2. There must be an LPT1 elsewhere in the system for the onboard parallel port to become LPT2.

3.4.4 Floppy Interface Enable

Enable or disable the onboard floppy interface. When disabled, the I/O ports assigned to the floppy controller become available, allowing them to be used by other devices installed on the expansion bus.

3.4.5 IDE Interface Enable

Enable or disable the onboard IDE hard disk interface. When disabled, the I/O ports and IRQ assigned to the IDE controller become available, allowing them to be used by other devices installed on the expansion bus.

3.4.6 Hot Key Setup Enable

In some embedded systems, you do not want an end-user to use the *hot-key* sequence (CTRL-ALT-ESC) to enter SETUP. You can enable or disable hot-key access to SETUP with this parameter. (This also prevents "+++" from entering SETUP when using the serial console feature.)

3.4.7 Video State

You can set this option to Enable or Inhibited. Inhibited ***blanks*** the display until your program makes a call to the Video Restore State function in the video BIOS (via INT10h). This provides a means of controlling what appears on the screen when the system starts up. This option can be used to inhibit the POST test display and everything else that DOS or an application would display, until a call is made to the video BIOS.

The following is an example of code that reenables the display inhibited by this option:

```
;=====================================================================
init:   mov ah,1ch
        mov al,-1
        mov bx,414Dh
        mov cx,5052h
        int 10h
;=====================================================================
```

Compare this SETUP option with the POST Test Display option (see below), which affects only the POST display.

3.4.8 POST Test Display

Enable or disable POST display. If set to **Disable**, the messages from the POST will not be sent to the console. To inhibit display of a broader range of system and application messages, see Video State, above.

3.4.9 Byte-Wide Socket Configuration

There are three configuration values for the byte-wide sockets in SETUP.

- Each byte-wide socket, S0 and S1, can be independently configured for its starting address and the size of the memory block in which it appears to the processor, or it can be disabled.
- Specify which socket, S0, S1, both, or neither, is enabled at boot time using the Enable Socket parameter.

Table 3-3 lists the socket address configuration options that are available.

Size	Address
Disabled	None
64K bytes	D0000h – DFFFFh
64K bytes	E0000h – EFFFFh
128K bytes	D0000h – EFFFFh

Table 3-3 Byte-Wide Memory Configuration

If you configure both byte-wide sockets to occupy the same address space (or overlap), control logic on the board gives priority to socket S0. To access S1 in such cases, you must disable S0. The ROM BIOS provides a function for enabling and disabling the sockets. A code example is shown later in this chapter, in the section labeled “Byte-Wide Sockets”. Refer to Ampro Application Note AAN-9210 for a complete description of the BIOS functions that control the byte-wide sockets.

Devices larger than 64K or 128K can be installed, independent of the memory block size setting. The memory block size setting specifies a “window” in which the memory device is visible. You can use an extended BIOS call to select which 64K or 128K page of the installed device is visible to the processor. A code example is shown later in this chapter, in the section labeled “Byte-Wide Sockets”.

You must also set hardware jumpers to configure the byte-wide sockets for the devices you install. Refer to Chapter 2 for jumper positions. If you are using the byte-wide sockets for Solid State Disk (SSD), using Ampro's Solid State Disk software, follow the directions for setting the byte-wide sockets that are in the SSD Technical Manual.

3.4.10 Expansion BIOS ROM Configuration

The Little Board/486*i* provides 16K bytes of Flash EPROM storage (part of the ROM BIOS device) for the onboard Ethernet interface boot PROM. When enabled and properly programmed, it can be used to boot from an Ethernet network server. This SETUP option enables or disables the boot PROM region at CC000h–CFFFFh.

3.4.11 Serial Boot Loader Enable

This parameter enables or disables the Serial Boot Loader option in the Ampro ROM BIOS. The serial boot loader allows you to boot from any of the onboard serial ports, much in the same way you would boot from a local hard disk or from a LAN. A description of the Serial Boot Loader is provided in the Ampro Common Utilities manual (in descriptions of SERLOAD and SERPROG), and in Ampro Application Note AAN-9403. If you are not using the Serial Boot Loader, set this parameter to "Disable".

3.4.12 Watchdog Timer Configuration

This parameter allows you to set the time duration of the watchdog timer for monitoring the boot process. You can set it to 30, 60, or 90 seconds, or you can disable it.

Further information about the watchdog timer can be found later in this chapter under "Watchdog Timer." A description of the WATCHDOG utility program can be found in the Ampro Common Utilities manual.

3.4.13 Ethernet

These parameters control the Ethernet LAN interface on the Little Board/486*i*.

- **Ethernet Enable/Disable—**Use this parameter to enable or disable the Ethernet interface. When disabled, the interface is set to E0E0h, an unused I/O port address.
- **I/O Address—**Set the I/O port base address of the controller. The default base address is 320h. You can set it to 300h, 320h, 360h, or 380h.
- **Interface—**Select which connector (interface) you will use for your Ethernet media connection. The choices are AUI or TP (twisted pair).
- **IRQ—**Select which IRQ to use. The default is IRQ9. The choices are IRQ3, IRQ9, IRQ10, or IRQ11. (Note that the default IRQ for Serial 2 and Serial 4 is IRQ3, and the default IRQ for the SCSI interface is IRQ11.)

Ethernet Node Address—The SETUP screen displays the node address of the onboard Ethernet controller. This is just a display of the address. You cannot change it.

3.4.14 Local Bus Video Display

If you will be using a CRT display, select CRT. If you will be using a flat panel display, select FP. If you will be using both types of display, select FP&CRT. If you select FP or FP&CRT, select a flat panel display type (see below).

3.4.15 Flat Panel Display Type

There are up to 8 pre-installed flat panel video BIOS configurations available from SETUP, numbered 1 through 8. Select the panel you want by selecting its number.

The following panels are supported (numbers with no manufacturer's part numbers are still under development). Cable wiring lists for these flat panels are given in Appendix A.

Display Type Number	Manufacturer's Part Number	Description
1	Sharp LM64P839	640x480 Dual scan mono
2	Sharp LJ64ZU51	640x480 Gray-scale EL
3	Sharp LM64C35P	640x480 Dual scan STN color
4	Reserved	Reserved for future use by Ampro.
5	Sharp LQ10D131 Sharp LQ64D142	640x480 TFT color, 10.4 in. 640x480 TFT color, 6 in.
6	FPD LDH102T	640x480 TFT color, 10.4 in.
7	Reserved	Reserved for future use by Ampro.
8	Reserved	Reserved for future use by Ampro.

Table 3-4 Flat Panel Display Type Numbers

Note

Panel technology is changing rapidly. Flat panel support in the Little Board/486i ROM BIOS will changed from time to time to maintain compatibility with current panel technology. Contact Ampro Technical Support for a list of currently supported panels.

Installing a Modified BIOS to Support a New Panel

If you select an unsupported panel for your application, you must modify the video BIOS to support the new panel. Ampro provides a video BIOS modification kit to do this. Contact your Ampro sales representative or Ampro Technical Support for information about the Little Board/486*i* Flat Panel BIOS Modification Kit.

Once you have modified the video BIOS to support your new panel, you must install it on the Little Board/486*i*. Follow the instructions in "Developing a Custom BIOS for an Unsupported Flat Panel," later in this chapter.

3.4.16 SCSI-II Active Termination

The SCSI bus must be terminated by two sets of termination resistors, at each end of the SCSI bus. To enable the terminators resident on the Little Board/486*i*, set this option to Enable. If the Little Board/486*i*

is not at the end of the SCSI cable, set this option to Disable and install termination on the appropriate SCSI devices.

3.5 SETUP PAGE 3—SCSI HARD DISK

One unique feature of the Little Board/486*i* is that its ROM BIOS contains hard disk support functions that allow easy integration of SCSI and IDE drives. Use this SETUP screen to configure for your hard disk drives and other SCSI peripherals. Descriptions of each field are provided in sections below.

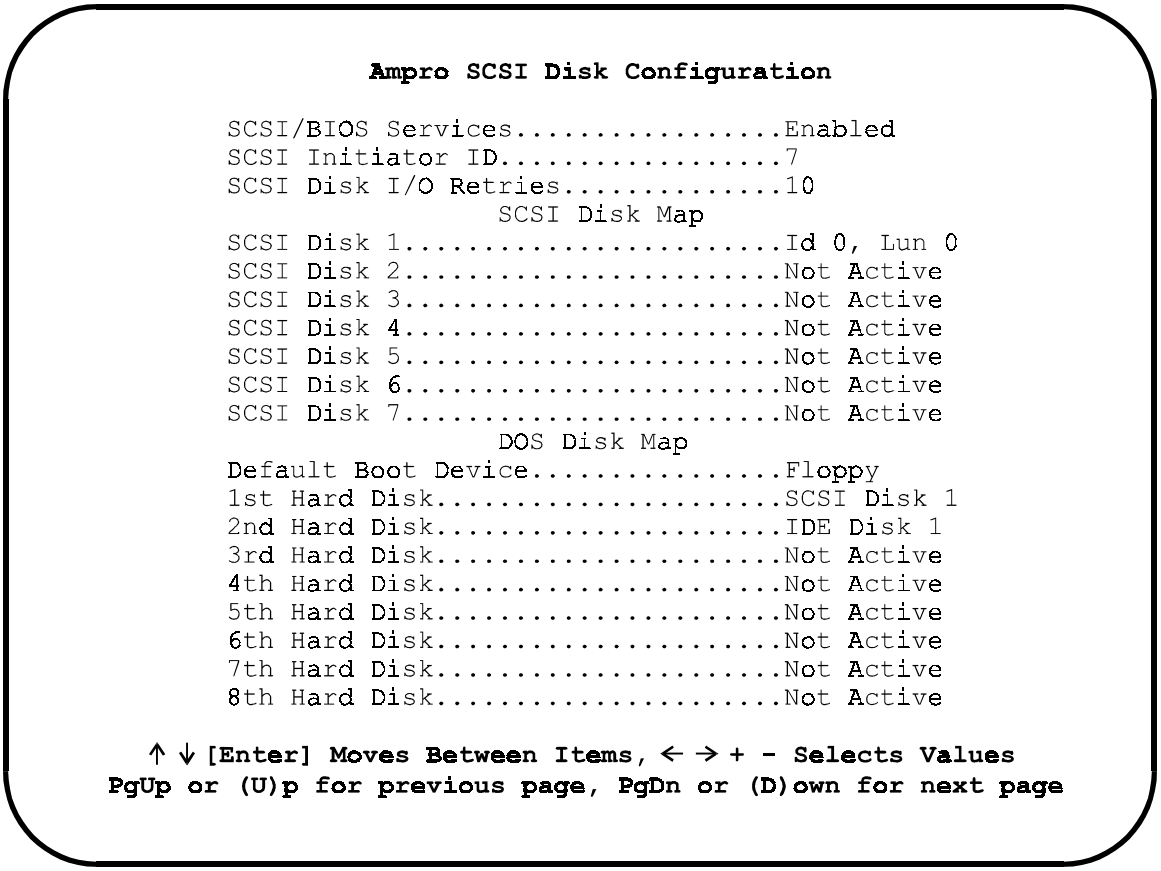


Figure 3-3 SETUP Page 3

With the Ampro Extended BIOS, SCSI hard disks are available to DOS through standard ROM BIOS functions (INT 13). SCSI functions are in the SCSI BIOS portion of the ROM BIOS. The ROM BIOS hard disk support allows direct system booting from SCSI Common Command Set direct access devices. Other types of SCSI direct access devices can be used to provide a compatible hard disk function. These include CD ROMs, tape drives, SCSI RAM disks, and other peripherals.

Most DOS applications run normally in this SCSI-based hard disk environment. Programs nearly always use either DOS or ROM BIOS functions for disk drive access. It is rare for software to attempt to access hard disk controller hardware directly. If a program does require SCSI disk controller hardware access, it must conform to the Adaptec AIC6x60 conventions.

Utilities for SCSI drive formatting, and other SCSI functions are included on the Ampro Common Utilities diskette. These are described in the Ampro Common Utilities manual.

3.5.1 SCSI Drive Parameter Setup

Several SCSI drive parameters need to be set in the configuration memory using SETUP.

- **SCSI/BIOS Services**—To use the SCSI BIOS for hard disks, it must be enabled. When disabled, the system will not boot from an attached drive, nor will standard disk-related BIOS calls (INT13) be able to see a drive. SCSI services are still available from BIOS calls in your program, even when SCSI/BIOS Services is disabled. Disabling the SCSI BIOS services will speed up system booting when you don't use the SCSI port.

- **SCSI Initiator ID**—The Ampro Little Board/486*i* is the *SCSI Initiator* in its transactions with SCSI target devices such as hard disk drives. Every SCSI device (target or initiator) must have a unique ID between 0 and 7. The default ID for the SCSI controller on the Little Board/*486i* is **7**. It is the highest priority ID, and this ID tells the SCSI BIOS to reset the SCSI bus on system powerup or reset.

- **SCSI Disk I/O Retries**—You can specify the number of read/write retries when using SCSI drives as DOS drives.

- **SCSI Disk Map: Target Device IDs and LUNs**—The specification of SCSI target device IDs and Logical Unit Numbers (LUNs) are stored in the configuration memory. Enter the IDs and LUNs of the SCSI drives you have installed in your system. Assign each drive to a SCSI Disk position in the SCSI Disk Map. Normally, you set the LUN to 0.

  The SCSI ID for target devices can be 0 to 6 (since the CPU is set for ID 7). A device's ID is usually set by jumpers or switches on the device. If you have multiple SCSI drives, assign each one a separate device ID.

- **BOOT Device Specification**—You can choose to boot the system from a hard or floppy drive using the Default Boot Device parameter. You can specify Floppy for floppy A: or Hard Disk for drive C:. (When you select Hard Disk, the drive shown as 1st Hard Disk on the DOS Disk Map becomes the boot drive.)

- **DOS Disk Map**—Assign your disk drives, both IDE drives and SCSI drives, to positions on the DOS Disk Map. You can assign them in any order and in any mix. The 1st Hard Disk becomes drive C:, 2nd Hard Disk becomes drive D:, and so on. Configure any non-SCSI device that will appear to the system as a drive (C:, D:, etc.) as an *IDE* drive.

Note

SETUP screen 1, "Standard (CMOS) SETUP" is used for defining hard drives connected to the IDE interface. Do not attempt to use the IDE configuration menu to define disk drive parameters for SCSI-connected drives.

3.6 SETUP PAGE 4—SERIAL CONSOLE

The ROM BIOS includes a unique set of features which allow full access to the system at any time over standard RS232 serial ports. An embedded system may take advantage of these remote access capabilities using the serial console functions in the following ways:

Serial console—Use Serial 1 or Serial 2 as a console, replacing the standard video monitor and keyboard.

Serial boot loader—Boot off Serial 1 or Serial 2 much like you would boot from a local hard disk or from a network. (This is configured on Page 2 of SETUP.)

Serial programming—Automatically update system software, such as an SSD, through Serial 1 or Serial 2. This feature allows you to write new code into a Flash device installed in a byte-wide socket. It also provides a means of upgrading the ROM BIOS itself.

For more information about these serial console functions, see "Serial Console Features," under "Serial Ports", later in this chapter. For a thorough explanation of the serial console features, refer to Ampro Application Note AAN-9403.

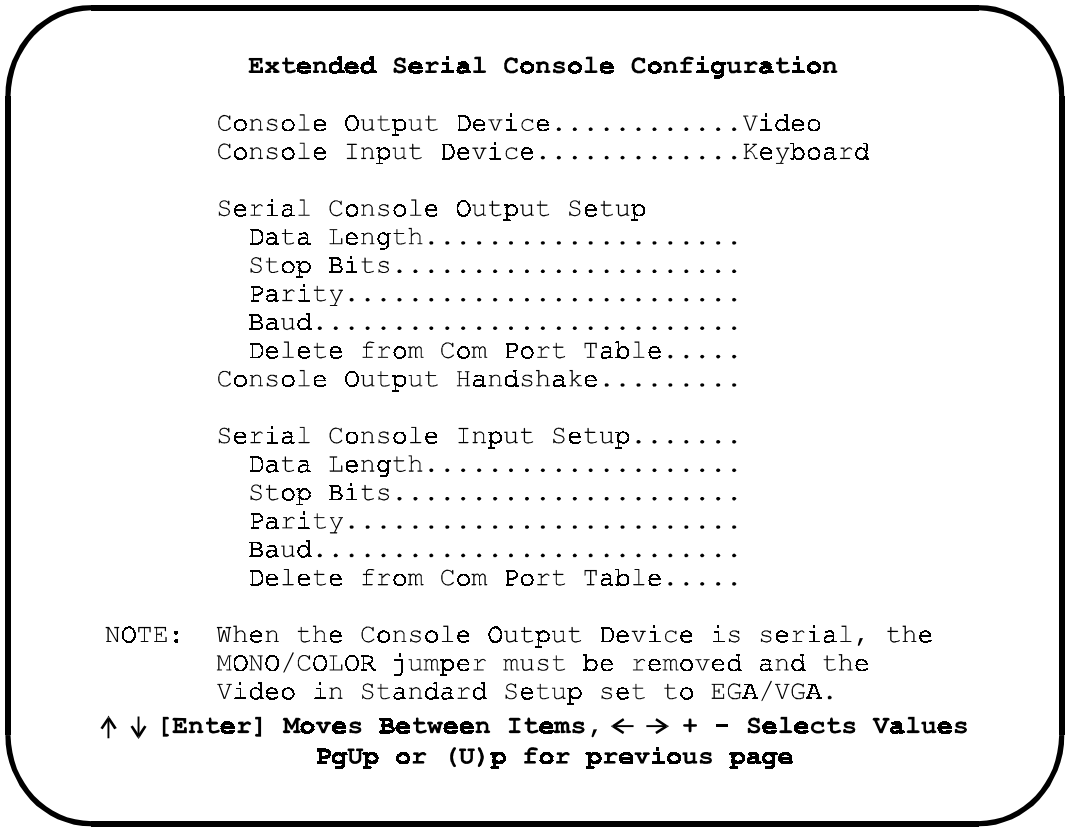


Figure 3-4 SETUP Page 4

Console Output Device—Select the console output device, either Video, Serial 1, Serial 2, or None.

Console Input Device—Select the console input device, either the PC Keyboard, Serial 1, Serial 2, or None.

Serial Console Output Setup—Enter the communication parameters for your console *output* serial port. Set the data length, stop bits, parity, and baud rate to match your serial output device.

Console Output Handshake—Enable or disable hardware handshaking. If enabled, the DSR and CTS signals control the data flow. Be sure to connect the DSR and CTS signals on the serial port's connector to the appropriate handshake signals on the external serial device's interface connector.

Serial Console Input Setup—Enter the communication parameters for your console *input* serial port. Set the data length, stop bits, parity, and baud rate to match your serial input device.

Delete from COM Port Table—When DOS boots, it initializes the system serial ports. (Different versions of DOS may set the ports to different default settings.) By enabling this option, the BIOS does not include your console serial device(s) in the COM port table. This prevents DOS from changing the values you assign to the port in this SETUP screen.

Caution

Be careful when changing the console configuration. If you specify "None" for console input and output, there will be no console access to the system. (You can recover from this state by removing the serial console plug from the primary serial port connector and shorting pins J11-7/8.)

3.7 THE SETUP.COM PROGRAM

You can use the SETUP.COM utility from the command line to access the same SETUP function as the "hot key" code, CTRL-ALT-ESC. In addition, SETUP.COM also adds additional functionality, such as the ability to load and store configuration settings to a disk file. This same feature is used to store up to 512 bits of OEM information in the configuration memory EEPROM. SETUP.COM is on the Ampro Common Utilities diskette, included with the Little Board/486*i* Development Kit.

3.7.1 Creating Configuration Files with SETUP.COM

The Ampro SETUP utility, SETUP.COM, offers the following options for command line entry:

```
SETUP [-switches]  [ @file.ext  |  Wfile.ext ]
```

The supported switches and their meaning are as follows:

Switch	Function
?	Display a usage help screen
T	Set the (hardware) real-time clock time and date from the current DOS time and date.
@*file.ext*	Writes the specified file to the board's CMOS RAM and configuration EEPROM. Drive and path are optional in the file name.
W*file.ext*	Write CMOS RAM and EEPROM contents to the file specified. The file name may contain an optional drive and path.

Table 3-5 SETUP.COM Command Switches

You can save a copy of the current contents of the board's configuration memory to a disk file by using the W switch. The data saved includes the entire contents of the nonvolatile configuration EEPROM. The first 512 bits are the SETUP information (excluding time and date), the next 512 bits are available for OEM storage. See Ampro Application Note AAN-8805 for a description of how to use the OEM storage portion of the EEPROM.

The file you create with this menu option can be used as a source for programming the configuration memory of a Little Board/486*i* at a later time.

As an example, the following command initializes the EEPROM values with a previously saved configuration:

```
C>SETUP  @SYSTEM.A
```

Assuming you created the file SYSTEM.A with SETUP's write option, SETUP will initialize the EEPROM configuration memory using the contents of SYSTEM.A.

Using SETUP with the write and read parameters can be useful when many boards must be initialized automatically, or when you want to change between several predefined system configurations.

3.8 OPERATION WITH DOS

The Little Board/486*i* supports IBM's PC-DOS or Microsoft's MS-DOS, Version 3.3 or later, or any version of Digital Research's DR DOS as the disk operating system. Any differences between these similar operating systems are noted in the text where applicable.

Caution

Sometimes MS-DOS is customized by a manufacturer for a specific system and may not work on the Little Board/486*i*. Use DR DOS (supplied by Ampro), IBM PC-DOS (supplied by IBM), or the generic version of MS-DOS (supplied by Microsoft on an OEM basis).

EMS Option—The Little Board/486*i* can emulate the Lotus-Intel-Microsoft Expanded Memory Specification Version 4.0 (LIM EMS 4.0), with the memory management capability of the 80486DX2/4 CPU, under control of a device driver. Such drivers are available with the newer versions of DOS. With Microsoft MS-DOS, the driver is called EMM386.EXE.

Serial Ports—DOS normally supports the board's four serial ports as COM1, COM2, COM3, and COM4.

At boot time, DOS initializes the serial ports, assigning them their COM port designations and their communication parameter settings. Although this might vary with different types and versions of DOS, typical communication parameter settings are 2400 baud, even parity, 7 bits, and 1 stop bit.

Usually an application program that uses a serial port will access the port's hardware and reinitialize the communication parameters to other values, based on settings that the user has entered when configuring the application program.

Parallel Port—The Parallel Printer port is normally the DOS LPT1 device. Most application software uses LPT1 as the default printer port. If you enable the port, printing to it is automatic.

The following DOS commands can be used to test printing with the parallel printer:

`A>COPY CONFIG.SYS LPT1`	Prints contents of CONFIG.SYS
`A>DIR >LPT1`	Prints the directory

In addition, the <PrtSc> (Print Screen) key will print the contents of the video screen to the LPT1 device. Also, you can use the Printer Echo function to print all characters typed on the keyboard. The command <Ctrl-P> enables the Printer Echo function. Entering <Ctrl-P> again disables Printer Echo.

Disk Drives—Older versions of DOS require you to divide disk drives larger than 32M bytes into more than one partition. More recent versions permit drives to be up to 2G bytes, though IDE drives are BIOS limited to 512M bytes. Larger IDE drives typically provide a driver to get around the BIOS limit.

3.9 SERIAL PORTS

The four serial ports on the Little Board/486*i* are standard PC-compatible ports based on the 16550-class UART controller. This device provides increased performance by utilizing a 16-byte FIFO memory.

3.9.1 Interrupt Sharing

Having four serial ports reveals a weakness in the standard PC architecture. Namely, if you require all four ports to use interrupts, you must determine how to deal with the interrupts for the third and fourth serial ports. Normally, Serial 3 attaches to IRQ4 and Serial 4 attaches to IRQ3, but, since interrupts are not normally a sharable resource, you could do this only if you enabled and disabled the conflicting interrupt lines, a less than ideal solution.

Ampro provides two solutions to this problem, selectable with jumper options. If you want to assign different interrupts to Serial 3 and Serial 4, you can use jumpers to assign IRQ12 to Serial 3 and IRQ10 to Serial 4. As an alternative, you can jumper the ports to participate in true interrupt sharing. That is, Serial 1 and Serial 3 share IRQ4 and Serial 2 and Serial 4 share IRQ3. This is accomplished by circuitry that connects the interrupt lines from each port in a wired-OR arrangement.

Interrupt ORing allows true interrupt sharing, because it assures that an interrupt is detected as soon as any device requests it. It is then necessary only to determine which of the devices sharing the common interrupt assignment produced the interrupt request. This can be accomplished by simple device status read operations.

3.9.2 Sample Code for Interrupt Sharing

The following assembly language code is an example of software that supports the wired-OR approach to interrupt sharing. In the code sample shown, Serial 1 and Serial 3, located at hardware addresses 03F8h and 03E8h, respectively, have both been assigned to interrupt IRQ4. The interrupt line will be activated whenever either of the serial ports contain a new byte of received data. When an interrupt is detected on IRQ4, the interrupt service routine reads the status register of each serial port to determine whether that port caused the interrupt (is holding a byte of received data). If data is present, it is read from that port and written to the other port. After both ports have been serviced in this manner, the interrupt is cleared. Then both ports are interrogated again. This second set of status reads covers the case in which a new byte of data arrives while the first set of status reads are taking place, before the interrupt is cleared. This assures that all the received bytes will be read.

```
INTR  EQU  20H          ; 8259 interrupt controller is 20h,21h
INTR1 EQU  INTR+1
;
;  ************ INTERRUPT SERVICE ROUTINE ************
;
SerInt:
  PUSH AX
  PUSH DX
  MOV DX,CS:IFl1
  IN AL,DX
  AND AL,1             ; see if data received
  JNZ NIn1
In1:
  SUB DX,2             ; point to data register
  IN AL,DX             ; read data in
  MOV DX,CS:Ser1
  OUT DX,AL            ; write data to other port
NIn1:
  MOV DX,CS:IFl3
  IN AL,DX
  AND AL,1             ; see if data received
  JNZ NIn2
In2:
  SUB DX,2             ;point to data register
  IN AL,DX             ;read data in
  MOV DX,CS:Ser3
  OUT DX,AL            ;write data to other port
Nin2:
  MOV AL,64H           ;clear IRQ4 to enable new interrupt
  OUT INTR,AL
  MOV DX,CS:IFl1
  IN AL,DX
  AND AL,1             ;see if data received
  JZIn1
Ninb1:
  MOV DX,CS:IFl3
  IN AL,DX;
```

```
  AND AL,1              ;see if data received
  JZ In2
  POP DX
  POP AX
  IRET
;
;  *********INTERRUPT INITIALIZATION ROUTINE*********
;
  MOV DX,OFFSET SerInt
  MOV AL,0Ch            ;set the vector for IRQ4
  PUSH DS
  PUSH CS
  POP DS
; set the vector for INT13 using a DOS function call
  MOV AH,25h            ;set the interrupt vector in AL
  INT 21h               ;the vector is in DS:DX
;
  POP DS                ;restoreDS
  IN AL,INTR1
  AND AL,0EFh           ;unmask IRQ4
  OUT INTR1,AL
  MOV AL,64h            ;clear interrupt 4 flag
  OUT INTR,AL
;
;  ****************PORT ADDRESS TABLE****************
;
Ser3  DW    3E8h        ;base address of Serial 3
Ser1  DW    3F8h        ;base address of Serial 1
;
Ifl3  DW    3eah        ;status register of Serial 3
Ifl1  DW    3fah        ;status register of Serial 1
;
```

3.9.3 Serial Console Features

To use the serial console features, connect the serial console device(s) to Serial 1 or Serial 2. Use SETUP to configure the Little Board/486*i* to use its serial console support feature. The configuration memory stores serial console support parameters.

Caution

Be careful when changing the console configuration using SETUP. If you specify "None" for console input and output, there will be no console access to the system. (You can recover from this state by removing the serial console plug from the primary serial port connector and shorting pins 7/8.)

SETUP provides separate configurations for serial console input and output. Thus, you can use a serial port (and attached serial device) for either or both input and output. For instance, you can use a modem or

other serial device for input, and a standard video display for output. Or you can use a standard keyboard with a serial display, or use a standard ASCII terminal for both input and output.

To use an ASCII terminal as the console device for your system, set both the input and output parameters to Serial Port 1 (or 2), and set the serial baud rate, data length, and stop bits to match the setting of your terminal. For proper display of SETUP and POST messages from the BIOS, you must use IEEE-compatible terminals that implement certain cursor commands. The required commands and their hexadecimal codes are given in Table 3-6.

Hex	Command
08	Backspace
0A	Line Feed
0B	Vertical Tab
0C	Non-destructive Space
0D	Carriage Return

Table 3-6 Required Commands

Note

Some modem programs that emulate an ASCII terminal do not properly support the basic ASCII command functions shown in Table 3-6. If you have problems, try using TVTERM, provided by Ampro on the Common Utilities diskette.

After booting this system, the keyboard and screen of the terminal become the system console. The programs you use this way must use ROM BIOS video functions (rather than direct screen addressing) for their display I/O. You can enter keyboard data from both the external serial device and the standard AT keyboard.

Note

DOS programs that write directly to video RAM will not display properly on a serial console device.

COM Port Table

When the system boots DOS, it initializes the serial ports to 2400 baud (typical). To preserve the serial port parameters stored in SETUP, the ROM BIOS deletes the console port(s) from the internal COM port table, normally used by DOS to locate the serial ports. With the port(s) deleted from the COM port table, DOS cannot change the parameters entered in SETUP for the serial console. If you use a serial console, be sure to select the option that deletes the console ports from the COM port table.

Serial Handshake

The serial console device data format and the Little Board/486*i* serial port data format must match for the devices to properly communicate. In addition, the hardware handshake behavior must be compatible. Normally, a serial port's Data Set Ready (DSR) and Clear To Send (CTS) input handshake signals must be true (active) for the ROM BIOS to send data out. On the Little Board/486*i*, the hardware handshake can be enabled or disabled with SETUP. When hardware handshaking is enabled, be sure to connect the DSR and CTS signals to appropriate handshake signals on the external serial device's interface connector. As an alternative, loop the Little Board/486*i*'s serial output handshake signals to its input signals as follows:

- DTR (out) to DSR (in)
- RTS (out) to CTS (in)

3.9.4 Serial Booting and Serial Programming

Serial console functionality has been expanded to incorporate two additional features useful in embedded applications. The *serial boot* facility enables the Little Board/486*i* to boot from code downloaded through a serial port in a manner similar to booting from a local hard disk or from a network. The *serial programming* facility permits updating Flash memory devices installed in the byte-wide sockets over the serial port. Refer to Ampro Application Note AAN-9403 for a complete description of these features. Refer to the Ampro Common Utilities manual for descriptions of SERLOAD and SERPROG, utility programs used to support serial booting and serial programming.

3.9.5 Using a Serial Modem

You can use any of the RS232C ports as a modem interface. You will not need to concern yourself with serial port initialization since most PC communications programs control the serial port hardware directly. If your program does not do this, use the DOS MODE command to initialize the port.

When installing a modem, be sure to connect appropriate input and output handshake signals, depending on what your communications software requires. Standard PC-compatible serial modem cables that connect all of the proper signals correctly are commonly available. The signal arrangement on the serial port connectors is described in Chapter 2.

Many powerful communications programs are available to control modem communications. Some of these programs offer powerful "script" languages that allow you to generate complex automatically functioning applications with little effort.

3.10 MULTIMODE PARALLEL PORT

The enhanced parallel printer port is a superset of the standard PC-compatible printer port. It supports four modes of operation:

- **Standard PC/AT printer port**—Centronics-type output only printer port, compatible with the original IBM PC printer port.
- **Bi-directional parallel port**—Sometimes called a PS/2-compatible parallel port. It behaves the same as the standard PC/AT port on outputs, and provides an input mode as well.
- **Enhanced Parallel Port (EPP)**—Bi-directional parallel port, compatible with the Standard and PS/2 ports, and adding automatic read- and write-cycle modes. Automatically generates input and output

handshaking signals for increased throughput. Data flow is monitored by a watchdog timer (separate from the board's watchdog timer) to ensure reliable transfers.

- **Extended Capabilities Parallel Port (ECP)**—Compliant with the IEEE 1284 Extended Capabilities Port Protocol and ISA Standard (Rev 1.09, January 7, 1993), developed by Microsoft. The ECP mode provides the highest level throughput for the parallel port. It provides interlocking handshaking, a 16-byte FIFO buffer, DMA transfers (optional), hardware RLE data compression (optional), and well-defined software protocols.

The low-level software interface to the parallel port consists of eight addressable registers. The address map of these registers is shown in the following table:

Register Name	Address
Data Port	Base address
Status Port	Base address + 1
Control Port	Base address + 2
EPP Address Port	Base address + 3
EPP Data Port 0	Base address + 4
EPP Data Port 1	Base address + 5
EPP Data Port 2	Base address + 6
EPP Data Port 3	Base address + 7
Note: EPP registers are only accessible when in EPP mode	

Table 3-7 Parallel Port Register Map

3.10.1 Standard and Bi-Directional Operation

You can use the parallel port as a standard output-only printer port or as a bi-directional data port with up to 12 output lines and 17 input lines. The bi-directional mode can be very valuable in custom applications. For example, you might use it to control an LCD display, scan keyboards, sense switches, or interface with optically isolated I/O modules. All data and interface control signals are TTL-compatible.

The default mode of the port is output only. To use the port as a bi-directional data port you must put it in bi-directional mode with a BIOS call. For example:

```
;-------------------------------------------------------
; Code to set the parallel port mode
;-------------------------------------------------------
MOV   AH,0CDh     ; AMPRO command
MOV   AL,0Ch      ; AMPRO function
MOV   BX,01h      ; Extended mode (00 for output-only mode)
INT   13h
```

This code leaves the port in input mode. Once the port is in bi-directional mode, you can directly access the control register without using the BIOS. The port address is 37Ah for LPT1 and 27Ah for LPT2. You can dynamically change the port between input and output modes by changing bit 5. A 1 in bit five sets

the port to input only; a 0 sets it to output only. Here is a sample of code for dynamically changing the port direction after it is in Extended Mode.

```
;-------------------------------------------------------
; Code to change the parallel port direction to input
;-------------------------------------------------------
MOV   DX,37Ah          ;(27Ah for LPT2)
IN    AL,DX
OR    AL,20h                ;set bit 5
OUT   DX,AL
;
;-------------------------------------------------------
; Code to change the parallel port direction to output
;-------------------------------------------------------
MOV   DX,37Ah          ;(27Ah for LPT2)
IN    AL,DX
AND   AL,0DFh          ;clear bit 5
OUT   DX,AL
```

Besides the eight data lines, you can use the four control lines (-STROBE, -AUTOFD, -INIT, and -SEL IN) as general purpose output lines. Similarly, you can use the five status lines (-ERROR, SEL OUT, PAPER EMPTY, -ACK, and BUSY) as general purpose input lines.

You can read the four control lines and use them as input lines. These lines have open collector drivers with 4.7K ohm pullups. To use a control line as an input line, you must first write to its corresponding bit in the control register. Refer to Table 3-9. If the line is inverting, write a 0, otherwise write a 1. This will cause the line to float (pulled up by the 4.7K ohm resistors). When they float, you can use them as inputs. Table 3-8 is a summary of the uses of the parallel port lines.

Signal Type	Number of Lines	Function	Output Drive
Data	8 lines	Read/Write	24 mA @ .5V 12 mA @ 2.4V
Control	4 lines	Read/Write*	24 mA @.5V 4.7K PU
Status	5 lines	Read Only	--

* Open collector control lines convert to TTL outputs in PS/2 and EPP/ECP modes. Output under those conditions is 4 mA @ 2.4V

Table 3-8 Parallel Port Use

Bit 4 in the control register (Table 3-9) enables the parallel port interrupt. If this bit is high 1, then a rising edge on the -ACK (IRQ) line will produce an interrupt on the interrupt selected by W24, either IRQ5 or IRQ7.

Register	Bit	Signal Name or Function	In/Out	Active High/Low	J15 Pin	DB25F Pin
DATA	0	Data 0	I/O	High	3	2
(378h)	1	Data 1	I/O	High	5	3
(278h)	2	Data 2	I/O	High	7	4
	3	Data 3	I/O	High	9	5
	4	Data 4	I/O	High	11	6
	5	Data 5	I/O	High	13	7
	6	Data 6	I/O	High	15	8
	7	Data 7	I/O	High	17	9
STATUS	0	TMOUT	In	---	---	---
(379h)	1	0	---	---	---	---
(279h)	2	0	---	---	---	---
	3	-ERROR	In	Low	4	15
	4	SLCT	In	High	25	13
	5	PE	In	High	23	12
	6	-ACK (IRQ)	In	Low	19	10
	7	BUSY	In	High	21	11
CONTROL	0	-STROBE	Out*	Low	1	1
(37Ah)	1	-AUTOFD	Out*	Low	2	14
(27Ah)	2	-INIT	Out*	High	6	16
	3	SLC	Out*	High	8	17
	4	IRQE	---	High	---	---
	5	PCD	---	High	---	---
	6	1	---	---	---	---
	7	1	---	---	---	---
* Can also be used as input (see text).						

Table 3-9 Parallel Port Register Bits

Register Bit Definitions:

Signal Name	Full Name	Description
TMOUT	Timeout	Valid only in EPP mode , this signal goes true after a 10 uS time-out has occurred on the EPP bus. This bit is cleared by reset.
-ERR	Error	Reflects the status of the -ERROR input. 0 means an error has occurred.
SLCT	Printer selected status	Reflects the status of the SLCT input. 1 means a printer is on-line.
PE	Paper end	Reflects the status of the PE input. 1 indicates paper end.
-ACK	Acknowledge	Reflects the status of the ACK input. 0 indicates a printer received a character..
-BUSY	Busy	Reflects the complement of the BUSY input. 0 indicates a printer is busy.
STROBE	Strobe	This bit is inverted and output to the -STROBE pin.
AUTOFD	Auto feed	This bit is inverted and output to the -AUTOFD pin.
-INIT	Initiate output	This bit is output to the -INIT pin.
SLC	Printer select input	This bit is inverted and output to the pin. It selects a printer.
IRQE	Interrupt request enable	When set to 1, interrupts are enabled. An interrupt is generated by the positive-going -ACK input.
PCD	Parallel control direction	When set to 1, port is in input mode. In printer mode, the printer is always in output mode regardless of the state of this bit.
PD0-PD7	Parallel Data Bits	

Table 3-10 Standard and PS/2 Mode Register Bit Definitions

3.10.2 EPP and ECP Operation

The board's parallel port is compliant with the IEEE 1284 Extended Capabilities Port Protocol and ISA Standard (Rev 1.09, January 7, 1993), developed by Microsoft. Contact IEEE Customer Service and request IEEE Std 1284 for information about EPP and ECP operation.

IEEE Customer Service
445 Hoes Lane
PO Box 1331
Piscataway, NJ 08855-1331 USA

Phone: (800) 678-IEEE (in the US and Canada)
(908) 981-0060 (outside the US and Canada)
FAX: (908) 981-9667
Telex: 833233

3.11 BYTE-WIDE SOCKETS

The two 32-pin byte-wide memory sockets at S0 and S1 support a variety of 28- and 32-pin JEDEC pinout memory devices, including EPROM, Flash EPROM, and SRAM. You can configure one socket, S0, to supply backup battery power to convert an SRAM into a Non-Volatile RAM (NOVRAM). Chapter 2 gives examples of the memory devices each socket will support.

Ampro's solid state disk (SSD) drive support in the ROM BIOS and optional SSD Support Software treat these sockets as one or more DOS disk devices, containing up to 1M byte of storage each. The sockets are highly configurable with jumpers to accept nearly any common JEDEC byte-wide device. Instructions on how to configure the byte-wide sockets for common devices are in Chapter 2.

The BIOS accesses the byte-wide sockets as 8-bit devices on the PC expansion bus. If the sockets are configured to non-overlapping address spaces, both sockets can remain enabled at the same time. If they overlap, your program must manually enable and disable the sockets to access both devices. Use SETUP to configure how the byte-wide sockets appear in memory. Refer to the SETUP section earlier in this chapter for details.

If you install a smaller device than specified in SETUP, (for example, a 32K byte component in a 64K window) the device will appear at multiple addresses in the socket's address window.

The byte-wide sockets can be disabled by the ROM BIOS at powerup and boot time via an option in the configuration memory. Additionally, the sockets can be enabled or disabled under software control, using a ROM BIOS call provided for this purpose (see the code example below). When you disable a byte-wide socket (with SETUP or the BIOS call), its address space is available on the expansion bus. When you enable a socket, its address space is not available on the bus, even if there is no memory device installed in the socket.

Devices used in the byte-wide sockets must have access times of 250 nS or less.

3.11.1 Accessing Large Devices

For devices over 64K bytes, select the 64K byte window size in SETUP. You must then select which segment of the device you want to appear in that window, using code equivalent to that illustrated below. Table 3-11 gives the byte (in hex) to write to the BH register to select each segment of a large device. Here is a simple assembly language routine that controls the byte-wide memory sockets. The segment byte is given in binary.

```
;-------------------------------------------------------
; Page select code for byte-wide sockets
;-------------------------------------------------------
MOV   AH,0CDH          ; AMPRO function call
MOV   AL,nn            ; Use 03 for S0, 04 for S1
MOV   BL,nn            ; Use 01 to turn ON or 00 to turn OFF
MOV   BH,x0h           ; The upper nibble of BH contains the page
                       ; number for devices larger than 64 K.
INT   13H
```

Device Size	64KB Segments	Segment Address (Upper Nibble of BH)
128K	2	FIRST BH=00h SECOND BH=10h
256K	4	FIRST BH=00h SECOND BH=10h THIRD BH=20h FOURTH BH=30h
512K	8	FIRST BH=00h SECOND BH=10h THIRD BH=20h FOURTH BH=30h FIFTH BH=40h SIXTH BH=50h SEVENTH BH=60h EIGHTH BH=70h
1M	16	FIRST BH=00h SECOND BH=10h THIRD BH=20h FOURTH BH=30h FIFTH BH=40h SIXTH BH=50h SEVENTH BH=60h EIGHTH BH=70h NINTH BH=80h TENTH BH=90h ELEVENTH BH=A0h TWELFTH BH=B0h THIRTEENTH BH=C0h FOURTEENTH BH=D0h FIFTEENTH BH=E0h SIXTEENTH BH=F0h
NOTE: For a 128K byte window, use any of the odd numbered values (for instance, FIRST or THIRD)		

Table 3-11 Segment Addressing in Large Memory Devices

3.11.2 Byte-Wide Socket Signals

Jumper arrays W14 (for S0), W15 (for S1) configure the byte-wide sockets for specific memory devices. In addition, jumpers W2, W21, control backup battery to S0 for use with SRAMs.

The following table list the signals that appear on the pins of W14 and W15.

W14/W15 Pin	Signal Name	Description
1	--	No connection
2	Vpp	Programming power for Flash devices
3	--	No connection
4	A18	Address A18 (static)
5	Pin 3	Connection to pin 3 of the byte-wide socket
6	A19	Address A19 (static)
7	Pin 33	Connection to pin 33 of the byte-wide socket
8	-SMEMR	Write strobe
9	Pin 31	Connection to pin 31 of the byte-wide socket
10	A15	Address SA15 from the expansion bus
11	Pin 5	Connection to pin 5 of the byte-wide socket
12	A14	Address SA14 from the expansion bus
13	A17	Address A17 (static)
14	Pin 32	Connection to pin 32 of the byte-wide socket
15	Vcc or backup battery	Connected to the center pin of W21. W21-1 connects to the backup battery; W21-3 connects to +5V.

Table 3-12 Byte-Wide Jumper Pin Signals (W14, W15)

3.11.3 Flash EPROM Programming

To program Flash devices, use the FLASHWRI utility supplied on the Common Utilities diskette. The Common Utilities manual describes its operation.

Programming power is handled automatically for both 5V and 12V Flash devices. The board provides 12V power for programming 12V Flash EPROMs. There are no jumpers to set, as the onboard 12V Flash programming supply is controlled by software.

Note that there is a 5 mS delay for the 12V Flash programming supply to come up to its full voltage after being switched on by software. Refer to Ampro Application Note AAN-9210 for information about the extended BIOS call provided for Flash programming power control.

3.11.4 Battery Backup for SRAMs

To connect the onboard battery (and external battery, if installed on J16) to byte-wide socket S0 to backup an SRAM, install jumpers on W2 and W21-1/2. Read the section “Backup Battery” in Chapter 2 to calculate the battery life of the backup battery.

3.12 SCSI CONTROLLER

The SCSI controller can serve many purposes, including controlling hard disk drives, tape drives, text scanners, and printer and communications servers. The ROM BIOS supports booting DOS from a SCSI device such as a hard disk. With Ampro's ROM BIOS support, you can use any device compatible with the SCSI Common Command Set for "direct access devices."

The Little Board/486*i* Development Kit comes with a diskette containing an assortment of SCSI utilities for use with DOS. It includes a SCSI hard disk formatting utility that allows low-level formatting and changing the disk interleaving. Refer to the Ampro Utilities manual for details about using the SCSI utilities.

Older versions of PC-DOS, for instance Version 3.x, requires you to divide drives larger than 32M bytes into multiple partitions. Under PC-DOS or MS-DOS 3.x, you can logically divide each drive into as many as four partitions of 32 megabytes each or smaller, allowing you to use drives as large as 128 megabytes. More recent versions of MS-DOS remove these restrictions. The Ampro SCSI Common Command Set implementation puts no realistic limit on drive size (1.8T bytes).

Besides direct access, SCSI devices include sequential access devices (tape), printer devices, read-only devices (CD-ROM), and processor devices (CPUs). These device types require special application programs, utilities, or driver software not included on the Ampro Utility diskette.

Hard disk support for operating systems other than DOS may or may not be available through the ROM BIOS hard disk driver. This depends on two things: whether the operating system in question uses ROM-BIOS calls exclusively for the hard disk function; and whether the operating system has any special ROM BIOS constraints, such as reentrancy. Some operating systems—multitasking ones in particular such as UNIX—bypass the BIOS and attempt to program the hard disk controller directly. With such systems, you must modify the operating system to add an appropriate SCSI hard disk driver that can take advantage of the SCSI interface. An alternative is to use the IDE interface instead of SCSI, as the IDE drive standard is more widely supported.

3.12.1 The Ampro SCSI BIOS

You can use a variety of mass storage devices with the SCSI universal bus interface and command protocols. Ampro has added a further layer of universality, the SCSI BIOS.

The SCSI BIOS, a set of low level functions in the ROM BIOS, is a hardware-independent interface between system software and SCSI peripherals. The advantage of the Ampro SCSI BIOS is in interfacing to devices. Programmers can write software for SCSI devices without concern for the operational details of the SCSI interface. Also, the SCSI BIOS enables you to import software from other environments more safely, quickly, and easily.

Application Note AAN-8804, available from Ampro, provides details of the SCSI BIOS functions.

3.12.2 SCSI Drive Preparation for DOS Use

To use a hard disk drive on the SCSI port, you must properly connect and jumper it, set the appropriate parameters in SETUP, and then format the drive for use with DOS.

Here is a procedure you can use to prepare (format and partition) a SCSI hard disk drive for use with DOS:

1. **Set the SCSI Device IDs**—using the options in SETUP's Extended SCSI and Hard Disk Configuration menu, specify the appropriate SCSI device IDs for both the drive and the Little Board/486*i*. This ID must match jumpers on the drive. If you set the SCSI controller on the CPU board to SCSI ID 7, a SCSI bus Reset command will be issued on system powerup or system reset.

Typically, SCSI drives come preset to SCSI ID 0, LUN 0. The "SCSI Initiator ID" option sets the CPU board's SCSI Initiator ID. The SCSI Disk Map options are used to specify the ID and LUN of up to seven SCSI drives. DOS Disk Map options assign SCSI devices as DOS drives. For example, in a system with one SCSI drive, set SCSI Initiator to 7, SCSI Disk 1 to Id 0, LUN 0, and 1st Hard Disk to SCSI Disk 1.

2. **Drive Partitioning**—Reboot the system from a floppy diskette in drive A: containing the operating system, and run the DOS FDISK utility as described in your DOS documentation. You may be creating one or multiple partitions, depending on the size of the drive and the partition limitations of the particular DOS you are using.

3. **Final Preparation for System Access**—Again, reboot the system from a floppy diskette in drive A:. What you do next depends on which operating system you use.

   DR DOS—Run the DOS SYS command to copy the operating system to the hard disk drive(s) that you have created in the above steps. Finally, copy anything else you need to the drive(s), and then reboot the system without the floppy diskette in drive A: to verify that you have installed everything properly.

   PC-DOS or MS-DOS—Use the FORMAT /S command to copy the operating system to the DOS boot drive (drive C:); or the FORMAT command for drives or drive partitions other than the DOS boot partition. Finally, copy anything else you need to the drive(s), and then reboot the system without the floppy diskette in drive A: to verify that you have installed everything properly.

3.13 ETHERNET LAN INTERFACE

This section discusses the hardware and software considerations when setting up a network using the Ethernet LAN interface.

Should you need further information on Ethernet standards, you may contact IEEE Customer Service:

IEEE Customer Service
445 Hoes Lane
PO Box 1331
Piscataway, NJ 08855-1331 USA

Phone: (800) 678-IEEE (in the US and Canada)
(908) 981-0060 (outside the US and Canada)

FAX: (908) 981-9667

Telex: 833233

3.13.1 Network Terms

The following are some of the terms used in this section:

- **Trunk or network segment**—The cable over which network stations communicate. A segment cable is usually made up of several cable lengths connected together. A segment is limited in its total length and the number of network stations it can support. However, a network is not limited to one segment.

- **Network trunk —**The sum of all the segment cables. Several segments can be interconnected with repeaters, routers, or bridges to form the network trunk cable.

- **Repeater**, **router**, **or bridge**—Devices that extend the size of a network beyond the limitations of one segment. These devices not only form a pathway for network signals traveling from one trunk segment to another; they also regenerate and strengthen network signals.
- **Station**—Any device that is connected to a network by means of a network interface card (such as the Little Board/486*i*).
- **Node**—Another term for a network station. Each node has its own network interface card.
- **Attachment Unit Interface**—(AUI) One of the standard interfaces used to connect a node to the net, often used between a network interface card and a hub or concentrator.

3.13.2 Twisted-Pair Installations

This section discusses the guidelines for twisted-pair installations.

Cables and Connectors

- **Connector jack**—You can plug a standard RJ45-terminated cable directly to the female RJ45 connector on the Little Board/486*i*.
- **Connector plug**—The RJ45 connector plugs, attached to both ends of twisted-pair Ethernet cable lengths, are used to connect the Little Board/486*i* to a hub or concentrator.
- **Terminators**—There are no external termination devices required. Termination is handled automatically by the hub devices.

Twisted-pair Ethernet cable is 22 or 24 gauge copper wire twisted together in pairs. Ethernet twisted-pair uses two pairs (four wires), one for transmit, one for receive. It is available from many industry suppliers. Standard RJ45 connectors are used for all connections in a twisted-pair cable network.

Twisted-pair Ethernet cables must be 100 meters or less between any node and hub or repeater.

3.13.3 AUI Installations

This section discusses the guidelines for installations that use the AUI port for connection to an external transceiver device.

You can connect the Little Board/486*i* to a LAN through the standard Adapter Unit Interface (AUI) connection. The AUI connects to an external device such as a hub or concentrator, or MAU. The AUI enables you to connect your node to fiber optic, thick net cable, or other Ethernet media via an external transceiver.

Cables and Connectors

The AUI interface consists of a 10-pin ribbon cable connector. You can attach an optional transition cable (available from Ampro) consisting of a female 10-pin ribbon cable connector on one end and a female DB-15 on the other.

3.13.4 Using Network Operating Systems

The most common method of using the Little Board/486*i* Ethernet LAN interface is by means of a "network operating system." In some cases the network operating system is part of the computer's operating system. In other cases (as with DOS and Windows 3.1) the network operating system is provided separately. One example of a network operating system for DOS is Novell's Netware, which supports server-client communications. That is to say, a central computer that runs Netware as its network operating system provides file server and network services to the distributed systems connected to the LAN. Each node on the network must also have a compatible network operating system installed .

Modern network architectures are based on the OSI model which defines layers of software between the network hardware, the network operating system, and the applications that use the network services. At the "bottom" level is the actual Ethernet cable and the hardware interface, in this case, the Little Board/486*i* LAN interface. A driver is used to talk directly with the hardware, masking any unique differences in the hardware from the layers above it, including the network operating systems. Several network operating system drivers compatible with the Little Board/486*i*'s LAN hardware are provided on the Utilities diskette that is included with Little Board/486*i* Development Kit. New drivers or new versions of existing drivers are made available on Ampro's Technical Support bulletin board. The driver is the only unique software needed to use the LAN interface. The supported network operating systems provide the other layers in the OSI model.

3.13.5 Network OS Drivers

The following Ethernet drivers are provided on the Utilities diskette. The table shows what driver to use with each network operating system. For instance, if you are using Netware 4.1 on a network server, you would use the SMC9000.LAN driver.

Driver installation procedures vary from one network operating system to another. No detailed description can be given here. Follow the instructions that come with the network operating system you choose for your system.

Program Name	Vendor	Function	Driver Name
Netware 4.1 Server Driver	Novell	ODI on server	SMC9000.LAN
Netware 3.11 Server Driver	Novell	ODI on server	SMC9000.LAN
Netware 2.2 Server Driver	Novell	IPX on server	SMC9000.LAN
Netware ODI Workstation Driver	Novell	ODI on workstation	SMC9000.COM
OS/2 ODI Workstation Requester	Novell	ODI on workstation	SMC9000.SYS
Lan Manager	Microsoft	NDIS for DOS	SMC9000.DOS
Lan Manager	Microsoft	NDIS on Windows for Workgroups	SMC9000.DOS
Lan Manager	Microsoft	NDIS for Windows NT 3.1 and NT 3.5	SMC9000.SYS
Lan Manager	Microsoft	NDIS for OS/2 on server	SMC9000.OS2

Table 3-13 Ethernet Drivers

3.13.6 Controlling the Ethernet LAN Interface Directly

Of course, you can create any application or software driver to directly control the SMC Ethernet controller chip used on the Little Board/486*i*. Ampro has designed the interface to conform to the

standards and recommendations set forth by the controller chip manufacturer. To develop a custom driver, you will need detailed information on the SMC9000-series controller chip, which is available from SMC. Contact SMC at the following address:

SMC
80 Arkay Drive
Hauppauge, NY 11788

Phone: (516) 435-6000
FAX: (516) 231-6004

3.13.7 Manufacturer's Ethernet ID

Each manufacturer of Ethernet network adapters and interfaces is assigned a unique manufacturer's ID by the IEEE Standards Office. A network address consists of 48 bits. The upper 24 bits are the manufacturer's ID and the lower 24 bits are the board's unique ID.

For developers who are creating network applications, knowing the manufacturer's ID for network adapters attached to the network may or may not be important.

Ampro's 24-bit manufacturer's ID for Ethernet controllers is displayed in hex as follows:

00 40 53

Ethernet IDs are sometimes displayed by diagnostic or network analysis programs in binary format. Refer to your equipment manual for information on possible byte swapping in the display, as shown in this example.

0010 1100 1010 0000 0000 0000

3.13.8 Installing a Boot PROM

Most network interface cards provide a means for installing a boot PROM. The boot PROM code enables the node to boot from a network server, much like the BIOS boots from a local hard disk or floppy.

Boot PROM code varies from one network operating system to another. You must have boot PROM code compatible with the network operating system you select for use with the onboard LAN controller. Boot PROMs for Novell Netware, Microsoft Lan Manager, QNX, and other popular network operating systems are available from LanWorks.

Contact LanWorks at the following address for information about their “Bootware”:

LanWorks Technologies Inc.
2425 Skymark Ave.
Mississauga, Ontario, Canada
Phone: 800-808-3000
905-238-5528
FAX: 905-2238-9407
E-mail: sales@mhs.lanworks.com

Addresses and phone numbers of companies providing compatible LAN drivers:

Novell, Inc.
1640-D Berryessa Rd.
San Jose, CA 95133
Phone: 408-729-6700

Microsoft Corporation
One Microsoft Way
Redmond, WA 98052-6399
Phone: 800 426-9400

QNX Software Systems
175 Terrence Matthews Cr.
Kanata, ON K2M 1W8
CANADA
Phone: 613-591-0931
FAX: 613-591-3579

Installing a Boot PROM

The Little Board/486*i* can be configured for a boot PROM in two ways:

1. By installing the boot PROM in byte-wide socket S0.

2. By installing the boot PROM code in a 16K-portion set aside for it in the BIOS ROM at CC000h.

Installing a Boot PROM in Byte-Wide Socket S0

You may install a LAN boot PROM in byte-wide socket S0. The boot PROM code is run at boot time as a “BIOS extension.” (This is a standard feature of a PC BIOS.) The BIOS scans certain areas of upper memory looking for a trigger code of 55h AAh. When it finds this trigger code, it executes the boot PROM code.

Note

The minimum byte-wide socket address window on the Little Board/486*i* is 64K bytes. Any devices smaller than 64K bytes will be visible in the address space at multiple addresses. For instance, a 16K byte device will be "mirrored" at (for instance) D0000h, D4000h, D8000h, DC000h. The boot PROM code you use must be intelligent enough to prevent itself from being run multiple times during the boot process.

To install a LAN boot PROM in byte-wide socket S0, follow these guidelines:

1. Either obtain a preprogrammed boot PROM device, or program a PROM or Flash EPROM with the boot PROM image. Use a 64K byte device, such as a 27C512, if possible.
2. Jumper byte-wide socket S0 for the device you will be using. Refer to the diagrams in Chapter 2 for byte-wide socket jumpering.
3. Install the boot PROM device in S0.
4. In SETUP, set socket S0 for 64K bytes at D0000h and select S0 to be enabled at boot time.

Installing Boot PROM Code in the Onboard Flash Device

Ampro supplies a Flash programming utility to program a boot PROM code into the Flash device on the Little Board/486*i*. The program is called PGMIBIOS and is supplied on the Utilities diskette that accompanies the Little Board/486*i* Development Kit.

To install boot PROM code, follow this procedure:

1. Using SETUP, verify that the onboard video BIOS is shadowed (on SETUP Page 1). It must be shadowed for this procedure to work properly.
2. Using SETUP, verify that ExBIOS @ CC000 is enabled (on SETUP Page 2).
3. Remove EMM386, HIMEM, and other extended memory managers from your CONFIG.SYS or AUTOEXEC.BAT files. No extended memory managers can be loaded. (You must reboot the system for these changes to take effect.)
4. Remove the jumper on W9 to enable programming and install it on W13 to connect +12V programming power to the target Flash device.
5. Enter the following command on the DOS command line:

   `PGMIBIOS EXBIOS=`*`filename`*

   where *`filename`* is the name of the boot PROM code file. (Frame the command so that DOS accesses the utility wherever it resides on your system.)

   Files are assumed to be in BINARY format. There is no conversion of HEX, ASCII, or other formats. Leading and trailing spaces around the "=" are ***not*** allowed.

   PGMIBIOS will display a message indicating when programming is complete.
6. Turn system power off.
7. Remove jumper W13 and install it on jumper W9.

3.14 FLAT PANEL/CRT VIDEO CONTROLLER

3.14.1 Developing a Custom BIOS for an Unsupported LCD Flat Panel

Ampro supplies flat panel BIOS images for several popular flat panels, accessible under SETUP. If you select an unsupported panel, you must create a custom BIOS. A custom BIOS is created from an existing BIOS using a customizing program. Ampro provides a BIOS modification kit containing the program and complete documentation. Contact your Ampro sales representative or Ampro Technical Support for information about the Little Board/486*i* Flat Panel BIOS Modification Kit.

Once you have modified a BIOS, you must load it into the video BIOS section of an onboard Flash EPROM device (already on the Little Board/486*i*). Ampro provides a Flash programming utility to do this.

To install a new video BIOS, follow this procedure:

1. Using SETUP, verify that the onboard video BIOS is shadowed (Page 1). It must be shadowed for this procedure to work properly.
2. Remove EMM386, HIMEM, and other extended memory managers from your CONFIG.SYS or AUTOEXEC.BAT files. No extended memory managers can be loaded. (You must reboot the system for these changes to take effect.)
3. Remove the jumper on W9 to enable programming, and install it on W13 to connect +12V programming power to the target Flash device. (You do not need to install a device—the new BIOS will be stored in an unused portion of the ROM BIOS chip.
4. Enter the following command on the DOS command line:

   `PGMIBIOS VIDEO=`*`filename`*

   where *`filename`* is the name of the new video BIOS code file. (Frame the command so that DOS accesses PGMIBIOS wherever it resides on your system.)

   Leading and trailing spaces around the "=" are ***not*** allowed.

   PGMIBIOS will display a message indicating when programming is complete. DO NOT REBOOT!
5. DO NOT remove power. Remove jumper W13 and restore jumper W9.
6. Reboot the system and test the result

3.14.2 External Video Overlay (PC Video)

The video controller supports up to 16 bits of external RGB video data to be input and merged with the internal VGA data stream through the External Video Overlay port (J6). This interface allows you to display "live" video on flat panel displays.

The controller supports two forms of video windowing:

1. Color key input
2. X-Y window keying

Color key input is the familiar video overlay technique in which a particular color is designated as a "key" for switching between two video sources. The PC video interface provides for an externally-generated color key signal input, which switches between the external video source and internally-generated video.

X-Y window key input can be used to position the live video window coordinates.

A complete description of the PC Video interface is beyond the scope of this manual. To find out more about the PC Video interface, its timing and architecture, contact:

Chips and Technologies
2950 Zanker Road
San Jose, CA 95134
Phone: 408 434-0600
Telex: 272929 CHIPS UR
FAX: 408 526-2275

Ask for information pertinent to the 65545 High Performance Flat Panel/CRT VGA controller and its use with "PC Video".

3.15 PC SPEAKER

One of the core control logic devices includes a standard AT-compatible speaker port. The speaker logic signal is buffered by a transistor amplifier, and provides about 100 milliwatts to an external 8 ohm speaker.

The audio output is based on two signals: the output of Timer 2; and the programming of two bits, 0 and 1, at I/O port 61h. Bit 1 of I/O port 61h is one term of a 2-input AND gate. The other term is the output from Timer 2. Thus, setting bit 1 to a logic 1 enables the output of Timer 2 to the speaker, and a logic 0 disables it. If you disable Timer 2 by setting bit 0 of port 61h to a 0, then you can use bit 1 of port 61h to control the speaker directly.

3.16 WATCHDOG TIMER

The purpose of a watchdog timer function is to restart the system should some mishap occur. Possible problems include: a failure to boot properly; the application software losing control; temporary power supply problems including spikes, surges, or interference; the failure of an interface device; unexpected conditions on the bus; or other hardware or software malfunctions. The watchdog timer helps assure proper start-up after an interruption.

The Little Board/486*i* ROM-BIOS supports the board's watchdog timer function in two ways:

- There is an initial watchdog timer setting, specified using SETUP, which determines whether the watchdog timer will be used to monitor the system boot, and if so, how long the time-out is (30, 60, or 90 seconds).

- There is a special ROM-BIOS function which may be used by application software to start, stop, and retrigger the watchdog timer function.

The initial time-out should be set (using SETUP) to be long enough to guarantee that the system can boot and pass control to the application. Then, the application must periodically retrigger the timer so that the time-out does not occur. If the time-out does occur, the system will respond in a manner determined by how the watchdog timer jumper, W11, is set (see Chapter 2).

The following simple assembly language routine illustrates how to control the watchdog timer using the Ampro ROM-BIOS function that has been provided for this purpose:

```
;---------------------------------------------------------
; Watchdog timer control program
;---------------------------------------------------------
MOV   AH,0C3h          ; Watchdog Timer BIOS function
MOV   AL,nn            ; Use “00” to disable, “01” to enable
                       ; timer.
MOV   BX,mm            ; Selects time, in seconds
                       ;(00-FFh; 1-255 seconds)
INT   15h
```

Ampro provides a simple DOS program that can be used from the command line or in a batch program to manage the watchdog timer. It is called WATCHDOG, and is described in the Ampro Common Utilities manual.

Note

Some versions of DOS turn off the real-time clock alarm at boot time. If your DOS does this, make sure that your application program enables the alarm function using this BIOS call.

3.17 POWERFAIL MONITOR

A hard reset is generated by a powerfail circuit if power falls below 4.5V.

If you have jumpered W20, the power management circuitry generates a power-fail Non-Maskable Interrupt (NMI) if the power falls below 4.7V.

When an NMI occurs, the BIOS detects the NMI and displays the message “Power Fail NMI” on the console. At this point you have two options via the keyboard. You can mask the NMI and continue (the PC architecture provides a mask bit for the non-maskable interrupt), or reboot the system.

If you want to do something else with the NMI, you must provide your own power fail NMI handler and patch the NMI interrupt vector address to install it.

3.18 SYSTEM MEMORY MAP

The Little Board/486*i* architecture allows it to address up to 64M bytes of memory. Table 3-14 shows how this memory is used.

The DRAM, the byte-wide sockets, and ROM BIOS occupy the first megabyte (starting at 00000h). You can install up to 64 megabytes of DRAM onboard with 1M, 4M, 8M, 16M, and 32M byte 72-pin SIMMs.

Memory Address	Function
0100000h - 3FFFFFFh	Extended memory
00F0000h - 00FFFFFh	64K ROM BIOS.
00D0000h - 00EFFFFh	Byte-wide memory sockets S0 and S1 if enabled. Otherwise, free.
00CC000h - 00CFFFFh	Onboard BIOS Expansion Flash device for Ethernet boot PROM code
00C0000h - 00CBFFFh	Video BIOS for onboard flat panel video controller.
00A0000h - 00BFFFFh	Normally contains video RAM, as follows: CGA Video: B8000-BFFFFh Monochrome: B0000-B7FFFh EGA and VGA video: A0000-AFFFFh
000000h - 09FFFFh	Onboard DRAM

Table 3-14 Little Board/486*i* Memory Map

3.19 SYSTEM I/O MAP

Table 3-15 is a list of the I/O port assignments used on the Little Board/486*i*. The I/O port functions and addresses (except for a few "Ampro reserved" addresses) shown in Table 3-15 are all standard for PC compatibles from both a hardware and software perspective.

Typically, the ROM BIOS provides all the services needed to use the onboard devices and devices connected to I/O ports. If you need to directly program the standard functions, refer to a programming reference for the PC/AT.

I/O Address	Function
3F8h - 3FFh	Primary serial port
3F2h - 3F7h	Floppy disk controller ports 3F2: FDC Digital output register 3F4: FDC Main status register 3F5: FDC Data register 3F7: FDC Control register
3F0h - 3F1h	Ampro reserved
3E8h - 3EFh	Third serial port
3D0h - 3DFh	Video controller
3C0h - 3CFh	Flat Panel/CRT VGA display adapter
3B0h - 3BFh	Monochrome display adapter
378h - 37Fh	Primary parallel printer port
340h - 35Fh	SCSI interface (0140H-015Fh if W24 installed)
320h - 32Fh	Ethernet interface (default)
2F8h - 2FFh	Secondary serial port
2F0h - 2F3h	Ampro reserved
2E8h - 2EFh	Fourth serial port
278h - 27Fh	Secondary parallel printer port
1F8h - 1FFh	Ampro reserved
1F0h - 1F7h	IDE hard disk interface
0F0h - 0FFh	Reserved
0C0h - 0DFh	DMA controller 2 (8237 equivalent)
0A0h - 0A1h	Interrupt controller 2 (8359 equivalent)
092h	Fast A20 gate and CPU reset
080h - 08Fh	DMA page registers (74LS61 equivalent)
070h - 071h	Real-time clock and NMI mask
060h, 064h	Keyboard controller (8042 equivalent)
040h - 043h	Programmable timer (8254 equivalent)
020h - 021h	Interrupt controller 1 (8359 equivalent)
000h - 00Fh	DMA controller 1 (8237 equivalent)
E0E0h - E0EFh	Ethernet disable address (full 16-bit address)

Table 3-15 Little Board/486*i* I/O Map

Note

Other I/O ports below 100h are reserved for internal system functions and should not be accessed.

3.20 UTILITY SOFTWARE OVERVIEW

The Little Board/486*i* Development Kit provides a number of software utilities on the Ampro Common Utilities diskette. Some of the programs provided on this diskette are:

FLASHWRI—Flash PROM utility for writing program images to Flash devices in byte-wide sockets.

SETUP—A utility used to access the ROM BIOS SETUP function from the DOS command line.

SCSICOMP—A SCSI utility that compares data from two SCSI direct access devices.

SCSICOPY—A SCSI copy utility that copies data between two SCSI direct access devices

SCSIFMT—A hard disk utility for low-level SCSI drive formatting.

SCSITOOL—A SCSI debugger that issues low level commands to any SCSI bus device.

SERLOAD—A serial loader utility for downloading files from a remote host prior to system boot.

SERPROG—A utility to program Flash byte-wide devices from a serial port.

TVTERM—A Televideo 900-series terminal emulator.

WATCHDOG—Used to stop, start, or retrigger the watchdog timer function.

These utilities and others are described in the Ampro Common Utilities manual.

APPENDIX A

FLAT PANEL CABLES

This section lists the cable wiring for the flat panels supported by the ROM BIOS. Use these lists to construct cables for the supported panels. Wiring for the Little Board/486*i* connector J3, the flat panel's connector, and backlight inverter (where required) is shown. In some cases, a third-party support board is used in the assembly.

Use SETUP to select the video BIOS parameters for the panel you will be using.

Note

Panel technology is changing rapidly. Flat panel support in the Little Board/486*i* ROM BIOS will changed from time to time to maintain compatibility with current panel technology. Contact Ampro Technical Support for a list of currently supported panels.

A.1 SHARP LM64P839 PASSIVE MONOCHROME LCD PANEL

LB486*i* J3		Flat Panel Connector		Backlight Inverter	
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	GND				
2	+5VDC				
3	+12VDC				
4	GND	6	GND		
5	SHFCLK	3	CP2		
6	GND				
7	ACDCLK				
8	GND				
9	LP	2	CP1		
10	FLM	1	S		
11	BLANK*				
12	PNL00	11	DU3		
13	PNL01	10	DU2		
14	PNL02	9	DU1		
15	PNL03	8	DU0		
16	PNL04	15	DL3		
17	PNL05	14	DL2		
18	PNL06	13	DL1		
19	PNL07	12	DL0		
20	PNL08				
21	PNL09				
22	PNL10				
23	PNL11				
24	PNL12				
25	PNL13				
26	PNL14				
27	PNL15				
28	PNL16				
29	PNL17				
30	PNL18				
31	PNL19				
34	+5VDC				
35					
36	ENABKL				
37	+5VDC				
38	ENAVEE				
39	ENAVDD				
40	GND				
41	PNL20				
42	PNL21				
43	PNL22				
44	VDDSAFE	4, 5	DISP, Vdd		
45	PNL23				
46	VEESAFE	7	Vee		
47	ECON				
48	GND				
49	GND			2	GND
50	+12SAFE			1	VIN

Notes: Sharp LM64P839 Passive Monochrome LCD Panel

1. This wiring list assumes that you have installed Ampro's optional LCD Bias Supply board on connector J4.
2. Recommended backlight inverter is Xentek LS280.
3. Mating connector for the Little Board/486*i* connector J3 is 3M 3425-6600 (or equivalent).
4. Mating connector to the flat panel is Molex 51021-1500 (or equivalent).
5. Mating connector to the Xentek LS280 backlight inverter is Molex 51021-0200 (or equivalent).

A.2 SHARP LJ64ZU51 GRAY SCALE ELECTROLUMINESCENT

LB486*i* J3		Flat Panel Connector	
Pin	**Signal**	**Pin**	**Signal**
1	GND	A10	GND
2	+5VDC		
3	+12VDC		
4	GND	B10	GND
5	SHFCLK	A7	CK
6	GND	B9	GND
7	ACDCLK		
8	GND	B8	GND
9	LP	A8	H.D
10	FLM	A9	V.D
11	BLANK*		
12	PNL00		
13	PNL01		
14	PNL02		
15	PNL03		
16	PNL04		
17	PNL05		
18	PNL06		
19	PNL07		
20	PNL08	B4	D00
21	PNL09	A4	D01
22	PNL10	B5	D02
23	PNL11	A5	D03
24	PNL12	B2	D10
25	PNL13	A2	D11
26	PNL14	B3	D12
27	PNL15	A3	D13
28	PNL16		
29	PNL17		
30	PNL18		
31	PNL19		
34	+5VDC	B12	V1 [1]
35			
36	ENABKL		
37	+5VDC	A12	V1 [1]
38	ENAVEE		
39	ENAVDD		
40	GND	B7	GND
41	PNL20		
42	PNL21		
43	PNL22		
44	VDDSAFE		
45	PNL23		
46	VEESAFE		
47	ECON		
48	GND		
49	GND		
50	+12SAFE		
		A11	Vd [2]
		B11	Vd [2]

Notes: Sharp LJ64ZU51 Gray Scale Electroluminescent

1. Power management can be obtained by connecting the panel's Vcc to the LB486*i*'s VDDSAFE (pin 44) and utilizing the optional LCD Bias Supply board.
2. These panel pins must be connected to an external +24V power supply.
3. Mating connector for the Little Board/486*i* connector J3 is 3M 3425-6600 (or equivalent).
4. Mating connector to the flat panel is 3M 3399-6626 (or equivalent).

A.3 SHARP LM64C35P DUAL SCAN STN COLOR

LB486*i* J3		Adapter Board Quadrangle PCB-LM002-1		Backlight Inverter	
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	GND			3	GND
2	+5VDC	16	DISP		
3	+12VDC			2	VIN
4	GND	2	GND		
5	SHFCLK	24	XCK		
6	GND	4	GND		
7	ACDCLK				
8	GND	14	GND		
9	LP	28	LP		
10	FLM	30	YD		
11	BLANK*				
12	PNL00	1	DU7		
13	PNL01	3	DU6		
14	PNL02	9	DU5		
15	PNL03	11	DU4		
16	PNL04	25	DL7		
17	PNL05	27	DL6		
18	PNL06	29	DL5		
19	PNL07	31	DL4		
20	PNL08	12	DU3		
21	PNL09	10	DU2		
22	PNL10	8	DU1		
23	PNL11	6	DU0		
24	PNL12	13	DL3		
25	PNL13	15	DL2		
26	PNL14	21	DL1		
27	PNL15	23	DL0		
28	PNL16				
29	PNL17				
30	PNL18				
31	PNL19				
34	+5VDC	17	VDD [1]		
35					
36	ENABKL			1	ON/OFF
37	+5VDC	18	VDD [1]		
38	ENAVEE				
39	ENAVDD				
40	GND	26	GND		
41	PNL20				
42	PNL21				
43	PNL22				
44	VDDSAFE				
45	PNL23				
46	VEESAFE				
47	ECON				
48	GND				
49	GND	32	GND		
50	+12SAFE				
		12	VCON [2]		

Notes: Sharp LM64C35P Dual scan STN color

1. Power management can be obtained by connecting the panel's Vcc to the LB486*i*'s VDDSAFE (pin 44) and utilizing the optional LCD Bias Supply board.
2. This input (VCON) must have a contrast adjustment voltage applied, in the range of 0.8 to 2.8 volts.
3. Recommended backlight inverter is Xentek LS380.
4. Mating connector for the Little Board/486*i* connector J3 is 3M 3425-6600 (or equivalent).
5. Mating connector for the Quadrangle adapter board is Hirose DF11-32DP-DS (or equivalent).
6. Mating connector to the backlight inverter is Molex 51021-0500 (or equivalent).

A.4 SHARP LQ10D131 TFT COLOR

LB486*i* J3		Adapter Board Quadrangle PCB-LQ001-1		Backlight Inverter	
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	GND			3	GND
2	+5VDC				
3	+12VDC			2	VIN
4	GND	1	GND		
5	SHFCLK	11	CK		
6	GND	13	GND		
7	ACDCLK				
8	GND	16	GND		
9	LP	9	HSYNC		
10	FLM	7	VSYNC		
11	BLANK*				
12	PNL00				
13	PNL01	24	B0		
14	PNL02	26	B1		
15	PNL03	30	B2		
16	PNL04	32	B3		
17	PNL05				
18	PNL06				
19	PNL07	10	G0		
20	PNL08	12	G1		
21	PNL09	18	G2		
22	PNL10	20	G3		
23	PNL11				
24	PNL12	2	R0		
25	PNL13	4	R1		
26	PNL14	6	R2		
27	PNL15	8	R3		
28	PNL16				
29	PNL17				
30	PNL18				
31	PNL19				
34	+5VDC	21	VCC [1]		
35					
36	ENABKL			1	ON/OFF
37	+5VDC	22	VCC [1]		
38	ENAVEE				
39	ENAVDD				
40	GND	28	GND		
41	PNL20				
42	PNL21				
43	PNL22				
44	VDDSAFE				
45	PNL23				
46	VEESAFE				
47	ECON				
48	GND				
49	GND	31	GND		
50	+12SAFE				

Notes: Sharp LQ10D131 TFT Color

1. Power management can be obtained by connecting the panel's Vcc to the LB486*i*'s VDDSAFE (pin 44) and utilizing the optional LCD Bias Supply board.
2. Recommended backlight inverter is Xentek LS380.
3. Mating connector for the Little Board/486*i* connector J3 is 3M 3425-6600 (or equivalent).
4. Mating connector for the Quadrangle adapter board is Hirose DF11-32DP-DS (or equivalent).
5. Mating connector to the backlight inverter is Molex 51021-0500 (or equivalent).

A.5 SHARP LQ64D142 TFT COLOR

LB486*i* J3		Adapter Board Quadrangle PCB-LQ001-1		Backlight Inverter	
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	GND			3	GND
2	+5VDC	15	NBH		
3	+12VDC			1	VIN
4	GND	1	GND		
5	SHFCLK	11	CK		
6	GND	13	GND		
7	ACDCLK				
8	GND	16, 19	GND, NBV		
9	LP	9	HSYNC		
10	FLM	7	VSYNC		
11	BLANK*				
12	PNL00				
13	PNL01	24	B0		
14	PNL02	26	B1		
15	PNL03	30	B2		
16	PNL04	32	B3		
17	PNL05				
18	PNL06				
19	PNL07	10	G0		
20	PNL08	12	G1		
21	PNL09	18	G2		
22	PNL10	20	G3		
23	PNL11				
24	PNL12	2	R0		
25	PNL13	4	R1		
26	PNL14	6	R2		
27	PNL15	8	R3		
28	PNL16				
29	PNL17				
30	PNL18				
31	PNL19				
34	+5VDC	21	VCC [1]		
35					
36	ENABKL			5	ON/OFF
37	+5VDC	22	VCC [1]		
38	ENAVEE				
39	ENAVDD				
40	GND	28	GND		
41	PNL20				
42	PNL21				
43	PNL22				
44	VDDSAFE				
45	PNL23				
46	VEESAFE				
47	ECON				
48	GND				
49	GND	31	GND		
50	+12SAFE				

Notes: Sharp LQ64D142 TFT Color

1. Power management can be obtained by connecting the panel's Vcc to the LB486*i*'s VDDSAFE (pin 44) and utilizing the optional LCD Bias Supply board.
2. Recommended backlight inverter is Xentek LS460.
3. Mating connector for the Little Board/486*i* connector J3 is 3M 3425-6600 (or equivalent).
4. Mating connector for the Quadrangle adapter board is Hirose DF11-32DP-DS (or equivalent).
5. Mating connector to the backlight inverter is Molex 51021-0700 (or equivalent).

A.6 FLAT PANEL DISPLAY LDH102TTFT COLOR

LB486*i* J3		LDH102T	
Pin	**Signal**	**Pin**	**Signal**
1	GND	22	GND
2	+5VDC	40, 46, 48, 50	+5V
3	+12VDC		
4	GND	1, 17	GND
5	SHFCLK	2	CLK
6	GND	3, 12	GND
7	ACDCLK	43	ENAB
8	GND	5, 7	GND
9	LP	4	HSYNC
10	FLM	6	VSYNC
11	BLANK*		
12	PNL00	36	B0
13	PNL01	35	B1
14	PNL02	34	B2
15	PNL03	33	B3
16	PNL04	31	B4
17	PNL05	30	B5
18	PNL06	29	B6
19	PNL07	28	B7
20	PNL08	26	G0
21	PNL09	25	G1
22	PNL10	24	G2
23	PNL11	23	G3
24	PNL12	21	G4
25	PNL13	20	G5
26	PNL14	19	G6
27	PNL15	18	G7
28	PNL16	16	R0
29	PNL17	15	R1
30	PNL18	14	R2
31	PNL19	13	R3
34	+5VDC	39	+5V
35			
36	ENABKL		
37	+5VDC		+5V
38	ENAVEE		
39	ENAVDD		
40	GND	37, 41, 42	GND
41	PNL20	11	R4
42	PNL21	10	R5
43	PNL22	9	R6
44	VDDSAFE		
45	PNL23	8	R7
46	VEESAFE		
47	ECON		
48	GND	32, 44, 45, 47	GND
49	GND	27, 51	GND
50	+12SAFE		

INDEX

D

E

F

H

I

J

K

L

M

N

O

P

Q

R

S

T

U

V

W