		JP11:5-6	JP 11:3-4	JP11:1-2	JP 12 state
25					1-2
30		■			1-2
33			■	■	1-2
40				■	1-2
50			■		2-3
60		■	■		Unsure
66		■	■	■	1-2
80		■		■	can't POST

Other description info and notes:

Of special note is the BIOS I am uploading: When used, the system POSTs faster than when using the BIOS images already hosted on TRW (namely those with "4/01/96" and "02/02/96" in their POST strings). I don't know why this is the case, as it's dated only one day after the older BIOS image, and the remainder of the POST string is identical to that of the younger one. My guess is the boot code somehow wasn't optimized for 486 speeds when building the later BIOS; the difference is rather noticable and unpleasant @ 25MHz FSB. Some in the Intel DX4 line toggles between 2X and 3X FSB modes when a jumper is inserted in JP30 (either 1-2 or 2-3 is fine; tested with SK101 variant iDX4). Am486DX4's and Am5x86's will toggle between 3X and 4X mode only, and should only use JP30:2-3 when setting it to 3X mode. Finally, and perhaps to be treated apocryphally, the IMISC466 PLL, used to synthesize the FSB clock, also supports supports configuring the board to 30, 60, 66.6 and 80MHz FSB speeds. In these less-public modes, **30** and **66.6 MHz FSB** are stable with compatible/overclockable CPUs (with the latter speed needing custom cache and RAM timing tweaks, as set in the system BIOS; 60ns RAM is probably required, and I only have the 15ns cache that came with the board.). 60MHz has been *mostly* stable in my tests, but I haven't found a configuration comfortable enough to endorse it. I have nothing that's okay with overclocking to an 80MHz bus. In addendum to my BIOS, attached below is my chart for the relevant jumpers, and I have posted a note on BIOS settings for getting the FSB working @66.6 MHz.

For 66MHz FSB, I was able to get full system stability (as best observable) with my Intel 486DX4 SK101 set to 2X FSB mode, as well as my Intel DX1 rated for 50MHz, using 60ns RAM and 15ns onboard cache, by setting these options under Chipset Features Setup in my Award BIOS (dated 02-03-1996):

- Auto Configuration: Disable
- ISA Bus Clock: 1/3 PCLK
- LBD# Sample Point: End of T2
- Cache Write Cycle: 3 CCLK
- Cache Burst Read Cycle: 2 CCLK
- L2 Cache/DRAM Cycle WS: 3 CCLK
- DRAM RAS to CAS Delay: 3 CCLK
- DRAM Write Cycle: 0 WS
- DRAM Write CAS Pulse: 2 CCLK
- DRAM CAS Precharge Time: 1 CCLK
- DRAM RAS to MA Delay: 2 CCLK
- DRAM Speed: Faster
- DRAM Slow Refresh: Disable

All other settings as found in the BIOS should have no relevant bearing. Also, if it doesn't work for your build, you can try increasing WS and CCLK numbers, as well as lowering "DRAM Speed". Maybe a peripheral card won't be happy unless you lower the ISA Bus Speed (note: if your keyboard has a longer cable, it may not work until you lower this. One of mine only works when this is set to 7.159MHz; while it would seem the PCI bus clock is what's being divided for the ISA bus, I theorize the keyboard BIOS/"bus" speed is being changed by this as well). Basically, using this "recipe" as a blueprint, tinker with the settings until it works... unless it doesn't.

Naturally, ***USE AT YOUR OWN RISK***