TABLE OF CONTENTS

CHAPTER 1

1-1 OVERVIEW

The J435,J437 mainboards are a cost-effective implementation of a high integration, high performance and high energy efficient VL/ISA system based on the 80486SX/DX/DX2/DX4 or compatible processor. With an optional VT82C505 VL-PCI bridge, the system can be extended to the PCI/VL/ISA platform that offers top rated PCI performance and proven PCI-2.0 compliance. In either case, the J435,J437 mainboards interfaces directly with the VT82C406MV IXP (Integrated X-bus Peripherals) that replaces the multi-clock generator, the keyboard controller with PS2 mouse support, the DS-1285 style real time clock with 128 byte of CMOS RAM and certain amount of glue logic. Less than ten TTLs are required for a complete main board implementation in addition to the chips mentioned above.

The J435,J437 mainboards support the state-of-art 80486 families from major CPU vendors including Intel, AMD and Cyrix. The write-back internal cache, burst write transfer, CPU clock stop and switching protocol and system management mode are supported to the full capability of individual CPUs. The J435 mainboards support two VL devices in addition to the embedded local bus IDE controller without any glue logic. Both VL devices can be of the master type and the arbitration logic is integrated inside the chip. More VL devices can be supported with external glue logic.

The integrated power management unit monitors I/O events, interrupt, DMA and VL master request signals to detect the status of system activity. Each event can be turned off or assigned to one of two event classes tracked by two independent idle timers. Two additional general purpose timers are also provided for house-keeping or mode switching purposes. One of the timers can also be used to keep track the activity of specific peripheral devices. The system management interrupt (SMI) may be triggered by multiple sources including time-out of individual timers, occurrence of system activities, external input and software programming for flexible applications. The SMI routine checks the status and takes appropriate actions including clock speed switching (or stop) and I/O and power control. On top of the SMI-oriented power management capability, the J435,J437 mainboards also support automatic conserve mode operation to conserve power under short and frequent system idleness (e.g. keyboard typing).
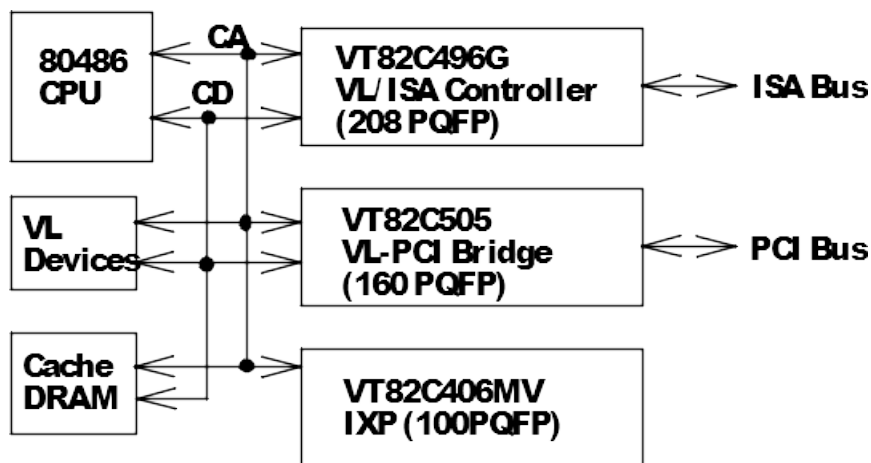
Main Board Based 80486 PCI/VL/ISA System

The embedded local bus IDE controller recognized IDE I/O port accesses as local bus cycles and provides prefect and post-write buffers to allow concurrent CPU/VL and IDE bus operation. The controller supports either the primary (1F0-1F7h) enhanced IDE channels with two devices. The command and recovery time of each device can be individually programmed in units of CPU clock to achieve the optimal speed of the device up to >10MB/s transfer rate. The IDE devices share the same bus with the ISA bus with separate control signals so that no external logic is required.

The J435,J437 mainboards support shadowing of system, video and other BIOS to speed up the access. The video and system BIOS can also be made cacheable and write-protect. Unused portion of the DRAM can be relocated to increase the size of the overall system memory.

Access to either E or C segment can be programmed to be an on-board EPROM cycle to allow the combination of system and video BIOS for an all-in-one system board implementation. The J435,J437 mainboards can also be programmed to recognize write cycles as EPROM cycles to support field upgradability of flash EPROM BIOS.

The ISA bus controller runs synchronously with the CPU clock to eliminate the synchronization overhead associated with an asynchronous system. The wait state, command delay and I/O recovery time are programmable to allow maximum flexibility in using ISA add-on cards. The bus conversion and data alignment are performed automatically if the sizes of the master and the slave of a command do not match. Push-button suspend and resume function is provided in addition to the traditional hardware and software de-turbo mechanism. Fast gate A20 and fast reset logic is also included to allow faster response in a protected mode environment.

A rich set of configuration registers are provided for fine-tuning the cost and performance of individual system. Standard parameters such as cache and DRAM configurations and ISA bus clock are automatically detected and programmed by the BIOS so that neither jumper nor BIOS settings is necessary.

The J435,J437 mainboards are ideal for high performance, high quality, high energy efficient and high integration desktop and notebook PCI/VL/ISA computer systems.

1-2 FEATURES

1. Fully IBM PC/AT Compatible

2. Flexible CPU and Local Bus Interface
- Supports 80486SX/DX/DX2/DX4 and compatible CPUs
- CPU speed up to 100 Mhz including 80486DX-50, 80486DX2-66 and 80486DX2-80，80486DX4-100
- Supports CPUs with write-back internal cache, e.g. and Cx486DX/DX2
- Snoop filtering for write-back CPUs
- Supports SMI protocols of Intel, AMD and Cyrix CPUs
- CPU clock stretching and throttling
- Zero frequency CPU suspend mode
- Soft and hard CPU reset
- Direct VESA and other local bus interface with DMA/master access
- Built-in arbitration for two local bus masters

3. Advanced Cache Controller
- Write back/write through scheme
- Direct map scheme
- Flexible cache size: 0K/128K/256K/512K/1MB
- One bank or two banks of data independent of cache size
- Integrated 8-bit tag comparastor
- Interleaved SRAM access to achieve 2-1-1-1 burst fill
- Supports burst read and burst write transfers
- System and video BIOS cacheable and write-protect
- Programmable cache timing
- Programmable non-cacheable region
- Optional combined tag and alter bit SRAM for the write-back scheme
- Eight bit tag under the combined tag-alter scheme without sacrifice of cacheable space

4. Fast Page Mode DRAM Controller
- Mixed 256K/512K/1M/2M/4M/8M/16MxN DRAMs
- 8 banks up to 128MB
- Flexible column and row addresses

- 72pin(x36) or 30pin SIM module support
- Programmable DRAM timing
- BIOS shadow at 16KB increment
- 256/384K memory relocation
- System management memory remapping
- Decoupled DRAM refresh with staggered RAS timing
- CAS-before-RAS and slow refresh

5. Synchronous ISA Bus Controller

- Synchronous ISA bus clock
- Programmable wait state, command delay and I/O recovery time
- Bus conversion and data alignment
- Hardware and software de-turbo control
- Fast reset and Gate A20 operation
- Integrated 82C206 peripheral controller
- Edge trigger or level sensitive interrupt controller
- Flash EPROM and combined BIOS support

6. Integrated Power Management Unit

- Normal, conserve, doze, sleep and suspend modes
- System event monitoring with two event classes and two idle timers
- Primary and secondary interrupt differentiation for individual
   channels
- One extended peripheral timer and one general purpose timer
- Automatic conserve mode operation for short and frequent system
   idleness
- Modular clock and modular power
- CPU clock stretching, throttling or stop without affecting the ISA
   bus clock
- Zero frequency operation with automatic resume
- Zero volt operation with leakage control
- Four general purpose I/O or power control ports
- APM 1.1 compliant

7. Integrated Local Bus IDE Controller

- 32-bit host data transfer
- Mode-3 transfer capabilities (>10MB/s)
- Programmable read/write, master/slave and active/recovery timing in
   units of CPU clock
- Prefect and write buffers
- Support either primary (1F0-1F7h) channel with two devices
- No external logic required

CHAPTER 2

2-1 J435 BOARD LAYOUT

2-2 J435 JUMPER SETTING

```
JT2  * 1-2   Other CPU
       2-3   P24T   CPU
JT5  * 1-2   Cyrix CPU
       2-3   P24D   CPU
*JRN3     Intel
 JRN4     Cyrix
 JRN5     AMD
```

	486SX/M6	486DX/DX2/DX4/M7	487SX/ODP/P24T
JC1	OFF	* 1-2	2-3
JC2	2-3	* 1-2	1-2
JC3	2-3	* 1-2	1-2

```
JT4      1-2   Cyrix CPU clock*1
         2-3   Cyrix CPU clock*2
J14   * 1-2   Other CPU for DX4-100 (AMD, Intel, P24D)
         2-3   AMD CPU clock for AMD DX2/80, AMD DX2/66
JG1   * 1-2   VL/CPU Sync
         2-3   VL/CPU Async
JG4   * 1-2   CPU clock no delay
         2-3   CPU clock delay
```

	JCK1	JCK2	JCK3	JCK4
25M	2-3	1-2	2-3	1-2
*33M	2-3	2-3	1-2	1-2
40M	1-2	1-2	2-3	1-2
50M	1-2	2-3	1-2	1-2

CPU POWER REGULATION

	5V	Changeable
JP1	3-5	1-3
	4-6	2-4

J11 3.3V
*J12   3.45V
J13 4.0V

I/O PORT ADDRESS SETTING

I/O port address select normal don't change it except there is the conflict.
Recommand : Default

Jumper setting also can set by BIOS (chipset features setup), I/O chipset have to be W83787

J2	1	2	RS232I
	Low	Low	COM4(2E8H)
	Low	High	COM1(3F8H,Default)
	High	Low	COM3(3E8H)
	High	High	Disable
	3	4	RS232II
	Low	Low	COM3(3E8H)
	Low	High	COM2(2F8H,Default)
	High	Low	COM4(2E8H)
	High	High	Disable
	5	6	Printer
	Low	Low	LPT1(3BCH)
	Low	High	LPT3(378H)(Default)
	High	Low	LPT2(278H)
	High	High	Disable
	7	8	ISA IDE / Floppy
	Low	High	Enable(Default)
	High	Hight	Disable

RS232 & LPT IRQ SELECT

I/O IRQ selector, Default by factory don't change by user except device there is IRQ conflict, please referance manual for any change.
Recommand : Default

J8	1-2	3-4	5-6	RS232I
	Short	Open	Open	IRQ4(Default)
	Open	Short	Open	IRQ3
	Open	Open	Short	IRQ5
	7-8	9-10	11-12	RS232II
	Short	Open	Open	IRQ3(Default)
	Open	Short	Open	IRQ4
	Open	Open	Short	IRQ5
	13-14	15-16		Printer
	Short	Open		IRQ7(Default)
	Open	Short		IRQ5

VL BUS TIMING

VESA Local Bus clock select depend on cpu clock
Recommand : Default set is CPU 33 MHz

		CPU_CLK>33MHZ	CPU_CLK<=33MHZ
JV1	VL_TIMING	* 2-3	1-2

		0-WAIT-STATE	1-WAIT-STATE
JV2	VL_WRITE	2-3	* 1-2

CMOS DATA

System CMOS configuration setup
Recommand : Don't remove the 1-2 jump except "ERASE DATA"

JCMS1	* 1-2	Keep CMOS data
	2-3	Erase CMOS data

FLUSH SIGNAL

CPU flush signal from chip or external TTL circuit, The system chip set support flush signal but not ready
Recommand : Flush from TTL

JF1	* 1-2	Flush from TTL
	2-3	From 496 Chip

HIGH ADDRESS DECOCTING

Some VGA card driver use Linner address, normally use system high address to mappig the address.
Recommand : Normal 1-2 short

```
JT6      * 1-2  CA26=A26
           2-3  CA26=A31
```

Solves some VESA VGA card (such as Diamond viper VESA VGA) use address A27 to A31

HARD DISK CONNECTOR

Hard disk cable connect

```
CN7   HDD2
CN8   HDD1
```

GAME PORT CONNECTOR

Game cable connect

```
CN12
```

PRINTER OUTPUT SELECT

Printer DATA path direction.   If the system use parallel port for specifical DATA communication can set this jump for bidirection.

```
J3         1-2 DMA Chennal 1 request    ,    5-6 DMA chennal acknowledge
           3-4 DMA Chennal 3 request    ,    7-8 DMA chennal acknowledge
```
If system use ECP/EPP device.   Need to select DMA chennal which will be used.
Ex: use DMA chennal 1 for ECP/EPP DATA transfer have to 1-2, 5-6 short

```
      * 9-10   On printer output only(Default)
               Off printer bidirection
```

IOCHRDY SETTING

I/O timing control, some device I/O speed cannot meet system speed sometime has DATA lose, or HDD can not find by BIOS auto detect HDD, try to Enable the signal.
Recommand : Normal open

J6   Short   Enable
         Open   Disable(Default)

BALE SETTING

Bus address latch enable, sometime if system run on high speed, the I/O have to latch the address ex. CPU CLK > 40MHz
*Recommand : Normal open*

J7   Short   Enable
         Open   Disable(Default)

ISA/VL IDE ACTIVITY LED CONNECTOR

Direct HDD DATA transfer status

CN5   1-2   VL IDE LED
          3-4   ISA IDE LED

GAME PORT

JR2   Open   Disable
      * Short   Enable(Default)
        Power LED/Key Lock   Turbo,SW
             (JW4)   (JW2)

Power LED/Key Lock (JW4)					Turbo,SW (JW2)		
○	○	○	○	○	○	○	○
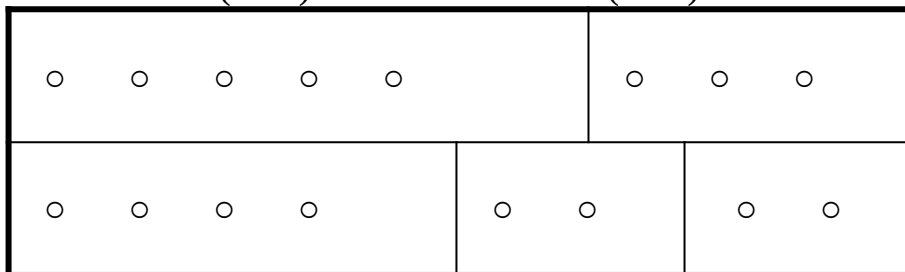
Speaker (JW5)				Reset (JW3)		Turbo LED (JW1)	
○	○	○	○	○	○	○	○

        Speaker   Reset   Turbo LED
         (JW5)   (JW3)   (JW1)

TURBO ON LED

When LED on, direct the system run on turbo speed

JW1   1-2 TB_LED

TURBO SWITCH

Select system CPU clock turbo or deturbo

JW2   1-2 On Deturbo Mode
          1-2 Open Turbo Mode

SYSTEM RESET SWITCH

System Re-start

JW3   1-2 On Rest
          1-2 Open normal

KEYBOARD LOCK & POWER ON LED

Direct system power status and keyboard lock

JW4   4-5 KEY_LOCK
          1-3 Power on LED

SPEAKER CONNECTOR

JW5   1-4 Speak

BATTERY

On board battery for keep CMOS setup

JP3   On   use chargeable battery
      * Off   use unchangeable battery
(Option Jumper)

PS/2 MOUSE CONNECT

CN3   PS/2 MOUSE

(Option)

P/S mouse function already OK

2-3 J437 BOARD LAYOUT

2-4 J437 JUMPER SETTING

JT4   * 1-2 Cyrix CPU
         2-3 P24D CPU
JT6   * 1-2 others CPU
JRN3   AMD CPU
JRN4   Cyrix CPU
*JRN5   Intel CPU

	486SX/M6	486DX/DX2/DX4/M7	487SX
JC1	OFF	* 1-2	2-3
JC2	2-3	* 1-2	1-2
JC3	2-3	* 1-2	1-2

JT5   * 1-2   Cyrix CPU clock*1
        2-3   Cyrix CPU clock*2
J15   * 1-2   Other CPU for DX4-100 (AMD, Intel, P24D)
        2-3   AMD CPU clock for AMD DX2/80, AMD DX2/66
JG1   * 1-2   VL/CPU sync
        2-3   VL/CPU async

JG4   * 1-2   CPU clock no delay
         2-3   CPU clock delay
JG2   * 1-2   PCI clock = CPU clock
         2-3   PCI clock = CPU clock/2

	JCK1	JCK2	JCK3	JCK4
25M	1-2	2-3	1-2	2-3
*33M	2-3	1-2	1-2	2-3
40M	1-2	2-3	1-2	1-2
50M	2-3	1-2	1-2	1-2

JG3   1-2   PCI slot3 clock no delay
       * 2-3   PCI slot3 clock delay

CPU POWER REGULATION   *Referance page 22*

	5V	Changeable
JV3	3-5	1-3
	4-6	2-4

J10   3.3V
J11   * 3.45V
J12   4.0V

I/O PORT ADDRESS SETTING
I/O port address select normal don't change it except there is the conflict.
Recommand : Default

Jumper setting also can set by BIOS (chipset features setup) I/O chipset have to be W83787

J1   1   2   RS232I
         Low   Low   COM4(2E8H)
         Low   High   COM1(3F8H,Default)
         High   Low   COM3(3E8H)
         High   High   Disable
         3   4   RS232II
         Low   Low   COM3(3E8H)
         Low   High   COM2(2F8H,Default)
         High   Low   COM4(2E8H)
         High   High   Disable
         5   6   Printer
         Low   Low   LPT1(3BCH)
         Low   High   LPT3(378H)(Default)

High	Low		LPT2(278H)
High	High		Disable
7	8		ISA IDE / Floppy
Low	Low		Enable(Default)
High	High		Disable

RS232 & LPT IRQ SELECT

I/O IRQ selector, Default by factory don't change by user except device there is IRQ conflict, please referance manual for any change.
Recommand : Default

J13	1-2	3-4	5-6	RS232I
	Short	Open	Open	IRQ4(Default)
	Open	Short	Open	IRQ3
	Open	Open	Short	IRQ5
	7-8	9-10	11-12	RS232II
	Short	Open	Open	IRQ3(Default)
	Open	Short	Open	IRQ4
	Open	Open	Short	IRQ5
	13-14	15-16		Printer
	Short	Open		IRQ7(Default)
	Open	Short		IRQ5

PCI INTERRUPT

PCI interrup select, direct set by BIOS don't change the jump.
Recommand : 1-2 short

PCI IRQ10 connect to ISA IRQ10 or ISA IRQ14
JT1　　* 1-2　PCI IRQ10 connect to ISA IRQ10
　　　　　2-3　PCI IRQ10 connect to ISA IRQ14

VL/BUS TIMING

VESA Local Bus clock select depend on cpu clock
Recommand : Default set is CPU 33 MHz.

		CPU_CLK>33MHZ	CPU_CLK<=33MHZ
JV1	VL_TIMING	* 2-3	1-2

	0-WAIT-STATE	1-WAIT-STATE
JV2 VL_WRITE	2-3	* 1-2

CMOS DATA

System CMOS configuration setup

Recommand : Don't remove the 1-2 jump except "ERASE DATA"

JCMS1   * 1-2   Keep CMOS data
          2-3   Erase CMOS data

FLUSH SIGNAL

CPU flush signal from chip or external TTL circuit, The system chip set support flush signal but not ready

Recommand : Flush from TTL

JF1   * 1-2   Flush from TTL
        2-3   Flush from 496 Chip

HIGH ADDRESS DECOCTING

Some VGA card driver use Linner address, normally use system high address to mappig the address.

Recommand : Normal 1-2 short

JT3   * 1-2   CA26=A26
       2-3   CA26=A31

Solves some VESA VGA card (such as Diamond viper VESA VGA) use address A27 to A31.

HARD DISK CONNECTOR

Hard disk cable connect

CN6   HDD1
CN8   HDD2

GAME PORT CONNECTOR

Game cable connect

CN4

PRINTER OUTPUT SELECT

Printer DATA path direction.   If the system use parallel port for specifical DATA communication can set this jump for bidirection.

J8   1-2 DMA Chennal 1 request,   5-6 DMA chennal acknowledge
          3-4 DMA Chennal 3 request,   7-8 DMA chennal acknowledge

If system use ECP/EPP device.   Need to select DMA chennal which will be used.
Ex: use DMA chennal 1 for ECP/EPP DATA transfer have to 1-2, 5-6 short

     * 9-10   On printer output only(Default)
              Off printer bidirection

IOCHRDY SETTING

I/O timing control, some device I/O speed cannot meet system speed sometime has DATA lose, or HDD can not find by BIOS auto detect HDD, try to Enable signal.
Recommand : Normal open

J3   Short Enable
     * Open   Disable(Default)

BALE SETTING

Bus address latch enable, sometime if system run on high speed, the I/O have to latch the address ex. CPU CLK > 40MHz
Recommand : Normal open

J4   Short   Enable
     * Open   Disable(Default)

ISA/VL IDE ACTIVITY LED CONNECTOR

Direct HDD DATA transfer status

CN7   1-2   VL IDE LED

3-4   ISA IDE LED

GAME PORT

JR1   Open   Disable
      * Short   Enable(Default)
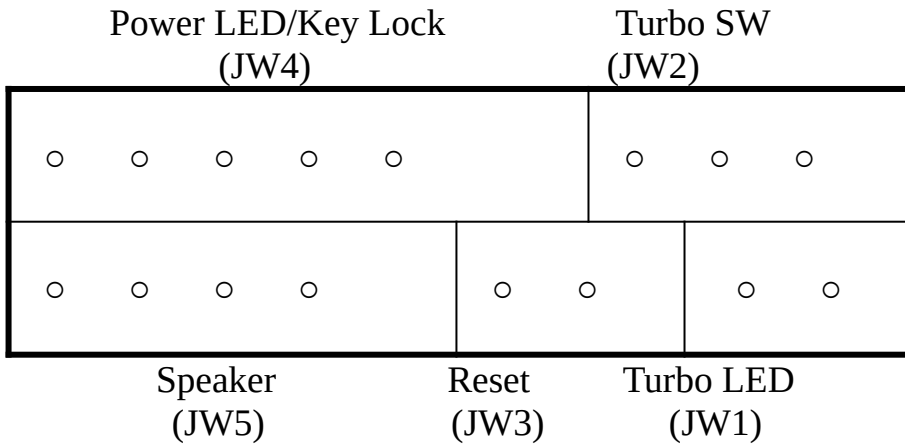
Power LED/Key Lock   Turbo SW
(JW4)   (JW2)

○   ○   ○   ○   ○   ○   ○   ○

○   ○   ○   ○   ○   ○   ○   ○

Speaker   Reset   Turbo LED
(JW5)   (JW3)   (JW1)

TURBO ON LED
When LED on, direct the system run on turbo speed

JW1   1-2 TB_LED

TURBO SWITCH
Select system CPU clock turbo or deturbo

JW2   1-2 On Deturbo Mode
       1-2 Open Turbo Mode

SYSTEM RESET SWITCH
System Re-start

JW3   1-2 On Rest
       1-2 Open normal

KEYBOARD LOCK & POWER ON LED
Direct system power status and keyboard lock

JW4   4-5 KEY_LOCK
          1-3 Power on LED

SPEAKER CONNECTOR

JW5   1-4 Speak

BATTERY

On board battery for keep CMOS setup

JP1   * On use chargeable battery
          Off use un-chargeable battery

PS/2 MOUSE CONNECT

CN3   PS/2 MOUSE
(OPTION)

P/S mouse function already OK

2-5 Quick FOR CPU Installation J435 & J437

CHAPTER 3

SYSTEM I/O ADDRESS MAP

    Other than the two 82C37A compatible DMA controllers, two 82C59A compatible interrupt controllers, one 82C54 compatible counter/timer, the   main board also includes the BIOS EPROM and VT82C406MV interface and the port B logic. Table 5 summarizes the I/O address map for the ISA system. I/O accesses are always run as ISA bus cycles, but the data steering depends on whether the I/O location is on-chip, in the VT82C406MV or in the expansion ISA bus.

Address	Device	Location
00-0Fh	82C37A#1	on-chip
10h-1Fh	not used	

20h-3Fh	823C59A#1	on-chip
40h-43h	82C54	on-chip
44h-5Fh	not used	
60h	keyboard controller	VT82C406MV
61h	Port B	on-chip
62h-63h	unused	
64h	keyboard controller	VT82C406MV
65h-6Fh	not used	
70h(bit 7)	NMI enable	on-chip
70h-71h	CMOS, real time clock	VT82C406MV
80h-8Fh	DMA page register	on-chip
90h-91h	not used	
92h	Port A	on-chip
93h-9Fh	not used	
A0h-A3h	82C59A#2	on-chip
A4h-A7h	not used	
A8h-A9h	configuration register	on-chip
AAh-BFh	not used	
C0h-DFh	82C37A#2	on-chip
E0h-EFh	not used	
F0h	co-proc. busy clear	on-chip
F1h	co-proc. reset	on-chip
F2h-FFh	not used	
100h-1EFh	General I/O location	ISA bus
1F8h-3F5h	General I/O location	ISA bus
3F6h-3F7h	IDE control block register	on-chip
3F8h-FFFFh	General I/O location	ISA bus

Table 5. I/O Address Map

CHAPTER 4

SOFTWARE INSTALLATION (ON BOARD IDE)

4-1 SOFTWARE SUPPORT LIST
-DOS
-NETWARE
-NT
-OS/2
-UNIX
-WINDOWS

4-2 IDE DRIVER INSTALLATION
Please reference read me for detail driver setup.

4-3 REMARK
1. Before install IDE driver, please make sure IRQ15 no occupied.
2. If use normal type CPU without SMM function, please Disable power

manager function when install IDE driver.
3. If use S series CPU (with SMM function), you can Enable power
    manager function when install IDE driver.

CHAPTER 5

5-1 AWARD BIOS SETUP GUIDE

J435,J437 mainboards are equipped with the BIOS for VT82C496 & VT82C505 & VT82C406 from Award Software Inc. This page briefly explains the function of a BIOS in managing the special features of you system. The following pages describe how to use the BIOS for J435,J437 mainboards Setup menu.

Your application programs (such as word processing, spreadsheets, and games) rely on an operating system such as DOS or OS/2 to manage such things as keyboard, monitor, disk drive and memory.

The operating system relies on a BIOS (Basic Input and Output system), a program stored on a ROM (Read-only Memory) chip to initialize and configure your computer's hardware. As the interface between the hardware and the operating system, the BIOS Enable you to make basic changes to your system's hardware without having to write a new operating system.

The SETUP program lets you specify your system's configuration of diskette drivers, hard disk drivers, video display, memory, date and time, and to make setting in the J437 VIP Green PC main board. The SETUP program can only be accessed when the main board has been installed in your system and all necessary power, drive and display connections have

been made. When you turn on your computer, the system will run a memory check, and you can see it counting through the memory on your screen. The following display will also appear on your screen:

Press <Del> to enter SETUP

As long as this message is present on the screen you may press the <Del> key (the one that shares the decimal point at bottom of the number keypad) to access the setup program. In a moment, the main menu of the Award SETUP program will appear on the screen:

ROM PCI/ISA BIOS (2A4L6J11)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.

STANDARD CMOS SETUP	SUPERVISOR PASSWORD
BIOS FEATURES SETUP	USER PASSWORD
CHIPSET FEATURES SETUP	IDE HDD AUTO DETECTION
POWER MANAGEMENT SETUP	SAVE & EXIT SETUP
PCI CONFIGURATION SETUP	EXIT WITHOUT SAVING
LOAD BIOS DEFAULTS	
LOAD SETUP DEFAULTS	
ESC : QUIT	↑↓ → ←　: Select Item
F10 : Save & Exit Setup	(Shift)F2 : Change Color
Time, Date, Hard Disk Type.....	

You may use the cursor up/down keys to highlight the individual menu items. As you highlight each item, a brief description of that item's function appears in the lower window. If you have a color monitor you can use the Shift F2 keys to scroll through the various color combinations available.

5-2 STANDARD CMOS SETUP

The first item in the main menu is the STANDARD CMOS SETUP You must run this part of the setup program in order to correctly setup your hardware configuration. Highlight STANDARD CMOS SETUP and press <ENTER> A message will appear on your screen as shown below:

ROM PCI/ISA BIOS (2A4L6J11)
STANDARD CMOS SETUP
AWARD SOFTWARE, INC.

```
Date (mm:dd:yy) : Thu, Feb, 9, 1995
Time (hh:mm:ss) : 22 :   5 : 40

HARD  DISKS             TYPE     SIZE    CYLS    HEAD     PRECOMP    LANDZ
SECTOR   MODE
Primary Master    : None      0       0      0       0       0        0 -----
Primary Slave     : None      0       0      0       0       0        0 -----
Secondary Master : None       0       0      0       0       0        0 -----
Secondary Slave   : None      0       0      0       0       0        0 -----


Drive A : 1.2M , 5.25 in.                      Base   Memory :    640K
Drive B : None                            Extended Memory :   7168K
                                            Other   Memory :    384K
Video    : EGA/VGA                        -----------------------
Halt On : All Errors                         Total Memory :   8192K

Esc : Quit              ↑↓ → ← : Select Item       Pu/Pd/+/- : Modify
F1   : Help                 (Shift)F2: Change Color
```

In the above table the base memory size and the extended memory size are displayed. This is automatically read from your systems, and you do not need to set these parameters. The screen shows a calendar. The week display will depend on the date set in your system clock and one day will flashing indicating the current date. Since you have not yet set the time and date, the date displayed is probably incorrect. Information on each item is given in the left, with details of the available options for each item and examples of setting.

This option is used to configure the following options:

<u>*Date:</u> Month, Date, and Year, Ranges for each value are listed below in prompt box in the lower left comer of the CMOS Setup Screen.

***Time:** Hour, Minute and Second, Uses 24 hour clock format. i.e., for PM number, add 12 to the hour. You would enter 4:30 PM as 16:30:00.

***Drive C: and Drive D:** The user can choose any of the standard hard disk types from 1 to 46 or he can choose type 47 which is the user definable type. The user must enter the hard disk parameters is he wants to choose the user - definable hard disk per driver, i.e,type 47 may be different for drive C: and for driver D: and you can choose Not Installed for SCSI hard disk. See table 3-4 for printed list of these drive types.

   Type: This is the number designation for a drive with certain identification parameters.

   Cyl: This is the number of cylinders found in the specified drive type.

   Heads: This is the number of cylinders found in the specified drive type.

   WPcom: WPcom is the read delay circuitry which takes into account the timing differences between the inner and outer edges of the surface of the disk platter. The number designates the starting cylinder of the signal.

   Lzone: Lzone is the landing zone of the heads this number determines the cylinder location where the heads will normally park when the system is shut down.

   Size (Capacity): This is the formatted capacity of the drive based on the following formula: (# of heads) X (# of cylinders) X (# of sects) X (512bytes/sects)

***Drive A and Drive B:** The option are 360KB 5.25 in. 1.2KB 5.25 in. 720KB 3.5 in, 1.44MB 3.5 in, 2.88MB 3.5 in and None. Not Installed could be used as an option for diskless workstations.

***Video:** Options are Monochrome, Color 40, VGA/EGA, Color 80.

   Having made all the above setting according to your system configuration, press <ESC> to return to the main menu. If you do not wish to use the advanced setup options you may now save the setting you made in the STANDARD CMOS SETUP by pressing the F10 key or highlight the SAVE SETTINGS AND EXIT item in the main menu. When you save the settings, your system will reboot and these settings will be automatically implemented every time you turn your computer on.

HARD DISK ATTRIBUTES:

Type	Cylinders	Heads	V-P comp	LZone	Sect	Capacity
1	306	4	128	305	17	10
2	615	4	300	615	17	20
3	615	6	300	615	17	30
4	940	8	512	940	17	62
5	940	6	512	940	17	46
6	615	4	65535	615	17	20
7	642	8	256	511	17	30
8	733	5	65535	733	17	30
9	900	15	65535	901	17	112
10	820	3	65535	820	17	20
11	855	5	65535	855	17	35
12	855	7	65535	855	17	49
13	306	8	128	319	17	20
14	733	7	65535	733	17	42
15	000	0	0000	000	00	00
16	612	4	0000	663	17	20
17	977	5	300	977	17	40
18	977	7	65535	977	17	56
19	1024	7	512	1023	17	59

20	733	5	300	732	17	30
21	733	7	300	732	17	42
22	733	5	300	733	17	30
23	306	4	0000	336	17	10
24	977	5	65535	976	17	40
25	1024	9	65535	1023	17	76
26	1224	7	65535	1223	17	71
27	1224	11	65535	1223	17	111
28	1224	15	65535	1223	17	152
29	1024	8	65535	1023	17	68
30	1024	11	65535	1023	17	93
31	918	11	65535	1023	17	83
32	925	9	65535	926	17	69
33	1024	10	65535	1023	17	85
34	1024	12	65535	1023	17	102
35	1024	13	65535	1023	17	110
36	1024	14	65535	1023	17	119
37	1024	2	65535	1023	17	17
38	1024	16	65535	1023	17	136
39	918	15	65535	1023	17	114
40	820	6	65535	820	17	40
41	1024	5	65535	1023	17	42
42	1024	5	65535	1023	26	65
43	809	6	65535	852	17	40
44	809	6	65535	852	26	61
45	776	8	65535	775	33	100
46	684	16	65535	685	38	203

Award Hard Disk Type Table

5-3 BIOS FEATURES SETUP

To access the BIOS setup program, highlight BIOS FEATURES SETUP in the main menu and press <enter> A warring message will appear on your screen and you may press any key to remove this and access the BIOS Features program.

ROM PCI/ISA BIOS (2A4L6J11)
BIOS FEATURES SETUP
AWARD SOFTWARE, INC.

Virus Warning	: Disabled	Video BIOS Shadow	: Enabled
CPU Internal Cache	: Enabled	C8000-CBFFF Shadow	: Disabled
External Cache	: Enabled	CC000-CFFFF Shadow	: Disabled
Quick Power On Self Test	: Disabled	D0000-D3FFF Shadow	: Disabled
Boot Sequence	: A,C	D4000-D7FFF Shadow	: Disabled
Swap Floppy Drive	: Disabled	D8000-DBFFF Shadow	: Disabled
Boot Up Floppy Seek	: Enabled	DC000-DFFFF Shadow	: Disabled
Boot Up Numlock Status	: ON		
Boot Up System Speed	: High		
Gate A20 Option	: Fast		
Memory Parity Check	: Disabled		
Typematic Rate Setting	: Disabled		

28

Typematic Rate (Chars/Sec): 6 Typematic Delay (Msec) : 250 Security Option : Setup IDE Second Channel Control: Enabled	 Esc: Quit ↑↓ → ← : Select Item F1 : Help Pu/Pd/+/-:Modify F5 : Old Values (Shift)F2 : Color F6 : Load BIOS Defaults F7 : Load BIOS Defaults

The BIOS FEATURES SETUP allows you find true certain features supported by the chipset and Award BIOS. It also includes support for shadow RAM under which the contents of he ROM BIOS can be copied into memory at boot up enhancing performance. When you change any of the setting you may recall the default settings at any time from the main menu. This is detailed later. To get help on each item, high the relevant item and press the F1 key. A windows will appear on your screen detailing he various options available for each item. A brief introduction of each of the setting in the BIOS FEATURES SETUP program is given below.

*CPU Internal Cache: This item should always be Enable. If you system is   main board Even if you have installed the external cache. If you have no external cache installed this item should be Enabled to allow use of the internal 8K cache in the 486 CPU.

*External Cache: Enable or Disable this function according to whether you want external cache Enabled or Disabled.

*Boot Sequence: You may define whether the system will look first at drive A: and then at drive C: when booting up or vice versa.

*Boot Up Floppy Seek: You may Enable/Disable this item to define whether the system will look for a floppy disk drive to boot at power-on or directly to the hard disk drive.

*Boot Up NumLock Status: Use to item to Enable/Disable the NumLock on your keyboard automatically at power-on.

*Boot Up System Speed: Select High to configure your system in the turbo speed mode at boot up, select Low to configure your system in normal speed mode. Whichever setting your choose you will still be able to use the turbo switch to toggle between the two modes during use.

*Memory Parity Check: Enable or Disable this item according to whether you wish the system to check the memory parity during boot up or not. If you Disable this item even if the BIOS encounters a parity error it will be ignored. We recommend that you always Enable the item in order to ensure that the memory is good each time you turn your PC on.

*Typematic Rate Setting: Enable this item if you wish to be able to configure the characteristics of your keyboard. Typematic refers to the way in which characters are entered

repeatedly if a key is held down. For example, if you press and hold down the "A" key the letter "a" will repeatedly appear on your screen on your screen on your screen until you release the key. This item is disable by default.

*Typematic Rate (Chars-Sec): You can use this item to define the typematic rate delay of your keyboard. i.e. the rate at which characters will be repeated when a key held down.

5-4 CHIPSET FEATURES SETUP

ROM PCI/ISA BIOS (2A4L6J11)
CMOS SETUP UTILITY
CHIPSET FEATURES SETUP

Decoupled Refresh : Enabled	Onboard local bus IDE : Enabled
Video BIOS Cacheable : Enabled	IDE HDD Block Mode : Enabled
System BIOS Cacheable : Enabled	IDE 32-bit Transfer Mode : Enabled
	IDE Primary Master PIO : Auto
External Cache Scheme : Write Back	IDE Primary Slave PIO : Auto
Combine Alter & Tag Bits : Disabled	2nd IDE Controller : Enabled
CHRDY for ISA Master : Disabled	Onboard Fdd Controller : Enabled
Memory Hole At 15MB Addr.: Disabled	Onboard Serial Port 1 : COM1 at 3F8h
Cache Timing Control : Normal	Onboard Serial Port 2 : COM2 at 2F8h
DRAM Timing Control : Normal	Onboard Parallel Port : 378H
Fast DRAM : Disabled	Onboard Parallel Mode : Normal
Burst Write : Disabled	
CPU Write Back Cache : Disabled	
486 Streaming : Disabled	Esc: Quit ↑↓→←: Select Item
Set Turbo Pin Function : Turbo	F1 : Help Pu/Pd/+/-:Modify
Set Mouse Lock : Disabled	F5 : Old Values (Shift)F2 : Color
	F6 : Load BIOS Defaults
	F7 : Load BIOS Defaults

*Decuple Refresh: Reduce CPU loading. When CPU refresh DRAM, the system performance will be going down, if Enable Decuple Refresh, when DRAM refresh, the system don't hold.

Recommand : **Enable**

*Relocate 256K/384K: If the system install VGA or install add on card, this segment don't relocate.

Recommand : **Enable**

*Video/System BIOS Cacheable: Enable it, that improve system performance.

Recommand : **Enable**

*External Cache Scheme: Write back/through if set write through system can get more performance.

Recommand : **Write back**

*Combine Alter & Tag: Cache schem for improve performance.

Recommand : **Disable**

*Memory Holt At 15MB ADDR.: Separate memory address space, Disable it normally.

Recommand : **Disable**, for some VGA card, need share on board DRAM.

*Cache/DRAM Timing Control: Depend on system installation condition. For Example: If the system use fast DRAM and fast SRAM, modify the timing can get more better performance. If CPU use up 40MHZ CPU frequency, please setup cache time control medium.

Recommand : **Cache/DRAM Normal**, (If use DX4 CPU can set cache time to fast)

*Fast DRAM: If system use fast DRAM Enable this register, get more performance.

Recommand : **Disable**, If the system use DRAM time < 60ns

*Burst Write:

Recommand : **Disable**, If the CPU can support burse write (Ex. DX4)

*CPU Write Back Cache: Cyrix CPU only.

Recommand : **Disable**, (If the CPU is Cyrix, can enable, improve CPU performance)

*486 Streaming: Disable (Default)

Recommand : **Disable**, (If you use Intel P24T CPU enable it)

*Set Turbo Pin Function: This pin is a Multi-Function pin. set to Turbo.

Recommand : **turbo**, If you want to use suspend switch, change to suspend

*Set Mouse Lock: Enbale (Default)

Recommand : **Enable**, If the system don't use PS/2 mouse can release IRQ12 for other device

*Onboard Local Bus IDE: If use onboard IDE, Enable it, please.

Recommand : Use on board IDE please **Enable**

REMARK: If use onboard IDE, please follow this step.
              1. Onboard Local bus IDE Enable.(CMOS features setup)
              2. Save & exit setup.
              3. IDE HDD auto detection.
              4. Save & exit setup

5-5 POWER MANAGEMENT SETUP

    Selecting Power management Setup on the Main menu displays an information windows as following:

ROM PCI/ISA BIOS (2A4L6J11)
CMOS SETUP UTILITY
POWER MANAGEMENT SETUP

Power Management	: Disabled	IRQ3 Activity	: Primary

Doze Timer : 32 sec	IRQ4 Activity : Primary
Sleep Time : 2 min	IRQ5 Activity : Primary
Sleep Mode : Sleep	IRQ7 Activity : Primary
	IRQ8 Activity : Primary
HDD Power Management : Disabled	IRQ10 Activity : Primary
VGA Activity Wakeup : Disabled	IRQ11 Activity : Primary
	IRQ12 Activity : Primary
I/O Activity : Disabled	
	Esc: Quit ↑↓→←: Select Item
	F1 : Help Pu/Pd/+/-:Modify
	F5 : Old Values (Shift)F2 : Color
	F6 : Load BIOS Defaults
	F7 : Load BIOS Defaults

VGA access event:
*IRQ1   (Keyboard)
*IRQ3   (COM2)
*IRQ4   (COM1)
*IRQ5   (Printer LPT2)
*IRQ6   (Floppy Disk)
*IRQ7   (Printer LPT1)
*IRQ9   (Redirect)
*IRQ10   (Reserved)
*IRQ11   (Reserved)
*IRQ12   (PS/2 mouse)
*IRQ14   (Hard Disk) (IDE 1 for J435＆J437 Version)
*IRQ15   (Reserved) (IDE 2 for J435＆J437 Version)

Caution: When the system(J435,J437) use secondary IDE, green function
         have to disable.

5-6 PCI CONFIGURATION SETUP

ROM PCI/ISA BIOS (2A4L6J11)
PCI CONFIGURATION SETUP
AWARD SOFTWARE, INC.

Slot 1 Using INT# : AUTO	CPU to PCI WRITE BUFFER : Enabled
Slot 2 Using INT# : AUTO	PCI Master WRITE BUFFER : Disabled
Slot 3 Using INT# : AUTO	PCI Master PRE-FCH BUFFER: Enabled
	PCI Master BURST READ : Enabled
1st Available IRQ : 10	PCI Dynamic Decoding : Enabled
2nd Available IRQ : 11	VL Bus 0-Wait State Write: Disabled
3rd Available IRQ : 9	FRAME Generation : Normal
PCI IRQ Actived by : Level	Local Memory Detect Point: Fast
PCI IDE IRQ Map to : PCI-AUTO	PCI Burst : Enabled

Primary IDE INT# : A Secondary IDE INT# : B	C2P Fast Back-to-Back : Enabled PCI Master 1 WS Write : Disabled
	Esc: Quit ↑↓→←: Select Item F1 : Help Pu/Pd/+/-:Modify F5 : Old Values (Shift)F2 : Color F6 : Load BIOS Defaults F7 : Load BIOS Defaults

PCI IRQ AND TRIGGER LEVEL SETUP

When system install PCI device in PCI slot,
1. please check PCI slot number, SLOT1, SLOT2, SLOT3.
2. Select slot using INTA OR INTB OR INTC OR INTD, auto, (Default:auto)
3. Select PIRQ using which one IRQ (sequential 1st→2nd→3rd)
4. Select trigger level (edge or level) (Default:level)
   NOTE: If use PCI VGA don't care which one slot and IRQ.

CPU TO PCI WRITE BUFFER

The buffers will improve significantly the system performance because the cycle to PCI slave can be terminated immediately after one or two CPU wait states.

Recommand : **Enable**

PCI MASTER WRITE BUFFER

PCI master byte and word to be merged into Dword. So it will improve efficiency of the data transaction.

Recommand : **Disable**, but it device support Byte Merge can Enable

PCI MASTER PRE-FCH BUFFER READ

This prefeching is effective only for non-locked memory-read cycle when a read to local memory is issued, up to 3 additional qword may be read and stored into buffers. Both the single and burst mode cycle will perform the prefectching function.

Recommand : **Enable**

PCI MASTER BURST READ

PCI device read from local memory, normal read cycle have inster wait state, if burst read enable, the read cycle will generation continue address, can improve PCI device to system performance.

Recommand : **Enable**

PCI DYNAMIC DECODING

When the system power on, system will scanning PCI device, check whitch device on PCI bus, initialize the device. If the write buffer enable already, you can turn on this dynamic decoding, others condition disable it.

Recommand : **Enable**

LOCAL BUS 0 WS WRITE

Local bus waite state, if Enable it, Local bus run in 0 wait state. Disable it, the system local bus run in 1 wait state. If use VL/IDE device please caution you device time, if low speed device please don't Enable this bit.

Recommand : **Enable**

FRAME GENERATION

PCI master device read a data from/write a data to local memory, PCI bus timing setting. If set it fast, the PCI bus between frame to frame just one access cycle. If set it normal, the PCI bus between frame to frame addition one access cycle.

Recommand : **Normal**

CPU TO PCI FAST BACK TO BACK

Back to back mode Enable can improve system performance. CPU to PCI bus cycle Enable the bus cycle will be shorten, and bus arbitration change fast.

Recommand : **Enable**

PCI MASTER 1 WS WRITE

PCI master write to system 1 wait state. If Disable it, the maste zero wait state to system.

5-7 LOAD BIOS DEFAULTS

Auto Configuration with BIOS Defaults

This Main Menu item loads the default BIOS values. If the CMOS is corrupted the defaults are loaded automatically. Choose this item and the following message appears.

" Load BIOS Default (Y/N)? Y "

To use the BIOS defaults change the prompt to "Y" and press <Enter>. The CMOS is load automatically form BIOS default values:

5-8 LOAD SETUP DEFAULTS

Auto Configuration with Setup Defaults

This Main Menu item uses the default SETUP values. Use this option as a diagnostic and of your system behaves erratically. Choose this item and the following message appears:

" Load SETUP Default (Y/N)? Y "

To use the SETUP defaults change the prompt to "Y" and press <Enter>. The CMOS is load automatically form SETUP default values:

5-9 PASSWORD SETTING

In the Advance CMOS SETUP Program is an item to allow you to Enable/Disable the password checking option. When Enable a password must be typed in each time the system boots up or each time you wish to access the setup program. If you Enable this item you should select PASSWORD SETTING in the main menu to type in the password you wish to use. The default password is Award so the first time you select Password setting the following message appear:

" Enter Password: "

You will than be prompted to enter the new password. You may type in up to six characters for your password and then press <Enter>. You will be asked to verify the password and then this password will be stored in the CMOS and must be entered every time you boot up your system or access the setup program. You have three chances to enter the correct password. If you fail to enter the correct password on the third attempt the system will hang. In case you forget your password and cannot enter the setup program to change it you will have to discharge the on-board battery to clear the information stored in the CMOS RAM before you will be able to access your system.

5-10 SAVING YOUR SETTING

When you have completed adjusting all the settings as required, you must have these setting into the CMOS RAM Select SAVE & EXIT and press <Enter> when you confirm that you wish to save settings your machine will be automatically rebooted and the changes you have made will be implemented. You may call up the setup program at any time to adjust any of the individual items by pressing the <Del> key during boot up. If wish to cancel any changes you have made select EXIT WITHOUT SAVING and the original setting stored in the CMOS will be retained.

CHAPTER 6

6-1 EASY MAINTAIN

The J435,J437 mainboards is designed by JET-WAY R&D department, include Integrated X-Bus Peripherals and VT82C505 PCI bridge. It supports both VESA/ISA and PCI bus, and power management function of many different CPUs including INTEL non S series CPU that has no SMM mode. The P24T, P24D and Cyrix M7 which have internal write back cache are also supported.

6-2 SPECIFICATIONS

- Chipset: VT82C496G Green PC single chip
            VT82C406MV Integrated X-Bus Peripherals
            VT82C505 VESA to PCI bridge (J437)

- Bus: 4 ISA slots (16bit).
            2 VESA slots (any one of them can be VESA master)
            3 PCI slots (all of them can be PCI master)

- CPU type: PGA CPU
            Intel 80486SX/DX/DX2/DX4, 80487SX, OverDrive, 80486 S series,
            P24T, P24C, P24D and Cyrix M6/M7, AMD 486 DXL,
            There is a 3.3V generation circuit for P24C CPU.

```
 ┌─────────────────┐        ┌─────────────────┐
 │ CPU Interface   │        │ ISA System      │
 │ VL Bus Controller│       │ Controller      │
 │ Cache Controller│        │                 │
 │ DRAM Controller │        │                 │
 └────────┬────────┘        └────────┬────────┘
          ↕                          ↕
 ┌────────┴────────┐        ┌────────┴────────┐
 │ Power           │        │ IDE             │
 │ Management      │        │ Accelerator     │
 │ Unit            │        │                 │
 └─────────────────┘        └─────────────────┘
```
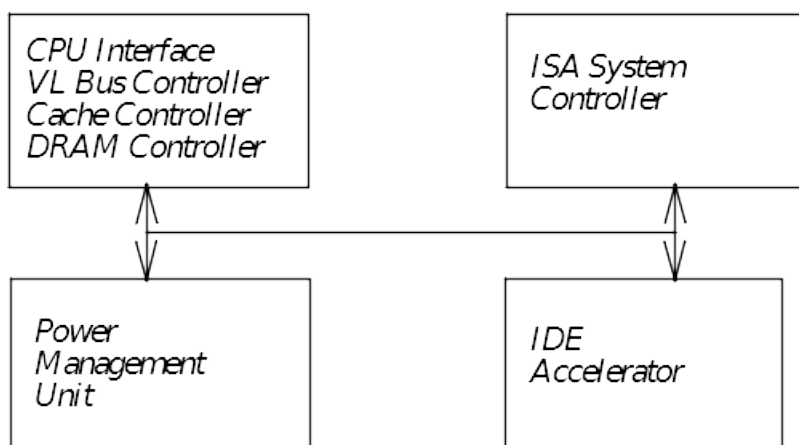
VT82C496G Function Block Diagram
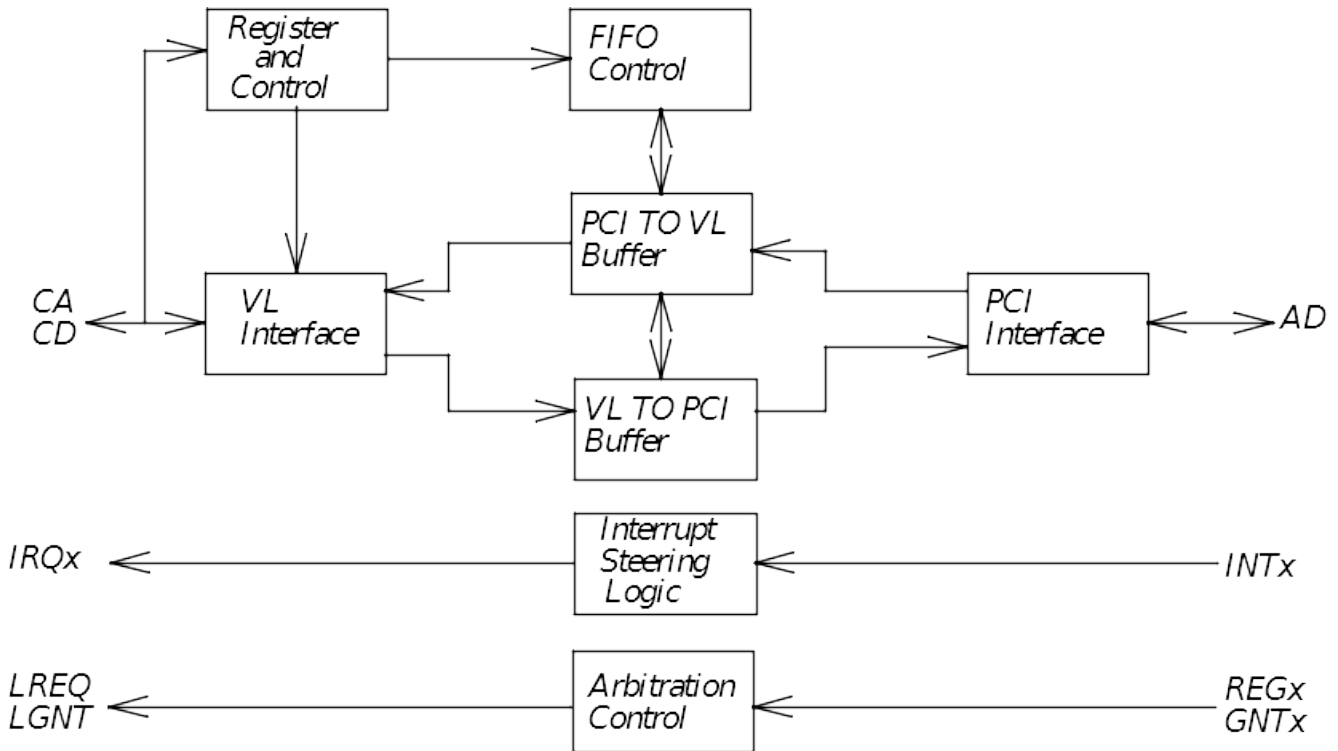
VT82C505 Functional Block Diagram

VT82C496G Pin Out in Numerical Order

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VSS	53	CD15	105	BE#3	157	LDEV#0
2	A3SEL0	54	CD14	106	BE#2	158	LDEV#1
3	A3SEL1	55	CD13	107	BE#1	159	LGNT#0
4	CWE#0	56	CD12	108	BE#0	160	LREQ#0
5	CWE#1	57	CD11	109	ADS#	161	LRDY#
6	CBOE#0	58	CD10	110	MIO#	162	CLKIN
7	CBOE#1	59	BRDY#	111	WR#	163	RTCAS
8	CCS#0	60	VSS	112	SMIACT#	164	VSS
9	CCS#1	61	VDD	113	READY#	165	VDD
10	VDD	62	CD9	114	VDD	166	XD7

11	TA0	63	CD8	115	HITM#	167	XD6
12	TA1	64	CD7	116	FLUSH#	168	XD5
13	TA2	65	CD6	117	STPCLK#	169	XD4
14	TA3	66	CD5	118	CPUCLKO	170	XD3
15	VSS	67	CD4	119	VSS	171	XD2
16	TA4	68	CD3	120	DC#	172	XD1
17	TA5	69	CD2	121	CD31	173	XD0
18	TA6	70	CD1	122	CD30	174	DACEN
19	TA7	71	CD0	123	CD29	175	IOR#
20	CWE#2	72	BLAST#	124	CD28	176	IOW#
21	CWE#3	73	KEN#	125	CD27	177	IO16#
22	RAS#0	74	IGNNE#	126	CD26	178	MS16#
23	RAS#1	75	FERR#	127	CD25	179	BLSEL#
24	MA0	76	A20M#	128	CD24	180	BHSEL#
25	MA1	77	NMI	129	CD23	181	MEMR#
26	MA2	78	CA26	130	CD22	182	MEMW#
27	MA3	79	CA25	131	CD21	183	REFRESH#
28	VDD	80	CA24	132	CD20	184	IOCHRDY#
29	VSS	81	CA23	133	CD19	185	VDD
30	MA4	82	CA22	134	CD18	186	VSS
31	MA5	83	CA21	135	CD17	187	OSC
32	MA6	84	CA20	136	CD16	188	AEN
33	MA7	85	CA19	137	CPURST	189	MASTER#
34	MPD0	86	CA18	138	EADS#	190	TC
35	MPD1	87	CA17	139	HOLD	191	INTR
36	MPD2	88	CA16	140	HLDA	192	XDIR
37	MPD3	89	CA15	141	SMI#	193	SPKR
38	VSS	90	CA14	142	VSS	194	SCANIN
39	MA8	91	CA13	143	INIT	195	SCANOUT
40	MA9	92	CA12	144	RESET#	196	SA7
41	MA10	93	CA11	145	CPUCLKI	197	SA6
42	VDD	94	CA10	146	PWGOOD	198	SA5
43	VDD	95	CA9	147	VDD	199	SA4
44	VSS	96	VSS	148	MAMUX#	200	VSS
45	CAS#0	97	VDD	149	SD15	201	VDD
46	CAS#1	98	CA8	150	SD14	202	SA3
47	CAS#2	99	CA7	151	SD13	203	SA2
48	CAS#3	100	CA6	152	SD12	204	SA1
49	RAS#2	101	CA5	153	SD11	205	SA0
50	RAS#3	102	CA4	154	SD10	206	SBEHE#
51	TAGWE#	103	CA3	155	SD9	207	BALE
52	WE#	104	CA2	156	SD8	208	SYSCLK

VT82C505 Pin Out in Numerical Order

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	ADS#	41	CD8	81	CD19	121	LOCK#
2	MIO#	42	CD9	82	CD20	122	AD17
3	WR#	43	CD10	83	CD21	123	AD18
4	DC#	44	CD11	84	CD22	124	AD19
5	SERR#	45	VDD	85	CD23	125	AD20
6	BE#0	46	FRAME#	86	AD8	126	AD21
7	BE#1	47	AD0	87	AD9	127	VDD
8	BE#2	48	AD1	88	AD10	128	REQ#1
9	BE#3	49	AD2	89	AD11	129	REQ#0
10	VSS	50	VSS	90	VSS	130	VSS
11	C/BE#0	51	AD3	91	AD12	131	AD22
12	C/BE#1	52	AD4	92	AD13	132	AD23
13	C/BE#2	53	AD5	93	AD14	133	AD24
14	C/BE#3	54	AD6	94	AD15	134	AD25
15	INTC#	55	AD7	95	AD16	135	AD26

16	INTD#	56	CD12	96	BRDY#	136	EADS#
17	CD0	57	CD13	97	NMI	137	TRDY#
18	CD1	58	CD14	98	INTA#	138	PERR#
19	CD2	59	CD15	99	INTB#	139	PAR
20	VDD	60	CD16	100	VDD	140	VSS
21	CD3	61	CD17	101	WBACK#	141	DEVSEL#
22	CD4	62	CA16	102	IRQ14	142	STOP#
23	CD5	63	CA17	103	RDYRTN#	143	IRQ5
24	CA2	64	CA18	104	LDEVI#	144	IRQ9
25	CA3	65	CA19	105	LRDY#	145	IRQ10
26	CA4	66	CA20	106	CD24	146	IRQ11
27	CA5	67	CA21	107	CD25	147	IRQ15
28	CA6	68	CA22	108	CD26	148	BLAST#
29	CA7	69	CA23	109	CD27	149	CCLK
30	VSS	70	VSS	110	VSS	150	VSS
31	CA8	71	CA24	111	CD28	151	PCLK
32	CA9	72	CA25	112	CD29	152	RESET#
33	CA10	73	VDD	113	CD30	153	VDD
34	CA11	74	CA26	114	CD31	154	AD27
35	CA12	75	CA27	115	LDEVO#	155	AD28
36	CA13	76	CA28	116	LREQO#	156	AD29
37	CA14	77	CA29	117	LGNTI#	157	AD30
38	CA15	78	CA30	118	GNT#0	158	ADD31
39	CD6	79	CA31	119	GNT#1	159	REQ#3
40	CD7	80	CD18	120	GNT#3	160	IRDY#
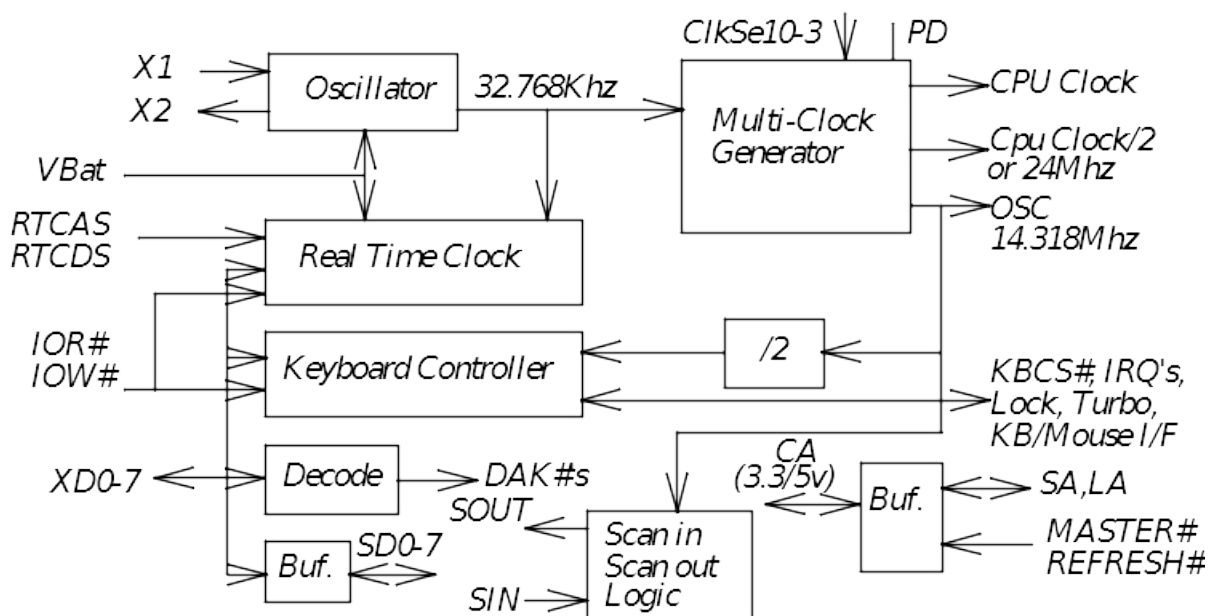
VT82C406MV Block Diagram

VT82C406MV Pin Order for the Standard Mode

The standard mode: pin 4 and pin 3 are sampled high at reset.

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VSS	31	VDD_3_5V	51	VSS	81	XD2
2	RTCDS#	32	CA15	52	RTCRW	82	XD1
3	KBCS#	33	CA14	53	XDIR	83	XD0
4	IRQ#8	34	CA13	54	SA14	84	SA12
5	VDD	35	CA12	55	SA13	85	SA11
6	RESET#	36	CA11	56	Pull-down	86	SA10
7	PS2MODE	37	CA10	57	RCKG	87	SA9
8	KBLOCK	38	CA9	58	MSLOCK	88	SA8
9	KBTURBO	39	CA8	59	A20Gate	89	VSS
10	KBCLK	40	SA2	60	IRQ12	90	RTCAS
11	KBDATA	41	VDD	61	IRQ1	91	IOR#
12	MSCLK	42	LA19	62	KBRC#	92	IOW#
13	MSDATA	43	LA18	63	SD7	93	CPUCLK
14	LA23	44	LA17	64	SD6	94	24Mhz
15	LA22	45	SA16	65	SD5	95	PD
16	LA21	46	SA15	66	SD4	96	VSS
17	LA20	47	RP13	67	SD3	97	VBAT
18	CLKSEL0	48	RP14	68	VSS	98	VDD_RTC
19	CLKSEL1	49	RP15	69	OCS	99	RTCX1
20	CLKSEL2	50	RP16	70	MASTER#	100	RTCX2
21	CLKSEL3			71	REFRESH#		
22	CA23			72	VDD		
23	CA22			73	SD2		
24	CA21			74	SD1		
25	CA20			75	SD0		
26	CA19			76	XD7		
27	CA18			77	XD6		
28	CA17			78	XD5		
29	CA16			79	XD4		
30	VSS			80	XD3		

6-3 BIOS REFERENCE-POST CODES

When the system is powered on, the BIOS will perform diagnostics and initialize all system components, including the video system.

All errors found by the BIOS will be put in I/O port 80H. (By installing the post code display card, the post codes can be displayed.)

POST	Name	Description
CO	Turn Off Chipset Cache	OEM Specific-Cache controller.
1	Processor Test 1	Processor Status (1 FLAGS) Verification. Tests the following processor status flags carry, zero, sign, overflow. The BIOS will set each of these flags, verify the are set, then turn each flag off and verify it is off.
2	Processor Test 2	Read/ Write/ Verify all CPU registers except SS, SP, and BP with data pattern FF and OO.
3	Initialize Chips	Disable NMI, PIE, AIE, UEI, SOWV. Disable video, parity checking, DMA. Reset math coprocessor. Clear all page registers, CMOS shutdown byte. Initialize timer 0, 1, and 2, including set EISA timer

		to a known state. Initialize DMA Controllers 0 and 1. Initialize interrupt controllers 0 and 1. Initialize EISA extended registers.
4	Test Memory Refresh Toggle	RAM must be periodically refreshed inorder to keep the memory from decaying. This function assures that the memory refresh function is working properly.
5	Blank video, Initialize keyboard	Keyboard controller initialization.
6	Reserved	
7	Test CMOS Interface and Battery Status	Verifies CMOS is working correctly, detects bad battery.

BE	Chipset Default Initialization	Program chipset registers with power on BIOS defaults.
C1	Memory presence test	OEM Specific-Test to size on-board memory.
C5	Early Shadow	OEM Specific-Early Shadow enable for fast boot.
C6	Cache presence test	External cache size detection.
8	Setup low memory	Early chip set initialization. Memory presence test. OEM chip set routines. Clear low 64K of memory. Test first 64K memory.
9	Early Cache Initialization	Cyrix CPU initialization. Cache initialization.
A	Setup Interrupt Vector Table	Initialization first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize INT 00h-1Fh according to INT_TBL
B	Test CMOS RAM Checksum	Test CMOS RAM Checksum, if bad, or insert key pressed, load defaults.
C	Initialize keyboard	Detect type of keyboard controller (optional) Set NUM_LOCK status.
D	Initialize Video Interface	Detect CPU clock. Read CMOS location 14h to find out type of video in use. Detect and Initialize Video Adapter.
E	Test Video Memory	Test video memory, write sign-on message to screen. Setup shadow RAM.Enable shadow according to Setup.
F	Test DMA Controller 0	BIOS checksum test. Keyboard detect and initialization.
10	Test DMA Controller 1	
11	Test DMA Page	Test DMA Page Registers.

	Registers	
12-13	Reserved	
14	Test Timer Counter 2	Test 8254 Timer 0 Counter 2.
15	Test 8259-1 Mask Bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.

16	Test 8259-2 Mask Bits	Verify 8259 Channel 2 masked interrupts by alternately turning off and on the interrupt lines.
17	Test Stuck 8259's Interrupt Bits	Turn off interrupts then verify no interrupt mask register is on.
18	Test 8259 Interrupt Functionality	Force an interrupt and verify the interrupt occurred.
19	Test Stuck NMI Bits (Parity I/O Check)	Verity NMI can be cleared.
1A		Display CPU clock.
1B-1E	Reserved	
1F	Set EISA Mode	If EISA non-volatile memory checksum is good, execute EISA initialization. If not, execute ISA tests an clear EISA mode flag. Test EISA Configuration Memory Integrity (checksum & communication interface).
20	Enable Slot 0	Initialization slot 0 (System Board).
21-2F	Enable Slot 1-15	Initialize slot 1 through 15.
30	Size Base and Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB.
31	Test Base and Extended Memory	Test base memory from 256K to 640K and extended memory above 1MB using various patterns. NOTE: This will be skipped in EISA mode and can be "skipped" with ESC key in ISA mode.
32	Test EISA Extended Memory	If EISA Mode flag is set then test EISA memory found in slots initialization. NOTE: This will be skipped in ISA mode and can be "skipped" with ESC key in EISA mode.
33-3B	Reserved	
3C	Setup Enabled	
3D	Initialize & install Mouse	Detect if mouse is present, initialize mouse, install interrupt vectors.
3E	Setup Cache Controller	Initialize cache controller.
3F	Reserved	

BF	Chipset Initialization	Program chipset registers with Setup values.
40		Display virus protest disable or enable.

41	Initialize Floppy Drive & Controller	Initialize floppy disk drive controller and drives.
42	Initialize Hard Drive & controller	Initialize hard drive controller and any drives.
43	Detect & Initialize Serial/Parallel Ports	Initialize any serial and parallel ports (also game port).
44	Reserved	
45	Detect & Initialize Math Coprocessor	Initialize math coprocessor.
46	Reserved	
47	Reserved	
48-4D	Reserved	
4E	Manufacturing POST Loop or Display Messages	Reboot if Manufacturing POST Loop pin is set. Otherwise display any messages (i.e., any non-fatal errors that were detected during POST) and enter Setup.
4F	Security Check	Ask password security (optional).
50	Write CMOS	Write all CMOS values back to RAM and clear screen.
51	Pre-boot Enable	Enable parity checker. Enable NMI, Enable cache before boot.
52	Initialize Option ROMs	Initialize any option ROMs present from C8OOOh to EFFFFh. NOTE: When FSCAN option is enabled, will initialize from C8OOOh to F7FFFh.
53	Initialize Time Value	Initialize time value in 40h:BIOS area.
60	Setup Virus Protect	Setup virus protect according to Setup.
61	Set Boot Speed	Set system speed for boot.
62	Setup Num Lock	Setup Num Lock status according to Setup.
63	Boot Attempt	Set low stack. Boot via INT 19h.
B0	Spurious	If interrupt occurs in protected mode.
B1	Unclaimed NMI	If unmasked NMI occurs, display. Press F1 to disable NMI, F2 reboot.
E1-EF	Setup Pages	E1-Page 1, E2-Page 2, etc.
FF	Boot	

CHAPTER 7

7-1 PERFORMANCE REPORT

CPU BRAND & TYPE	LAND MARK SYSTEM SPEED TEST V2.0 CPU:(MHz) FPU: (MHz)	POWER METER V1.81 CPU:(MIPS)	NORTON UTILITY SYSINFO V8.0 CPU SPEED: PERFORMANCE:

Intel 80486DX4 -100	361.66	814.88	30.3	197.1	135.0
Intel 80486DX2 -66	222.02	543.21	21.4	143.4	98.7
Cyrix Cx486DX2 -V66	218.92	589.76	19.2	112.7	78.7
Cyrix Cx486DX -V80	263.90	768.37	22.2	135.0	93.6
Cyrix Cx486DX -V33	109.45	294.86	9.6	56.3	40.5
Intel 80486DX -33	110.45	271.31	10.6	71.7	50.8
Cyrix Cx486DX -V40	131.95	355.48	11.6	67.9	48.7
AMD Am486DX -40	133.70	327.09	12.6	86.4	60.9

7-2 GENERAL UTILITY TEST

MS-DOS			
PROGRAM	VERSION	TIMES	RESULT PASS/FAIL
ET	3.51	1	PASS
CELEM CACHE TEST	1.0	1	PASS
QAPLUS	4.6	1	PASS
AUTO CAD	R10	1	PASS
AUTO CAD	R11	1	PASS
ORCAD	3.1	1	PASS

WINDOWS			
PROGRAM	VERSION	TIMES	RESULT PASS/FAIL
SPEEDY	1.0	1HR	PASS
DESIGER	3.01	1	PASS
QAPLUS FOR WINDOWS	5.0	1	PASS
WIN BENCH	3.11	1	PASS
WIN BENCH	4.0	1	PASS

7-3 SOFTWARE RELIABILITY TEST

STEP1.

PROGRAM	VERSION	LOOP/TIMES	RESULT/PASS FAIL
QAPLUS	4.52	1	PASS
QAPLUS	5.13	1	PASS
CHECKIT PRO	3.0	1	PASS
WINDOWS	3.1	1	PASS
AUTO CAD	2.6	1	PASS
WINSTON	1.0	1	PASS 34.6(SCORE)

STEP2.

PROGRAM	VERSION	TIMES	RESULT/PASS FAIL
OS/2 ENGLISH	2.0	1	PASS
INSTALL WINDOWS	3.1	1	PASS

STEP3.

PROGRAM	VERSION	TIMES	RESULT/PASS FAIL
DOS PC BENCH	8.0	1	PASS
	PROC:20.41 DISK:723.00 VIDEO:908.32 DOS MARK:304.90		
WINDOWS BAPCO	'93	1	PASS

STEP4.

PROGRAM	VERSION	TIMES	RESULT/PASS FAIL
WINDOW NT	3.1	1	PASS
NETWARE	3.11	1	PASS

STEP5.

PROGRAM	VERSION	TIMES	RESULT/PASS FAIL
OS/2 CHINES	2.1T	1	PASS
WINDOWS CHINES	3.1	1	PASS

7-4 ADD ON CARD COMPATIBLE TEST

VGA	CHIP BRAND	BUS TYPE	TOTAL DRAM	RESOLUTION	RESULT PASS/FAIL
1	CIRRUS GD-5434	PCI	1MGB	WIN 1024*768	PASS
2	CIRRUS GD-5430	PCI	1MGB	WIN 1024*768	PASS
3	S3-864	PCI	2MGB	3D-STUDIO V3.0	PASS
4	MX 86010	ISA	1MGB	WIN 640*480	PASS
5	WDC 90C30	ISA	1MGB	GAME 640*480	PASS
6	TRIDEN 8900	ISA	1MGB	GAME 640*480	PASS
7	TSENG ET-4000	PCI	2MGB	WIN 1240*1024*256C	PASS
8	AV-LOGIC ALG-2301	PCI	1MGB	ACAD-R10	PASS

IDE	CHIP BRAND	BUS TYPE	HDD TYPE	RESULT PASS/FAIL
1	ACER	ISA	ST-3660A SEAGATE	PASS
2	ON-BOARD	ISA	7245AT MAXTOR	PASS
3	GOLD STAR	ISA	CP30084E CONNER	PASS
4	ADD2 90C50	VL-BUS	ST-3660A SEAGATE	PASS

SOUND	CHIP BRAND	BUS TYPE 16/8	OPL3/OPL4

MOZART	OAK OTI601	16 BIT	OPL4

LAN	CHIP BRAND	BIS TYPE 16/8	OS
NE2000	UK0022	16 BIT	NOVELL

SCSI	CHIP BRAND	BIS TYPE 16/8	MEMO
BUS LOGIC	82C20	16 BIT	NA