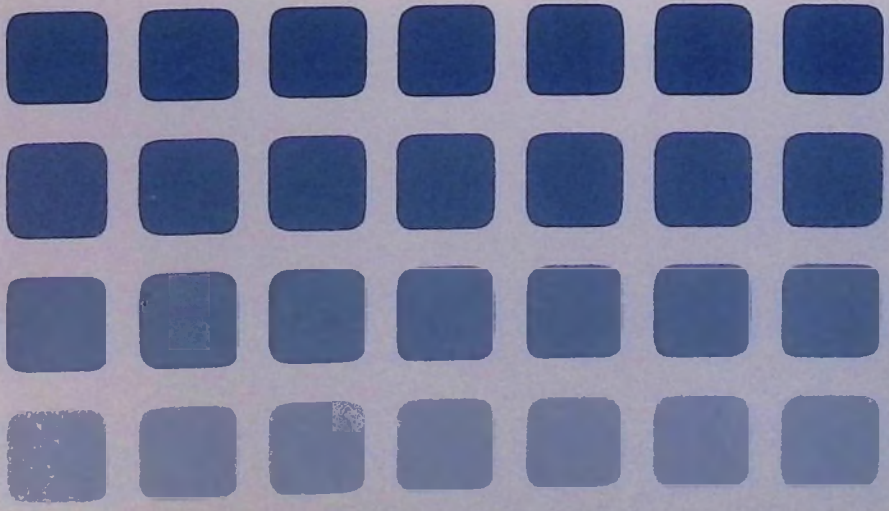
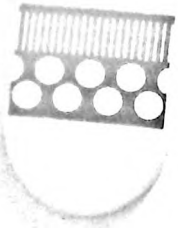
BABY-286
MOTHER BOARD
USERS MANUAL





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CHAPTER I

GENERAL DESCRIPTION

1. FEATURES OF THE ATBABY MOTHER BOARD.

This preliminary manual presents introductory, usage information on the ATBABY Motherboard. The user should also refer to the iAPX 286 Data Sheet, the iAPX 286 Programmer's Reference Manual, and the iAPX 286 Hardware Reference Manual. These are available from the Intel Literature Department in Santa Clara, Ca. Also of use is the IBMDOS 3.1 Manual and the IBM Technical Reference Manual. Installation and Setup Manual, and Guide to Operations for the IBM PC AT. This manual is divided into chapters and appendices with contents as follows:

Chapter I gives a general theory of operation, and a set of Hardware and interface specifications for the ATBABY board.

Chapter II describes the installation procedure for the ATBABY board when upgrading a system, as well as building a new system.

Chapter III describes the bios supplied with the ATBABY board. The chapter also describes the default memory map and I/O procedures for the ATBABY board.

Chapter V discusses ATBABY compatibility with the IBM PC AT as well as other IBM Personal Computers.

Appendix A lists some recommended reference material.

Appendix B chipset technical information.

2. GENERAL THEORY OF OPERATION

ATBABY is a single board computer offering the best features of the IBM PC family. ATBABY is 100% compatible with the IBM PC/AT. A program which runs on the AT should run on ATBABY without modification. The board supports MS-DOS 3.1 or later, Xenix 286, and RMS-286. ATBABY provides. Switch selectable clock speed allows 6, 8, 10 Mhz operation (12 Mhz is optignal). Free expansion slots for application-specific boards. A Time-of-Day Clock is standard. Up to 8 expansion slots are provided 6 AT Compatible (16 bit) and 2 XT (PC) Compatible (8 bit), 512K bytes of memory is standard (RAM expansion on board to one megabyte using expansion memory module).

The ATBABY board is approximately 33 by 22 cm and uses very large scale integration (VLSI) technology. Gate array technology is used wherever possbile to save 63 chips over the equivalent IBM PC AT design. These same gate arrays allow the system to run at speeds of up to 10 Mhz.

ATBAB' ' use the same CPU (80286) and hardware architecture as the PC/AT. The expansion slots accept add-on boards compatible with the IBM PC/AT. The user can run applications designed for the PC/AT on ATBABY without modification.

This critical compatibility allows the user to capitalize on the great mass of IBM PC/AT software and hardware products available today.

ATBABY is on the IBM PC (and PC/XT) form factor. ATBABY boards are identical to the PC/XT main board in size and connector arrangement. The I/O slots can be PC or PC/XT spacing Cyielding 7 or 8 I/O slots. The smaller board allows upgrades to present 8088

systems and compact system design.

The ATBABY board has the following components:

- Intel 80286 Microprocessor
- 7 Channel Direct Memory Access (DMA) using 2 8237A-5s
- 16-level interrupt using 2 8259 A-2 interrupt controllers
- System clock, bus clock, timing using CTI 82C201
- Three programmable timers using 8254 timer chip
- 128Kb read-only memory (ROM) subsystem
- 512Kb random-access memory (RAM) subsystem expandable to one megabyte on-board
- Speaker
- Complementary metal oxide semiconductor (CMOS) memory (RAM) to mantain system configuration
- Real Time clock calendar
- Battery backup for CMOS configuration table and Real-Time Clock
- Keyboard interace processor (8042)
- 7 or 8 (XT/AT version) input/output (I/O) slots:
  5 with a 36 Pin and a 62-pin card-edge connector
  2 or 3 with only the 62-pin card-edge connector

3. CPU SECTION

The Intel 80286 Microprocessor has a 24-bit address, 16-bit memory interface, an extensive instruction set, DMA and interrupt support capabilities, a hardware fixed-point multiply and divide, integrated memory management, four Level memory protection, a 1-gigabyte (1,073,741,824 bytes) virtual address space for each task, and two operating modes: the 8088 compatible real-address mode and the protected virtual-address mode.

In the real-address mode, the microprocessor's physical momory is a contiguous array of up to one megabyte. The micropocessor addresses memory by generating 20-bit physical addresses. The selector portion of memory address pointer is interpreted as the upper 16 bits of a 20 bit segement address. The lower 4 bits of the 20-bit segement address are always zero. Segment addresses begin on multiples of 16 bytes. All segments in the real-address mode are 64Kb in size and may be read, written, or executed. An exception or interupt can occur if data operands or instructions attempt to warp around the end of a segment; for example, a word with it's low-order byte at offset FFFF and it's high-order byte at 0000.

If, in the real-address mode, the information conteined in segment does not use the full 64Kb, the unused end of the segment may be overlayed by another segment to reduce physical memory requirements.

Protected mode offers extended physical and virtual memory address space, memory protection mechanisms, and new operations to support sophisticated operating systems and virtual memory. Protected mode provides a 1-gigabyte virtual address space per task mapped into a 16-megabyte physical address space. The virtual address space may be larger than the physical address space, because any use of a address that does not map to a phusical memory locations will cause a restartable interrupt trap. More detailed descriptions of the microprocessor may be found in the publications listed in the APPENDIX A of this manual.

4. SYSTEM PERFORMANCE

At 8 Mhz 80286 CPU is standard on the ATBABY board. This speed CPU provides nearly 50% more performance than the standard

6 Mhz IBM product. The 10 Mhz board option provides nearly twice the performance. Norton's Utillities SI performance analyzer rates the 8 Mhz ATBABY board at 7.1 times a IBM PC XT, and the 10 Mhz board at 9.2 times an XT's performance.

At 6 Mhz the 80286 microprocessor has a clock cycle time of 167 nanoseconds. A bus cycle requires three clock cycles (which includes 1 wait state) so that a 500-nanoseconds, 16-bit, microprocessor cycle time is achieved. 8-bit bus operations to 8-bit devices take 6 clock cycles (which include 4 wait states), resulting in a 1000-nanosecond microprocessor cycle. 16-bit bus operations to 8-bit devices take 12 clock cycles (which include 10 I/O wait states resulting in a 2000 nanosecond microprocessor cycle.

At 8 Mhz the 80286 microprocessor has a clock cycle time of 125 nanoseconds. A bus cycle requires three clock cycles (which includes 1 wait state) so that a 375-nanoseconds, 16-bit, microprocessor cycle time is achieved. 8 bit bus operations to 8-bit devices take 6 clock cycles (which include 4 wait states), resulting in a 750-nanosecond microprocessor cycle. 16-bit bus operations to 8-bit devices take 12 clock cycles (which include 10 I/O wait states) resulting in a 1500 nanosecond microprocessor cycle.

At 10 Mhz the 80286 microprocessor has a clock cycle time of 100 nanoseconds. A bus cycle requires three clock cycles (which includes 1 wait state) so that a 300-nanoseconds, 16-bit, microprocessor cycle time is achieved. 8-bit bus operations to 8-bit devices take 6 clock cycles (which include 4 wait states), resulting in a 600-nanosecond microprocessor cycle. 16-bit bus operations to 8-bit devices take 12 clock cycles (which include 10 I/O wait states resulting in a 1200 nanosecond microprocessor cycle.

The refresh controller operates at the CPU clock speed. Each

refresh cycle requires 5 clock cycles to refresh all of the systems's dynamic memory; 256 refresh cycles are required every 4 milliseconds. The following formula determines the percent of bandwidth used for refresh.

$$\%\ \text{Bandwidth used for Refresh} = \frac{5\ \text{cycles} \times 256}{4\ \text{ms/Tcpu ns}}$$

At 6 Mhz the refresh overhead is 5.3%, while the overhead falls to 4% at 8 Mhz and 3.2% at 10 Mhz. Refresh is provided by gate array logic, and doesn't use a channel from the DMA controllers.

5. DMA

The DMA controller operates at half the CPU speed, which results in a clock cycle time of 333 nanoseconds at 6 Mhz, 250 nanoseconds at 8 Mhz, and 200 nanoseconds at 10 Mhz. All DMA data transfer bus cycles are five clock cycles or 1.6 microseconds at 6 Mhz, 1.25 microseconds at 8 Mhz, and 1.0 microseconds at 10 Mhz. Cycles spent in the transfer of bus control are not included. DMA channels 0, 1, 2, and 3 are used for 8-bit data transfers, and channels 5, 6, and 7 process 16-bit transfers. Channel 4 is used to cascade channels 0 through 3 to the microprocessor. DMA page register addresses are:

Page Register	Hex I/O Address
Channel 0	0087
Channel 1	0083
Channel 2	0081
Channel 3	0082
Channel 5	008B
Channel 6	0089

Channel 7	008A
Refresh	008F

Source	DMA Page Registers	8237A-5
Address	A23 - - - - - - - - A16	A15 - - - - - - - - A0

Addresses generation for DMA Channels 3 though 0

Source	DMA Page Registers	8237A-5
Address	A23 - - - - - - - - A17	A16 - - - - - - - - A1

DMA channels 5 through 7 perform 16-bit data transfers to 16 bit memory or I/O devices. DMA memory transfers made with channels 5 through 7 must occur on even-byte boundaries. The base address for these channels is programmed with the real address divided by 2. Base word count for channels 5 through 7 is programmed with the number of 16-bit words to be transferred.
Command codes for DMA are:

Hex Address	Command Codes
OC0	CH0 base and current address
OC2	CH0 base and current word count
OC4	CH1 base and current address
OC6	CH1 base and current word count
OC8	CH2 base and current address
OCA	CH2 base and current word count
OCC	CH3 base and current address
OCE	CH3 base and current word count
OD0	Read Status Register/Write Command Register
OD2	Write Request Register
OD4	Write Single Mask Register Bit
OD6	Write Model Register
OD8	Clear Byte Pointer Flip-Flop
ODA	Read temprary Register/Write Master Clear

ODC	Clear Mask Register
ODE	Write All Mask Register Bits

6. SYSTEMS TIMERS

The system has three programmable timer/counters controlled by an 8254-2 timer/counter chip and defined as channel 0 through 2 as follows:

Channel 0	Systems Timer
Gate 0	Tied on
CLK IN 0	1.190 MHz OSC
CLK OUT 0	8259 IRQ O
Chanel 1	Refresh Request Generater
CLK IN 1	1.190 MHz OSC
CLK OUT 1	Request Refresh Cycle
Channel 1	is a 15 microsecond rate generator.
Channel 2	Tone Generater for Speaker
Gate 2	Controlled bv bit 0 of port 61H
CLK IN 2	1.190 MHz OSC
CLK OUT 2	Used to drive the speaker

7. SYSTEMS INTERRUPTS

NMI and two 8259A Interrupt Controller chips provide 16 levels of system interrupts. The following shows the interrupt assignments in descending priority:

NMI	Parity or I/O Ch Ck
CTLR 1	CTLR2
IRQ 0	Timer Out 0
IRQ 1	Keyboard

IRQ 2	From CTLR 2	
	IRQ 8	Clock Interrupt
	IRQ 9	to INT OAH
	IRQ 10	Reserved
	IRQ 11	Reserved
	IRQ 12	Reserved
	IRQ 13	Coprocessor
	IRQ 14	Hard Disk
	IRQ 15	Reserved
	IRQ 3	Serial Port 2
	IRQ 4	Serial Port 1
	IRQ 5	Parallel Port 2
	IRQ 6	Diskette Controller
	IRQ 7	Parallel Port 1

8. MATH COPROCESSOR

Numeric processing power may be enhanced by adding the 80287 math coprocessor in the provided socket. 8 or 10 Mhz 80287s provide more than double the math performance of the PC/AT. The math coprocessor runs at the same speed at the CPU in the ATBABY system.

9. EPROM

Two JEDEC standard 28 pin ROM/EPROM sites are provided. These normally hold the AT compatible BIOS and power-on self test programs. They can be replaced by other boot ROMS, for instance the boot code for RMX-286 in a real-time system application.

10. DRAM

The ATBABY board has two banks of memory sockets, each

supporting 18 256K by 1 modules for a total memory size of 512Kb, with parity checking. This memory can be expanded with a plug on module to 1 megabyte without using expansion slots.

11. ON-BOARD EXPANSION CAPABILITIES

Memory Expansion

The memory expansion module allows expansion of the base board RAM memory to either 640K or 1 megabyte. This expansion module is placed on a stake pin connector and fits directly over the DRAM on the board.

12. ON BOARD EXPANSION CAPABILITIES

The following figure shows the location and the numbering of the I/O channel connectors. These connectors consist of two or three 68-plus-36 pin edge connector sockets plus three 62 pin connectors. These positions can support only 62-pin I/O bus adapters.

I/O Pin (A-Side)	Signal Name	I/O
A1	–I/O CH CK	I
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	–I/O CH RDY	I
A11	GEN	O

A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O
A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

(B-Side)

B1	GND	Ground
B2	RESET DRV	O
B3	+5VDC	Power
B4	IRQ 9	I
B5	–5VDC	Power
B6	DRQ2	I
B7	–12VDC	Power
B8	OWS	I
B9	+12VDC	Power
B10	GND	Ground
B11	–SMEMW	O

B12	–SMEMR	O
B13	–IOW	I/O
B14	–IOR	I/O
B15	–DACK3	O
B16	DRQ3	I
B17	–DACK1	O
B18	DRQ1	I
B19	–Refresh	I/O
B20	CLK	I
B21	IRQ7	I
B22	IRQ6	I
B23	IRQ5	I
B24	IRQ4	I
B25	IRQ3	I
B26	–DACK2	O
B27	T/C	O
B28	BALE	O
B29	+5VDC	Power
B30	OSC	O
B31	GND	Ground

(C-Side)

C1	SBHE	I/O
C2	LA23	I/O
C3	LA22	I/O
C4	LA21	I/O
C5	LA20	I/O
C6	LA19	I/O
C7	LA18	I/O
C8	LA17	I/O
C9	–MEMR	I/O
C10	–MEMW	I/O
C11	SD08	I/O

C12	SD09	I/O
C13	SD10	I/O
C14	SD11	I/O
C15	SD12	I/O
C16	SD13	I/O
C17	SD14	I/O
C18	SD15	I/O

(D-Side)

D1	MEMCS16	I
D2	–I/O CS16	I
D3	IRQ10	I
D4	IRQ11	I
D5	IRQ12	I
D6	IRQ15	I
D7	IRQ14	I
D8	–DACK0	O
D9	DRQO	I
D10	–DACK5	O
D11	DRQ5	I
D12	–DACK6	O
D13	DRQ6	I
D14	–DACK7	I
D15	DRQ7	I
D16	+5VDC	Power
D17	–MASTER	I
D18	GND	Ground

SAO-SA19 (I/O) is the address bus for 1st meg of memory and I/O space. LA17-LA23 (I/O) are used to complete the 16 Mb address space.

CLK (0) is the system clock which runs at CPU speeds.

Reset DRV (O) is the system reset signal.

SDO-SD15 (I/O) is the data bus.

BALE (O) (buffered) is used to latch valid addresses for the current cycle.

- I/O CH CK (I) provides error information about memory or devices on the I/O channel. Indicates an uncorrectable system error.

I/O CH DRY (I) is the ready signal for the I/O channel.

IRQ3 – IRQ7, IRQ9 – IRQ12 and IR!14 – IRQ15 (I) are the interrupt request Lines for the system.

- IOR (I/O) is I/O Read strobe.
- IOW (I/O) is the I/O Write cycle strobe.
- SMEMW (O) – SMEMR (I/O) are memory R/W signals for the I/O chennel.

DRQ0 – DRQ3 and DRQ5 – DRQ7 (I) are the DMA service request Lines.

- DACKO to – DACK3 and – DACK5 to – DACK7 (O) are used to acknowledge DMA requests (DRQO through DRQ7).

AEN (O) indicates DMA is on the address bus, not CPU.

- REFRESH (I/O) is used to indicate a refresh cycle.

T/C (O) indicates DMA cycle is finished.

- BHE indicates is bit data transfer.
- MASTER (I) is used with a DRQ line to gain control of the system.
- MEM CS16 (I) indicates one wait-state 16-bit memory cycle.
- I/O CS16 bit (I) indicates one wait-state 16-bit I/O cycle.

OSC (O) is a high speed 14.31918 Mhz clock.

OWS (I) tells CPU no wait-states are needed in transfer.

13. BOARD SPECIFICATIONS

Word Size

Instructions –8, 16, 24, 32, or 40 bits
Data – 8 or 16 bits
Addresses – 20 or 24 bits

System Clock

CPU 6, 8, 10 MHz or 6, 8, 12 MHz
Numberic Coprsessor – 6, 8, 10 MHz
DMA – 3, 4, 5 MHz or 3, 4, 6 MHz

Memory Capacity

EPROM – 64K bytes using 27256s
DRAM – 512K to one megabyte (W/O I/O slots); up to 15 megabytes (using expansion module plus 3 16-bit I/O slots for memory expansion)

I/O Capability

Expansion – Up to 6 PC expansion slots
(3 8-bits, 3 16-bit slots)

Physical Characteristics

Width – 22cm
Depth – 33cm
Weight – 1kgs

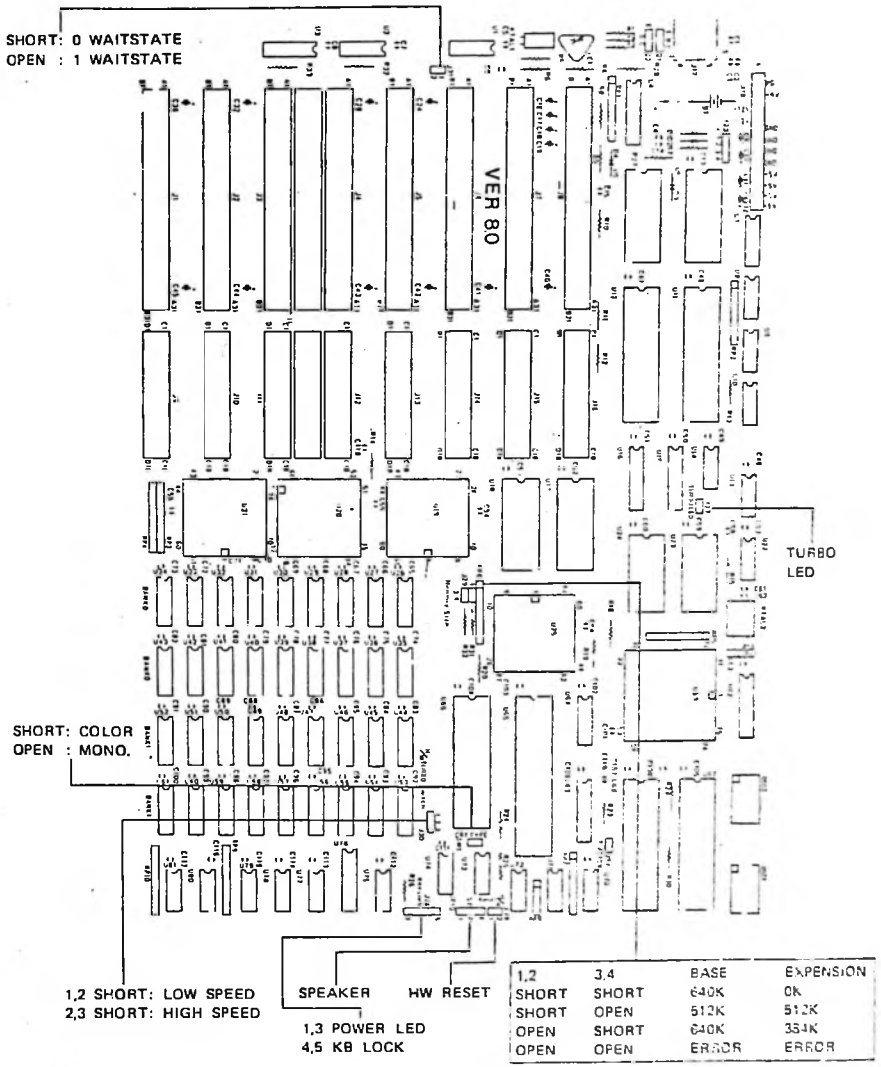
DC Power Requirements

+ 5V 5.0 Amps makimun – 2.5 Amps typical
+ 12V 50 milliAmps
– 12V, 50 milliAmps
(does not include expansion boards)

NOTE: Recommended Power Supply is 135W minimum.

Environmental Characteristics

Operating Temperature 0 to 55 degress Celsius
Relative Humidity – to 90% without condensation



1,2	3,4	BASE	EXPENSION
SHORT	SHORT	640K	0K
SHORT	OPEN	512K	512K
OPEN	SHORT	640K	384K
OPEN	OPEN	ERROR	ERROR

CHAPTER II

1. SYSTEM CLOCK SELECTION:

The speed of the system can be changed by the keyboard software switch. You can select LOW SPEED or HIGH SPEED system clock speed.

A. Turn on computer was under LOW SPEED
B. Press and hold "CTRL" and "ATL" keys
C. Press the "—" key on the unmeric keyboard
D. The system speed will be changed to HIGH SPEED

2. DEFAULT DISPLAY SELECTION

SW1 tells the system which display adapter to use on power up. If this switch is on, the system will come up using the color graphics display. If this switch is off, the system will come up using the monochrome display. If there is no display adapter in the system matching the setting of this switch, a CRT error message will be issued on power on, and the system will use whatever display adapter is actually installed in the system.

3. SUPPLYING POWER TO THE ATBABY BOARD

Once the proper cables and options are mounted and set, the actual board installation may begin. The ATBABY board requires at least a 135W power supply for proper operation. Before proceeding, make sure such a supply is installed in you system.

4. FINAL INSTALLATION

Now to mount the board in the system. In a PC system (5 slot) the board mounts on the existing standoffs using the offset mounting

holes contained on the board.

In an XT or AT system, the board mounts through the holes that are not offset. All installations use the nylon standoffs for holes which are not drilled with offsets. When mounting the board, particular care must be taken not to short the board against the metal case. On older systems this is particularly likely around the middle hole on the front edge of the board. Insulating tape should be used over the metal chassis, before the board and mounting screw are installed where necessary.

TIP: Once the board is mounted, if possible check to make sure no shorts occur with an Ohmmeter. If no Ohmmeter is available, it is good practice to insulate the two extruded mounting flanges which come up from the case on IBM PC and XT cases with electrical tape. After insulating, tap the mounting screw through the tape into the mounting hole.

Now that the board is mounted, plug the power connectors back into the new board, they are keyed to prevent mistakes. Next turn the system on momentarily to insure proper operation of the mounted board and power supply. A check of supply voltages for normal is advised before plugging and boards into your new system.

Once the power supply check is complete (see Chapter 2 for details), power off the system and re-install add-in cards (see Chapter V for compatibility details to determine which old cards can be used).

The additional connectors on the board, and their functions are described next. Just connect as keyed, making sure to attach the battery to the four pin connector with the word BATT printed next to the connector. Now you're ready to begin enjoying your

new high performance ATBABY system.

5. CONNECTORS

The speaker connector is a 4-pin Berg strip (J21):

1	Data out
2	+5 DC
3	Data out
4	+5VDC

The pin assignments for power-supply connector S19 is:

1	Power good
2	+5V VDC
3	+12 VDC
4	–12 VDC
5	Ground
6	Ground
7	Ground
8	Ground
9	–5VDC
10	+5VDC
11	+5VDC
12	+5VDC

The Keyboard (J22) connector is a 5-pin DIN connector. The pins are:

1	Keyboard clock
2	Keyboard Data
3	Spare
4	Ground
5	+5VDC

The power LED and keylock connector (J24) is 1 5-pin Berg strip. Its pins are:

1	LED Power
2	Key
3	Ground
4	Keyboard inhibit
5	Ground

The battery connector is a 4-pin Berg strip (J23):

1	6 VDC
2	Not Used
3	Ground
4	Ground

The Turbo LED connector is a 2-pin Berg strip (J27). The pin are:

The Hardware Reset is 2-pin Berg strip (J28).

1	RESET
2	Ground

The Hardware speed select is 3-pin Berg strip (J30)

1.2	ON	LOW SPEED
2.3	OFF	HIGH SPEED

The Hardware wait state select is 2-pin Berg strip (J31)

ON	ZERO WAIT STATE
OFF	ONE WAIT STATE

CHAPTER III

BIOS INFORMATION

1. INTRODUCTION

This chapter presents detailed information on the SOYO Technology ATBABY BIOS. For maximum benefit, this chapter should be used in conjunction with the IBM PC AT Technical Reference Manual, Chapter 5.

2. SYSTEM MEMORY MAP

ADDRESS	SIZE	FUNCTION
000000 to 07FFFF	512Kb	main board memory
080000 to 09FFFF	128Kb	Expansion memory on or off board
0A0000 to	128Kb	Video display buffer
0C0000 to 0DFFFF	128K	Reserved for ROM on I/O adapters
0E0000 to 0EFFFF	64Kb (Reserved)	Duplicated code assignment at address FEOOOO
0F0000 to 0FFFFF	64Kb ROM on main board	Duplicated code assignment at address FFOOOO
100000 to FDFFFF	Maximum Memory 15Mb	I/O channel or on-board memory

FE000 to FEFFFF	64Kb (Reserved)	Duplicated code assignment at address OE0000
FF0000 to FFFFF	64Kb (Reserved)	Duplicated code assignment at address OF0000

3. PERIPHERAL AND I/O SETUP

The peripheral and I/O space of the ATBABY board is defined as follows:

Hex Range	Device
000-01F	DMA controller 1,8237A-5
020-03F	Interrupt controller 1, 8259A, Master
040-05F	Timer, 8254.2
060-06F	8042 (Keyboard)
070-07F	Real-Time clock, NMI (non-maskable interrupt)
080-09F	DMA page register, 74LS612
0A0-0BF	Interurupt controller 2,8259A
0C0-0DF	DMA controller 2,8237A-5
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel printer port 2
2F8-2FF	Serial port 2
300-31F	Prototype card
360-36F	Reserved
378-37F	Parallel printer port 1

380-38F	SDLC or bisync 2
3A0-3AF	Bisync 1
3BO-3BF	Monochrome Display and Printer Adapter
3C0-3CE	LAN controller
3D0-3DF	Color/Graphics Monitor Adapter
3F0-3F7	Diskette controller
3F8-3FF	Serial Port

Hex 000 to OFF are reserved for the system board I/O. Hex 100 to 3FF are available on the I/O channel.

4. CMOS CLOCK/RAM

The internal clock circuitry uses 14 bytes of the 64 byte CMOS RAM, and the rest is used for configuration information. The CMOS RAM addresses are:

Address	Description
00-0D	Real-time clock information
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drives A and B type
11	Reserved
12	Hard disk type – drives C and D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte

19-2D	Reserved
2E-2F	2-byte checksum
30	0 Low expansion memory byte
31	0 High expansion memory byte
32	0 Data century byte
33	0 Information flags (set during power on)
34-3F	Reserved by IBM

CHAPTER V

HARDWARE COMPATIBILITY

This section shows the differences between the AT compatible computers, such as the ATBABY board, and the rest of the IBM Personal Computer family. It also contains information on what expansion cards will be compatible with the ATBABY board or any AT class machine.

The following are hardware features of the IBM Personal Computer AT and the ATBABY board that are not supported by the rest of the IBM Personal Compter family:

The ATBABY board uses an intel 80286 microprocessor. Programming considerations because of the faster processing capablity of the 80286 require programs to be written without loops or routines which are dependent on execution speed by the CPU. This is usually no problem, since thisis just good programming practice.

The expansion slots have a 36-pin connector in addition to the 62-pin connector. Adapters designed to make use of the 36-pin connector are not compatible with other machines with only the 62-pin connector.

The I/O channel is different:

1. The system clock signal should only be used for synchronization and not for applications requiring a fixed frequency.
2. The 14.31818 MHz osillator is not synchronous with the system clock.
3. 'ALE' is active during DMA cycles.

4. The I/O write signal is not active during refresh cycles.
5. Pin BO4 supports IRQ 9.

Cards which IBM declares to be incompatible with the AT architecture and thus the ATBABY board include:

- 8-bit cards (62--pin connector only) containing system memory

Cards which will work in the ATBABY expansion bus include:

- AT compatible cards
- PC floppy disk controller card
- Some XT type hard disk controllers (including Xebec, Western Digital, and CDC – see Technical Reference Naual for installation details)
- Most 8-bit display adapters
- Most 8-bit cards containing I/O functions only
- DTC 5290 or equivalent Hard + Floppy disk controller

APPENDIX A

RECOMMENDED REFERENCES

1. HARDWARE

Information is available for each of the devices included on the ATBABY board from Intel and other semiconductor companies. Sources are shown below.

From Intel:

1985 Component Data Book
80286 data sheet
iAPX 286 Hardware Reference Manual

From IBM:

Guide to Operations – Personal Computer AT Installation and Setup – Personal Computer AT Technical Reference Manual – Personal Computer AT

2. SOFTWARE

From Intel:

iAPX 286 Programmer's Reference Manual
iAPX 286 Operating Systems Writer's Guide

From IBM:

PC-DOS 3.1 Reference Manual

APPENDIX B

82C201/82C202/82A203/82A204/82A205 PC/AT COMPATIBLE CHIPSet™

- Fully IBM PC AT Compatible
- FLexible architecture allows usage in any iAPX 286 design
- Early ALE Generation
- Early RAS Generation
- Low Power CMOS Process Technology for 82C201 and 82C202, and Advance Low Power Schottky Process Technology for 82A203, 82A204 and 82A205
- 6 Mhz Zero Wait State or 8 Mhz One Wait State Capability
- Complete System Board Memory Decode
- Configurable RAM Selects
- 16 Bit to 8 Bit Conversion Logic
- Variable Wait State Selection
- 24 mA sink and −3.3 mA source current for System Bus outputs
- Single 5 Volt Supply

82C201

The 82C201 is the system controller which generates most of the clocks and control signals for the entire system. Signals from the 82C201 are used throughout the system for control and steering of logic. All bus cycles are decoded and timed by this device. The 82C201 functions as the one part which holds the entire system together.

82C202

Decode for RAM, ROM and a portion of the I/O takes place in the 82C202. This decode takes the form of RAS/CAS enables and chip select signals to the various memory devices. Additional support is provided for controlling the Real Time Clock and providing chip selects to the Keyboard Controller and the system control/status

port (Port B.)

82A203

The 82A203 provides address latching and control buffering for the system. Control signals from the 82C201 are buffered by the 82A203 and tri-stated (when necessary) for the expansion and the I/O buses. Also integrated in the 82A203 is the system status and control port, which is referred to as Port B.

82A204

The 82A204 buffers the lower address lines for the expansion bus, I/O bus and memory bus. In addition to buffering memory addresses, the 82A204 provides the row/column multiplexing and refresh counter.

82A205

The 82A205 is the system data bus buffer. In the process of providing data bus buffering, two related functions are provided by the 82A205. Since the 80286 is a true 16-bit CPU, transfers of 16-bit data to and from 8-bit devices require additional logic. The additional logic to perform the latching and low/high byte translation are included in the 82A205. Another function of the 82A205 is parity generation and checking for the system. Included as part of this function is the logic to determine when an error has occurred.

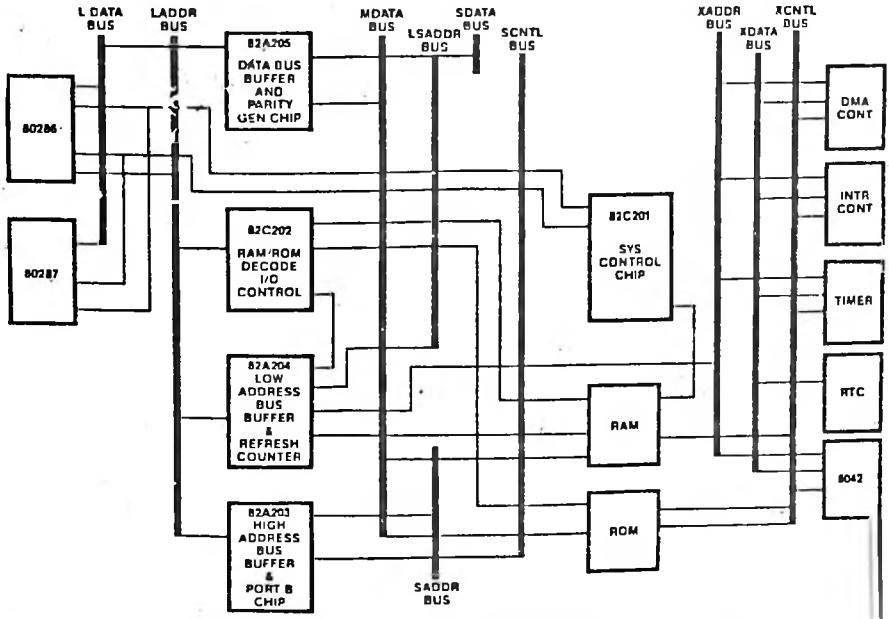


Figure 1. PC/AT System Diagram

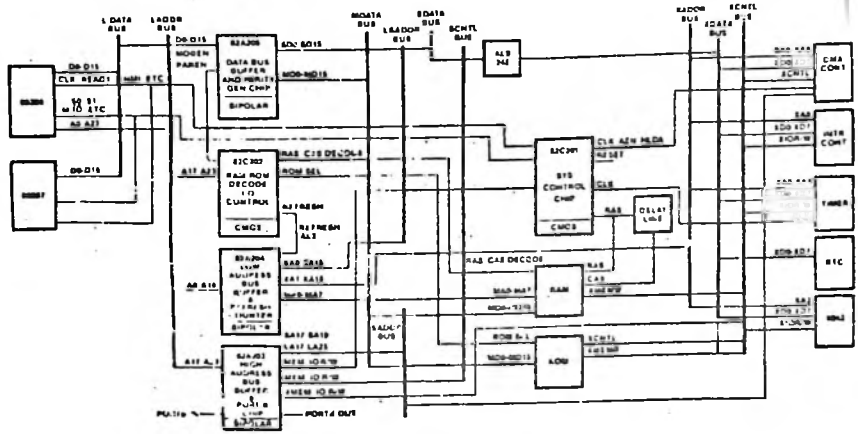
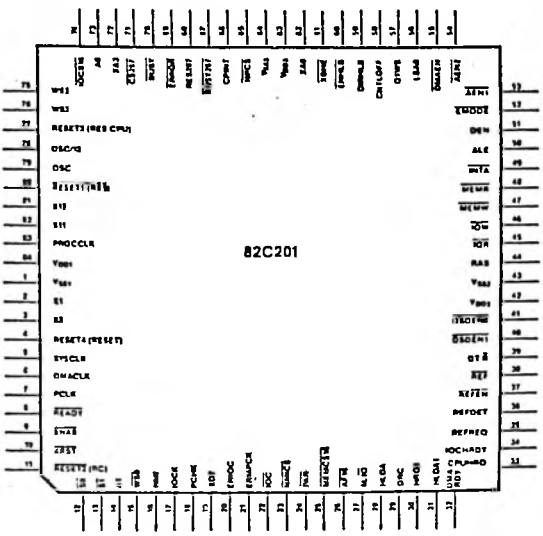
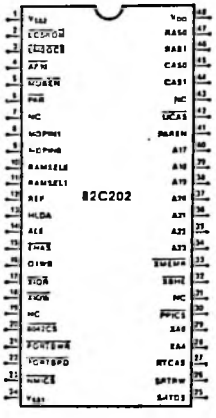
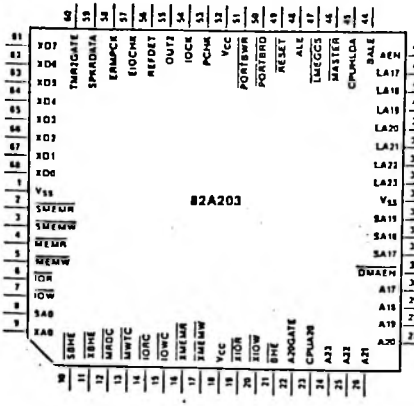
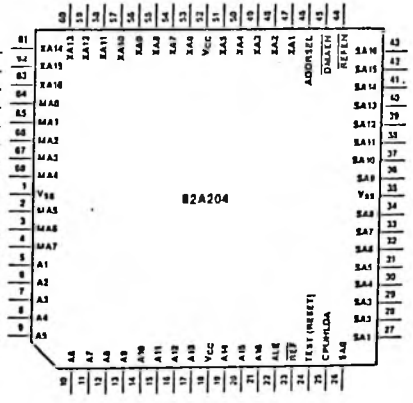


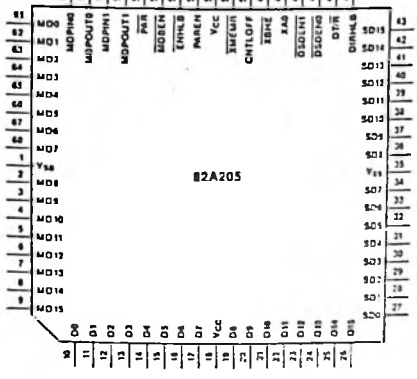
Figure 1. PC/AT Block Diagram

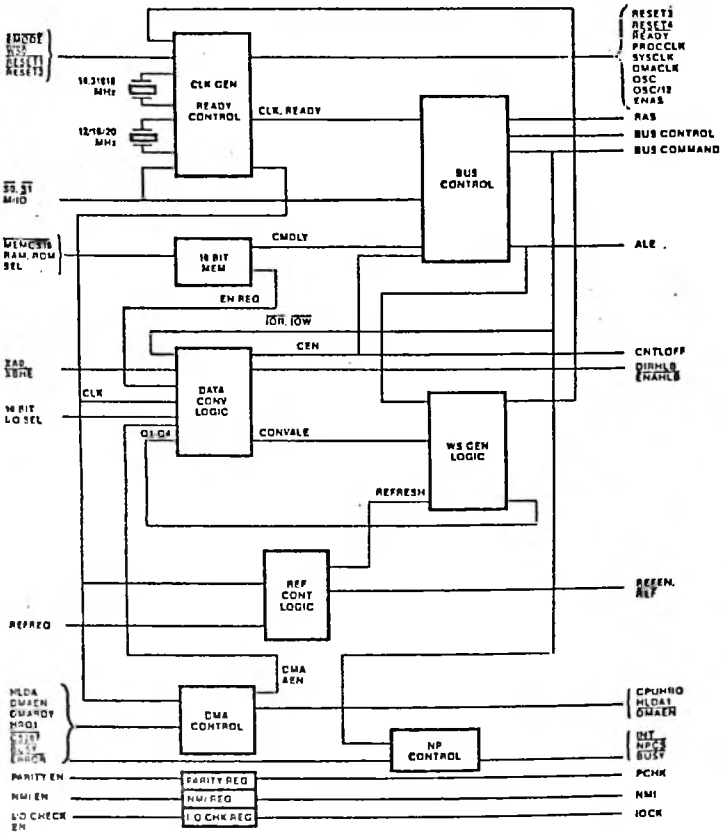

82C201


82C202


82A203


82A204


82A205



Functional Description 82C201

The 82C201 block diagram is illustrated in Figure 2. The device consists of the following functional blocks:

- Clock Generation and Reset/Ready Synchronization
- Command and Control Signal Generation
- Conversion Logic
- Wait State Control
- DMA and Refresh Logic
- Numerical Processor Control
- NMI and Error Logic

Functional Description 82C202

The 82C202 consists of the following functional blocks:

- ROM/RAM Decode and Latch
- Parity Error Detection Logic
- I/O Decode Logic

ROM/RAM Decode and Latch

The 82C202 contains the circuitry to decode the CPU's Address bus and provide the necessary latched signals for controlling both ROMS and RAMS on the user's system board. In order to make the 82C202 more flexible, a user-configurable decode is incorporated into the device. Decode configuration is accomplished by strapping the SEL0 and SEL1 input pins. Table 3 shows the different strapping options available. Strapping allows the user to configure the system for either 64K RAMs, 256K RAMs, or both 64K and 256K devices. Memory configurations ranging from 128K bytes to 1M bytes are now possible using the decode selects.

Additional support for Memory Refresh is also provided in the 82C202. During a Refresh Cycle, the assertion of the REF input will cause the 82C202 to ignore the current Address inputs. Instead, it will activate both the RAS0 and RAS1 outputs while inhibiting CAS0, CAS1, and LCSROM.

$\overline{\text{LCSROM}}$ is the decoded and latched ROM chip select from the 82C202. This output is asserted whenever either of two addresses ranges is detected and $\overline{\text{REF}}$ is inactive. The address ranges for $\overline{\text{LCSROM}}$ are also listed in Table 3.

The two outputs, $\overline{\text{LMEGCS}}$ and $\overline{\text{MDBEN}}$, are intended to be used as memory buffer enable signals. $\overline{\text{LMEGCS}}$ is active whenever any memory access is made to an address below 100000h or when REF is active. For memory data bus buffer control, the signal $\overline{\text{MDBEN}}$ should be used. This signal will become active whenever either CAS0, CAS1, or $\overline{\text{LCSROM}}$ is active. The $\overline{\text{MDBEN}}$ signal may also be externally ANDed with MEMR to create the necessary directional control signal for the memory data buffer.

The 82C202 internal latch is controlled by two input signals —HLDA and ALE. During a CPU Memory Cycle, ALE will enable the RAM Decode Latch and allow the output from the decoder to be transferred to the output pins. When ALE is deasserted, the decoder output is latched for the remainder of the cycle. HLDA also enables the RAM Decode Latches. Asserting HLDA will enable the decoder outputs to the output pins and force $\overline{\text{LCSROM}}$ inactive. Forcing $\overline{\text{LCSROM}}$ inactive occurs regardless of the state of the input addresses.

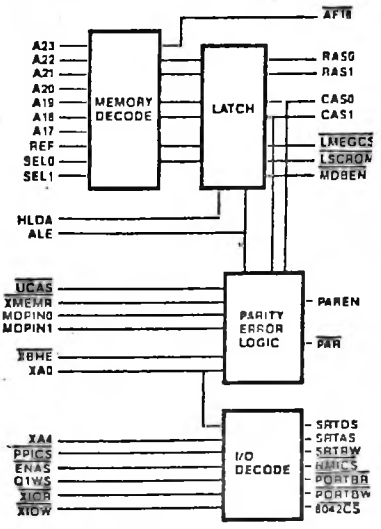


Figure 6. 82C202 Functional Block Diagram

Table 3

Select Input		RAM Address Range		RAM Type		ROM Address Range	
SEL0	SEL1	RAS0/CAS0	RAS1/CAS1	BANK0	BANK1	Low Addr Range	High Addr Range
0	0	000000h-01FFFFh	020000h-03FFFFh	64K	64K	0E0000h-0FFFFFh	FE0000h-FFFFFFh
1	0	000000h-07FFFFh		256K	NONE	0E0000h-0FFFFFh	FE0000h-FFFFFFh
0	1	000000h-07FFFFh	080000h-09FFFFh	256K	64K	0E0000h-0FFFFFh	FE0000h-FFFFFFh
1	1	000000h-07FFFFh	100000h-17FFFFh	256K	256K	0E0000h-0FFFFFh	FE0000h-FFFFFFh

Functional Description 82C203

Figure 7 illustrates a TTL equivalent of the logic implemented by the 82A203. As is shown in the figure, the 82A203 provides the drivers and buffers for the CPU, the System and Local I/O control buses. The memory read and write and the I/O read and write signals are bidirectional. The direction and control of the bus is determined by the $\overline{\text{DMAEN}}$ and the $\overline{\text{MASTER}}$ inputs. The chip also provides the drive and buffer capability for the high address bus signals, A17-A23. The direction and control is provided by the CPU Hold Acknowledge and ALE inputs, as shown in the figure. In addition to providing the drivers and buffers, the 82A203 also integrates the status latch (PORT B in the AT implementation). The latch can be written into and read through $\overline{\text{PORTWR}}$ and $\overline{\text{PORTRD}}$ signals.

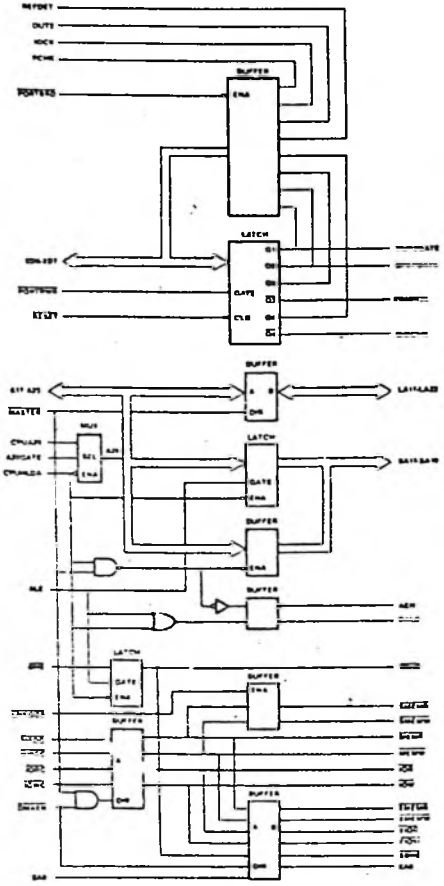


Figure 7. Functional Block Diagram

Functional Description 82A204

Figure 8 illustrates a TTL equivalent of the logic implemented by the 82A204. The chip provides the drive and buffering for the address signals A1-A16. Additionally, it provides the drivers for the memory address bus MA0-MA7. The direction and control for the Address buffers for A1-A16 are provided by the CPU Hold Acknowledge and $\overline{\text{DMAEN}}$ inputs, as shown in the figure. The refresh addresses are provided by a refresh counter, which is enabled by the $\overline{\text{REFEN}}$ input. The addresses for the memory are multiplexed as shown in the figure. The SA0 is an output which is active only during the refresh cycle.

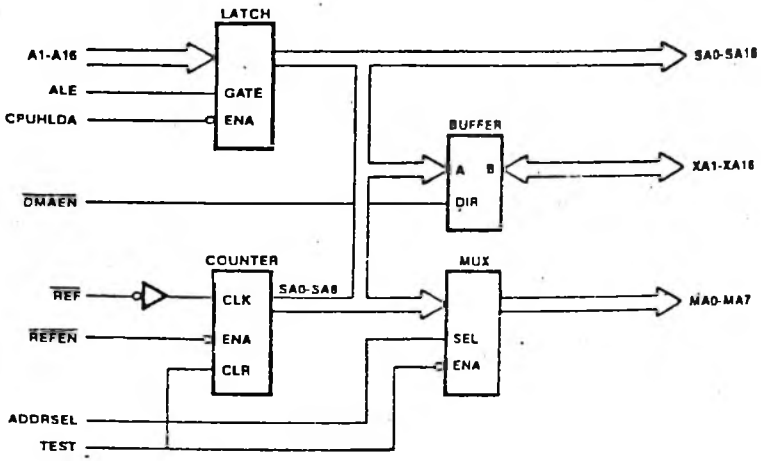


Figure 8. Functional Block Diagram

Functional Description 82A205

Figure 9 illustrates a TTL equivalent of logic implemented by the 82A205. The chip provides the data bus buffers and drivers for D0-D15. The three data buses controlled are the CPU bus (D0-D15), the System bus (SD0-SD15), and the Memory Data bus (MD0-MD15). The direction and control for these drivers are provided by the DT/$\overline{R}$, $\overline{DSDEN0}$, $\overline{DSDEN1}$, $\overline{XBHE}$, and XA0 inputs, as shown in the figure. The low byte to high byte conversion logic is also implemented on the chip. The conversion logic is controlled by the $\overline{ENHLB}$ and DIRHLB inputs. The chip also integrates the parity generation and check logic. The parity is computed on the memory data bus signals and output as MDPIN0 and MDPIN1. During a read cycle, the parity check is computed on the data read from the memory and the parity bits MDPOUT 0 and MDPOUT 1. On a parity error, the $\overline{PAR}$ output is activated.