HS-4500

MMX™/Pentium® Little Board

• PCI Slot • PC/104 Bus • CRT/Panel •
• 100MHz • DMA33 • WDT • CTA • DOC •
• GPS Socket • Sound • 10/100-based LAN •
Embedded Size Industrial Single Board Computer

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Chapter-1

General Information

The HS-4500 is a Little Board size Embedded Pentium®MMX™ Industrial Single Board (I.S.B.) The board design combine together with all necessary input and output effects interfaces which makes it an ideal all-in-one industrial single board computer. The board design with 100 MHz internal bus clock rate architecture.

With the PCI-bus slot for provides to a PCI add-on card where necessary. One set of PC/104-bus connector for industrial PC/104 board add-in. For GPS system application, the board provides a 2x10 pin-field internal I/O connector for easy add-in Rockwell's "Jupiter" Global Positioning System (GPS) Receiver. The board also design with an ESS® Solo1 3D sound interface which provides an ideas sound adapter in any sound application. The IDE interface with DMA33 access of mode 4 to IDE drive interface architecture, supports with maximum 33.3 MB/sec in data transfer rating to 2 pieces IDE drive connection. The board also provides a on-board 10/100-based LAN for easy network connection.

A single Flash chip holds the system BIOS, and you can change the Flash BIOS by the Utility Update. Advanced IR also provides a faster data transmission. You can also use the DOS version of the "DiskOnChip™" socket by issuing commands from the DOS prompt without the necessity of other software supports up to 144MB.

The board design with 69000 VGA provides internal connections to VGA Monitor and-or Flat Panel. The VGA supports up to 1280x1024 256 colors resolution.

The HS-4500 support BEDO, EDO, FPM DRAM and SDRAM memory with 2 pcs SIMM sockets and one DIMM sockets. This gives you the flexibility of configuring your system from 1 to 384 MB DRAM by using the most economical SIMMs and DIMM memory modules for its on-board system DRAM.

If a non-expect program cause halts, the onboard Watch-Dog Timer (WDT) will automatically reset the CPU or generate an interrupt. The WDT is designed with pure hardware and doesn't need any arithmetical functions of a real-time clock chip. This ensures the reliability in an unmanned or standalone system.

1.1 Major Features

- ✓ PCI & PC/104 Bus supported.
- ✓ Intel Pentium® CPU 75~350 MHz, AMD k5, k6, Cyrix 6x86, M2, Intel MMX™, Socket 7 ZIF socket.
- ✓ ALi® M1541, M1543 chipsets.
- ✓ Provides internal bus clock rate at 100 MHz.
- ✓ Supports EDO, Fast Page DRAM or S-DRAM up to 384 MB.
- ✓ Ultra DMA33 Supported two fastest PCI enhanced IDE drives (large hard disks, CD-ROM, tape backup, UFD-FDD etc.).
- ✓ One FD Drive connector supports two Floppy disk drives.
- ✓ PnP I/O address & IRQ selection.
- ✓ On-board SMC® 37C669 super I/O chipset. Three high-speed serial RS-232 ports (with 16C550 UART 16-byte FIFO) and one RS-422/485 port. One enhanced bi-directional parallel port supports SPP/EPP/ECP.
- ✓ On-board internal 8-pin header Keyboard and Mouse connector.
- ✓ On-board INTEL® 69000 VGA provides internal connections to VGA Monitor and-or Flat Panel. The VGA supports up to 1280x1024 256 colors resolution.
- ✓ On-board 2x10 pin-field internal I/O connector for easy add-in Rockwell's "Jupiter" Global Positioning System (GPS) Receiver.
- ✓ The board also design with an ESS® Solo-1 3D sound interface which provides an ideas sound adapter in any sound application.
- ✓ The board also provides a on-board 10/100-based LAN with Realtek® RT-8139 chipset for easy network connection.
- ✓ "DiskOnChip™" socket supports, memory size up to 144 MB.
- ✓ Switch Power Regulator supports all various CPU's core voltage levels.
- ✓ If a non-expect program cause halts, the onboard Watch-Dog Timer (WDT) will automatically reset the CPU or generate an interrupt. The WDT is designed with pure hardware and doesn't need any arithmetical functions of a real-time clock chip. This ensures the reliability in an unmanned or standalone system.

1.2 Specifications

- **CPU:** Intel MMX™Pentium® 75~350MHz, AMD k5, k6, Cyrix 6x86,M2.
- **Bus interface:** PC/104 & PCI Bus
- **Chipset:** ALi® M1541, M1543
- **Data bus:** 64-bit
- **Processing ability:** 64-bit
- **Internal Bus Rate:** 100 MHz
- **VGA Controller:** INTEL® 69000 chipset.
- **VGA Resolution:** Resolutions up to 1280x1024 256 colors resolution. Provides internal connections 16-pin header to VGA Monitor and 50-pin header to Flat Panel.
- **DMA/33 Enhanced IDE interfaces:** Supports up to two IDE devices. Support Ultra DMA/33 mode with data transfer rate 33MB/Sec.
- **RAM memory:** Up to 384MB, uses two 72-pin SIMM sockets and-or one DIMM socket supports BEDO, EDO, FastPage and S-DRAM memory modules.
- **Cache memory:** 512KB Pipeline burst cache memory.
- **Floppy disk drive interface:** Supports up to two floppy disk drives.
- **Parallel port:** One bi-directional parallel port. Supports SPP/ECP/EPP.
- **Serial ports:** Three RS-232 ports and one RS-232/422/485 port. All including 16C550 compatible UART with 16-byte FIFO.
- **GPS Connection:** One 2x10 pin-field internal I/O connector for Rockwell's "Jupiter" GPS Receiver module add-in.
- **Sound Interface:** On-board ESS® Solo-1 3D sound interface.
- **LAN Interface:** On-board 10/100-based by Realtek® RT-8139 chipset compatible to NE2000 application.
- **BIOS:** Award.
- **Watchdog timer:** Hardware circuit can be set by 1, 2, 10, 20, 110, or 220 seconds period Reset or NMI were generated when CPU did not periodically trigger the timer.
- **DMA channels:** 7
- **Interrupt levels:** 15
- **Keyboard & Mouse:** 8-pin header connector supports Keyboard and Mouse port.

- **USB:** 2 USB header supported.(version 1.4 only)
- **Flash Memory Disk:** Reserved socket for "DiskOnChip™", support up to 144MB Flash memory disk.
- **CMOS:** Real-time clock/calendar and battery backup by DS12B887 or equivalent device.
- **Power supply voltage:** +5V and +12V power supply.
- **Max. Power requirement:** +5V @3.5A(K6-300), +12V @500mA.
- **Operating temperature:** 0-55°C (CPU need cooler)
- **Board size:** 8"(L) x 5.75" (W) (203mm x 146mm)

1.3 Delivery Package

The delivery package of HS-4500 includes all following items:

- HS-4500 Industrial Single Board
- One Printer port Flat Cable
- One IDE port Flat Cable
- One FDD port Flat Cable
- One 40-pin COM ports Cable
- One Panel Connection Flat Cable
- One Front Panel Cable
- One Ethernet Cable
- One PS/2 Keyboard and Mouse Transfer Cable
- One MIC/SPK Cable
- VGA Utility CD-ROM
- User's Manual

Please contact with your dealer if any of these items are missing or damaged when purchasing. And please keep all parts of the delivery package with packing materials in case of you want to ship or store the product in feature.

Chapter-2

Hardware Installation

This chapter provides the information on how to install the hardware of HS-4500. At first, please follow up sections 1.3, 2.1 and 2.2 in check the delivery package and carefully unpacking. Following after, the jumpers setting of switch, watchdog timer, and the DiskOnChip™ address selection etc.

2.1 Caution of Static Electricity

The HS-4500 has been well package with an anti-static bag in protect its sensitive computer components and circuitry from the damage of static electric discharge.

Note: DO NOT TOUCH THE BOARD OR ANY OTHER SENSITIVE COMPONENTS WITHOUT ALL NECESSARY ANTI-STATIC PROTECTION.

You should follow the steps as following to protect the board in against the static electric discharge whenever you handle the board:

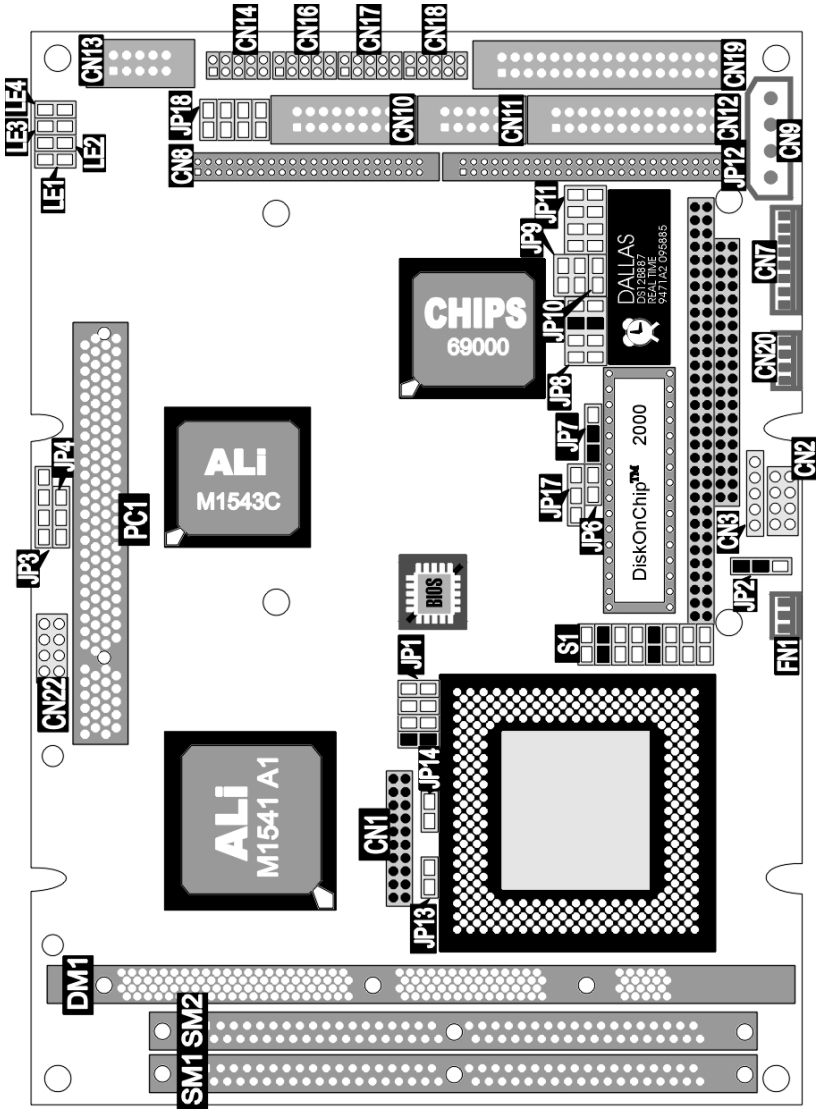
1. Please use a grounding wrist strap on whoever needs to handle the HS-4500. Well clip the ALLIGATOR clip of the strap to the end of the shielded wire lead from a grounded object. Please put on and connect the strap before handle the HS-4500 for harmlessly discharge any static electricity through the strap.
2. Please use anti-static pad for put any components or parts or tools on the pad whenever you work on them outside the computer. You may also in use the anti-static bag instead the pad. Please ask from your local supplier in help up your necessary parts on anti-static requirement.

2.2 Caution on Unpacking and Before Installation

First of all, please follow with all necessary steps of section 2.1 in protection the HS-4500 from electricity discharge. With refer to section 1.3, please check the delivery package again with following steps:

1. Unpacking the HS-4500, keep well storage of all packing material, manual and diskette etc. if has.
2. Is there any components lose or drop from the board? DO NOT INSTALL IF HAPPENED.
3. Is there any visual damaged of the board? DO NOT INSTALL IF HAPPENED.
4. Well check from your optional parts (i.e. CPU, SRAM, DRAM, ROM-Disk etc.) for completed setting all necessary jumpers setting to jumper pin-set and CMOS setup correctly. Please also reference to all information of jumpers setting in this manual.
5. Well check from your external devices (i.e. Add-On-Card, Driver Type etc.) for completed add-in or connection and CMOS setup correctly. Please also reference to all information of connector connection in this manual.
6. Please keep all necessary manual and diskette in a good condition for your necessary re-installation if you change your Operating System or whatever needs.

2.3 HS-4500's Layout



2.4 Quick Listing of Jumpers

JP1 (1-8)	➢	CPU Clock-in Select
JP2	➢	WATCH-DOG Active Select
JP5	➢	RS-232 COM-2 disable setting
JP6	➢	RS-232 COM-4 disable setting
JP7	➢	for DiskOnChip™ address setting
JP8	➢	WATCH-DOG Time-out period selection
JP9	➢	RS-422/485 Receiver Enable Control
JP10	➢	CMOS Data Clear
JP11	➢	RS-422/485 Transceiver Enable Control
JP13, JP14	➢	GPS Protocol Selection
JP15	➢	RS-232 COM-3 disable setting
JP17	➢	Panel Power Selection
S1 (1-6)	➢	CPU's Core/Bus Clock-Ratio Setting
S1 (7-16)	➢	CPU's Vcore voltage level selection setting

2.5 Quick Listing of Connectors

CN1: GPS CONNECTOR (FEMALE 10x2)
CN2: FRONT PANEL CONNECTOR (PIN-BASED 4x2)
CN3: KEYLOCK (PIN-BASED 5x1)
CN4: PC/104 BUS 64-P CONNECTOR (FEMALE 32x2)
CN5: PC/104 BUS 40-P CONNECTOR (FEMALE 20x2)
CN7: KEYBOARD & MOUSE CONNECTOR (PIN-BASED 8x1)
CN8: 1st HDD (IDE) CONNECTOR (HEADER 20x2)
CN9: +5V/+12V POWER CONNECTOR (FEMALE 4-pin)
CN10: INTERNAL VGA CONNECTOR (HEADER 8x2)
CN11: RS-422/485 COM-4 CONNECTOR (HEADER 5x2)
CN12: PARALLEL PORT (HEADER 13x2)
CN13: 10/100-BASED LAN CONNECTOR (HEADER 5x2)
CN14: RS-232 COM-1 CONNECTOR (HEADER 5x2)
CN16: RS-232 COM-2 CONNECTOR (HEADER 5x2)
CN17: RS-232 COM-3 CONNECTOR (HEADER 5x2)
CN18: RS-232 COM-4 CONNECTOR (HEADER 5x2)
CN19: FDD CONNECTOR (HEADER 17x2)
CN22: USB CONNECTOR (VER:1.4 above only)
JP3: SOUND AUXA CONNECOTR (HEADER 4x1)
JP4: SOUND AUXB CONNECOTR (HEADER 3x1)
JP12: LCD PANEL CONNECTOR (HEADER 25x2)
JP18: SOUND MIC/SPK CONNECTOR (HEADER 4x2)
U9: DiskOnChip™ SOCKET
LED2: PIN 2x1 10-BASED INDICATING LED CONNECTOR
LED3: PIN 2x1 100-BASED INDICATING LED CONNECTOR
LED4: PIN 2x1 NETWORK ACTIVE INDICATING LED CONNECTOR
LE4: POWER LED CONNECTOR
FN1: FAN POWER CONNECTOR (VER:1.4 above only)

2.6 Jumper Setting Description

A jumper pin-set is **ON** as a shorted circuit with a plastic cap inserted over two pins. A jumper pin-set is **OFF** as a open circuit with a plastic cap inserted over one or no pin(s) between pins. The below figure 2.2 shows the examples of different jumper pin-set setting as **ON** or **OFF** in this manual.

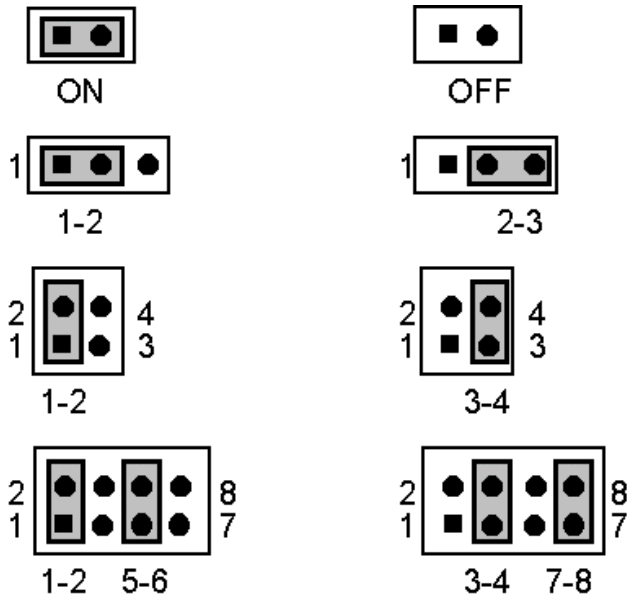


Figure 2.2

All jumper pin-set already has its default setting with the plastic cap inserted as ON, or without the plastic cap inserted as OFF. The default setting may reference in this manual with a " * " symbol in front of the selected item.

2.7 VGA Controller

The onboard INTEL® 69000 chipset provides with up to 1280x1024 256 colors resolution. The board provides to user in auto disable VGA if another PCI-bus display card plug in into the PCI-slot.

There is no need to setting any jumper to disable the on board VGA if any 2nd PCI-bus VGA card plug-in into the PCI-slot.

2.8 DiskOnChip™ Address Setting

The HS-4500 provides a U9 socket for install the DiskOnChip™ module.

A JP7 may select the starting memory address of the DiskOnChip™ (D.O.C.) for avoid the mapping area with any other memory devices. If you have another extra memory devices in the system, please setting both at different memory address mapping.

- **JP7 : DiskOnChip™ Address**

PIN NO.	Address
***1-2**	**D000**
3-4	D800

The D.O.C. function allows the system in using without FDD nor HDD. The D.O.C. may formatting as driver C: or driver A:. User may also easily uses the DOS's commands such as FORMAT, SYS, COPY, XCOPY, DISCOPY and DISKCOMP etc. This is means that the D.O.C. may uses as driver-A if the system without FDD-A for ambient application. Please contact with your supplier for different size D.O.C. module.

2.9 Setting the CPU of HS-4500

The HS-4500 provides all possibility in jumper setting for wide using all types of CPU with S1 (pin 7-16) for CPU Vcore Voltage, JP1 (pin 1-8) for internal Host Bus Clock Rate and S1 (pin 1-6) for CPU Clock-in Multiplex Weighted Value setting as following. **Please contact with your CPU's supplier in getting those information for correctly setting. Any wrong setting may cause CPU defect.**

- **CPU Vcore Voltage Selection**

Correspond to different type CPU, it is request to set S1 (7-16) for match the CPU's Vcore operating voltage. Here shows at below of the proper jumper settings for their respective Vcore at range 1.8V to 3.5V.

CPU Vcore Voltage	S1 (7-16)
1.8V	9-10, 13-14, 15-16
1.9V	11-12, 13-14, 15-16
2.0V	9-10, 11-12, 13-14, 15-16
2.1V	7-8
2.2V	9-10
2.3V	7-8, 9-10
2.4V	11-12
2.5V	7-8, 11-12
2.6V	9-10, 11-12
2.7V	7-8, 9-10, 11-12
2.8V	13-14
***2.9V**	**7-8, 13-14**
3.0V	9-10, 13-14
3.1V	7-8, 9-10, 13-14
3.2V	11-12, 13-14
3.3V	7-8, 11-12, 13-14
3.4V	9-10, 11-12, 13-14
3.5V	7-8, 9-10, 11-12, 13-14

- **Host Bus Clock Rate select JP1 (1-8)**

JP1 (pin 1-8) used to setting the Host Bus Clock Rate. The setting of internal host bus clock rate is for defined the operating clock base rate of the internal bus of core logic.

System Clock	JP1 (1-8)
60 MHz	1-2, 3-4, 5-6, 7-8
***66.8 MHz**	**3-4, 5-6, 7-8**
75 MHz	1-2, 3-4, 7-8
83.3 MHz	3-4, 7-8
100 MHz	7-8

*) : default setting

- **CPU Clock-in Multiplex Weighted Value select S1 (1–6)**

S1 (1-6) used to setting the CPU Clock-in Multiplex Weighted Value. The setting value is for multiplex to internal host bus clock rate and obtain the CPU operating clock value.

S1			CPU Type			
5-6	3-4	1-2	Pentium MMX 2.8V(66MHz)	Tillamook 1.9V(66MHz)	AMD K6 (66MHz)	AMD K6 (100MHz)
ON	ON	ON	166MHz	166MHz	300MHz	450MHz
ON	ON	OFF	200MHz	266MHz	166MHz	250MHz
ON	OFF	ON	133MHz	133MHz	266MHz	400MHz
ON	OFF	OFF	200MHz	266MHz	400MHz	600MHz
OFF	ON	ON	233MHz	200MHz	333MHz	500MHz
OFF	ON	OFF	200MHz	266MHz	200MHz	300MHz
OFF	OFF	ON	200MHz	233MHz	366MHz	550MHz
OFF	OFF	OFF	166MHz	266MHz	233MHz	350MHz

*) : default setting

2.10 Watch-Dog Timer

There are three access cycles of Watch-Dog Timer as Enable, Refresh and Disable. The Enable cycle should proceed by READ PORT 443H. The Disable cycle should proceed by READ PORT 043H. A continue Enable cycle after a first Enable cycle means Refresh.

Once if the Enable cycle activity, a Refresh cycle is request before the time-out period for restart counting the WDT Timer's period. Otherwise, it will assume that the program operation is abnormal when the time counting over the period preset of WDT Timer. A System Reset signal to start again or a NMI cycle to the CPU comes if over.

The JP2 is using for select the active function of watch-dog timer in disable the watch-dog timer, or presetting the watch-dog timer activity at the reset trigger, or presetting the watch-dog timer activity at the NMI trigger.

- **JP2 : Watch-Dog Active Type Setting**

JP2	DESCRIPTION
***1-2**	**System Reset**
2-3	Active NMI
OFF	disable Watch-dog timer

- **JP8 : WDT Time - Out Period**

PERIOD	1-2	3-4	5-6	7-8
***1 sec**	**OFF**	**OFF**	**ON**	**OFF**
2 sec	OFF	OFF	ON	ON
10 sec	OFF	ON	OFF	OFF
20 sec	OFF	ON	OFF	ON
110 sec	ON	OFF	OFF	OFF
220 sec	ON	OFF	OFF	ON

The Watch-dog timer is disabled after the system Power-On. The watch-dog timer can be enabled by a Enable cycle with reading the control port (443H), a Refresh cycle with reading the control port (443H) and a Disable cycle by reading the Watch-dog timer disable control port (043H). After a Enable cycle of WDT, user must constantly proceed a Refresh cycle to WDT before

its period setting comes ending of every 1, 2, 10, 20, 110 or 120 seconds (Please reference to the selection table of JP8 for WDT Time-Out period setting). If the Refresh cycle does not

active before WDT period cycle, the on board WDT architecture will issue a Reset or NMI cycle to the system.

The Watch-Dog Timer is controlled by two I/O ports.

443H	I/O Read	The Enable cycle.
443H	I/O Read	The Refresh cycle.
043H	I/O Read	The Disable cycle.

The following sample programs showing how to Enable, Disable and Refresh the Watch-dog timer:

```
WDT_EN_RF       EQU     0433H
WDT_DIS         EQU     0043H

WT_Enable       PUSH    AX              ; keep AX DX
                PUSH    DX
                MOV     DX,WDT_EN_RF    ; enable the watch-dog timer
                IN      AL,DX
                POP     DX              ; get back AX, DX
                POP     AX
                RET

WT_Refresh      PUSH    AX              ; keep AX, DX
                PUSH    DX
                MOV     DX,WDT_ET_RF    ; refresh the watch-dog timer
                IN      AL,DX
                POP     DX              ; get back AX, DX
                POP     AX
                RET

WT_DISABLE      PUSH    AX
                PUSH    DX
                MOV     DX,WDT_DIS      ; disable the watch-dog timer
                IN      AL,DX
                POP     DX              ; get back AX, DX
                POP     AX
                RET
```

2.11 CMOS Data Clear

The HS-4500 provides a JP10 for clear the data in CMOS memory. Please keep OFF when normal operating.

- **JP10 : CMOS Data Clear**

PIN NO.	Activity
ON	Clear Data
***OFF**	**Normal Operating**

*) : default setting

2.12 System Memory DRAM

The HS-4500 provides a wide range on-board DRAM memory by two pieces SIMM sockets (Bank0 & Bank1) to accept 1 MB, 2MB, 4MB, 8MB, 16MB, 32MB or 64MB. The SIMMs (Single In-Line Memory Modules) RAM request the access time should be 70 n-second or faster. The total capacities of the on board SIMM's memory are between 2MB to 128MB. With one additional DIMM socket of maximum 256MB-memory capacity, the total memory size may up to 384MB on board.

See the figure on section 2.3 for get the identifying the banks. Please take notes that the memory capacity of both SIMMs should be the same.

Chapter-3

Connection

This chapter gives all necessary information of the peripheral's connections, switches and indicators.

3.1 VGA Connectors

The HS-4500 provides one internal connector for the VGA monitor connection.

- **CN10 : 16-pin header VGA connector**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	RED	2	GROUND
3	GREEN	4	GROUND
5	BLUE	6	GROUND
7	GROUND	8	GROUND
9	GROUND	10	HSYNC
11	GROUND	12	VSYNC
13	GROUND	14	NC
15	GROUND	16	NC

3.2 Serial Ports Connectors

The HS-4500's CN14, 16, 17 and 18 headers provides four high speeds NS16C550 compatible UARTs with Read/Receive 16 byte FIFO serial ports. Please see the following pin assignment. With the delivery package, user may uses the 40-pin COM cable for plug into CN14, 16, 17 and 18 for get COM1 to COM4 connection. The pin number inside the ( ) are for 40-pin cable.

- **CN14, 16, 17, 18 : Serial Port 10-pin Headers (COM1~COM4)**

COM Port	PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
COM 1 (CN14)	1(1)	DCD	2(2)	DSR
	3(3)	RXD	4(4)	RTX
	5(5)	TXD	6(6)	CTX
	7(7)	DTR	8(8)	RI
	9(9)	GND	10(10)	NC
COM 2 (CN 16)	1(11)	DCD	2(12)	DSR
	3(13)	RXD	4(14)	RTX
	5(15)	TXD	6(16)	CTX
	7(17)	DTR	8(18)	RI
	9(19)	GND	10(20)	NC
COM 3 (CN17)	1(21)	DCD	2(22)	DSR
	3(23)	RXD	4(24)	RTX
	5(25)	TXD	6(26)	CTX
	7(27)	DTR	8(28)	RI
	9(29)	GND	10(30)	NC
COM 4 (CN 18)	1(31)	DCD	2(32)	DSR
	3(33)	RXD	4(34)	RTX
	5(35)	TXD	6(36)	CTX
	7(37)	DTR	8(38)	RI
	9(39)	GND	10(40)	NC

If the GPS is in used. Please set COM-2 at Disable mode by JP5.

- **JP5 : COM2 Selection**

JP5	DESCRIPTION
ON	Disable
***OFF**	**Enable**

*) : default setting

- **JP15 : COM3 Selection**

JP15	DESCRIPTION
ON	Disable
***OFF**	**Enable**

*) : default setting

The HS-4500 also provides for user in select to using the COM4 as an RS-232/422/485. The CN18 for uses as an RS232, the CN11 for uses as an RS422 or RS485.

Please reference to the following for setting the JP9 & JP11 at disable and JP6 at enable if uses as RS232 at CN18. Or setting the JP9 & JP11 at non-disable and JP6 at disable if uses as RS422 or RS485 at CN11. The default setting is RS-232 at CN18.

- **CN11 : RS422/485**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	TX-	2	TX+
3	RX+	4	RX-
5	GND	6	RTS-
7	RTS+	8	CTS+
9	CTS-	10	NC

- **JP9 : Receiver Enable Control**

JP9	DESCRIPTION
1-2 ON	Always Enable
3-4 ON	Enable by writing the REG : 2 EFH BIT1=1
***1-2 OFF**	**Always Disable**

- **JP11 : Transceiver Enable Control**

JP11	DESCRIPTION
1-2 ON	Always Enable
3-4 ON	Enable by ”-RTS” signal
5-6 ON	Enable by writing the REG : 2 EFH BIT0=1
***7-8 OFF**	**Always Disable**

- **JP6 : COM4 Selection**

JP6	DESCRIPTION
ON	Disable
***OFF**	**Enable**

*) : default setting

3.3 Keyboard & Mouse Connector & FAN Power

The HS-4500 offers a possibility for Keyboard & Mouse connection with the Transfer Cable in obtain the connectors for Keyboard and Mouse by connect to header 8-pin CN7 header connector.

- **CN7 : 8-pin Header Keyboard & Mouse Connector**

PIN NO.	DESCRIPTION
1	GND
2	VCC
3	MS-DATA
4	MS-CLOCK
5	GND
6	VCC
7	KB-DATA
8	KB-CLOCK

The HS-4500 also offers a possibility for extra Keyboard connection with a 5-pin CN6 header connector.

- **CN6 : 5-pin Header Keyboard Connector**

PIN NO.	DESCRIPTION
1	KB-CLOCK
2	KB-DATA
3	N.C.
4	GND
5	VCC

- **FN1 : FAN Power in Connector**

PIN NO.	DESCRIPTION
1	NC
2	+12V
3	GND

3.4 Front Panel Connector

The onboard front panel connector CN2 provides a multi connection to Reset Button, WDT Indicator, Speaker Connector and IDE-Drive's Activity Indicator.

A ON between pin-7 and pin-8 may cause a Hardware Reset cycle to system. The Reset Button may connection to pin-7 and pin-8. Normal OFF is necessary for operating.

The pin-5 and pin-6 provides a WDT (Watch-Dog Timer) Indicator for the user application. It may also to used as an control signal in WDT activity control.

The pin-3 and pin-4 provides a Speaker out put connection for extra sound out.

The pin-1 and pin-2 provides a IDE-Drive's Activity Indicator connection to a LED for indicate the IDE-Drive activity status. A light ON says Activity.

- **CN2 : Front Panel Connector**

PIN NO.	DESCRIPTION	Input / Output
1	IDE-Drive's Indicator	Output
2	VCC	Power Vcc
3	Speaker-Out	Output
4	GND	Power Ground
5	GND	Power Ground
6	WDT Indicator	Output
7	GND	Power Ground
8	Reset Button	Input

3.5 PCI E-IDE Drive Connector

One standard 40-pin header daisy-chain driver connector provides as CN8 with following pin assignment. Total two IDE (Integrated Device Electronics) drivers may connect.

- **CN8 : IDE Interface Connector**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	N/C
21	N/C	22	GROUND
23	IOW#	24	GROUND
25	IOR#	26	GROUND
27	N/C	28	BALE - DEFAULT
29	N/C	30	GROUND# -DEFAULT
31	INTERRUPT	32	IOCS16#-DEFAULT
33	SA1	34	N/C
35	SA0	36	SA2
37	HDC CS0	38	HDC CS1#
39	HDD ACTIVE	40	GROUND

3.6 Parallel Port Connector

A standard 26-pin flat cable driver connector provides as CN12 with following pin assignment for connection to parallel printer.

- **CN12 : Parallel Port Connector**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	STROBE	2	DATA 0
3	DATA 1	4	DATA 2
5	DATA 3	6	DATA 4
7	DATA 5	8	DATA 6
9	DATA 7	10	ACKNOWLEDGE
11	BUSY	12	PAPER EMPTY
13	PRINTER SELECT	14	AUTO FORM FEED
15	ERROR#	16	INITIALIZE
17	PRINTER SELECT LN#	18	GROUND
19	GROUND	20	GROUND
21	GROUND	22	GROUND
23	GROUND	24	GROUND
25	GROUND	26	GROUND

3.7 Key-Lock Connector

The following provides the pin information for Key-Lock with Power's LED indicator connection from CN3.

- **CN3 : KEYLOCK with POWER LED Connector**

PIN NO.	DESCRIPTION
1	POWER LED ANODE
2	N.C.
3	GROUND
4	KEYLOCK
5	GROUND

3.8 GPS Connector

Caution: The information that provides herein this section is reference only. For detail and correctly information, please reference to your document along with the GPS Receiver that you have.

The HS-4500 provides a 2x10 pin-header optional connector for user place in the Rockwell's "Jupiter" Global Positioning System (GPS) Receiver. Firstly, please reference to the chapter 5 in this manual before using "Jupiter". For detail application, please contact with your nearest Rockwell office.

Please set COM-2 at Disable mode by JP5 when GPS in used.

- **CN1 : GPS Optional Connector**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	NOTE (0)	2	VCC
3	N.C.	4	N.C.
5	RESET#	6	N.C.
7	NOTE (1)	8	NOTE (1)
9	N.C.	10	GND
11	TXD2	12	RX2
13	GND	14	N.C.
15	NOTE (2)	16	GND
17	GND	18	GND
19	NOTE (3)	20	NOTE (4)

Note(0): No use in the first version of GPS application.
Note(1): Please reference to the next table for detail.
Note(2): No use in the first version of GPS application.
Note(3): Test only. 1PPS time mark output, rising edge synchronized with each set valid navigation binary message data.
Note(4): Test only. 10KHz clock waveform, positive logic synchronized to the pin-19.

- **JP14 & JP13: Host Communications Protocol Select**

JP14	JP13	DESCRIPTION
OFF	OFF	Data stored in SRAM or EEPROM determines message format, host port communication settings, and default message set.
OFF	ON	Binary message format; host port communication settings=9600bps, no parity, 8 data bits, 1 stop bit. The receiver operates from default initialization values stored in ROM.
ON	OFF	NMEA message format; host port communication settings=4800bps, no parity, 8 data bits, 1 stop bit. The receiver selects the default NMEA output message set and uses initialization values from the data stored in SRAM or EEPROM.
ON	ON	NMEA message format; host port communication settings=4800bps, no parity, 8 data bits, 1 stop bit. The receiver operates from default initialization values stored in ROM and will output the default NMEA message set from ROM.

3.9 The Floppy Disk Drive Connector

A standard 34-pin header daisy-chain driver connector provides as CN19 with following pin assignment. Total two FDD drivers may connect.

- **CN19 : FDD CONNECTOR**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GROUND	2	REDUCE WRITE
3	GROUND	4	N/C
5	GROUND	6	N/C
7	GROUND	8	INDEX#
9	GROUND	10	MOTOR ENABLE A#
11	GROUND	12	DRIVE SELECT B#
13	GROUND	14	DRIVE SELECT A#
15	GROUND	16	MOTOR ENABLE B#
17	GROUND	18	DIRECTION#
19	GROUND	20	STEP#
21	GROUND	22	WRITE DATA#
23	GROUND	24	WRITE DATA#
25	GROUND	26	TRACK 0#
27	GROUND	28	WRITE PROTECT#
29	GROUND	30	READ DATA#
31	GROUND	32	SIDE 1 SELECT
33	GROUND	34	DISK CHANGE#

3.10 DC Main Power Connector

The HS-4500 provides a CN9 connector for the main DC power input connection as following pin assignment of +5V and +12V.

- **CN9 : POWER CONNECTOR**

PIN NO.	DESCRIPTION
1	+12V
2	GROUND
3	GROUND
4	VCC

- **CN20 : POWER**

PIN NO.	DESCRIPTION
1	-12V
2	GND
3	-5V
4	GND

3.11 Connectors of the on-board Sound Adapter

The HS-4500 has an on-board ESS® Solo-1 3D sound interface. The following are the connectors of AUXA, AUXB and MIC/SPEAKER connectors.

The AUXA and AUXB connectors are for audio sound input. The AUXA provides for 4-pin connection, and AUXB provides for 3-pin connection.

- **JP3 : AUXA Connector**

PIN NO.	DESCRIPTION
1	AUXAL
2	GND
3	AUXAR
4	GND

- **JP4 : AUXB Connector**

PIN NO.	DESCRIPTION
1	AUXAL
2	GND
3	AUXAR

- **JP18 : MIC/SPEAKER Connector**

PIN NO.	DESCRIPTION		PIN NO.	DESCRIPTION	
1	AOUTL	Red	2	AOUTR	White
3	GND	Black	4	GND	Key
5	MIC	Red	6	N.C.	White
7	GND	Black	8	GND	Key

With MIC/SPEAKER cable, user may connect R/L Speaker to the AOUTL and AOUTR pins of JP18, and connect Microphone to the MIC pin of JP18.

3.12 Fast Ethernet Connector

The Fast Ethernet controller provides with 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3 10/100Based-T specifications.

For 10/100Base-T operation, please connect the network connection by plugging one end of the cable into the 10-pin header of the CN13 Connector.

- **CN13 : Ethernet Connector (header 10-pin)**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	VCC	2	N.C.
3	RX+	4	RX-
5	N.C.	6	GND
7	N.C.	8	GND
9	TX+	10	TX-

3.13 PC/104 Bus Connection

The HS-4500's PC/104 expansion bus provides you in connect to all kind of PC/104 modules. The PC/104 bus has been already become the industrial embedded 16-bit PC standard bus. You can easily install to over thousands type of PC/104 modules from hundreds of venders in the world. The detailed pin assignment of the PC/104 expansion bus connectors CN4 and CN5 are specified as following tables:

Note : The PC/104 connector allows to directly plug-in Stack-thru PC/104 modules without the PC/104 mounting kit.

- **CN4&CN5 : PC/104 Expansion Bus**

(CN4 = 64-pin female connector; CN5 = 40-pin female connector.)

Pin No.	CN4 Row A	Pin No.	CN4 Row B
1	IOCHECK*	33	0V
2	SD7	34	RESETDRV
3	SD6	35	+5V
4	SD5	36	IRQ9
5	SD4	37	-5V
6	SD3	38	DRQ2
7	SD2	39	-12V
8	SD1	40	NOW*
9	SD0	41	+12V
10	IOCHRDY	42	(KEY)
11	AEN	43	SMEMW*
12	SA19	44	SMEMR*
13	SA18	45	IOW*
14	SA17	46	IOR*
15	SA16	47	DACK3*
16	SA15	48	DRQ3
17	SA14	49	DACK1*
18	SA13	50	DRQ1
19	SA12	51	REFRESH*
20	SA11	52	SYSCLK
21	SA10	53	IRQ7
22	SA9	54	IRQ6
23	SA8	55	IRQ5
24	SA7	56	IRQ4
25	SA6	57	IRQ3
26	SA5	58	DACK2*
27	SA4	59	TC
28	SA3	60	BALE
29	SA2	61	+5V
30	SA1	62	OSC
31	SA0	63	0V
32	0V	64	0V

Pin No.	CN5 Row D	Pin No.	CN5 Row C
1	0V	21	0V
2	MEMCS16*	22	SBHE*
3	IOSC16*	23	LA23
4	IRQ10	24	LA22
5	IRQ11	25	LA21
6	IRQ12	26	LA20
7	IRQ15	27	LA19
8	IRQ14	28	LA18
9	DACK0*	29	LA17
10	DRQ0	30	MEMR*
11	DACK5*	31	MEMW*
12	DRQ5	32	SD8
13	DACK6*	33	SD9
14	DRQ6	34	SD10
15	DACK7*	35	SD11
16	DRQ7	36	SD12
17	+5V	37	SD13
18	MASTER*	38	SD14
19	0V	39	SD15
20	0V	40	(KEY)

3.14 Flat-Panel Connector

The HS-4500 provides a 50-pin 2.0 mm pitch header connector (JP12) for 3.3V Flat panel connection with following pin-assignment.

+12V	1	2	+12V
GND	3	4	GND
+3V PVcc	5	6	ENAVdd
FPVee	7	8	GND
P_0	9	10	P_1
P_2	11	12	P_3
P_4	13	14	P_5
P_6	15	16	P_7
P_8	17	18	P_9
P_{10}	19	20	P_{11}
P_{12}	21	22	P_{13}
P_{14}	23	24	P_{15}
P_{16}	25	26	P_{17}
P_{18}	27	28	P_{19}
P_{20}	29	30	P_{21}
P_{22}	31	32	P_{23}
P_{24}	33	34	P_{25}
SHFCLK	35	36	FLM
M	37	38	LP
GND	39	40	ENABKL
P26	41	42	P27
P28	43	44	P29
P30	45	46	P31
P32	47	48	P33
P34	49	50	P35

- **JP17 : Panel Power Selection**

JP17	DESCRIPTION
1-2	3V Power
2-3	**5V Power**

3.15 USB Ports Connector

The HS-4500 provides one 10-pin connector for USB-0 & USB-1 ports. Please refer to the following default pin information.

- **CN22 : USB Ports Connector**

PIN NO.	USB-0	PIN NO.	USB-1
1	VCC	2	VCC
3	USB PO-	4	USB P1-
5	USB PO+	6	USB P1+
7	GND	8	GND

Chapter-4

AWARD BIOS Setup

The HS-4500 uses Award PCI/ISA BIOS for the system configuration. The Award BIOS setup program is designed to provide the maximum flexibility in configuring the system by offering various options which could be selected for end-user requirements. This chapter is written to assist you in the proper usage of these features.

To access AWARD PCI/ISA BIOS Setup program, press <Del> key during memory testing when first power on. The Main Menu will be displayed at this time.

4.1 Main Menu

Once you enter the Award BIOS CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to enter the sub-menu.

ROM PCI/ISA BIOS (xxxxxxxx)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.

STANDARD CMOS SETUP	INTEGRATED PERIPHERALS
BIOS FEATURES SETUP	SUPERVISOR PASSWORD
CHIPSET FEATURES SETUP	USER PASSWORD
POWER MANGEMENT SETUP	IDE HDD AUTO DETECTION
PCI CONFIGURATION SETUP	SAVE & EXIT SETUP
LOAD BIOS DEFAULTS	EXIT WITHOUT SAVING
LOAD SETUP DEFAULTS	
Esc : Quit	↑↓→← : Select Item
F10 : Save & Exit	(Shift)F2 : Change Color

Note that a brief description of each highlighted selection appears at the bottom of the screen.

4.2 Standard CMOS Setup

The Standard Setup is used for the basic hardware system configuration. The main function is for Data/Time and Floppy/Hard Disk Drive settings. Please refer to the following screen for the setup. When the IDE hard disk drive you are using is larger than 528MB, please set the HDD mode to **LBA** mode. Please use the IDE Setup Utility in BIOS SETUP to install the HDD correctly.

ROM PCI/ISA BIOS (2A5KKD29)
STANDARD CMOS SETUP
AWARD SOFTWARE, INC.

Data (mm:dd:yy) : Fri, Oct 19 1999

Time (hh:mm:ss) : 00:00:00

			CYLS	HEAD	PRECOMP	LANDZ	SECTOR	MODE
Driver C	:	Auto (0Mb)	0	0	0	0	0	Auto
Driver D	:	Auto (0Mb)	0	0	0	0	0	Auto

Drive A : 1.44M , 3.5in.
Drive B : None

LCD&CRT : CRT

Halt On : All, But keyboard

Base	Memory	:	640K
Extended	Memory	:	130048K
Other	Memory	:	384K
Total	Memory	:	131072K

ESC : Quit ↑↓→← : Select Item PU/PD/ + / - : Modify
F1 : Help (Shift) F2: Change Color

4.3 BIOS Features Setup

This section allows you to configure your system for the basic operation. You have the opportunity to select the system's default speed, boot-up sequence, keyboard operation, shadowing and security.

ROM PCI/ISA BIOS (2A5KKD29)
BIOS FEATURES SETUP
AWARD SOFTWARE, INC.

Virus Warning	: Disabled	Video BIOS	Shadow	: Enabled	
CPU Internal Cache	: Enabled	C8000-CBFFF	Shadow	: Disabled	
External Cache	: Enabled	CC000-CFFF	Shadow	: Disabled	
Quick Power On Self Test	: Disabled	D0000-D3FFF	Shadow	: Disabled	
Boot Sequence	: C,CDROM,A	D4000-D7FFF	Shadow	: Disabled	
Swap Floppy Drive	: Disabled	D8000-DBFFF	Shadow	: Disabled	
Boot Up Floppy Seek	: Enabled	DC000-DFFFF	Shadow	: Disabled	
Boot Up NumLock Status	: On	Cyrix 6x86/MII CPUID		: Enabled	
Boot Up System Speed	: High				
Gate A20 Option	: Fast				
Typematic Rate Setting	: Disabled				
Typematic Rate (Chars/Sec)	: 6				
Typematic Delay (Msec)	: 250				
Security Option	: Setup				
PCI/VGA Palette Snoop	: Disabled				
Assign IRQ For VGA	: Enabled	ESC	: Quit	↑↓→←: Select Item	
OS Select For DRAM > 64MB	: Non-OS2	F1	: Help	PU/PD/+/-: Modify	
Report No FDD For WIN 95	: Yes	F5	: Old Values	(Shift) F2 : Color	
		G6	: Load BIOS Defaults		
		G7	: Load Setup Defaults		

4.4 Chipset Features Setup

This section allows you to configure the system based on the specific features of the installed chipset. This chipset manages bus speeds and the access to the system memory resources, such as DRAM and the external cache. It also coordinates the communications between the conventional ISA and PCI buses. It must be stated that these items should never be altered. The default settings have been chosen because they provide the best operating conditions for your system. You might consider and make any changes only if you discover that the data has been lost while using your system.

ROM PCI/ISA BIOS (2A5KKD29)
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.

Auto Configuration	: Enabled	
AT Bus Clock	: CLK2/4	
L2 TA RAM Size	: 8	
DRAM Timing	: Nomal	
SDRAM CAS Latency	: 3	
Pipilined Function	: Enabled	
Graphics Aperture Size	: 64 MB	
DRAM Date Integrity Mode	: Disabled	
Memory Hole At 15M-16M	: Disabled	
Host Read DRAM Command Mode	: Syn.	
AGP Read Burst	: Enabled	
ISA Line Buffer	: Enabled	
Passive Release	: Enabled	
Delay Transaction	: Disabled	
Primary Frame Buffer	: All	
VGA Frame Buffer	: Enabled	ESC : Quit ↑↓→←: Select Item
Data Merge	: Disabled	F1 : Help PU/PD/+/-: Modify
IO Recovery Period	: 1 us	F5 : Old Values (Shift) F2 : Color
		F6 : Load BIOS Defaults
		F7 : Load Setup Defaults

4.5 Integrated Peripherals

The IDE hard drive controllers can support up to two separate hard drives. These drives have a master/slave relationship which is determined by the cabling configuration used to attach them to the controller. Your system supports two IDE controllers--a primary and a secondary--so you can install up to four separate hard disks.

PIO means Programmed Input /Output. Rather than having the BIOS issue a series of commands to affect the transfer to or from the disk drive, PIO allows the BIOS to tell the controller what it wants and then let the controller and the CPU perform the complete task by them. This is much simpler and more efficient (also faster).

ROM PCI/ISA BIOS (2A5KKD29)
INTEGRATED PERIPHERALS
AWARD SOFTWARE, INC.

On-Chip Primary Mode	:	Enabled			
Master PIO	:	Auto			
Slave PIO	:	Auto	KBC clock source	:	8 MHz
Master UDMA	:	Auto	Onboard FDC Controller	:	Enabled
Slave UDMA	:	Auto	Onboard UART Port 1	:	3F8/IRQ4
			Onboard UART Port 2	:	2F8/IRQ3
IDE HDD Block Mode	:	Enabled	Onboard Parallel Port	:	378/IRQ7
On-Chip USB Controller	:	Disabled	Parallel Port Mode	:	ECCEPP 1.9
			ECP Mode Use DMA	:	3
Init Display First	:	PCI Slot	Onboard IrDA Port	:	Disabled
Ring/Wake On LAN Control	:	Disabled			
RIC Alarm Controller	:	Disabled	Onboard Serial Port 3	:	3E8
			Serial Part 3 Use IRQ	:	IRQ3
			Onboard Serial Port 4	:	2E8
			Serial Port 4 Use IRQ	:	IRQ3
			LCD Panel Type	:	Panel 5

Panel#	Panel Type
0	1024*768 Dual Scan STN Color Panel
1	128*1024 TFT Color Panel
2	640*480 Dual Scan STN Color Panel
3	800*600 Dual Scan STN Color Panel
4	640*480 Sharp TFT Color Panel
5	640*480 18-bit TFT Color Panel
6	1024*768 TFT Color Panel
7	800*600 TFT Color Panel
8	800*600 TFT Color Panel (Large BIOS ONLY)
9	800*600 TFT Color Panel (Large BIOS ONLY)
10	800*600 Dual Scan STN Color Panel (Large BIOS ONLY)
11	800*600 Dual Scan STN Color Panel (Large BIOS ONLY)
12	1024*768 TFT Color Panel (Large BIOS ONLY)
13	1280*1024 Dual Scan STN Color Panel (Large BIOS ONLY)
14	1024*600 Dual Scan STN Color Panel (Lange BIOS ONLY)
15	1024*600 TFT Color Panel (Lange BIOS ONLY)

4.6 Power Management Setup

The Power Management Setup allows user to configure the system for saving energy in a most effective way while operating in a manner consistent with his own style of computer use.

ROM PCI/ISA BIOS (2A5KKD29)
POWER MANAGEMENT SETUP
AWARD SOFTWARE, INC.

Power Management	:	User Define	** External Switch **		
PM Control by APM	:	Yes	Power Button Mode	:	Instant-off
MODEM Use IRQ	:	3	DOCK I/O SMI	:	Disabled
Video Off Option	:	Susp, stby ->Off	AC Power SMI	:	Disabled
Video Off Method	:	DPMS Support	Thermal SMI mode	:	Disabled
** PM Times **					
HDD Off After	:	Disabled			
Doze Mode	:	Disabled			
Standby Mode	:	Disabled			
Suspend Mode	:	Disabled			
FAN Off Option	:	Suspend-> Off			
Wake on LAN Use	:	NA			
** PM Events **					
Primary HDD	:	Disabled	ESC : Quit		↑↓→←: Select Item
Floppy	:	Disabled	F1 : Help		PU/PD/+/-: Modify
COM Ports Activity	:	Enabled	F5 : Old Values		(Shift) F2 : Color
LPT Ports Activity	:	Enabled	F6 : Load BIOS Defaults		
			F7 : Load Setup Defaults		

Chapter-5

Software Utilities

This chapter the detailed information of VGA and LAN function. How to install the configuration is also included.

Section include:

- VGA DRIVER INSTALLATION
- NETWORK DRIVER INSTALLATION

5.1 VGA DRIVER INSTALL FOR WIN95&98

1. Click Start, then Setting, then Control Panel.
2. Start the Display applet program.
3. Select the setting page, push the Advanced properties button.
4. Push the change button in the adapter area.
5. Continue to click “Next”. Select

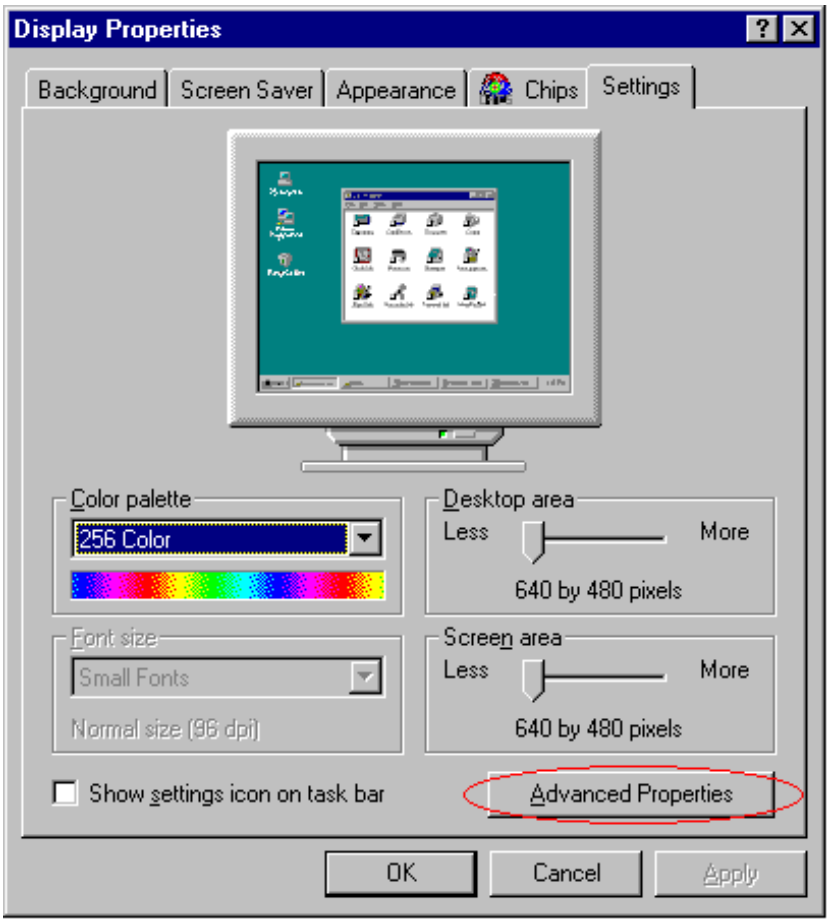
   Display a list of all drivers in a specific location,

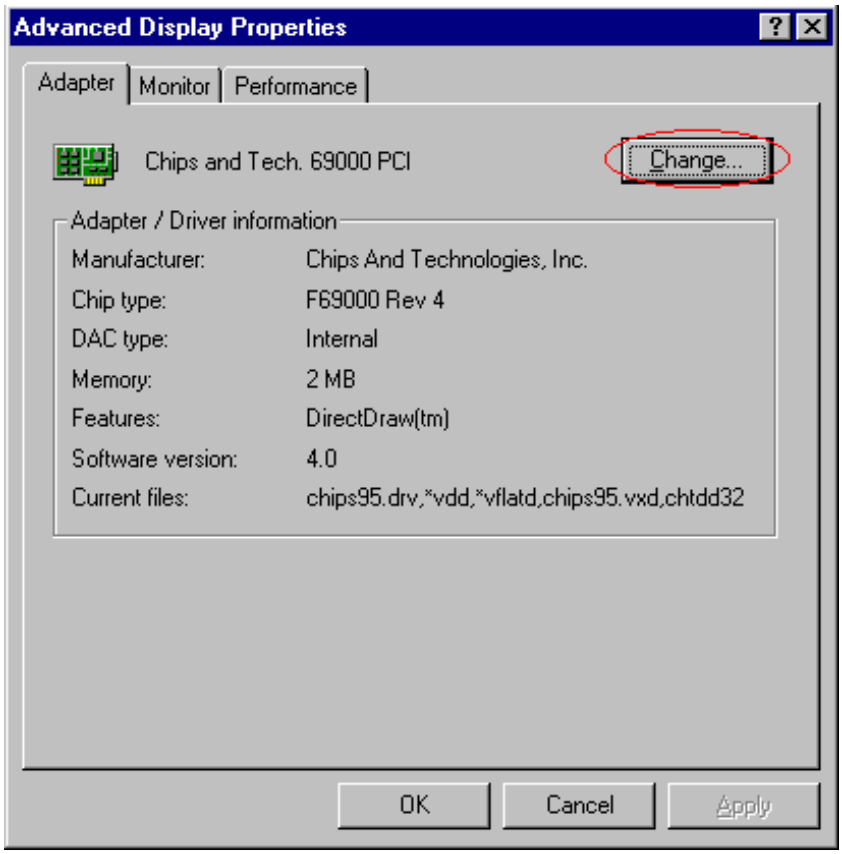
   so you can select the drivers you want.
6. Click “Next”.
7. Select the Specify a location checkbox and click “Browse”.
8. Specify the path to the new driver and press the ,<ENTER> key.

   (if in driver A:, select a:\win95)
9. The Select device dialog box will appear.

   Select Chips and Tech. 69000 PCI
10. Continue choosing close until asked to restart machine.
11. After the system has restarted, you can go back into the display applet and select alternate screen resolutions and color depths.

Note: Installation procedure for Windows 98 is similar to Windows95.


Display Properties
Background
Screen Saver
Appearance
Chips
Settings
Color palette
256 Color
Desktop area
Less
More
640 by 480 pixels
Font size
Small Fonts
Normal size (96 dpi)
Screen area
Less
More
640 by 480 pixels
Show settings icon on task bar
Advanced Properties
OK
Cancel
Apply

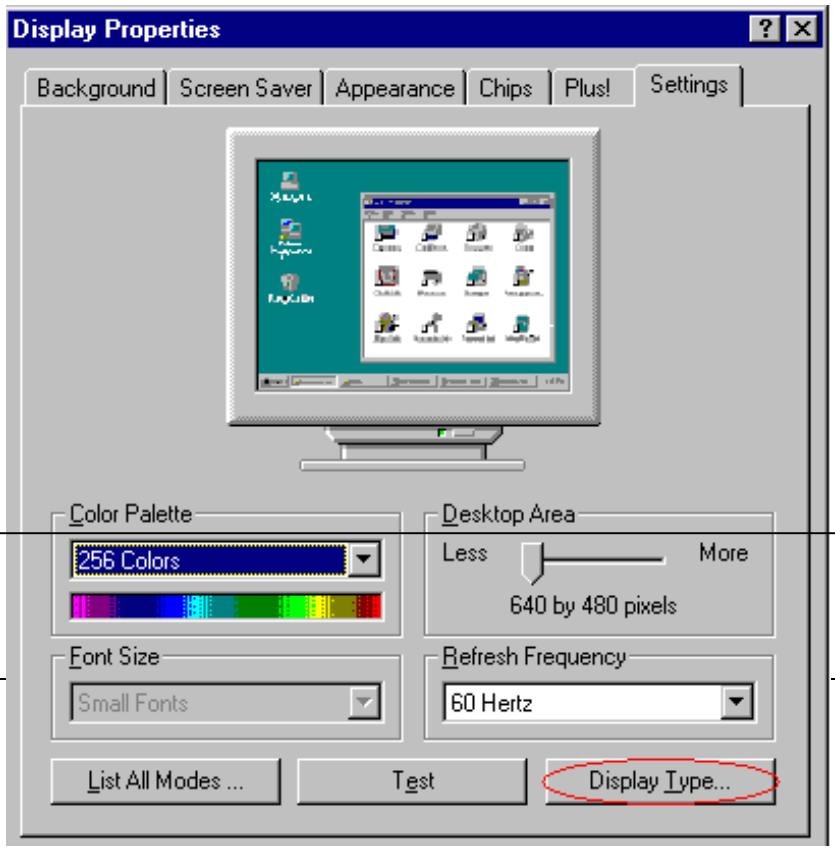


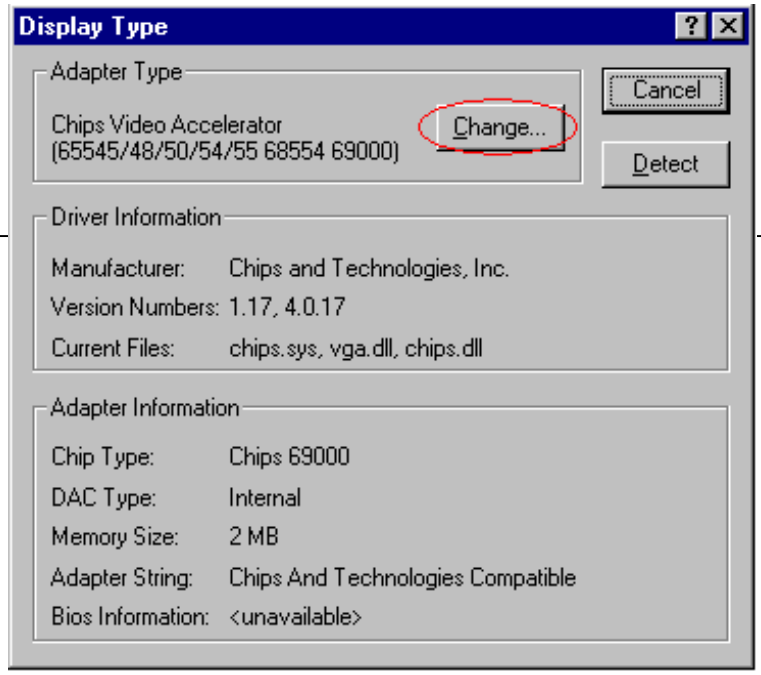
5.2 VGA DRIVER INSTALL FOR WIN NT4.0

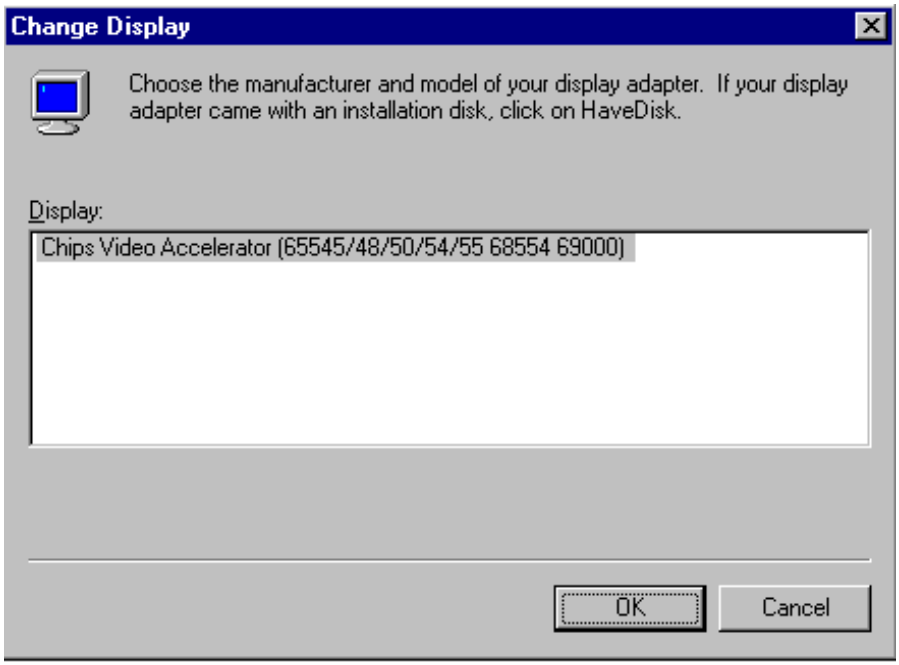
1. Click the Start button, then go to Settings and click on Control Panel.
2. Click on Display icon to start the Display Properties window.
3. Click on the Settings tab, and then click on Display Type.
4. In the Change Display Type window, click on “Have Disk”.
5. Specify the path to the new driver and press the <ENTER>key.

   (if in driver A:, type a:\nt40)

   select Chips Video Accelerator (655545/48/50/54/55/68554 69000)
6. click OK or press Enter
7. You will then see warning panel about Third Party Drivers. Click on Yes to finish the install.
8. Once the installation is complete, the system must shut down and restart for the new driver to take effect.




Display Type
Adapter Type
Chips Video Accelerator
(65545/48/50/54/55 68554 69000)
Change...
Cancel
Detect
Driver Information
Manufacturer: Chips and Technologies, Inc.
Version Numbers: 1.17, 4.0.17
Current Files: chips.sys, vga.dll, chips.dll
Adapter Information
Chip Type: Chips 69000
DAC Type: Internal
Memory Size: 2 MB
Adapter String: Chips And Technologies Compatible
Bios Information: <unavailable>


Change Display
Choose the manufacturer and model of your display adapter. If your display adapter came with an installation disk, click on HaveDisk.
Display:
Chips Video Accelerator (65545/48/50/54/55 68554 69000)
OK
Cancel

Chapter-6

The GPS Receiver

The HS-4500 is designed to facilitate options of Rockwell's "Jupiter" Global Positioning System (GPS) receiver engine based on the Zodiac chip set. The HS-4500 with GPS engine can be used in both static and mobile operations for evaluation purposes.

The HS-4500 implements the receiver control operation and input/output (I/O) functions of the GPS receiver through a serial port, external antenna, and LABMON software. The GPS receiver is connecting by a 2x10 header connector to the HS-4500. Please reference to the section 3-8 for pin-assignment.

For detail application, please reference to the attached manual of the GPS engine.

For application information, please contact with your supplier of your GPS engine device, or please browse at **http:\\www.rockwell.com**