Vectra XU Hardware and BIOS Technical Reference Manual

Introduction

Summary of the HP BIOS

The Integrated Ultra VGA Controller

Power-On Self Tests

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Introduction

Preface

This manual is a technical reference and BIOS document for engineers and technicians who provide system level support, or who are engaged in the design of system-compatible products. It is assumed that the reader possesses a fairly detailed understanding of AT-compatible microprocessor functions and digital addressing techniques.

Technical information that is readily available from other sources, such as manufacturer's proprietary publications, has not been reproduced.

For additional reference material, refer to the bibliography.

This manual contains summary BIOS information only. For detailed information, we recommend the reference work cited in the next section.

Conventions

The following conventions are used throughout this manual to identify specific elements:

- Hexadecimal numbers are identified by a lower case h.

  For example, 0FFFFFFFh or 32F5h
- Binary numbers and binary bit patterns are identified by a lower case b.

  For example, 11101b or 1001011b

Ordering Information for the Phoenix BIOS Manual

System BIOS for IBM PCs, Compatibles, and EISA Computers (ISBN 0-201-57760-7) by Phoenix Technologies is available in many bookstores. It can also be ordered directly from the publisher as follows:

In the U.S.A.

Call Addison-Wesley in Massachusetts at +1-800-447-2226, and be prepared to give a credit card number and expiry date.

In Europe

Send a request to:

Addison-Wesley
Concertgebouwplein 25
1071 LM Amsterdam, The Netherlands
Tel.: +31 (20) 671 72 96
Fax: +31 (20) 675 21 41

Bibliography

- *Vision864 GUI Accelerator*© S3 Incorporated, 2770 San Tomas Expressway, Santa Clara, CA 95051-0981
- *Am79C960 PCnet-ISA, Single-Chip Ethernet Controller for ISA*™ Advanced Micro Devices, Incorporated
- *System BIOS for IBM PCs, Compatibles, and EISA Computers* (ISBN 0-201-57760-7) by Phoenix Technologies. Addison-Wesley (publisher)

The following Hewlett Packard publications may also assist the reader of this manual.

- HP Vectra XU PC *Setting Up Your PC* and *Getting Started* manuals (D3080B xxxxx, where xxxxx is the language option)
- *HP Vectra XU PC Familiarization Guide* (D308xA+49A+90001)
- *HP Vectra PC Service Handbook* (5963-6104)

The following Intel® publications provide more detailed information:

- *PENTIUM Processor* (241595-1)
- *82430 PCIset for the PENTIUM Processor* (290481-001)
- 82424TX Cache and DRAM Controller (290471-001)
- 82423TX Data Path Unit (290472-001)
- 823781B System I/O (290473-001)

System Overview

Introduction

This chapter provides a description of the HP Vectra XU PC Series, and includes detailed system specifications.

PCI Local Bus Architecture

This HP Vectra PC uses the PCI local bus architecture. The PCI (Peripheral Component Interconnect) architecture lets system devices operate at speeds approaching that of the processor and removes the data transfer bottleneck imposed by the ISA, EISA, and MCA buses.

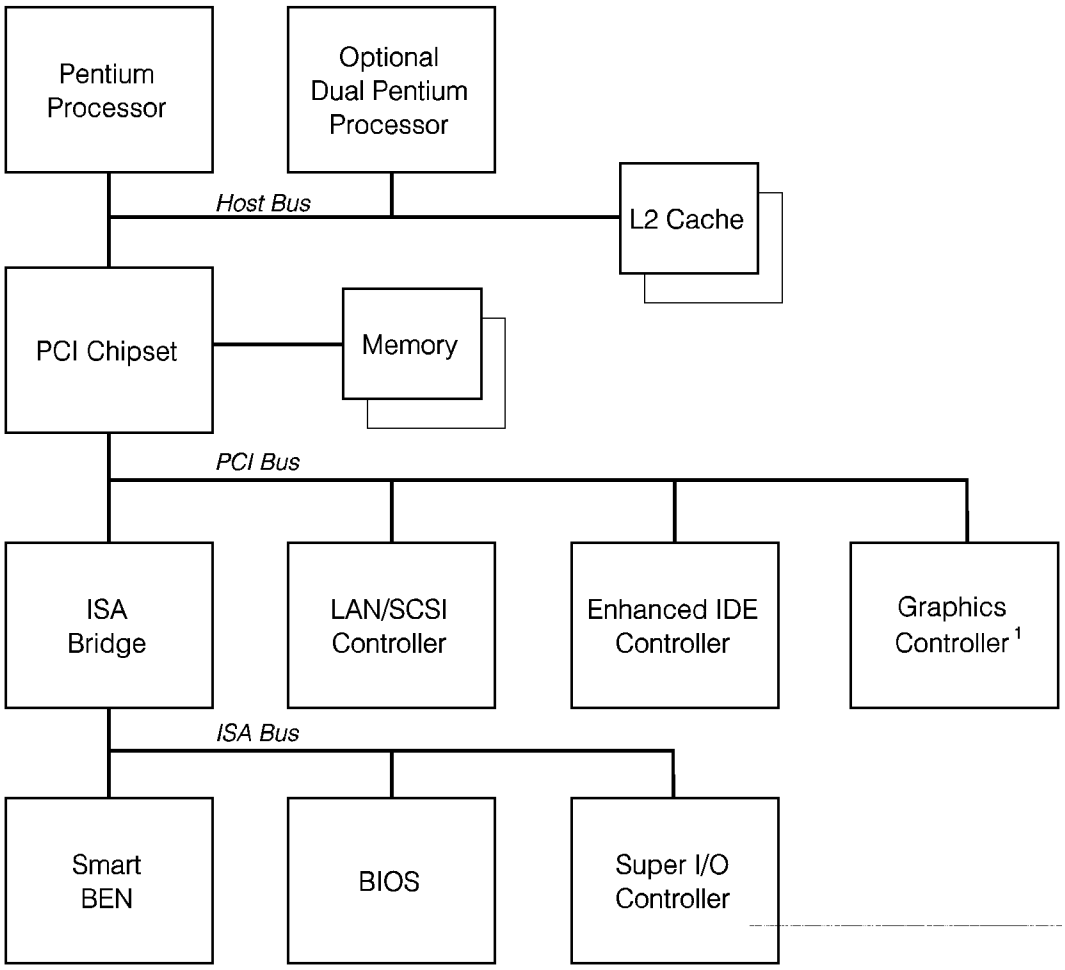
This performance improvement is of particular value to graphics accelerators, disk controllers, and network adapters which need to transfer large blocks of data very quickly.

The principal features of the PCI bus are:

- Processor independence
- Support for up to 21 physical PCI device packages (each device package may contain up to 8 PCI devices, which enables support for up to 168 PCI devices)
- 132 MByte per second peak transfer rate for both read and write transfers
- PCI bus speed of up to 33 MHz.

NOTE The PCI bus specification was developed by Intel Corporation. For information regarding the specification, contact: PCI Special Interest Group c/o Intel Corporation, 5200 NE Elam Young Parkway, HF3-15A Hillsboro, OR 97124, U.S.A.

System Block Diagram

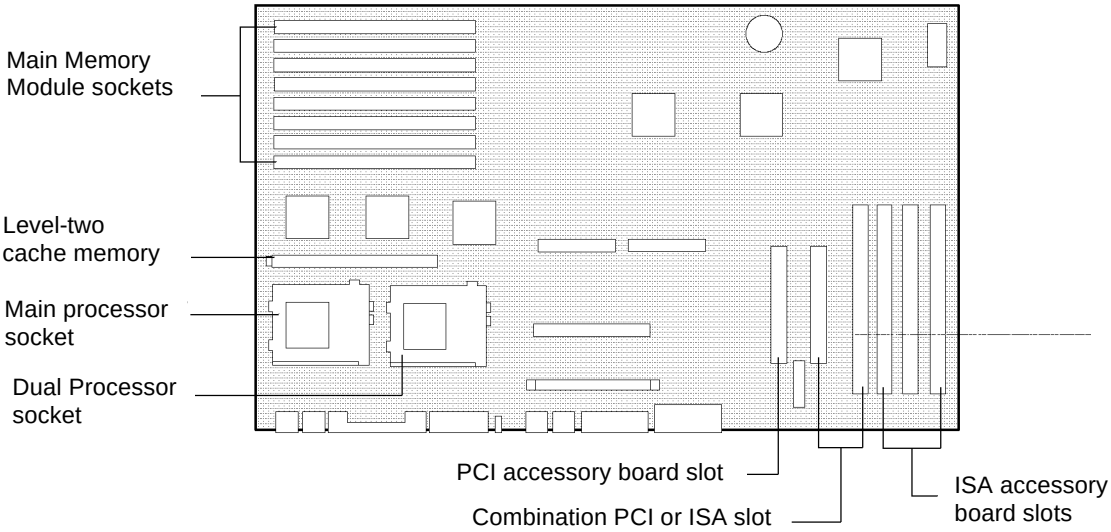


[1] S3 Graphics Accelerator , or
Matrox PCI video board , according to model

Principal Components and Features

The HP Vectra XU PC is an ISA/PCI-based PC and features the Pentium&TM; microprocessor and the 82430 chip set.

System Board



The main features of the system board are:

- a Pentium 75, 90 or 100 MHz microprocessor
- a socket for a dual companion processor
- a PCI bus video controller:
  - the HP Vectra XU 5/75 and XU 5/90 has an integrated Ultra VGA+ video controller on the PCI bus with 2 MB of video memory (for 1280 x 1024 resolution in 256 colors)
  - the HP Vectra XU 5/90C and XU 5/100C do not have an integrated video controller. They are supplied with a pre-installed Matrox MGA PCI/2+ video board or a Matrox Impression Plus video board. Both Matrox video boards have 2 MB of video memory (for 1600 x 1200 resolution in 256 colors). The video boards can be upgraded to 4 MB (for 1600 x 1200 in 64K colors).
- a combined LAN/SCSI controller on the PCI bus
- an Enhanced IDE controller on the PCI bus, with one IDE device connector
- an integrated flexible disk controller for two flexible disk drives
- eight sockets for DRAM main memory modules--allowing installation of up to 256 MB
- a system ROM (using flash ROM technology) that can be easily updated using an *HPROMInit*, containing:
  - the BIOS
  - a power-on hardware test that allows you to view the results of the diagnostics as well as a corrective action message
  - SETUP in local language with context-sensitive help
  - LAN boot code (to start the PC from a LAN server) for use with Ethernet LAN adapters and either a Novell Netware or LAN Manager server

- a keyboard/mouse controller and interface
- one serial connector and one parallel connector--for attaching peripherals
- an integrated 16-bit Ethernet interface, configurable from SETUP
- a system board mounted LAN connector (UTP) and link beat LED
- a system board mounted Coax LAN connector

Processor

The Pentium processor uses 64-bit architecture and is 100% compatible with Intel's family of x86 microprocessors. All application software that has been written for Intel 386 and Intel 486 microprocessors can run on the Pentium without any modification. It contains all the features of the Intel 486 microprocessor, with the following features added to enhance performance:

- Superscaler Architecture
- Floating Point Unit
- Dynamic Branch Prediction
- Instruction and Data cache
- Data Integrity
- Supports MultiProcessor Specification (MPS) 1.1
- PCI Bus Architecture.

The microprocessor is seated in a Zero Insertion Force (ZIF) socket.

Superscalar Architecture

The Pentium processor's superscaler architecture has two instruction pipelines and a floating-point unit, each capable of independent operation. The two pipelines let the Pentium execute two integer instructions, in parallel, in a single clock cycle. Using the pipelines halves the instruction execution time and almost doubles the performance of the processor, compared to an Intel486 microprocessor of the same frequency.

Frequently, the processor can issue two instructions at once (one instruction to each pipeline). This is called instruction pairing. Each instruction must be simple. One pipeline will always receive the next sequential instruction of that issued to the other pipeline.

Floating Point Unit (FPU)

The Floating Point Unit incorporates optimized algorithms and dedicated hardware for multiply, divide, and add functions. This increases the processing speed of common operations by a factor of three.

Dynamic Branch Prediction

The Pentium processor uses dynamic branch prediction. To dynamically predict instruction branches, the processor uses two prefetch buffers. One buffer is used to prefetch code in a linear way and one to prefetch code depending upon the contents of the Branch Target Buffer (BTB). The BTB is a small cache that keeps a record of the last instruction and address used. It uses this information to predict the way that the instruction will branch, the next time it is used. When it has made a correct prediction the branch is executed without delay, enhancing performance.

Instruction and Data Cache

The Pentium processor has separate code and data caches on-chip. Each cache is 8 KB in size with a 32-bit line. The caches act as temporary storage for data and instructions from the main memory. As the system is likely to use the same data several times, it is faster to get it from the on-chip cache than from the main memory.

Each cache has a dedicated Translation Lookaside Buffer (TLB). The TLB is a cache of the most recently accessed memory pages.The data cache is configured to be Write-Back on a line-by-line basis(a line is an area of memory of a fixed size).

The data cache tags (directory entries used to reference cached memory pages) are triple ported to support two data transfers and an inquire cycle in the same clock cycle.

The code cache tags are also triple ported to support snooping (a way of checking for accesses to main memory by other devices) and split line accesses.

Individual pages of memory can be configured as cacheable or non-cacheable by software or hardware, they can also be enabled and disabled by software or hardware.

Data Integrity

The processor uses a number of techniques to maintain data integrity. It employs two methods of error detection:

- Data Parity Checking

  This is supported on a byte-by-byte basis, generating parity bits for data addresses sent out of the microprocessor. These parity bits can be checked by the external subsystems that will be using the data.

- Internally

  The processor uses functional redundancy checking to provide maximum error detection of the processor and its interface. When functional redundancy checking is used, a second processor (the checker) operates in lock step with the master processor. The checker samples the master's outputs and compares them with the values it computes internally. An error signal is produced if a mismatch is detected.

PCI Chip Set

The chip set consists of three devices:

- The PCI, Cache, and Memory Controller (PCMC)
- The Local Bus Accelerator (LBX)
- The PCI/ISA bridge (PCEB and ESC).

The PCMC and LBX provide the core cache and memory system architecture and PCI interface. The PCEB/ESC is a PCI master/slave which bridges the core architecture to the standard ISA bus.

PCI, Cache, and Memory Controller (PCMC)

The 82434LX PCMC integrates cache and main memory control functions and provides bus control functions for the transfer of information between the microprocessor, cache, main memory and the PCI bus. The cache controller supports the Pentium Cache Write-Back mode and 256 KB of direct mapped Level Two cache using standard or burst SRAMs.

Local Bus Accelerator (LBX)

The two 82433LX LBX components provide the following data paths:

- 64-bit data path between the host bus and main memory
- 32-bit data path between the host microprocessor and the PCI local bus
- 32-bit data path between the PCI bus and the main memory.

The dual port architecture permits concurrent operations on the host bus and the PCI bus. There are three write posting buffers and two read prefetch buffers to increase the performance of the Pentium processor and of PCI master devices. During bus operations the PCMC commands the LBXs to perform functions such as latching address and data, merging data, and enabling the output buffers.

The PCI/ISA Bridge (PCEB and ESC)

The PCEB and ESC serve as a bridge between the PCI local bus and the ISA expansion bus. They incorporate the logic for a PCI interface, an ISA interface, a DMA controller that supports fast DMA transfers, data buffers to isolate the PCI and ISA buses, Timer/Counter logic, and NMI control logic.

The PCI/ISA bridge also provides decode for the following peripheral devices:

- Flash BIOS
- Real Time Clock
- Keyboard/Mouse Controller
- Flexible Disk Controller
- Two Serial Ports
- One Parallel Port
- IDE Hard Disk Drive
- Two PCI Accessory Board Slots (supporting 7.5W/3.3V boards).

Super I/O Chip Set

The basic input/output control functions are provided by the Super I/O chip, PC87332VF. This chip set has the following features:

- an integrated flexible drive controller that supports 5.25-inch 360 KB and 1.2 MB drives, and 3.5-inch 1.44 MB and 2.8 MB drives
- a multi-mode parallel port
- one serial port.

Flexible Drive Controller (FDC)

The FDC is software and register compatible to the 82077AA and 100% IBM compatible. It has an A and B drive-swapping capability and a non-burst DMA option.

Serial/Parallel Ports

One serial port and one bidirectional parallel port are supported by the Super I/O chip set. The serial port is a high speed UART with 16 Byte FIFO and can be programmed as COM1, COM2, COM3, COM4, or disabled.

The parallel port can operate in three modes:

- Standard mode (PC/XT, PC/AT, and PS/2 compatible)
- Enhanced mode (Enhanced parallel Port (EPP) compatible)
- High speed mode (MS/HP Extended Capabilities Port (ECP) compatible).

It can be programmed as LPT1 (378h, IRQ7), LPT2 (278h, IRQ5), or disabled with PC87332VF registers.

Graphics/Integrated Video

According to model, the video subsystem is composed of an Vision864 Graphical User Interface (GUI) accelerator for the PCI bus, a 64-bit true color RAMDAC and DRAM array, or it may have a Matrox Video Board. Refer to the documentation supplied with your Matrox Board.

The highest mode that is supported is 1280 x 1024 with a screen refresh rate of 75 Hz.

Video Controller

The S3 Vision864 video controller offers full compatibility with VGA, CGA, HGC, and MDA. In addition, its features are enhanced beyond Super VGA by hardware that accelerates graphical user interface operation in environments such as Microsoft Windows® or OS/2 Presentation Manager.

The enhanced features include:

- 64-bit pixel bus
- direct connectivity to PCI bus
- a true acceleration for 8, 16 and 32-bit pixel depths
- fully software programmable Pixel Clock Generator
- supports 2 MB DRAM
- zero wait state write for low latency
- fast linear addressing with full software relocation.

Video Clock Generator

The PC uses an XXX as a video clock generator, providing the dot clock of up to 135 MHz and the memory clock for the video section. If the video mode required is greater than 135 MHz then the frequency doubler in the XXX DAC must be enabled by the BIOS driver.

Video Resolutions Supported

A table detailing all the video resolutions supported can be found under "Video Modes".

PCI LAN/SCSI-2 Controller

The LAN and SCSI-2 PCI devices are integrated in one chip.

- The PCI LAN controller supports the Ethernet LAN protocol. An UTP (Unshielded Twisted Pair) RJ-25 connector and a BNC coax connector are provided. The MAC address is stored in an EEPROM. The LAN remote start code in the system ROM allows the PC to start (boot) from either a Novell NetWare or LANManager server using the integrated Ethernet interface.
- High-performance single-chip Fast SCSI-2 controller with glueless interface to the PCI local bus. The Fast SCSI-2 core provides an 8-bit SCSI interface supporting single-endedSCSI with transfer rates up to 10 MB/sec. 32-bit memory transfers in burst mode across the PCI bus at 132 MB/sec.

IDE to PCI Controller

This IDE to PCI controller implementation supports the full Enhanced IDE feature set. The BIOS uses the auto-detected drive geometry information to select the fastest configuration supported by the installed IDE drive.

- Supports data transfer rate of up to 12 MB/sec
- 32-bit Windows and DOS I/O transfers (many IDE controllers use Window's integral IDE driver which only supports 16-bit I/O transfers)

Flash ROM

The PC uses one 256 KB x 8 Flash ROM and one 128 KB x 8 200 ns Flash ROM. In addition to the base HP BIOS, the Flash contains SETUP, video BIOS, error messages, and ISA and PCI initialization. During programming of the Flash ROM, the power supply switch and the reset button are disabled to prevent accidental interruption.

Security Features

The PC has many security features to protect stored data, to protect the SETUP configuration, and to prevent unauthorized operation of software applications:

- user password
- system administrator password
- screen blanking and keyboard lock
- keyboard lock timer
- communications port protection (ports can be disabled in SETUP)
- disk drive protection (disks can be disabled or "boot" protected in SETUP; flexible disks can also be write-protected)
- system configuration protection
- cover lock and security bracket
- hard-coded serial number and customisable PC identification field

System Specifications

Physical Characteristics

System Processing Unit

Weight:	24 lbs (11 kg)
Dimensions:	16.1 inches (D) by 17.1 inches (W) by 6.6 inches (H) (41 cm by 44 cm 17 cm)
Footprint:	2.1 sq ft (0.18 m sq)

Keyboard

Flat:	18 inches (W) by 7 inches (D) by 1.3 inches (H) (464 mm by 178 mm by 33 mm)
Standing:	18 inches (W) by 7 inches (D) by 2 inches (H) (464 mm by 178 mm by 51 mm)

Electrical Specifications

Input voltage:

The HP Vectra XU PC is equipped with a 120 W (rated), full range power supply.

This power supply requires an input voltage in the following range:

- 90 Vac to 264 Vac at a frequency of 47 Hz to 63 Hz.

Heat Dissipation:

Maximum thermal dissipation: 130 W equivalent to 111.8 kcal per hour (443.6 BTUs per hour).

Power Availability (continuous operation):120 W maximum

- For each ISA accessory board:

  1.4 A at 5 V
  0.13 A at 12 V
  0.1 A at –12 V
  0.03 A at –5 V.

- For PCI accessory boards:

  2 x 5V PCI slots
  3.3V supplied for 7.5W/3.3V PCI accessory boards

Environmental Specifications

System Controller (with hard disk)

Operating Temperature	+41°F to +104°F (+5°C to +40°C)
Recommended Operating Temperature	+59°F to +86°F (+15°C to +30°C)
Storage Temperature	-40°F to +158°F (-40°C to +70°C)
Over Temperature Shutdown	+122°F (+50°C)
Operating Humidity	15% to 80% (relative)
Storage Humidity	8% to 80% (relative)
Operating Altitude	10000 ft (3100 m) max
Storage Altitude	15000 ft (4600 m) max

NOTE Operating temperature and humidity range may vary depending upon the mass storage devices installed. High humidity levels can cause improper operation of disk drives. Low humidity levels can aggravate static electricity problems and cause excessive wear of the disk surface.

Summary of the HP BIOS

Overview

This chapter is a summary of the main features of the HP system BIOS. For a more detailed and general description of the system BIOS refer to the *System BIOS for IBM PCs, Compatibles, and EISA Computers* manual by Phoenix Technologies Ltd. Ordering information for this manual can be found in the preface.

The HP BIOS is very similar to the Phoenix BIOS, with the exception of the CMOS memory layout and the POST routines. Refer to this chapter and to “Power-On Self Tests” for information on these exceptions.

Overview of Address Space

Peripheral devices, accessory devices, and system controllers are accessed via the system I/O space, which is not located in system memory space. The 64 KB of addressable I/O space comprises 8-bit and 16-bit registers (called I/O ports) located in the various system components. When installing an accessory board, ensure that the I/O address space selected is in the free area of the space reserved for accessory boards (100h to 3FFh).

I/O Addresses Used by the System

1F0h–1F7h	Hard Disk Controller 1
278h–27Fh	Parallel Port 2
2E8h–2EFh	Serial Port 4
2F8h–2FFh	Serial Port 2
378h–37Ah	Parallel Port 1
398h–399h	Integrated I/O Controller
3B0h–3DFh	Video Adapter
3E8h–3EFh	Serial Port 3
3F0h–3F7h	Primary Flexible Disk Drive Controller
3F8h–3F7h	Serial Port 1

Refer to "HP BIOS I/O Port Map" for more detailed information.

System Memory Map

00000h–9FFFFh	640 KB — DOS Application Area
A0000h–BFFFFh	128 KB — Video Buffer
C0000h–C7FFFh	32 KB — Video BIOS
C8000h–CFFFFh	32 KB — SCSI BIOS (relocatable)
D0000h–DFFFFh	64 KB — ISA Expansion Memory
E0000h–EFFFFh	64 KB — Extended System BIOS
F0000h–FFFFFh	64 KB — System BIOS
100000h–FFFFFFFFh	1 MB plus — Extended memory

NOTE Reserved memory used by accessory boards must be located in the area from C8000h to 0EFFFh.

After the computer has booted via the LAN, the LAN boot ROM area (E0000 to F0000) is again freed for use by accessory boards.

Product Identification

The following product identification strings are located in the 64 KB BIOS ROM data area.

Location	Size	Contents	Description
0F000:00F0h	byte	10100111b	Extension of capability marker
0F000:00F2h	byte	49h	System number
0F000:00F3h	byte	0Dh	Extended identification byte
0F000:00F4h	byte	*speed* (in MHz)	High Processor Clock Rate
0F000:00F5h	byte	08h	Low Processor Clock Rate
0F000:00F8h	word	FFh	HP Vectra PC ID
0F000:00FAh	byte	FFh	Product identification
0F000:00FBh	byte	10101100b	Machine capability marker
0F000:00FCh	word	*pps*sh	BIOS version number *pp* = primary number *ss* = secondary number
0F000:00FEh	byte	*yy*h	ROM release year (since 1960) stored in BCD
0F000:00FFh	byte	*nn*h	Week of the year stored in BCD
0F000:0102h	word	'HP'	Computer ID

Machine Capability and Extension of Capability Markers

These bytes identify some of the features and capabilities of the computer.

0F000:00FBh = Machine capability marker
Length = one byte

BIOS Version Number

0F000:00FCh = BIOS version number
Length = two bytes

Encoding is as follows:

ppss

Where *pp* = Primary version number and *ss* = Secondary version number

For example, BIOS release A.01.05 would be expressed as:

0105

NOTE If you use DEBUG to look at the bytes, the numbers will be reversed (**05 01**).

Year of the ROM BIOS Release

0F000:00FEh = Year of ROM BIOS release in Binary Coded Decimal (BCD).
Length = one byte

Encoded as follows:

yy

Where *yy* is the difference between the current year and 1960 in BCD.

For example, if the current year is 1990, you would enter 1990 minus 1960 which is 30h (when expressed in BCD).

Week of the ROM BIOS Release

0F000:00FFh = Week of the ROM BIOS release in BCD.
Length = one byte

Encoded as follows:

nn

Where *nn* is the week in which the BIOS ROMs were released in BCD. The range is 00h to 51h.

HP BIOS I/O Port Map

This section describes the HP BIOS I/O port map. "Addressing System Board Components" provides more details on how the BIOS uses the system board components mentioned in the I/O port list.

Within the port map:

- *Reserved* I/O addresses are reserved for HP private use. To avoid compatibility issues, do not use these addresses.
- *Undefined* I/O addresses can be used, but compatibility issues may still occur.
- Hex addresses from 0 to FF are 8-bit ports.
- Hex addresses from 100 to FFFF are either 8, 16, or 32-bit ports.
- 8237-CP = DMA controller (8237-compatible).
- Ch. = Channel(s).
- Int. Cont. = Interrupt Controller (8259-compatible).
- PI Timer = Programmable Interval Timer (8254-compatible).

HP Vectra I/O Port Map

I/O Address Ports	Function	Bits
0000–000F	DMA Controller 1	8
0020–0021	Interrupt Controller 1	8
0040–0043	Interval Timer 1	8
0060,0064	Keyboard Controller	8
0061	NMI Status and Control	8
0070	NMI mask reg., RTC address	8
0071	RTC data	8
0080–008F	DMA Low Page Register	
0092	Alternate reset and A20 function	8
0896–089B	Internal ports	8
088C–089F	Hardware counter	8
00A0–00A1	Interrupt Controller 2	8
00C0–00DF	DMA Controller 2	x
00F0	Co-processor error	
0170–0177	Secondary IDE Controller	
01F0–01F7	IDE Controller	
0278–027F	Parallel Port 3	
02E8–02EF	Serial Port 4	
02F8–02FF	Serial Port 2	
0370–0377	Secondary Floppy Controller	
0378–037F	Parallel Port 2	
03B0– 03DF	S3 PCI Video	

03BC–3BF	Parallel Port 1
03E8–03EF	Serial Port 3
03F0–03F7	Floppy Controller
03F8–03FF	Serial Port 1
0CF8	PCI Configuration Address register
0CFC–0CFF	PCI Configuration Data register

Addressing System Board Components

This section provides more details on how the BIOS uses the system board components mentioned in the I/O port list.

DMA Channel Controllers

The system controller supports seven DMA channels, each with a page register used to extend the addressing range of the channel to 16 MB. The only types of DMA transfer allowed are "I/O-to-memory" and "memory-to-I/O".

"I/O-to-I/O" and "memory-to-memory" transfers are disallowed by the hardware configuration. The following table summarizes how the DMA channels are allocated.

DMA Channel Allocation

First DMA controller (used for 8 bit transfers):

Channel	Function
0	Available
1	ECP mode for parallel port
2	Flexible disk I/O
3	Available

Second DMA controller (used for 16 bit transfers):

Channel	Function
4	Cascade from first DMA controller
5–6	Available
6–7	Available

Interrupt Controllers

The system has two 8259A compatible interrupt controllers. They are arranged as a master interrupt controller and a slave that is cascaded through the master.

The following table shows how the master and slave controllers are connected. The Interrupt Requests (IRQ) are numbered sequentially, starting with the master controller and followed by the slave.

8259A Master to Slave Connections

IRQ (Interrupt Vector)		Interrupt Request Description
IRQ0(08h)		System Timer
IRQ1(09h)		Keyboard Controller
IRQ2(0Ah)	SlaveIRQ	Cascade connection from INTC2 (Interrupt Controller 2)
	IRQ8(70h)	Real Time Clock
	IRQ9(71h)	Available for accessory board (ISA/PCI)
	IRQ10(72h)	Available for accessory board (ISA/PCI)
	IRQ11(73h)	Available for accessory board (ISA/PCI)
	IRQ12(74h)	Mouse
	IRQ13(75h)	PENTIUM
	IRQ14(76h)	IDE
	IRQ15(77h)	Available for accessory board (ISA/PCI)
IRQ3(0Bh)		Serial port 2
IRQ4(0Ch)		Serial port 1
IRQ5(0Dh)		Available for accessory board (ISA/PCI)
IRQ6(0Eh)		Flexible Disk Controller
IRQ7(0Fh)		Parallel Port 1

- IRQ12 can be made available by disabling the computer's mouse interrupt using the ROM-based Setup program.
- IRQ3 can be made available by disabling the computer's serial port 1 using the ROM-based Setup program.
- IRQ4 can be made available by disabling the computer's serial port 1 using the ROM-based Setup program.
- IRQ7 can be made available by disabling the computer's parallel port 1 using the ROM-based Setup program.

PCI Interrupt Request Lines

PCI devices generate interrupt requests using up to four PCI interrupt request lines (INTA#, INTB#, INTC#, and INTD#).

When a PCI device makes an interrupt request, the request is redirected to the system interrupt controller. The interrupt request will be redirected to one of the IRQ lines made available for PCI devices.

All PCI devices with interrupt transfer support will use and share INTA#. A PCI device supporting multiple functionalities may support several INT lines (for example, the LAN/SCSI-2 controller uses INTA# and INTB#). These devices will also require more than one system interrupt request line.

The Integrated Ultra VGA Controller

Overview

The HP Vectra XU 5/90C and XU 5/100C systems use either a Matrox MGA PCI/2+ or a Matrox Impression Plus Video board. These video boards are documented in an English-language manual supplied with the board.

Matrox Electronic Systems Ltd.
1055 St. Regis Blvd.
Dorval, Quebec
Canada H9P 2T4
Telephone: (514) 685-2630
Fax: (514) 685-2853
BBS: (514) 685-6008

The HP Ultra VGA+ video subsystem uses the PCI bus for data transfers between the processor and video subsystem, and has the following features:

- 64-bit video memory access for display refresh schemes
- hardware acceleration of major graphics operations to speed up applications using graphical user interfaces (GUIs)
- 2 MB of 70 ns or faster DRAM support
- graphics resolutions up to 1280×1024
- acceleration of 8- (pseudo-color), 16- (high color), and 32- (true color) bits per pixel operations (more bits per pixel means more colors can be displayed)
- Color Graphics Adapter (CGA), Enhanced Graphics Adapter (EGA), and Hercules monochrome (HGA) emulation modes
- Standard and Enhanced Video Graphics Array (VGA) modes.

For information on developing S3 compatible drivers and video applications, contact:

S3 Incorporated
2770 San Tomas Expressway
Santa Clara, CA 95051-0981
Telephone: (408) 980-5400

Video Memory

2 MB of Video DRAM is preinstalled on the system board.

Video Modes

The video subsystem is responsible for generating the video data which is placed in memory to be accessed by the display. The video subsystem supports the following video modes:

- Monochrome Display Adapter (MDA)
- Color Graphics Adapter (CGA)
- Enhanced Graphics Adapter (EGA)
- MultiColor Graphics Array (MCGA)
- Video Graphics Array (VGA)
- Video Electronics Standard Association (VESA).

The following table details the standard VGA modes which are currently implemented in the video BIOS of the HP Vectra XU PC. These modes are supported by standard BIOS and DOS functions; that is, the video BIOS (which is mapped contiguously between addresses C0000h and C7FFFh) contains all the routines required to configure and access the video subsystem.

Standard VGA Modes

Mode No.	Standard	Interface Type	Resolution	No. of Colors	Vertical Refresh	Horizontal Refresh	Buffer Start Address
00h	CGA	text	40 x 25	16	70 Hz	31.5 kHz	B8000h
01h	CGA	text	40 x 25	16	70 Hz	31.5 kHz	B8000h
02h	CGA	text	80 x 25	16	70 Hz	31.5 kHz	B8000h
03h	CGA	text	80 x 25	16	70 Hz	31.5 kHz	B8000h
04h	CGA	graphics	320 x 200	4	70 Hz	31.5 kHz	B8000h
05h	CGA	graphics	320 x 200	4	70 Hz	31.5 kHz	B8000h
06h	CGA	graphics	640 x 200	2	70 Hz	31.5 kHz	B8000h
07h	MDA	text	720 x 350	2	70 Hz	31.5 kHz	B0000h
0Dh	EGA	graphics	320 x 200	16	70 Hz	31.5 kHz	A0000h
0Eh	EGA	graphics	640 x 200	16	70 Hz	31.5 kHz	A0000h
0Fh	EGA	graphics	640 x 350	2	70 Hz	31.5 kHz	A0000h
10h	EGA	graphics	640 x 350	16	70 Hz	31.5 kHz	A0000h
11h	VGA	graphics	640 x 480	2	60 Hz	31.5 kHz	A0000h
12h	VGA	graphics	640 x 480	16	60 Hz	31.5 kHz	A0000h
13h	VGA	graphics	320 x 200	256	70 Hz	31.5 kHz	A0000h

When the PC is operating in one of the enhanced modes, all accesses to the controller must be made with HP Ultra VGA drivers and utilities such as those supplied with the HP Vectra XU PC. For further details, refer to the README files that come with the utilities.

Enhanced graphics controller functions and video memory are accessed via I/O instructions to the video controller. For programming information refer to the manufacturer's data book.

The VESA video modes supported by the video BIOS are:

VESA Video Modes

Enhanced Mode	VESA Mode No.	Interface Type	Resolution	No. of Colors	Vertical Refresh	Horizontal Refresh	Buffer Start Address
Not Applicable	10Ah	text	132 x 43	16	70 Hz	31.5 kHz	B8000h
	109h	text	132 x 43	16	70 Hz	31.5 kHz	B8000h
201	101h	text	132 x 25	256	60 Hz	31.5 kHz	A0000h
	101h ergo	text	132 x 25	256	72 Hz	37.9 kHz	A0000h
202	102h	graphics	640 x 480	16	60 Hz	37.9 kHz	A0000h
	102h ergo	graphics	640 x 480	16	72 Hz	48.1 kHz	A0000h
203	103h	graphics	800 x 600	256	60 Hz	37.9 kHz	A0000h
	103h ergo	graphics	800 x 600	256	72 Hz	48.1 kHz	A0000h
204	104h	graphics	1024 x 768	16	70 Hz	56.5 kHz	A0000h
	104h ergo	graphics	1024 x 768	16	75 Hz	60 kHz	A0000h
205	105h	graphics	1024 x 768	256	70 Hz	56.5 kHz	A0000h
	105h ergo	graphics	1024 x 768	256	75 Hz	60 kHz	A0000h
208	106h	graphics	1280x1024	16	60 Hz	63 kHz	A0000h
	106h ergo	graphics	1280x1024	16	72 Hz	76 kHz	A0000h
Not Applicable	107h	graphics	1280x1024	256	60 Hz	63 kHz	A0000h
	107h ergo	graphics	1280x1024	256	72 Hz	76 kHz	A0000h
Not Applicable	110h		640 x 480	32,768	60 Hz	31.5 kHz	A0000h
	110h ergo	graphics	640 x 480	32,768	72 Hz	37.9 kHz	A0000h
211	111h	graphics	640 x 480	65,536	60 Hz	31.5 kHz	A0000h
	111h ergo	graphics	640 x 480	65,536	72 Hz	37.9 kHz	A0000h
220	112h	graphics	640 x 480	16.7 M	60 Hz	31.5 kHz	A0000h
	112h ergo	graphics	640 x 480	16.7 M	72 Hz	37.9 kHz	A0000h
214	114h	graphics	800 x 600	65,536	60 Hz	31.5 kHz	A0000h
	114h ergo	graphics	800 x 600	65,536	72 Hz	37.9 kHz	A0000h
221	115h	graphics	800 x 600	16.7 M	60 Hz	31.5 kHz	A0000h
	115h ergo	graphics	800 x 600	16.7 M	72 Hz	37.9 kHz	A0000h
217	117h	graphics	1024 x 768	65,536	60 Hz	48.4 kHz	A0000h

Energy Saving Screen Blanking

If the display has power management capabilities, the video controller can reduce the display's power consumption by blanking the screen. This can be enabled by selecting power management options in the PC's SETUP program. When the PC enters a power-saving mode, the video controller is instructed to cut the horizontal and vertical synchronization signals to the monitor. This action blanks the screen and reduces the display's power consumption.

Supported Enhanced Video Modes

The following table lists the HP displays which may be used, and the supported enhanced video modes for use with each. For non-HP displays, refer to the manufacturers' documentation.

Supported Enhanced Video Modes

	HP VGA Display							
Enhanced Mode	**D1196A Ergo Ultra VGA 15-inch**	**D1199A Ultra VGA 1600 21-inch**	**D2801 A/B Mono VGA 14-inch**	**D2802A SVGA 14-inch**	**D2804A SVGA 1024i 14-inch**	**D2805A Ergo 1024 14-inch**	**D2806A Ergo Ultra VGA 15-inch**	**D2807A Ultra VGA 1280 17-inch**
201	X	X	X	X	X	X	X	X
202	X	X	X	X	X	X	X	X
203	X	X		X	X	X	X	X
204	X	X		X	X		X	X
205	X	X		X	X		X	X
208		X				X	X	X
211	X	X		X	X	X	X	X
214	X	X		X	X	X	X	X
217	X	X		X	X		X	X
21A		X				X	X	X
220	X	X		X	X		X	X
221	X	X		X	X	X	X	X
222	X	X					X	X
223		X					X	X
224		X					X	X

VESA Connector

The Video Electronics Standards Association (VESA) defines a standard video connector variously known as the VESA feature connector, auxiliary connector, or pass-through connector. The HP Vectra XU supports an output-only VESA feature connector. This connector is integrated on the system board (or on the Matrox MGA II PCI Video board) and is connected directly to the pixel data bus and the synchronization signals.

To ensure synchronization of colors between the integrated video controller and a second PCI video controller on an accessory board, a snooping utility is employed to communicate color-synchronization information to the PCI accessory board via the VESA feature connector.

Power-On Self Tests

Overview

This chapter describes the power-on self tests (POST) contained in the ROM BIOS.

Power-On Self Test (POST)

Each time the system is powered on or a reset is performed, the POST is executed. The POST process verifies the basic functionality of the system components and initializes certain system parameters. The POST performs the tests in the order described in this chapter.

If the POST is initiated by a soft reset **[CTRL]**+**[ALT]**+**[DEL]**, the RAM tests are not executed and shadow RAM is not cleared. A POST initiated by a hard reset (by pushing the reset button on the PC control panel) will not count memory.In all other aspects, the POST executes in the same way following power-on, a hard reset, or a soft reset.

NOTE The POST does not detect the replacement of a hard disk or changes in the size of the hard disk.

Shadow RAM

On HP personal computers, access to certain ROM data is enhanced by using shadow RAM. During the POST, the BIOS and other ROM data is copied into high-speed shadow RAM. The shadow RAM is addressed at the same physical location as the original ROM in a manner which is completely transparent to applications. This technique provides faster access to the system BIOS firmware.

POST Test	Description
System BIOS Tests	
LED test	Flash the LEDs on the control panel.
Processor Test	Tests the processor's registers. Test failure causes the boot process to abort.
System (BIOS) ROM Test	Calculates an 8-bit checksum. Test failure causes the boot process to abort.
RAM Refresh Timer Test	Tests the RAM refresh timer circuitry. Test failure causes the boot process to abort.
Interrupt RAM Test	• Tests for RAM parity errors. • Checks the first 64 KB of system RAM used to store data corresponding to various system interrupt vector addresses. Test failures cause the boot process to abort.
Shadow the System	
ROM BIOS	Tests the system ROM BIOS and shadows it. Failure to shadow the ROM BIOS will cause an error code to display. The boot process will continue, but the system will execute from ROM. This test is not performed after a soft reset (using **[CTRL]**+**[ALT]**+**[DEL]**).
Load CMOS Memory	Checks the serial EEPROM and returns an error code if it has been corrupted. Copies the contents of the EEPROM into CMOS RAM.
CMOS RAM Test	Checks the CMOS RAM for start-up power loss, verifies the CMOS RAM checksum(s). Test failure causes error codes to display.
Internal CacheMemory Test	Tests the processor's internal level-one cache RAM. Test failure causes an error code to display and the boot process to abort.
Video Tests	
Initialize the Video	Initializes the video subsystem, tests the video shadow RAM, and, if required, shadows the video BIOS. A failure causes an error code to display, but the boot process continues.
System Board Tests	
Test External Cache	Tests the level-two cache. A failure causes an error code to display and disables the external cache.
Shadow SCSI ROM	Tests for the presence of SCSI ROMs. If SCSI ROMs are detected, their contents are copied into the shadow RAM area. A failure will cause an error code to display.

8042 Self-Test	Downloads the 8042 and invokes the 8042 internal self-test.A failure causes an error code to display.
Timer 0/Timer 2 Test	Tests Timer 0 and Timer 2.Test failure causes an error code to display.
DMA Subsystem Test	Checks the DMA controller registers. Test failure causes an error code to display.
Interrupt ControllerTest	Tests the interrupt masks, the master controller interrupt path (by forcing an IRQ0), and the industry-standard slave controller (by forcing an IRQ8).Test failure causes an error code to display.
Real-Time Clock Test	Checks the real-time clock registers and performs a test that ensures the clock is running.Test failure causes an error code to display.
Memory Tests	
RAM Address LineIndependence Test	Verifies the address independence of real-mode RAM (no address lines stuck together). Test failure causes an error code to display.
Size Extended Memory	Sizes and clears the protected mode (extended) memory and writes the value into CMOS bytes 30h and 31h.If the system fails to switch to protected mode an error code is displayed.
Real-Mode Memory Test(First 640 KB)	Read/write test on real-mode RAM. (This test is !!not!! done during a reset using **[CTRL]**+**[ALT]**+**[DEL]**.)The test checks each block of system RAM to determine how much is present. Test failure of a 64 KB block of memory causes an error code to display, and the test is aborted.
Shadow RAM Test	Tests shadow RAM in 64 KB segments (except for segments beginning at A000h, B000h, and F000h). If they are !!not!! being used, segments C000h, D000h, and E000h are tested. Test failure causes an error code to display.
Protected Mode RAMTest (Extended RAM)	Tests protected RAM in 64 KB segments (above 1MB). (This test is *not* done during a reset using **[CTRL]**+**[ALT]**+ **[DEL]**.) Test failure causes an error code to display.
Keyboard/Mouse Tests	
Keyboard Test	Invokes a built-in keyboard self-test of the keyboard's microprocessor and tests for the presence of a keyboard and for stuck keyboard keys.Test failure causes an error code to display.
Mouse Test	If a mouse is present, invokes a built-in mouse self-test of the mouse's microprocessor and for stuck mouse buttons. Test failure causes an error code to display.
Flexible Disk Drive A Tests	
Flexible Disk ControllerSubsystem Test	Tests for proper operation of the flexible disk controller. Test failure causes an error code to display.
Coprocessor Tests	
Internal NumericCoprocessor Test	Checks for proper operation of the numeric coprocessor part of the processor.Test failure causes an error code to display.

Parallel Port Tests	
Parallel Port Test	Tests the integrated parallel port, if it is enabled, as well as any other parallel ports. Test failure causes an error code to display.
Serial Port Tests	
Serial Port Test	Tests the integrated serial port registers, as well as any other serial ports. Test failure causes an error code to display.
Hard Disk Drive C Tests	
Hard Disk Controller Subsystem Test	Tests for proper operation of the hard disk controller. Test failure causes an error code to display. The test does not detect hard disk replacement or changes in the size of the hard disk.
Ethernet (Integrated) Tests	
Ethernet HardwareTest	Tests for proper operation of theintegrated Ethernet hardware. This is aninternal test only and does not test theconnection to the network.Test failurecauses an error code to display.
System Configuration Tests	
System Generation	Initiation of the system generation (SYSGEN) process, which compares the configuration information stored in the CMOS memory with the actual system. If a discrepancy is found, an error code will be displayed.

Error Codes

POST error codes are returned, and displayed if possible, when an error is detected during the execution of the power-on self-test procedures.

A complete description of the error can be displayed by running theROM-based Error Management Utility (EMU).

For a list of error codes, refer to the HP Vectra PC Service Handbook.

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