Motherboard HOT-523

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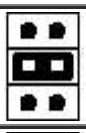
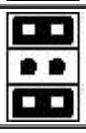
HOT-523 configuration tables

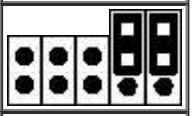
Subchapter: System or processor clock | Cache memory configuration | AT bus clock setting | PCI clock source | Vesa Local Bus Configuration |

System or processor clock

system clock frequency	Jumpers JP 13
60MHz	
66MHz	

View: CPU socket below these jumpers

Cache memory configuration

cache memory capacity	JP21	JP26 ... JP22
64KB		
128KB		
256KB		
512KB		

View: to the left of the CPU socket JP21, to the right of the CPU socket the other jumpers

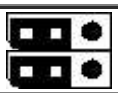
cache memory capacity	Data SRAM bank 0 U37 to U44	Data SRAM bank 1 U55 to U62	Tag SDRAM U45, U63	Dirty Bit U17 (Optional)
64KB	8k x 8	empty	8k x 8 on U63	16k x 1
128KB	8k x 8	8k x 8	8k x 8 on U63	16k x 1
256KB	32k x 8	empty	8k x 8 on U63	16k x 1
512KB	32k x 8	32k x 8	8k x 8 on U63, U45	16k x 1

AT bus clock setting

AT bus clock	JP7 JP8	System clock = 60MHz PCI clock = 30MHz	System clock = 66MHz PCI clock = 33MHz
PCI clock / 5		6.0MHz	6.6MHz
PCI clock / 4		7.5MHz	8.3MHz
PCI clock / 3		10.0MHz	11.0MHz
PCI clock / 2		15.0MHz	16.5MHz

Source of the PCI clock

This determines whether the PCI clock (LCLK) is generated by a quartz oscillator fitted in the U54 socket, or whether it is derived internally from the system clock.

PCI clock (LCLK)	JP19 JP20	U54	JP11
External (default)		Quartz is equipped	
Internal		Quartz is not loaded	

Vesa local bus configuration

VL bus configuration	JP15	JP16
PCI clock >=33MHz	x	
PCI clock <30MHz	x	
High Speed Write 0 queues		x
High Speed Write 1 queues		x

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Source of the PCI clock
Vesa local bus configuration