JP2	on-board local bus IDE write wait state
1-2	wait state determined by the setting of JP1
2-3	forced to 1 wait state **(default)**

System board connectors

	Description
P1	Hardware reset switch
P2	Speaker connector
P3	Turbo LED connector
P4	Turbo switch
P5	Hard disk LED connector
P6	Power LED and keylock connector
P7	IDE hard disk connector
P8	Floppy drive connector
P9	Parallel port connector
P10,P11	Power connectors
P12	Primary Serial port connector
P13	Secondary Serial port connector
P14	Game port connector
P15	External Battery connector
KB1	Keyboard connector

P1 Hardware reset switch

Pin	Assigment
1	Signal pin
2	GND

P2 Speaker connector

Pin	Assignment
1	Data out
2	+5V
3	Ground
4	+5V

P3 Turbo LED connector

Pin	Assignment
1	+5V
2	LED signal

VL slot configuration

JP1	
1-2	1 WS VL-write cycle
2-3	0 WS VL-write cycle

JP31	VL-bus ID3
1-2	VL slot clock greater than 33.333MHz
2-3	VL slot clock less than or equal to 33.333MHz **(default)**

CPU Type

	JP18	JP19	JP20
486DX, 486DX2	2-3	1-2	1-2 (default)
486SX	1-2	2-3	2-3

P10, P11 Power connectors

Pin	Assignment
1	Power Good
2	+5V
3	+12V
4	-12V
5	Ground
6	Ground

Pin	Assignment
1	Ground
2	Ground
3	-5V
4	+5V
5	+5V
6	+5V

on-board floppy controller

JP21	
1-2	enabled **(default)**
2-3	disabled

on-board game port

JP22	
1-2	enabled **(default)**
2-3	disabled

on-board printer port

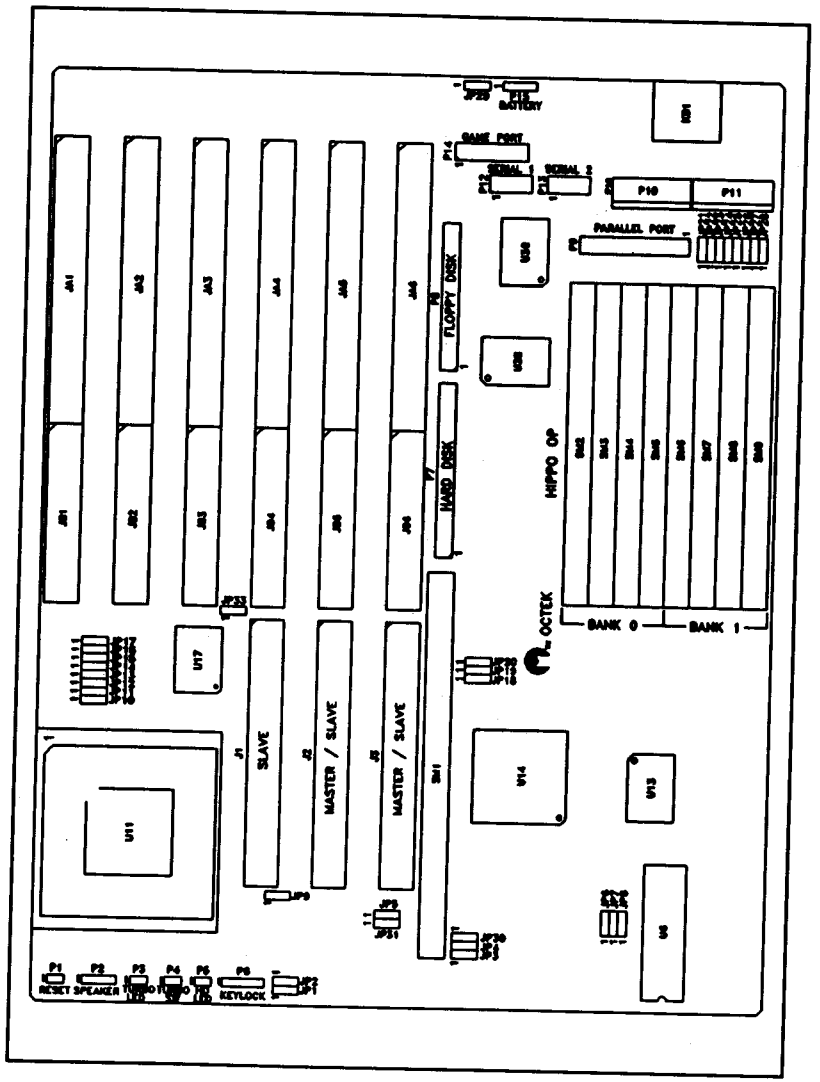
JP23	
1-2	enabled **(default)**
2-3	disabled

Printer port selection

JP24	
1-2	LPT1 (378H) **(default)**
2-3	LPT2 (278H)

I/O Map

0-1Fh	DMA Controller 1
20-3Fh	Interrupt Controller 1
40-5Fh	Timer
60-6Fh	Keyboard Controller
70-7Fh	Real Time Clock
80-9Fh	DMA Page Register
A0-BFh	Interrupt Controller
C0-DFh	DMA Controller 2
F0	Clear Math Coprocessor Busy flag
F1	Reset Math Coprocessor
F8-FFh	Math Coprocessor Port



Level	Function
NMI	Parity or I/O Channel Check

Interrupt Controllers

Controller 1	Controller 2	
IRQ0		Timer Output 0
IRQ1		Keyboard
IRQ2		
	IRQ8	Real-time Clock Interrupt
	IRQ9	Software Redirected to INT 0AH (IRQ2)
	IRQ10	Reserved
	IRQ11	Reserved
	IRQ12	Reserved
	IRQ13	Coprocessor
	IRQ14	Fixed Disk
	IRQ15	Reserved
IRQ3		Serial Port 2
IRQ4		Serial Port 1
IRQ5		Parallel Port 2
IRQ6		Diskette Controller
IRQ7		Parallel Port 1

Power Saving Features

Whenever the system is not in used (e.g. No key has been hit in the keyboard for a certain period of time), the clock chip of the main board will be signaled to slow down the CPU clock. The system subsequently enters a "sleep" mode. When an external request for system usage is detected (as the pressing of a key or the movement of a mouse), the clock is stepped up to full operating frequency. The time limit for entry to "sleep" mode is selectable in CMOS setup.

IDE drive spin-down is also controllable. The fixed disk will stop spinning after a pre-selected time interval of inactivity.

The Video Electronics Standards Association (VESA) has developed a preliminary standard Display Power Management Signaling (DPMS) specification, which utilizes the synchronization signals as an indication that the monitor should power down.

State	Horizontal sync	Vertical sync,	Video
ON	pulses	pulses	active
standby	no pulses	pulses	blanked
Suspend	pulses	no pulses	blanked
OFF	no pulses	no pulses	blanked

New VGA adapters with video BIOS supporting VESA DPMS can be installed in the HIPPO OP to reduce power consumption in the monitors.

Reset CMOS setup information

Sometimes it may be desirable to clear the existing content of the CMOS RAM. This may be accomplished by allowing the shunt connector to join pin 2 and pin 3 of the header at JP29 for a while. When the system is re-booted, CMOS RAM content is regarded as invalid and the user is prompted to setup the CMOS again.

CMOS RAM address map

Addresses	Description
00-0Dh	Real-time clock information
0Eh	Diagnostic status byte
0Fh	Shutdown status byte
10h	Diskette drive type byte - drives A and B
11h	Reserved
12h	Fixed disk type byte - drives C and D
13h	Reserved
14h	Equipment byte
15h	Low base memory byte
16h	High base memory byte
17h	Low expansion memory byte
18h	High expansion memory byte
19-2Dh	Reserved
2E-2Fh	2-byte CMOS checksum
30h	Low expansion memory byte
31h	High expansion memory byte
32h	Date century byte
33h	Information flags
34-3Fh	Reserved

Maximum number of VL-Bus devices and slots

The following guidelines are recommended by VESA:

Speed	Max. no. of VL adapter cards installed
40 MHz	2
50 MHz	1

One VL master adapter card may be installed in slot J2 OR slot J3

The on-board VL IDE

The VL Local Bus IDE controller supports high speed data transfer (ANSI ATA standard mode0, mode 1, mode 2). The cycle time of the IDE cycle is jumper selectable. The chip incorporates 4-level write FIFO and 4-level prefetch FIFO with write-posting. This allows IDE cycles and CPU cycles to run concurrently. This parallelism (or cycle overlapping) is a key component in speeding up transfer rate. Additional fine-tuning of the IDE cycle timing via registers allow further performance optimization.

Fast GATEA20 and RESET Emulation

Commands to ports 60h and 64h are intercepted so that the the functions of the GATEA20 and RESET of the keyboard controller are emulated. This decode sequence is software transparent and requires no BIOS modifications. The result is that the protected mode switching operation is much faster.

VL-slot (side A)

I/O Pin	Signal Name
A29	A18
A30	A16
A31	A14
A32	A12
A33	A10
A34	A8
A35	GND
A36	A6
A37	A4
A38	WBACK#
A39	BEO#
A40	VCC
A41	BE1#
A42	BE2#
A43	GND
A44	BE3#
A45	ADS#
A48	LRDY#
A49	LDEV#
A50	LREQ#
A51	GND
A52	LGNT#
A53	VCC
A54	ID2
A55	ID3
A56	ID4
A57	LKEN#
A58	LEADS#

The DRAM system

The memory controller supports fast page mode DRAM accesses. This feature is instrumental in sustaining a high memory bandwidth between the DRAM array and the 486 operating in burst mode.

Both normal and hidden refresh are supported. Normal refresh refers to the classical refresh scheme in which the CPU is held while refresh cycles take place in the local DRAM and the ISA bus memory. Hidden refresh scheme allows the CPU to continue executing instructions during DRAM refresh period as long as the CPU does NOT access DRAM or the ISA bus. Refresh overhead is therefore minimized.

Shadow RAM is available as an option. System BIOS and video BIOS residing in slow EPROM can be copied to local DRAM to speed up accesses to BIOS code. Shadow RAM addresses range from C0000h to FFFFFh. 16K granularity is provided for address range C0000h to EFFFFh, while the area F0000h - FFFFFh can only be shadowed as a whole. Video BIOS at C0000h - C7FFFh can be cached in the external cache after shadowing.

VL-slot (side B)

I/O Pin	Signal Name
B29	GND
B30	A17
B31	A15
B32	VCC
B33	A13
B34	A11
B35	A9
B36	A7
B37	A5
B38	GND
B39	A3
B40	A2
B41	N.C.
B42	RESET#
B43	D/C#
B44	M/IO#
B45	W/R#
B48	RDYRTN#
B49	GND
B50	IRQ9
B51	BRDY#
B52	BLAST#
B53	ID0
B54	ID1
B55	GND
B56	VLCLK
B57	VCC
B58	LBS16#

Cache :

8 KB internal cache in CPU
SIMM socket for installation of a 256KB secondary cache module

On-board I/O facility:

floppy controller,
2 serial ports,
1 parallel port,
1 game port,

Power Saving Feature:

CPU clock step down hardware
BIOS support of VESA DPMS

Others:

Fast GateA20 and reset emulation

ISA slot (side B)

I/O Pin	Signal Name
B1	GND
B2	RESET DRV
B3	+5 V
B4	IRQ9
B5	-5 V
B6	DRQ2
B7	-12 V
B8	OWS
B9	+12 V
B10	GND
B11	SMEMW
B12	SMEMR
B13	I0W
B14	I0R
B15	DECK3
B16	DRQ3
B17	DECK1
B18	DRQ1
B19	REFRESH
B20	CLK
B21	IRQ7
B22	IRQ6
B23	IRQ5
B24	IRQ4
B25	IRQ3
B26	DECK2
B27	T/C
B28	BALE
B29	+5 V
B30	OSC
B31	GND

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ISA slot (side D)

I/O Pin	Signal Name
D1	MEMCS16
D2	I0CS16
D3	IRQ10
D4	IRQ11
D5	IRQ12
D6	IRQ15
D7	IRQ14
D8	DECK0
D9	DRQ0
D10	DECK5
D11	DRQ5
D12	DECK6
D13	DRQ6
D14	DECK7
D15	DRQ7
D16	+5 V
D17	MASTER
D18	GND

Table of Content

RADIO FREQUENCY INTERFERENCE STATEMENT

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference with radio and television reception.

If this equipment does cause interference to radio or TV reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

* Reorient the receiving antenna.
* Relocate the computer away from the receiver.
* Move the computer away from the receiver.
* Plug the computer into a different outlet so that computer and receiver are on different branch circuits.
* Ensure that card slot covers are in place when no card is installed.
* Ensure that card mounting screws, attachment connector screws, and ground wires are tightly secured.
* If peripherals are used with this system, it is suggested to use shielded, grounded cables, with in-line filters if necessary.

If necessary, the user should consult the dealer service representative for additional suggestions.

The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications to this equipment. It is the responsibility of the user to correct such interference.

The material in this manual is for information only and is subject to change without notice.

REVISION: 1.0

Table of Content

Chapter 1
Introduction

The usage of PC systems in the office environment has seen dramatic increase over this few years. With increase in the power consumption due to growth of the PC installation base, the United States Environmental Protection Agency (EPA) issued a guideline stating that systems must have the capability to be put into a low power state (less than 30 W) during period of inactivity to conserve energy. Therefore the major benefit of incorporating power management to desktop PCs is to reduce electrical operating cost over the lifetime of the system.

OCTEK HIPPO OP brings the new technology of power saving to desktop computing. Compliance with the EPA requirement, high throughput VESA Local Bus, advanced chipset with power user-programmable features and integrated on-board I/O are some of the real benefits of HIPPO OP.

The key components of the advanced power-saving capabilities are HIPPO OP's built-in support of DPMS functions (Display Power Management Standard) of VESA (Video Electronics Standard Association), support for Windows APM and CPU clock step-down hardware. The energy saving feature of HIPPO OP is compatible with MS-DOS 3.3 (or later versions) and Windows 3.1.

ISA slot (side C)

I/O Pin	Signal Name
C1	SBHE
C2	LA23
C3	LA22
C4	LA21
C5	LA20
C6	LA19
C7	LA18
C8	LA17
C9	MEMR
C10	MEMW
C11	SD8
C12	SD9
C13	SD10
C14	SD11
C15	SD12
C16	SD13
C17	SD14
C18	AS15

Chapter 2
General Features

Specifications:

Processor:

80486DX, 80486DX2, 80486SX or 80487SX

Processor Clock:

25/33/40/50 MHz clock selectable

Speed:

Turbo/normal speed

Expansion Bus:

Six 16-bit ISA slots
Three VESA Local Bus slots (supporting one VL master)

On-board VESA local bus device:

VL-IDE controller

DRAM upgrade capacity:

1 MB (min. config.)
32 MB (max. config.)

DRAM configuration:

256K X 9, 1M X 9, 4M X 9 SIMM sockets

ISA slot (side A)

I/O Pin	Signal Name
A1	IOCHCK
A2	SD7
A3	SD6
A4	SD5
A5	SD4
A6	SD3
A7	SD2
A8	SD1
A9	SD0
A10	IOCHRDY
A11	AEN
A12	SA19
A13	SA18
A14	SA17
A15	SA16
A16	SA15
A17	SA14
A18	SA13
A19	SA12
A20	SA11
A21	SA10
A22	SA9
A23	SA8
A24	SA7
A25	SA6
A26	SA5
A27	SA4
A28	SA3
A29	SA2
A30	SA1
A31	SA0

The 80486 CPU

In simple terms, an 80486 is a combination of a microprocessor (80386), a floating point math coprocessor (80387), a cache controller and 8KB of cache RAM, all in one chip.

The 80486 CPU is binary-compatible with the 8086, 8088 , 80186, 80286, 80386DX and 80386SX CPUs. Software developed for older members of the 80x86 family (such as the 8086 and the 80286) can be run without modification on the 80486. Frequently used instructions can be executed in one clock cycle owing to architectural enhancement:

1. an 8 KB on-chip cache
2. pipelined instruction execution
3. most 486s (DX, DX2) contain on-chip floating point units

The burst bus interface of the 80486 enables it to attain a transfer rate of 106 MB/sec at 33 MHz CPU clock. Burst cycles are done at the continuous rate of one 32-bit transfer per clock. Another advanced feature is the implementation of the write-buffers. If the bus is currently busy, memory writes are directed to one of the four write-buffers. This write buffering allows the 80486 to continue the next instruction.

In summary, the 80486 CPU provides a high performance level and retains compatibility with a large base of existing software.

VL-slot (side B)

I/O Pin	Signal Name
B1	D0
B2	D2
B3	D4
B4	D6
B5	D8
B6	GND
B7	D10
B8	D12
B9	VCC
B10	D14
B11	D16
B12	D18
B13	D20
B14	GND
B15	D22
B16	D24
B17	D26
B18	D28
B19	D30
B20	VCC
B21	A31
B22	GND
B23	A29
B24	A27
B25	A25
B26	A23
B27	A21
B28	A19

DRAM CONFIGURATION

Bank 0	Bank 1	Total
256K x 32	---	1M
256K x 32	256K x 32	2M
256K x 32	1M x 32	5M
256K x 32	4M x 32	17M
1M x 32	---	4M
1M x 32	1M x 32	8M
1M x 32	4M x 32	20M
4M x 32	---	16M
4M x 32	4M x 32	32M

80ns DRAM can be used in all operating frequencies.

The external cache system

An external cache module is available to further boost the system performance. The external cache is direct-mapped and employs a write-back scheme. The cache size is 256 KB and organized in interleaved banks.

VESA Local Bus

Connecting devices to a CPU local bus can dramatically increase the speed of the I/O bound peripherals. The Video Electronics Standards Association (VESA) VL Bus is a widely accepted local bus standard.

VL-slot pinout

The "A" side of the connector is the add-in board component side. The "B" side of the connector is the add-in board solder side.

I/O Pin	Signal Name
A1	D1
A2	D3
A3	GND
A4	D5
A5	D7
A6	D9
A7	D11
A8	D13
A9	D15
A10	GND
A11	D17
A12	VCC
A13	D19
A14	D21
A15	D23
A16	D25
A17	GND
A18	D27
A19	D29
A20	D31
A21	A30
A22	A28
A23	D26
A24	GND
A25	A24
A26	A22
A27	VCC
A28	A20

The on-board I/O controller

The on-board I/O controller offers

1. support for two floppy drives (360K 5 1/4", 1.2M 5 1/4", 720K 3 1/2", 144M 3 1/2")
2. one parallel port
3. two serial ports
4. game port

Control of system speed

System speed can be controlled by the keyboard and the turbo switch. When the keys "Ctrl", "Alt", "-" are pressed simultaneously, the system switches to low speed. When the keys "Ctrl", "Alt", "+" are pressed at the same time, the system returns to high speed mode (turbo mode).

The header P4 should be connected to the turbo switch of the cabinet. Whenever the system speed is set low by the turbo switch, the key strobes "Ctrl", "Alt", "+" and "Ctrl", "Alt", "-" will have NO impact on the system speed.

DMA channel

Channel	Function
0	Spare (8 bit)
1	SDLC (8 bit)
2	Floppy Disk (8 bit)
3	Spare (8 bit)
4	Cascade for DMA Controller 1
5	Spare (16 bit)
6	Spare (16 bit)
7	Spare (16 bit)

Installing DRAM modules

Follow the steps below to install DRAM SIMMs :

(a) Turn off the PC.
(b) The SIMMs (in groups of four) are inserted in Bank 0 first. The memory modules should be carefully installed into the SIMM sockets in such a way that the modules are properly oriented and aligned.
(c) Allow the two metal latches at each end of the socket to lock onto the memory module.
(d) Further memory capacity upgrade should be directed to Bank 1.

Installing the cache module

Follow the steps below to install the cache module.

(a) Turn off the PC
(b) The cache module is inserted the 72-pin cache socket.
(c) Allow the two metal latches at each end of the socket to lock onto the cache module.
(d) Install the jumper JP5.
(e) Power up the PC.
(f) Enable the external cache in the CMOS setup.
(g) Allow the system to boot.

I/O Map

170-177h	Fixed Disk (secondary)
1F0-1F7h	Fixed Disk (primary)
200-207h	Game port
278-27Fh	Parallel port 2
2E8-2EFh	Serial port 4
2F8-2FFh	Serial port 2
300-31Fh	Prototype card
360-36Fh	Reserved
370-377h	Floppy Disk Controller (secondary)
378-37Fh	Parallel port 1
380-38Fh	SDLC, bisync 2
3A0-3AFh	Bisync 1
3B0-3BFh	Monochrome Display and Printer Adapter
3C0-3CFh	Reserved
3D0-3DFh	Color Graphics Adapter
3E8-3EFh	Serial port 3
3F0-3F7h	Floppy Disk Controller (primary)
3F8-3FFh	Serial port 1

Jumper Setting

Cache configuration

JP5	
1-2	Single cache bank
2-3	Two cache banks **(default)**

Clock selection

JP3	JP4	JP30	Clock Frequency	CPU
2-3	1-2	1-2	50MHz	DX50
2-3	2-3	2-3	33MHz	DX33,DX2-66
1-2	2-3	2-3	40MHz	DX40
1-2	1-2	2-3	25MHz	DX25,DX2-50

CMOS content of the Real Time Clock

JP29	
1-2	CMOS content preserved **(default)**
2-3	CMOS content cleared

Color/mono selection

JP6	
1-2	mono
2-3	color **(default)**

Chapter 4
Technical Information

This section provides technical information about HIPPO OP and is particularly useful to advanced users.

Memory map

Address	Range	Function
0 - 9FFFFh	0 - 640K	Base Memory
A0000 - BFFFFh	640 - 768K	Video Display Buffer
C0000 - DFFFFh	768 - 896K	Adapter ROM
E0000 - EFFFFh	896 - 960K	System ROM (optional)
F0000 - FFFFFh	960 - 1024K	System ROM
100000 - 1FFFFFFh	1024 - 3276K	Extended Memory

Serial port 1

JP25	
1-2	enabled **(default)**
2-3	disabled

JP26	
1-2	COM1 (3F8 - 3FFh) **(default)**
2-3	COM3 (3E8 - 3EFh)

Serial port 2

JP28	
1-2	enabled **(default)**
2-3	disabled

JP27	
1-2	COM2 (2F8 - 2FFh)
2-3	COM4 (2E8 - 2EFh)

ROM

JP7	
1-2	Flash ROM installed
2-3	EPROM installed **(default)**

P4 Turbo switch

Pin	Assignment
1	Signal pin
2	Ground

P6 Power LED & keylock connector

Pin	Assignment
1	+5V
2	Key
3	Ground
4	Keyboard inhibit
5	Ground

Reserved jumpers

JP8 2-3 (DEFUALT)
JP11 1-2 (DEFAULT)
JP10 2-3 (DEFAULT)
JP33 1-2 (DEFAULT)

on-board IDE

JP12	JP17	
1-2	1-2	enabled (default)
2-3	2-3	disabled

JP13	
1-2	primary IDE (1FXh, 3FXh)
2-3	secondary IDE (17Xh, 37Xh)

JP14	JP15	16-bit cycle time
1-2	1-2	> 200ns (mode 3)
2-3	1-2	> 240ns (mode 2)
1-2	2-3	> 383ns (mode 1)
2-3	2-3	> 480ns (mode 0) default setting

JP16	8-bit cycle time
1-2	> 600ns
2-3	> 840ns (default)