HIPPO PRO
486

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REVISION: 1.2

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RADIO FREQUENCY INTERFERENCE STATEMENT

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference with radio and television reception.

If this equipment does cause interference to radio or TV reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

* Reorient the receiving antenna.
* Relocate the computer away from the receiver.
* Move the computer away from the receiver.
* Plug the computer into a different outlet so that computer and receiver are on different branch circuits.
* Ensure that card slot covers are in place when no card is installed.
* Ensure that card mounting screws, attachment connector screws, and ground wires are tightly secured.
* If peripherals are used with this system, it is suggested to use shielded, grounded cables, with in-line filters if necessary.

If necessary, the user should consult the dealer service representative for additional suggestions.

The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications to this equipment. It is the responsibility of the user to correct such interference.

Note

1. Electronic components are sensitive to dust and dirt. Do inspect and clean the computer system regularly.

2. Turn off the power whenever you install or remove any connector, memory module and add-on card. Before turning on the power, make sure that all the connectors, memory modules and add-on cards are secured.

3. After power is on, wait for a minute. The system BIOS are going through a self-test during this period and nothing is shown on the screen. After the self-test, the system BIOS will initialize the display adaptor and show messages.

4. The SIMM sockets are fragile device. Do not force the SIMM modules into the sockets. It may break the locking latches.

Preface

The manual provides information about the installation and maintenance of OCTEK HIPPO PRO motherboard. In-depth explanations of the functions of this motherboard are provided. In the appendix, the system BIOS setup is explained.

The content in this manual is only for reference and is intended to provide the basic information for the general users. There are also technical information for hardware and software engineers.

In this manual, there are 4 chapters. Chapter 1 contains a brief introduction and specification of OCTEK HIPPO PRO motherboard. In the Chapter 2, the functions of OCTEK HIPPO PRO are explained. It also outlines many advanced features of the CPU and the system architecture. Chapter 3 explains the installation of coprocessor, DRAM modules and jumpers. Technical information is provided in the Chapter 4.

System BIOS is described in the attached BIOS Manual. Additional information is given in the Appendix B and C for maintenance purpose.

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Chapter 1
Introduction

OCTEK HIPPO VL PRO is designed to be a powerful platform for sophisticated software available now and in the future. It contains the most powerful microprocessor 80486 which combines CPU, numeric coprocessor and internal cache memory on a single chip. OCTEK HIPPO VL PRO fully takes advantage of the power of 80486 and provides high performance, reliability and compatibility to the user.

Fast A20 gate and fast reset generation are incorporated to improve the performance of advanced operation system and expanded memory managers.

Compatibility and reliability are important issues. I/O channel is compatible to standard AT bus and any peripheral may be used. On board POWERGOOD generator is essential to ensure the reliability of the system and is well-designed to work with all power supplies.

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Chapter 2
General Features

SPECIFICATION

Processor :

486 SX/DX 25/33MHz
486 DX/2 50/66MHz
Overdrive Processor Optional

I/O Slot :

Compatible to standard AT bus
Six 16-bit slots
Three VESA VL-BUS slots
(2 Master & 1 Slave)

Cache :

Dynamic Cache Architecture DCA
8KB four way set associative internal cache

Memory :

4 level deep write buffer with byte gathering
Shadow RAM for system and video BIOS
Page mode and hidden refresh
Flexible configuration
SIMM sockets for 256KB, 1MB or 4MB modules
128M Byte on board RAM Maxcimum

System Support Functions :

- 8-Channel DMA (Direct Memory Access)
- 16-level interrupt
- 3 programmable timers
- CMOS RAM for system configuration
- Real time clock with battery back-up
- Fast A20 gate and fast reset

Intergrated Features :

- Enchaned VL-IDE (VESA) Controller inteface
  (block mode tranfer & support mode 1 to mode 3)
- Floppy disk controller support 360K, 1.2M, 720K, 1.44M and 2.88M drive
- Two serial ports
- One parallel port
- One game port

Other Features :

- On board POWERGOOD generation
- External battery connector

PROCESSOR

The power of OCEAN HIPPO PRO comes from 80486. It is the state-of-art microprocessor which merges many innovative features on a single chip for advanced applications and operation systems. With such high density, this CPU incorporates as many as new features to make itself the most powerful microprocessor.

80486 is a 32-bit microprocessor with 32-bit external data bus and 32-bit external address bus. It not only contain a central processing unit, but also integrates a numeric processor and a four-way set associate cache memory. It is fully binary compatible with 80386 and 80387. All existing software can be due to the new internal architecture, the performance of 80486 is two to four times of 80386.

Cache memory can improve the overall performance of a computer system. If the cache memory is separated from CPU, CPU still needs to fetch code and data through external bus. That means the data transfer rate should not be too fast so that the external devices can keep pace with the CPU. In 80486, the cache controller and cache memory are integrated into the chip. Most of the operations can be carried out inside the CPU, which reduces the bus operations on external data and address bus and thus speeds up the internal execution.

The cache memory is a 8K bytes, 16 bytes line size, four-way set associative configuration. The hit rate of this configuration is much better than 32K bytes two-way set associative external cache because a four-way set associative architecture provides better performance in a multitasking and multi-processor environment.

Bus snooping feature keeps the cache memory consistent with the main memory. When an external processor overwrites the content in the main memory, the corresponding data in the internal cache memory will be invalidated and will be fetched from main memory when CPU reads this data.

If a read miss occurs, the CPU will initiate a burst mode read operation. In burst mode read operation, CPU performs four successive read operations each of which takes only one cycle. Total 128 bits data are fetched into the CPU's internal cache. Since burst mode read operation is very fast, the traffic of the CPU bus is greatly reduced and the bus is available to other bus masters, such as DMA controller.

Reading 128 bits data into CPU will take some times. In order to reduce the delay, the internal cache controller works parallel with CPU. It fetches the data for the present operation and is cycle is terminated. Then the other data are read into the internal cache memory while CPU is doing something else. This arrangement permits the CPU to run at zero wait state.

By eliminating the access to external bus, operations with the internal cache can be completed in a single cycle. 80386 at least needs two cycles for an operation. To further increase the rate of data transfer inside the CPU, the internal bus of the cache memory is increased to 128 bits, which is four times of the external bus. Since, in most of the time, the CPU is using the internal cache, the large bus size substantially improves the overall performance.

When the CPU writes data to the main memory, the data is first stored in a write buffer. There are four write buffers. When the external bus is idle, data will be sent to the main memory. If all buffers are filled, it can start write operation in burst mode. Since the internal cache is updated immediately, the CPU need not suspend its operation and there is no need to wait for the external device to update the main memory.

Many often-used instructions are executed in a clock cycle and some instructions are modified to take fewer cycles than in 80386. On the contrary, 80386 may take two to three more cycles for the same instruction. The CPU contains an advanced instruction pipeline structure and a 32-byte code queue to speed up the execution.

80486 includes all the functions of 80386 and is able to support sophisticated software and operation systems which are widely employed now. It is able to operate in real mode, protected mode and virtual 8086 mode.

Internal memory management unit provides a flexible addressing scheme for the next generation operation system. Multitasking, concurrent operation and manipulating huge data base can be accomplished with excellent performance. Paging mechanism is employed to allow powerful operating system to implement virtual memory. Each segment is divided into several pages which are 4K bytes per page. Page mechanism is transparent to software and allows software to address 64 terabytes. Furthermore, the 64KB segment boundary which is an barrier of 8088 and 80286 is removed and the segment length can be increased up to 4GB.

The demand for sophisticated, number-crunching scientific and business applications has rapidly increased in recent years. In the past, microprocessor features an integer Arithmetic Logic Unit which only handles simple integer operations such as addition and multiplication. Floating-point operations which are actually utilized by applications must be accomplished through software routines.

To meet the demand of floating-point calculation, a numeric coprocessor is necessary. However, an external coprocessor has been found to be the bottleneck of data transfer. 80486 integrates the coprocessor on chip and thus the data transfer to external bus is eliminated. The on-chip coprocessor is compatible with 80387. It works parallel with other units in the CPU, which results in a better performance of numeric process.

DYNAMIC CACHE ARCHITECTURE (DCA)

DCA (dynamic Cache Architecture) is a new Cache Memory DCA literally boosts the cache memory efficiency by as much as 300 percent over conventional external cache! It is integrated as part of the high speed logic of the motherboard.

A 486 system, until now, moves information in the same manner because the software written to take full advantage of the 486's 32 bit wide BUS has usually been restricted to CAD/CAM, Expert Systems, Virtual Simulations and other High End applications. DCA, and it's Byte Gathering Write Buffers collect 8 and 16 bit "packets" of information until a single 32 bit "packet" is formed. Using Burst Mode, it then "Writes" this single informational "string" back to RAM in one operation, rather than in several time consuming ones. This is a tremendous improvement on the efficiency of data transfer, as the information is handled solely through the CPU, the High Speed Chipset and the lightning fast Internal Cache of the 80486.

VL-IDE (VESA)

The VL-IDE interfaces between standard IDE drivers and the VL-Bus. Since the bus data transfer rate is much higher than what IDE drives can support, the drives will dictate the total throughput of the disk subsystem. The user has three speeds to select from normal speed, medium speed and high speed. Modern IDE drives should support normal speed or high speed. Since the electronic design of a drive could change with the model number, it is strongly recommended to set the speed initially to normal. Move to a higher speed grade only when your drive permits.

VL-IDE comes with an on-board BIOS ROM. Normally, hard disk operations are controlled by the system BIOS on the motherboard. The VL-IDE BIOS has certain performance enhancement features. It offers a better performance by placing the part of the sysytem BIOS that is responsible for the hard disk operations. Using the VL-IDE BIOS or the system BIOS for disk accessing is defermored by the user-selectable disk operation mode. The VL-ide BIOS will prompt you the a desired disk operation mode at boot up time. Four disk operation modes are selectable: Fastest mode 3 to normal mode 0.

If the system can't boot up from Hard disk another possible cause is the improper setting of the access time for IDE hard disk. The access time must match the timing of the Hard disk. Turn off the system and select the larger access time for low performance hard disk.

MEMORY SYSTEM

Two banks of DRAMs can be installed on board. So 8 SIMM modules may be installed on your system and the maximum memory size is up to 32MB, 256KB, 1MB and 4MB DRAM SIMM modules are supported. The DRAM should be fast-page mode DRAM with staggered refresh capability.

The memory system provides a flexible memory configuration. Several combinations of DRAM types are allowed. The DRAM type and the memory size are automatically detected by the system BIOS. So, you may easily change the configuration of the system.

The memory controller system supports fast page mode. The memory is divided into pages with equal size. Successive memory accesses within the same page need not require wait state. Furthermore, a burst line fill mode is implemented. In case of a read miss of cache memory, 16 bytes data will be fetched from main memory to cache memory. Using page mode operation will speed up the line fill operation.To enhance the system performance, shadow RAM mode is supported. In shadow RAM mode, system BIOS and video BIOS contained in low speed memory such as EPROM and ROM are copied into DRAM. Improvement is significant because access to DRAM is mush faster than ROM.

The memory refresh logic is redesigned to improve the system performance and power consumption. In the original PC/AT design, the memory refresh operation will suspend the CPU operation because it has to access the main memory. In a high speed system like OCTEK HIPPO PRO, the CPU indeed can process a large amount of operations in the memory refresh period.

By implementing hidden refresh method, the refresh operations for expansion card on the AT bus and for the main memory are separated. To be compatible, the refresh operation for AT bus will not be changed. But the refresh operation for main memory will be carried out individually and will be done when there is no access to main memory. Furthermore, the frequency of the main memory refresh operation may be set to 'normal' or 'slow'. All types of DRAM can be used in `normal' mode. When 'slow' mode is selected, the availability of main memory is increased but the refresh period of DRAM should be longer. Since the refresh period of DRAM from different manufacturers may vary, consult your dealer for detail.

Write Buffering with Byte Gathering

A sophisticated write-buffering scheme is implemented in OCTEK HIPPO PRO. Write-buffering is commonly found in cache-based system. Single CPU write operation is buffered and thus no write state is needed.

However, if there is a lot of write operation, the overall performance is down graded, because only a write operation is buffered and subsequent write operation have to be delayed.

The write policy of the OCTEK HIPPO PRO cache controller is 4-level write-buffering which provided the O wait state write during multiple write cycle. An importance feature of the Write-buffer is byte gathering. If data being written by the cache to the write-buffers happens to be a 'write buffer write hit' which means the location of the data is already in the write buffers, the data will be directly written to the buffer where the match occurred.

With multi-level write-buffer, the read operation needs to be specially handled. If the data is still in the write buffer, it will be directly retrieved from write buffer and the main memory is updated later. If the data is in the main memory, not in the cache, it will be fetched from the main memory, no matter how many data is still in the write buffer. The latency of the write buffer unload is eliminated.

8042 EMULATION

Now, there are many PC designs with a special feature for OS/2 optimization. It is intended to speed up the protected mode switching operation which is done by the slow speed keyboard controller in the original PC design. However, this feature often causes compatibility problem because they use different hardware logic design to bypass the keyboard controller. Thus, the BIOS is needed to be modified to take advantage of it. An application without modification may cause problem.

In OCTEK HIPPO PRO, there are some logic designs in the chipset to emulate the keyboard controller. An application can work in the usual way to send commands to keyboard controller, but these commands are in fact interpreted by the chipset. The protected mode switching operation is much faster. There will be no potential problem since modification of software is not needed.

ENERGY SAVING

The usage of PC systems in the office environment has seen dramatic increase over this few year. With increase the power consumption due to growth of PC system. The United States Environment Protection Agency (EPA) issued a guideline stating that systems must have the capability to be put into a low power state (less than 30W) during period of inactivity to conserve energy. Therefore, the major benefit of incorporating power management to desktop PCs is to reduce electrical operating cost over the lifetime of the system.

OCTEK HIPPO PRO brings to life the new technology of a low power consumption PC. HIPPO PRO GREEN STAR is designed to comply with the EPA requirements as well as VESA local bus standard through the use of a VL-bus and with 486DX, DX2 and Overdrive processors.

Clearly, power consumption is devoted by hard disk, memory, power supply and system board. To achieves the energy efficient function. The hard disk drive must include spin-down command. The VGA must have DPMS function from VESA's Display Power Management Standard. Energy saving feature of HIPPO PRO is fully compatible with MS-DOS 3.3 or later version and Windows 3.1.

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Chapter 3
Configuring The System

Important Note : Turn off the power before installing or replacing any component.

INSTALLING PROCESSOR

Processor 486DX/P24T overdrive is a PGA devices. There is a 238-pin PGA socket. To install processor, be sure to line up pin 1 of the CPU with pin 1 of the socket as shown below.

Before installing the processor, make sure that all the pins are straight. The pins are very fragile. Once these pins are bent, the processor may be damaged.

The Processor P24T or 486DX is automatically detected by the system. It need not to set any jumper.

Important Note : Turn off the power before installing or replacing any component.

INSTALLING RAM MODULES

OCTEK HIPPO PRO has eight sockets on board for SIMM modules. Whenever you add memory to the motherboard, install four modules at the same time. Also make sure that the chips on the modules face towards the slot for memory expansion board. The modules should be locked by the sockets. Please check carefully before turning on the power. Otherwise, the system will not work properly.

To install a module, the module edge is angled into the socket's contact and then the module is pivoted into position, where the locking latches will secure it. If the module edge is not completely inserted into the socket, it cannot be pivoted to be in vertical position and should be dragged out and re-inserted again. Do not force the module into the SIMM socket. It will damage the locking latches.

The modules should be locked by the locking latches of the sockets firmly. Please check carefully before turning on the power. Otherwise, the system will not work properly.

If the BIOS reports an memory error or parity error, drag out the modules and insert them again. If the locking latches are damaged, contact your dealer to replace the socket.

CONFIGURATION OF MEMORY

The configuration of the memory is very flexible. There are several combinations of DRAM types you may consider. 256KB, 1MB, 4MB or 16MB SIMM are acceptable. So, a basic system can be equipped with fewer memory and later more memory can be installed when upgrading the system. There are two banks of DRAM on the motherboard and another two banks on a memory expansion board. The memory size is detected automatically by system BIOS and indicated during memory test after reset. No jumper is needed to be set for the memory size and DRAM type.

To determine what DRAM speed rating should be used depends on the system speed and wait state. The highest performance is accomplished by using zero wait state, but high speed DRAM has to be used. If zero wait state is selected, fast page mode DRAM is needed. The wait state setting is applied to all banks of memory. Therefore make sure to install DRAM with the same speed rating, or accommodate the wait state setting to the slow DRAM type.

Because of the shadow RAM function, the 384KB memory between 640KB to 1MB can not accessed. So, the memory size found by the system BIOS is not equal to the actual memory size. For example, when there is 4MB on board, the BIOS will show 3712KB.

DRAM CONFIGURATION

Bank 0 Simm (1-4)	Bank 1 Simm (5-8)	Total Memory
256K	---	1M
256K	256K	2M
1M	---	4M
256K	1M	5M
1M	1M	8M
4M	---	16M
1M	4M	20M
4M	4M	32M
4M	16M	80M
16M	16M	128M

CONTROL OF SYSTEM SPEED

System speed can be controlled by keyboard and turbo switch. To change the speed by keyboard, use **`-'** and **`+'** of the numeric keypad. Press **`Ctrl' `Alt'** and **`-'** for slow speed and press **`Ctrl' `Alt'** and **`+'** for fast speed.

Connect P1 to the turbo switch of the case and P3 to the turbo LED of the case. When the turbo mode is selected, the turbo LED of the case will be turned on.

Whenever the system speed is set to be slow by turbo switch, it cannot be changed by the keyboard, and vice versa.

RESET CMOS SETUP INFORMATION

Sometimes, the improper setting of system setup may make the system malfunction. In this case, turn off the power and set JP34 to 2-3 for a while. The internal CMOS status register is reset. Then set the jumper to 1-2 of JP34 and turn on the power. The BIOS finds the CMOS status register is reset and regards the setup information is invalid. So it will prompt you to correct the information.

SYSTEM BOARD JUMPER SETTING

There are several options which allows user to select by hardware switches.

Display Selection

JP15	
1-2	CGA, EGA, VGA
2-3	Monochrome display *

CPU Type

	486DX\DX2	486SX	487SX
JP17	1 - 2*	2 - 3	1 - 2
JP18	2 - 3*	NO	1 - 2
JP19	2 - 3*	1 - 2	2 - 3

System Speed

	33MHz	25MHz
JP2	2 - 3*	1 - 2

IDE Selection

	Enable	Disable
JP5	2 - 3*	1 - 2
JP36	1 - 2*	2 - 3

IDE access time

Mode	JP10	JP12	Cycle time (ns)	Access time (ns)
3	1 - 2	1 - 2	150	90
2	2 - 3	1 - 2	240	190
*1	1 - 2	2 - 3	390	120
0	2 - 3	2 - 3	600	180

Game port

	Enable	Disable
JP21	1 - 2*	2 - 3

Print port

	278H	378H	380H	Disable
JP27	1 - 2*	2 - 3	1 - 2	2 - 3
JP28	1 - 2*	1 - 2	2 - 3	2 - 3

Floppy disk drive (2.88M)

	install	none
JP23,JP24,JP25	1 - 2*	2 - 3

Serial port 1

	COM 1	Disable

JP29	1 - 2*	2 - 3
JP30	1 - 2*	2 - 3

Serial port 2

	COM 2	Disable
JP31	1 - 2*	2 - 3
JP32	1 - 2*	2 - 3

Floppy disk controller

	Enable	Disable
JP19	1 - 2*	2 - 3

SYSTEM BOARD CONNECTORS

Under typical conditions, these connectors should be connected to the indicators and switches of the system unit. The functions of connectors on the motherboard are listed below.

	Description
P2	Turbo switch
P4	Speaker connector
P1	Hardware reset connector
P5	Power LED & Ext-lock connector
P3	Turbo LED
P13,P14	Power supply connector
P16	External battery connector
P6	Cooling fan connector
KB1	Keyboard connector
P10	Printer port connector
P8	Hard disk LED connector
P7	Hard disk connector
P9	Floppy diskette connector
P11,P12	Serial port interface
P15	Game port interface

Pin assignment of the connector are illustrated as follows:

P2 - Turbo Switch Connector

Pin	Assignment
1	Selection Pin
2	Ground

P4 - Speaker Connector

Pin	Assignment
1	Data out
2	+5 Vdc
3	Ground
4	+5 Vdc

P1 - Hardware Reset Connector

Pin	Assignment
1	Selection Pin
2	Ground

P5 - Power LED & Ext-Lock Connector

Pin	Assignment
1	+5 Vdc
2	Key
3	Ground
4	Keyboard inhibit
5	Ground

P3 - Turbo LED Connector

Pin	Assignment
1	+5Vdc
2	LED signal

P13,P14 - Power Supply Connector

Pin	Assignment
1	POWERGOOD
2	+5 Vdc
3	+12 Vdc
4	-12 Vdc
5	Ground
6	Ground

Pin	Assignment
1	Ground
2	Ground
3	-5 Vdc
4	+5 Vdc
5	+5 Vdc
6	+5 Vdc

P16 - External Battery Connector

Pin	Assignment
1	+ Vdc
2	not used
3	Ground
4	Ground

P6 - Cooling Fan Connector

Pin	Assignment
1	+ 5Vdc
2	Ground

KB1 - Keyboard Connector

Pin	Assignment
1	Keyboard clock
2	Keyboard data
3	Spare
4	Ground
5	+5 Vdc

P10 PRINTER PORT CONNECTOR

Pin	Function	I/O	Pin	Function	I/O
1	-STROBE	O	14	-AUTO FEED	O
2	DATA 0	O	15	-ERROR	I
3	DATA 1	O	16	-INIT	O
4	DATA 2	O	17	SLCT IN	O
5	DATA 3	O	18	GROUND	-
6	DATA 4	O	19	GROUND	-
7	DATA 5	O	20	GROUND	-
8	DATA 6	O	21	GROUND	-
9	DATA 7	O	22	GROUND	-
10	-PACK	I	23	GROUND	-
11	BUSY	I	24	GROUND	-
12	PAPER END	I	25	GROUND	-
13	SLCT	I			

P8 HARD DISK LED CONNECTOR

Pin No.	Function
1	+5 Vdc
2	SIGNAL OUT
3	SIGNAL OUT
4	+5 Vdc

P7 HARD DISK CONNECTOR

Pin	Function	I/O	Pin	Function	I/O
1	-Host Reset	I	2	Ground	-
3	Host Date 7	I/O	4	Host Data 8	I/O
5	Host Date 6	I/O	6	Host Data 9	I/O
7	Host Data 5	I/O	8	Host Data 10	I/O
9	Host Data 4	I/O	10	Host Data 11	I/O
11	Host Data 3	I/O	12	Host Data 12	I/O
13	Host Data 2	I/O	14	Host Data 13	I/O
15	Host Data 1	I/O	16	Host Data 14	I/O
17	Host Data 0	I/O	18	Host Data 15	I/O
19	Ground	-	20	KEY	-
21	Unused	-	22	Ground	-
23	-Host IOW	I	24	Ground	-
25	-Host IOR	I	26	Ground	-
27	Host IORDY	O	28	Host ALE	I
29	Unused	-	30	Ground	-
31	Host IRQ14	O	32	-Host IOCS16	O
33	Host ADR1	I	34	Unused	-
35	Host ADR0	I	36	Host ADR2	I
37	-Host CS0	I	38	-Host CS1	I
39	-ACTIVE	O	40	Ground	-

P9 FLOPPY DISKETTE CONNECTOR

Pin	Function	I/O	Pin	Function	I/O
1	Ground	-	2	-Reduced Write	O
3	Unused	-	4	Unused	-
5	KEY	-	6	Unused	-
7	Ground	-	8	-Index	I
9	Ground	-	10	-Motor Enable 1	O
11	Ground	-	12	-Drive Select 0	O
13	Ground	-	14	-Drive Select 1	O
15	Ground	-	16	-Motor Enable 0	O
17	Ground	-	18	-Direction	O
19	Ground	-	20	-Step	O
21	Ground	-	22	-Write Date	O
23	Ground	-	24	-Write Enable	O
25	Ground	-	26	-Track 00	I
27	Ground	-	28	-Write Protect	I
29	Ground	-	30	-Read Data	I
31	Ground	-	32	-Head Select 1	O
33	Ground	-	34	-Disk Change	I

* Noise generated from the transformer of switching power supply, will affect the operation of floppy drive unit. Please separate the case of power supply and floppy drive. Otherwise, connect the signal ground and chassis ground (frame ground) together.

P11,P12 SERIAL PORT INTERFACE

Pin	Function	I/O	Pin	Function	I/O
1	Carrier Detect	I	2	Receive Data	I
3	Transmit Data	O	4	Data Terminal Ready	O
5	Ground	-	6	Data Send Ready	I
7	Request To Send	O	8	Clear To Send	I
9	Ring Indicator	I	10	Unused	-

P15 GAME PORT INTERFACE

Pin	Function	I/O	Pin	Function	I/O
1	+5V	O	9	+5V	O
2	Button 0	I	10	---	-
3	Position 0	I	11	---	-
4	GND	-	12	GND	-
5	GND	-	13	---	-
6	Position 1	I	14	---	-
7	Button 1	I	15	+5V	O
8	+5V	O	---		

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Chapter 4
Technical Information

This section provides technical information about OCTEK HIPPO PRO and is intended for advanced users interested in the basic design and operation of OCTEK HIPPO PRO.

MEMORY MAPPING

Address	Range	Function
000000-7FFFFF	000K-512K	System Board Memory (512K)
080000-09FFFF	512K-640K	System Board Memory (128K)
0A0000-0BFFFF	640K-768K	Display Buffer (128K)
0C0000-0DFFFF	768K-896K	Adaptor ROM / Shadow RAM (128K)
0E0000-0EFFFF	896K-960K	System ROM / Shadow RAM (64K)
0F0000-0FFFFF	960K-1024K	System BIOS ROM / Shadow RAM (64K)
100000-7FFFFF	1024K-8192K	System Memory
800000-FFFFFF	8192K-16318K	System Memory

I/O ADDRESS MAP

I/O Address Map on System Board

I/O address hex 000 to 0FF are reserved for the system board I/O.

ADDRESS (HEX)	DEVICE
000-01F	DMA Controller 1, 8237
020-03F	Interrupt Controller 1, 8259, Master
040-05F	Timer, 8254
060-06F	Keyboard Controller
070-07F	Real Time Clock, NMI (non-maskable interrupt) mask
080-09F	DMA Page Register, 74LS612
0A0-0BF	Interrupt Controller 2, 8259
0C0-0DF	DMA Controller 2, 8237
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor Port

I/O address hex 100 to 3FF are available on the I/O channel.

ADDRESS (HEX)	DEVICE
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2
2F8-2FF	Serial Port 2
300-31F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	SDLC, bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome Display and Printer Adapter
3C0-3CF	Reserved
3D0-3DF	Color Graphics Monitor Adapter
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1

SYSTEM TIMERS

OCTEK HIPPO PRO has three programmable timer/counters controlled by Headland chipset and they are defined as channels 0 through 2:

Channel 0	System Timer
Gate 0	Tied on
Clk in 0	1.190 Mhz OSC
Clk out 0	8259 IRQ 0

Channel 1	Refresh Request Generator
Gate 1	Tied on
Clk in 1	1.190 Mhz OSC
Clk out 1	Request Refresh Cycle

Channel 2	Tone Generation of Speaker
Gate 2	Controlled by bit 0 of port hex 61 PPI bit
Clk in 2	1.190 Mhz OSC
Clk out 2	Used to drive the speaker

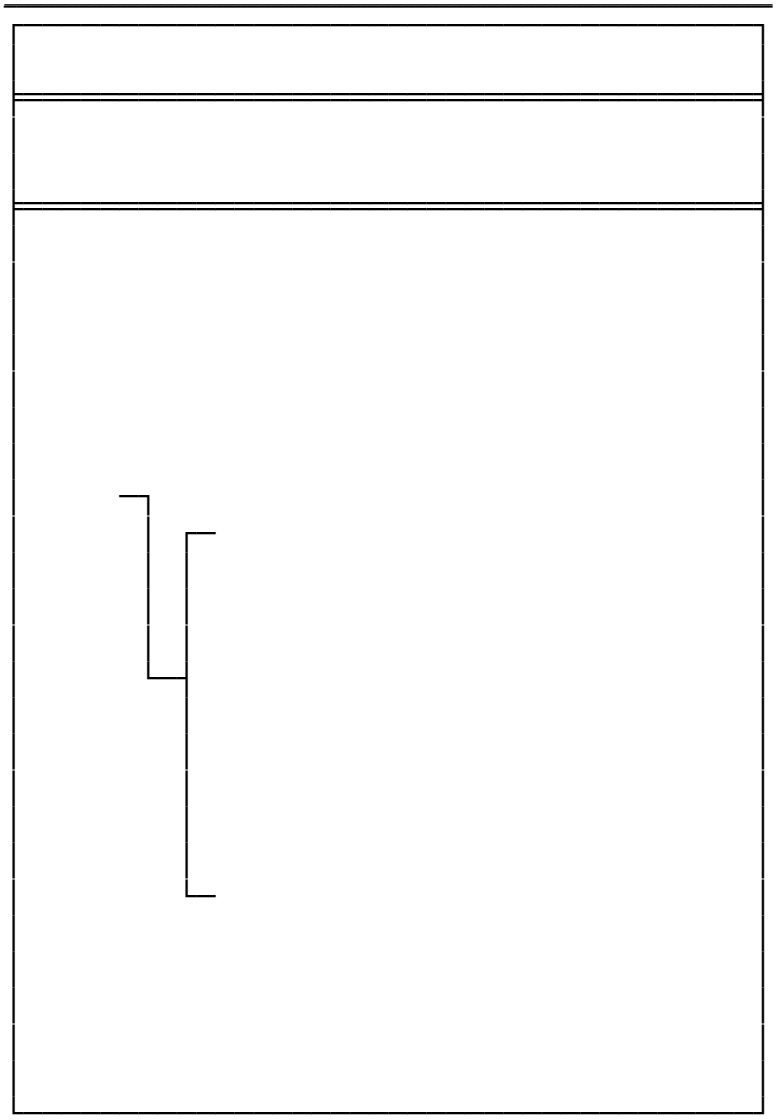
Note : Channel 1 is programmed to generate a 15-micro-second period signal.

The 8254 Timer/Counters are treated by system programs as an arrangement of four programmable external I/O ports. Three are treated as counters and the fourth is a control register for mode programming.

SYSTEM INTERRUPTS

Sixteen levels of system interrupts are provided on OCTEK HIPPO PRO. The following shows the interrupt-level assignments in decreasing priority.

Level		Function
Microprocessor NMI		Parity or I/O Channel Check
Interrupt Controllers		
CTLR 1	CTLR 2	
IRQ0		Timer Output 0
IRQ1		Keyboard (Output Buffer Full)
IRQ2		Interrupt from CTLR 2
	IRQ8	Real-time Clock Interrupt
	IRQ9	Software Redirected to INT 0AH (IRQ2)
	IRQ10	Reserved
	IRQ11	Reserved
	IRQ12	Reserved
	IRQ13	Coprocessor
	IRQ14	Fixed Disk Controller
	IRQ15	Reserved
IRQ3		Serial Port 2
IRQ4		Serial Port 1
IRQ5		Parallel Port 2
IRQ6		Diskette Controller
IRQ7		Parallel Port 1



DIRECT MEMORY ACCESS (DMA)

OCTEK HIPPO PRO supports seven DMA channels.

Channel	Function
0	Spare (8 bit transfer)
1	SDLC (8 bit transfer)
2	Floppy Disk (8 bit transfer)
3	Spare (8 bit transfer)
4	Cascade for DMA Controller 1
5	Spare (16 bit transfer)
6	Spare (16 bit transfer)
7	Spare (16 bit transfer)

The following shows the addresses for the page register.

Page Register	I/O Address (HEX)
DMA Channel 0	0087
DMA Channel 1	0083
DMA Channel 2	0081
DMA Channel 3	0082
DMA Channel 5	008B
DMA Channel 6	0089
DMA Channel 7	008A
Refresh	008F

REAL TIME CLOCK AND CMOS RAM

Real time clock and CMOS RAM are contained on board. Real time clock provides the system date and time. CMOS RAM stores system information. Both are backed up by battery and will not lose information after power off. The following page shows the CMOS RAM Address Map.

CMOS RAM ADDRESS MAP

Addresses	Description
00-0D	* Real-time clock information
0E	* Diagnostic status byte
0F	* Shutdown status byte
10	Diskette drive type byte - drives A and B
11	Reserved
12	Fixed disk type byte - drives C and D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	* Low expansion memory byte
31	* High expansion memory byte
32	* Date century byte
33	* Information flags (set during power on)
34-3F	Reserved

REAL TIME CLOCK INFORMATION

The following table describes real-time clock bytes and specifies their addresses.

Byte	Function	Address
0	Seconds	00
1	Second alarm	01
2	Minutes	02
3	Minute alarm	03
4	Hours	04
5	Hour alarm	05
6	Day of week	06
7	Date of month	07
8	Month	08
9	Year	09
10	Status Register A	0A
11	Status Register B	0B
12	Status Register C	0C
13	Status Register D	0D

SYSTEM EXPANSION BUS

OCTEK HIPPO PRO provides six 16-bit slots and three VL-bus slots.

The I/O channel supports:

* *I/O address space from hex 100 to hex 3FF*
* *Selection of data access (either 8 or 16 bit)*
* *24 bit memory addresses (16MB)*
* *Interrupts*
* *DMA channels*
* *Memory refresh signal*

The following figure shows the pin numbering for I/O channel connectors (A-side and B-side).

The following figure shows the pin numbering for I/O channel connectors (C-side and D-side).

The following tables summarize pin assignments for the I/O channel connectors.

I/O Channel (A-Side)

I/O Pin	Signal Name	I/O
A1	-I/O CH CK	I
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	-I/O CH RDY	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O

A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

I/O Channel (B-Side)

I/O Pin	Signal Name	I/O
B1	GND	Ground
B2	RESET DRV	I
B3	+5 Vdc	Power
B4	IRQ9	I
B5	-5 Vdc	Power
B6	DRQ2	I
B7	-12 Vdc	Power
B8	0WS	I
B9	+12 Vdc	Power
B10	GND	Ground
B11	-SMEMW	O
B12	-SMEMR	O
B13	-IOW	I/O
B14	-IOR	I/O
B15	-DACK3	I
B16	DRQ3	O
B17	-DACK1	I
B18	DRQ1	O
B19	-Refresh	I/O
B20	CLK	O
B21	IRQ7	I
B22	IRQ6	I
B23	IRQ5	I
B24	IRQ4	I
B25	IRQ3	I
B26	-DACK2	O
B27	T/C	O

B28	BALE	O
B29	+5 Vdc	Power
B30	OSC	O
B31	GND	Ground

I/O Channel (C-Side)

I/O Pin	Signal Name	I/O
C1	SBHE	I/O
C2	LA23	I/O
C3	LA22	I/O
C4	LA21	I/O
C5	LA20	I/O
C6	LA19	I/O
C7	LA18	I/O
C8	LA17	I/O
C9	-MEMR	I/O
C10	-MEMW	I/O
C11	SD8	I/O
C12	SD9	I/O
C13	SD10	I/O
C14	SD11	I/O
C15	SD12	I/O
C16	SD13	I/O
C17	SD14	I/O
C18	SD15	I/O

I/O Channel (D-Side)

I/O Pin	Signal Name	I/O
D1	-MEM CS16	I
D2	-I/O CS16	I
D3	IRQ10	I
D4	IRQ11	I
D5	IRQ12	I
D6	IRQ15	I
D7	IRQ14	I
D8	-DACK0	O
D9	DRQ0	I
D10	-DACK5	O
D11	DRQ5	I
D12	-DACK6	O
D13	DRQ6	I
D14	-DACK7	O
D15	DRQ7	I
D16	+5 Vdc	Power
D17	-MASTER	I
D18	GND	Ground

The following table summery pin assignments for VESA VL-bus connector.

VL-bus (side A)

I/O Pin	Signal Name
A1	CD1
A2	CD3
A3	GROUND
A4	CD5
A5	CD7
A6	CD9
A7	CD11
A8	CD13
A9	CD15
A10	GROUND
A11	CD17
A12	POWER
A13	CD19
A14	CD21
A15	CD23
A16	CD25
A17	GROUND
A18	CD27
A19	CD29
A20	CD31
A21	CA30
A22	CA28
A23	CD26
A24	GROUND

A25	CA24
A26	CA22
A27	POWER
A28	CA20

VL-bus (side A)

I/O Pin	Signal Name
A29	CA18
A30	CA16
A31	CA14
A32	CA12
A33	CA10
A34	CA8
A35	GROUND
A36	CA6
A37	CA4
A38	WBACK-
A39	BEO-
A40	POWER
A41	BE1-
A42	BE2-
A43	GROUND
A44	BE3-
A45	ADS-
A46	LRDY-
A47	LDEV-
A48	LREQ-
A49	GROUND
A50	LGNT-
A51	POWER
A52	ID2
A53	ID3
A54	ID4
A55	LKEN-

A56	LEADS-

VL-bus (side B)

I/O Pin	Signal Name
B1	CD0
B2	CD2
B3	CD4
B4	CD6
B5	CD8
B6	GROUND
B7	CD10
B8	CD12
B9	POWER
B10	CD14
B11	CD16
B12	CD18
B13	CD20
B14	GROUND
B15	CD22
B16	CD24
B17	CD26
B18	CD28
B19	CD30
B20	POWER
B21	CA31
B22	GROUND
B23	CA29
B24	CA27
B25	CA25
B26	CA23
B27	CA21

B28	CA19

VL-bus (side B)

I/O Pin	Signal Name
B29	GROUND
B30	CA17
B31	CA15
B32	POWER
B33	CA13
B34	CA11
B35	CA9
B36	CA7
B37	CA5
B38	GROUND
B39	CA3
B40	CA2
B41	n/c
B42	RESET-
B43	D/C-
B44	M/IO-
B45	W/R-
B46	RDY-
B47	GROUND
B48	IRQ9
B49	BRDY-
B50	BLAST-
B51	ID0
B52	ID1
B53	GROUND
B54	VLCLK
B55	POWER

B56	LBS16-

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Appendix A
Operation and Maintenance

STATIC ELECTRICITY

When installing or removing any add-on card, DRAM module or coprocessor, you should discharge the static electricity on your body. Static electricity is dangerous to electronic device and can build-up on your body. When you touch the add-on card or motherboard, it is likely to damage the device. To discharge the static electricity, touch the metal of your computer. When handling the add-on card, don't contact the components on the cards or their "golden finger". Hold the cards by their edges.

KEEPING THE SYSTEM COOL

The motherboard contains many high-speed components and they will generate heat during operation. Other add-on cards and hard disk drive can also produce a lot of heat. The temperature inside the computer system may be very high. In order to keep the system running stably, the temperature must be kept at a low level. A easy way to do this is to keep the cool air circulating inside the case. The power supply contains a fan to blow air out of the case. If you find that the temperature is still very high, it would be better to install another fan inside the case. Using a larger case is recommended if there are a number of add-

on cards and disk drives in the system.

CLEANING THE "GOLDEN FINGER"

Whenever inserting an add-on card to the motherboard, make sure that there is no dirt on the "golden finger" of the add-on card. If not, the contact between the "golden finger" and the slot may be poor and thus the add-on card may not work properly. Use a pencil eraser to clean the "golden finger" if dirt is found.

CLEANING THE MOTHERBOARD

The computer system should be kept clean. Dust and dirt is harmful to electronic devices. To prevent dust from accumulating on the mother-board, installing all mounting plates on the rear of the case. Regularly examine your system, and if necessary, vacuum the interior of the system with a miniature vacuum.

Appendix B
Troubleshooting

MAIN MEMORY ERROR

After power up, the monitor remains blank, and there are beep sounds indicating a main memory failure. In this case, turn off the power and remove all SIMM modules. Carefully place the modules back to the sockets and make sure that all the modules are locked by the locking latches firmly.

In some other cases, the total memory found by the BIOS is different from the actual amount of memory on board. (Note that 128K bytes memory is reserved for the shadow RAM function and will not be counted by the BIOS). It is also a memory failure and you can follow the instruction above.

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Appendix C
SUMMERY OF
JUMPER SETTING

Display Selection

JP15	
1-2	CGA, EGA, VGA
2-3	Monochrome display *

CPU Type

	486DX\DX2	486SX	487SX
JP17	1 - 2*	2 - 3	1 - 2
JP18	2 - 3*	NO	1 - 2
JP19	2 - 3*	1 - 2	2 - 3

System Speed

	33MHz	25MHz
JP2	2 - 3*	1 - 2

IDE Selection

	Enable	Disable
JP5	2 - 3*	1 - 2

JP36	1 - 2*	2 - 3

IDE access time

Mode	JP10	JP12	Cycle time (ns)	Access time (ns)
3	1 - 2	1 - 2	150	90
2	2 - 3	1 - 2	240	190
*1	1 - 2	2 - 3	390	120
0	2 - 3	2 - 3	600	180

Game Port

	Enable	Disable
JP21	1 - 2*	2 - 3

Printer port

	278H	378H	380H	Disable
JP27	1 - 2*	2 - 3	1 - 2	2 - 3
JP28	1 - 2*	1 - 2	2 - 3	2 - 3

	IRQ 5	IRQ 7
JP22	1 - 2*	2 - 3

Floppy disk drive (2.88M)

	install	none
JP23,JP24,JP25	1 - 2*	2 - 3

Serial port 1

	COM 1	Disable
JP29	1 - 2*	2 - 3
JP30	1 - 2*	2 - 3

Serial port 2

	COM 2	Disable
JP31	1 - 2*	2 - 3
JP32	1 - 2*	2 - 3

Floppy disk controller

	Enable	Disable
JP19	1 - 2*	2 - 3

CMOS contain

	Normal	Clear
JP34	1 - 2*	2 - 3

FACTORY DEFAULT SETTING

JP1 (1-2), JP3 (2-3), JP6 (OPEN), JP7 (OPEN),
JP8 (1-2), JP13(1-2), JP14(1-2), JP16(1-2),
JP20(1-2), JP26(1-2), JW1 (1-2), JW2 (2-3)

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Appendix D
System Board Layout

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