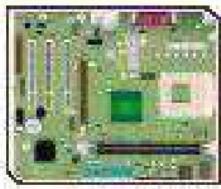
Galaxy P8 (MS6596 Ver 2.0) µATX motherboard



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Specifications

- **Form Factor**
  - µATX 24.4 cm. x 21.75 cm Form Factor
- **CPU Support**
  - Socket -A (Socket 462) for AMD PGA Athlon processor
  - 133 & 166 MHz Host bus speed (uses dual clocking to obtain 266 & 333 MHz FSB)
- **System Memory**
  - Two 184-pin DDR SDRAM DIMM sockets
  - Support for single-sided or double-sided DIMMs (DDR 266 and DDR 333)
  - Support for up to 2 GB system memory
- **KT400 Chipset: VT8377 System Controller and VT8235 V-Link South Bridge Chipset**
  - Single-Chip North Bridge for Socket-A (Socket-462)Based Athlon CPUs with 266 & 333 MHz Front Side Bus with 8x/4x/2x AGP and V-Link Interfaces plus Memory Controller supporting PC2700 / 2100 / 1600 DDR DRAM

Product Features

- **High Performance and High Integration Athlon AGP 8x / DDR Chipset with Advanced System**
  - Power Management
  - KT400 Chipset: VT8377 system controller and VT8235 V-Link south bridge
  - Single chip Athlon system controller with 64-bit Socket-A Athlon CPU, 64-bit 166 / 133 / 100 MHz DDR system memory, 266 MB/s high bandwidth V-Link NB / SB, and 32-bit AGP interfaces
  - V-Link south bridge chip includes UltraDMA-133 / 100 / 66 / 33 EIDE, 6 USB 2.0 Ports, AC97 / MC97 link (for Audio and Modem support), LPC, SM Bus, Power Management, and Keyboard / PS/2-Mouse Interfaces plus RTC / CMOS chip
  - Supports separately powered 3.3 V (5 V tolerant)interface to system memory and AGP
  - Modular power management and clock control for advanced system power management

- **High Performance Athlon CPU Interface**
  - Supports Socket-A (Socket-462) AMD Athlon processors
  - HSTL-like 1.5 V high-speed transceiver logic signal levels
  - Support independent address, data, and snoop interfaces
  - 166/133/100 MHz DDR (Double Data Rate) transfer on Athlon CPU address and data buses
  - Built-in PLL (Phase Lock Loop) circuitry for optimal skew control within and between clocking regions
  - Four-entry command queue to accommodate maximum CPU throughput
  - Four-entry probe queue to stores probes from the system to the processor
  - Twenty four-entry processor system data and control queue to store system data control commands in two separate read and write buffers for data movement in and out of processor interface
  - Supports WC (Write Combining) cycles
  - Sleep mode support
  - System management interrupt, memory remap and STPCLK mechanism
- **Full Featured Accelerated Graphics Port (AGP) Controller**
  - Supports 533 MHz 8x, 266 MHz 4x and 133 MHz 2x transfer modes for AD and SBA signaling
  - AGP v3.0 compliant with 8x transfer mode
  - Pseudo-synchronous with the host CPU bus with optimal skew control
  - Supports SideBand Addressing (SBA) mode (non-multiplexed address /data)
  - AGP pipelined split-transaction long-burst transfers up to 1 GB/s
  - Eight level read request queue
  - Four level posted-write request queue
  - Thirty two-level (quad-words)read data FIFO (256 bytes)
  - Sixteen level (quad-words)write data FIFO (128 bytes)
  - Intelligent request reordering for maximum AGP bus utilization
  - Supports Flush/Fence commands
  - Graphics Address Relocation Table (GART)
    - One level TLB structure
    - Sixteen entry fully associative page table
    - LRU replacement scheme
    - Independent GART lookup control for host / AGP / PCI master accesses
  - Windows 95 OSR-2 VXD and integrated Windows 98 /Windows 2000 miniport driver support
- **High Bandwidth 533 MB /Sec 8-bit -Link Host Controller**
  - Supports 66 MHz V-Link Host interface with peak bandwidth of 533 MB/s
  - Operates in 2x, 4x and 8x modes
  - Full duplex commands with separate command / strobe
  - Request / Data split transaction
  - Configurable outstanding transaction queue for Host to V-Link Client accesses
  - Supports Defer / Defer-Reply transactions
  - Transaction assurance for V-Link Host to Client access eliminates V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to eliminate data wait-state / throttle transfer latency
  - All V-Link transactions for both Host and Client have a consistent view of transaction data depth and buffer size to avoid data overflow
  - Highly efficient V-Link arbitration with minimum overhead
  - All V-Link transactions have predictable cycle length with known command / data duration
- **Advanced High-Performance DDR DRAM Controller**
  - DRAM interface may be faster than CPU by 33 MHz to allow use of 166 MHz memory with 133 MHz FSB
  - Concurrent CPU, AGP,and V-Link access
  - Clock Enable (CKE) control for DRAM power reduction in high speed systems
  - Mixed 1 MB / 2 MB / 4 MB / 8 MB / 16 MB / 32 MB / 64 MB /128 MB x 8/16/32 DRAMs
  - Supports 2 banks up to 2 GB DRAMs
  - Allows use of either unbuffered or registered memory modules
  - Flexible row and column addresses 64-bit data width only
  - 2.5 V SSTL-2 DRAM interface
  - Programmable I/O drive capability for MA, MD, and command signals
  - Dual copies of MA and control signals for improved drive
  - Two-bank interleaving for 16 Mbit DRAM support
  - Four-bank interleaving for 64 MB, 128 MB, 256 MB, 512 MB,and 1 GB DRAM support
  - Supports maximum 16-bank interleave (i.e.16 pages open simultaneously); banks are allocated based on LRU
  - Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g. precharge other banks while accessing the current bank)
  - Four cache lines (16 quad-words) of CPU to DRAM write buffers
  - Four cache lines of CPU to DRAM read prefetch buffers
  - Read around write capability for non-stalled CPU read
  - Speculative DRAM read before snoop result
  - Burst read and write operation
  - Burst length 4 and 8
  - Supports CL 2/2.5 and 1T per command
  - 1T and 2T command rate which can be specified bank by bank
  - Decoupled and burst DRAM refresh with staggered RAS timing (CAS before RAS or self refresh)

- **Advanced System Power Management Support**
  - Dynamic power down of DRAM (CKE)
  - PCI and AGP bus clock run and clock generator control
  - VTT suspend power plane preserves memory data
  - Suspend-to-DRAM and Self-Refresh operation
  - DRAM self-refresh power down
  - 8 bytes of BIOS scratch registers
  - Low-leakage I/O pads
- **Built-in NAND-Tree Pin Scan Test Capability**
- **2.5 V, 0.22 um, High Speed / Low Power CMOS Process**
- **High Density 828-Pin HSBGA Package**
  - Integrated heat spreader
  - 35 x 35 mm package body
  - 34 x 34 ball grid
  - 1.0 mm ball pitch

VT8235 Chipset

Specifications

- Low cost V-Link Client
- Highly integrated South Bridge
- High Bandwith V-Link Client Controller
- Integrated Fast Ethernet
- Integrated Direct Sound AC97 Audio
- UltraDMA-133/100/66/33 Master Mode EIDE Controller
- Six port USB 2.0 Controller, keyboard / mouse Controller
- RTC, LPC, SMBUS, Serial IRQ, Plug & Play, ACPI
- PC2001 Compliant Enhanced Power Management

Product Features

- **Inter-operable with VIA Host-to-V-Link Host Controller**
  - Combine with VT8377 (Apollo KT400) for a complete 333 / 266 / 200 MHz FSB Athlon Socket-A system
- **High Bandwidth 533 MB/s 8-bit V-Link Client Controller**
  - Supports 66 MHz V-Link Client interface with peak bandwidth of 533 MB/s
  - V-Link operates in 2x, 4x, and 8x modes
  - Full duplex commands with separate Strobe / Command
  - Request / Data split transaction
  - Configurable outstanding transaction queue for V-Link Client accesses
  - Auto Client Retry to eliminate V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to eliminate data wait state / throttle transfer latency; all V-Link transactions for both Host and Client have a consistent view of transaction data depth and buffer size to avoid data overflow.
  - Highly efficient V-Link arbitration with minimum overhead; all V-Link transactions have predictable cycle length
  - With known Command / Data duration
  - Auto connect / reconnect capability and dynamic stop for minimum power consumption
  - Parity checking to insure correct data transfers
- **Integrated Peripheral Controllers**
  - Integrated Fast Ethernet Controller with 1 / 10 / 100 Mbit capability
  - Integrated USB 2.0 Controller with three root HUBs and 6 function ports
  - Dual channel Ultra DMA-133 / 100 / 66 / 33 master mode EIDE controller
  - AC-link interface for AC-97 audio codec and modem codec
  - Integrated DirectSound compatible digital audio controller
  - LPC interface for Low Pin Count interface to Super-I/O or ROM
- **Integrated Legacy Functions**
  - Integrated Keyboard Controller with PS/2 mouse support
  - Integrated DS12885-style Real Time Clock with extended 256-byte CMOS RAM and Day/Month Alarm for ACPI
  - Integrated DMA,timer,and interrupt controller
  - Serial IRQ for docking and non-docking applications
  - Fast reset and Gate A20 operation

- **Concurrent PCI Bus Controller**
  - 33 MHz operation
  - Supports up to 6 PCI masters and 3 PCI used
  - Peer concurrency
  - Concurrent multiple PCI master transactions; i.e. allow PCI masters from both PCI buses active at the same time
  - Zero wait state PCI master and slave burst transfer rate
  - PCI to system memory data streaming up to 132 MB/s (data sent to north bridge via high speed V-Link Interface)
  - PCI master snoop ahead and snoop filtering
  - Eight DW of CPU to PCI posted write buffers
  - Byte merging in he write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
  - Enhanced PCI command optimisation (MRL, MRM, MWI, etc.)
  - Four lines of post write buffers from PCI masters to DRAM
  - Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
  - Delay transaction from PCI master accessing DRAM
  - Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
  - Symmetric arbitration between Host/PCI bus for optimised system performance
  - Complete steerable PCI interrupts
  - PCI-2.2 compliant, 32 bit 3.3 V PCI interface with 5 V tolerant inputs
- **Fast Ethernet Controller**
  - High performance PCI master interface with scatter /gather and bursting capability
  - Standard MII interface to external receiver
  - 1 / 10 / 100 MHz full and half duplex operation
  - Independent 2K byte FIFOs for receive and transmit
  - Flexible dynamically loadable EEPROM algorithm
  - Physical, broadcast, and Multicast address filtering using hashing function
  - Magic packet and wake-on-address filtering
  - Software controllable power down
- **UltraDMA-133 / 100 / 66 / 33 Master Mode EIDE Controller**
  - Dual channel master mode hard disk controller supporting four Enhanced IDE devices
  - Transfer rate up to 133 MB/s to cover PIO mode 4, multi-word DMA mode 2 drives, and Ultra DMA-133 interface
  - Increased reliability using Ultra DMA-133/100/66 transfer protocols
  - Thirty-two levels (double-words) of prefetch and write buffers
  - Dual DMA engine for concurrent dual channel operation
  - Bus master programming interface for SFF-8038i rev.1.0 and Windows-95 compliant
  - Full scatter gather capability
  - Support ATAPI compliant devices including DVD devices
  - Support PCI native and ATA compatibility modes
  - Complete software driver support
- **System Management Bus Interface**
  - Host interface for processor communications
  - Slave interface for external SM Bus masters
- **Universal Serial Bus Controller**
  - USB v2.0 and Enhanced Host Controller Interface (EHCI) v1.0 compatible
  - USB v1.1 and Universal Host Controller Interface (UHCI) v1.1 compatible
  - Eighteen level (double-words) data FIFO with full scatter and gather capability
  - Three root hubs and six function ports
  - Integrated physical layer transceivers with optional over-current detection status on USB inputs
  - Legacy keyboard and PS/2 mouse support

- **Sophisticated PC2001-Compatible Mobile Power Management**
  - Supports both ACPI (Advanced Configuration and Power Interface) and legacy (APM) power management
  - ACPI v1.0 Compliant
  - APM v1.2 Compliant
  - CPU clock throttling and clock stop control for complete ACPI C0 to C3 state support
  - PCI bus clock run, Power Management Enable (PME) control, and PCI/CPU clock generator stop control
  - Supports multiple system suspend types:power-on suspends with flexible CPU/PCI bus reset options, suspend to DRAM, and suspend to disk (soft-off), all with hardware automatic wake-up
  - Multiple suspend power plane controls and suspend status indicators
  - One idle timer, one peripheral timer and one general purpose timer, plus 24/32-bi ACPI compliant timer
  - Normal, doze, sleep, suspend and conserve modes
  - Global and local device power control
  - System event monitoring with two event classes
  - Primary and secondary interrupt differentiation for individual channels
  - Dedicated input pins for power and sleep buttons,external modem ring indicator, and notebook lid open/close for system wake-up
  - 32 general purpose input ports and 32 output ports
  - Multiple internal and external SMI sources for flexible power management models
  - Enhanced integrated real time clock (RTC)with date alarm, month alarm, and century field
  - Thermal alarm on external temperature sensing circuit
  - I/O pad leakage control
- **Plug and Play Controller**
  - PCI interrupts steerable to any interrupt channel
  - Steerable interrupts for integrated peripheral controllers: USB, floppy, serial, parallel, and audio
  - Microsoft Windows XP TM, Windows NT TM, Windows 2000 TM, Windows 98 TM and plug and play BIOS compliant
- **Built-in NAND-tree pin scan test capability**
- **0.22 um, 2.5 V, low power CMOS process**

I/O controller

Winbond W83697HF I/O Controller with the following features:

- PS/2 Keyboard and Mouse controller
- Floppy disk controller supporting one FDD with 360 KB, 720 KB, 1.2 MB and 1.44 MB-bytes
- 2 serial ports, both 16C550 Fast UART compatible
- 1 Parallel port supporting SPP (Standard parallel Port), EPP (Enhanced Parallel Port), and ECP (Extended Capabilities Port) modes
- 1 Fan controller
- 6 USB 2.0 ports 4 + 2 front USB

Audio Chipset

Audio Subsystem for AC'97 processing using the Analogue Devices ALC650 codec.

- DirectSound AC'97 2.2 Audio
- Inputs and Outputs: Stereo inputs for line-in, CD audio, Auxiliary, mono inputs for microphone
- Mixer Features: mixer with stereo for line, CD audio, auxiliary, music synthesizer, digital audio (wave files), and mono for microphone and speakerphone
- Features: 3D stereo enhancement for simulated surround, Power management support
- Stereo Microphone input with integrated preamp for enabling a 2-channel mic array

BIOS Specifications

Winbond BIOS, including support for:

- Plug and Play
- Advanced Configuration and Power Interface (ACPI) 1.0
- Advanced Power Management (APM) 1.2
- Y2K
- PC 2001
- S3/S1 mode
- Desktop Management Interface (DMI)
- 2 Mbits flash device.
- Language supported: English
- POST

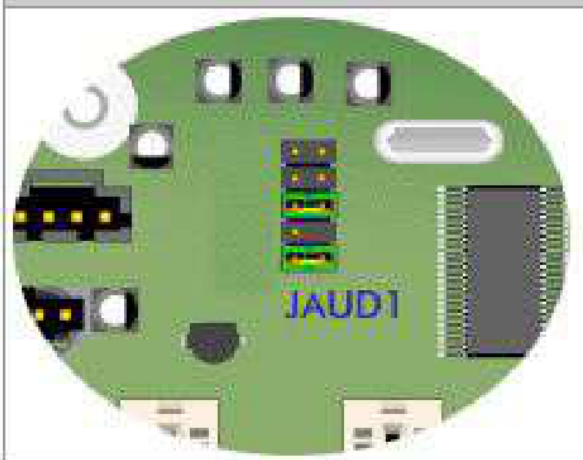
Compliance

SPECIFICATION	DESCRIPTION
Full ATX	Full ATX form factor specifications
AGP 2.0	Accelerated Graphics Port
APM	Advanced Power Management BIOS interface specification
ACPI	Advanced Configuration and Power management Interface
EPP	Enhanced Parallel Port IEEE 1284 standard, Mode [1 or 2]
ECP	Extended Capabilities Port
ATA-33	Synchronous DMA Transfer Protocol specification (to be proposed as Ultra DMA/33 standard)
PCI 2.2	PCI Local Bus specification
Plug and Play	Plug and Play BIOS specification
USB	Universal Serial Bus specification
ATA-66/100/133	Synchronous DMA Transfer Protocol specification

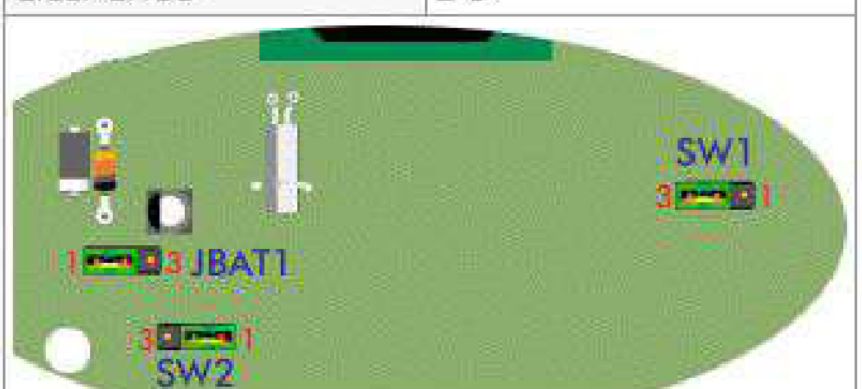
Motherboard Configuration

The Galaxy PB motherboard has three jumper settings:

- Front Panel audio connector JAUD1 (not used)
- CLEAR CMOS JBAT1
- FSB (SW1&SW2)

FRONT PANEL AUDIO CONNECTOR JAUD1


JBAT1: CLEAR CMOS CONFIGURATION	
Normal	1-2
Clear CMOS	2-3

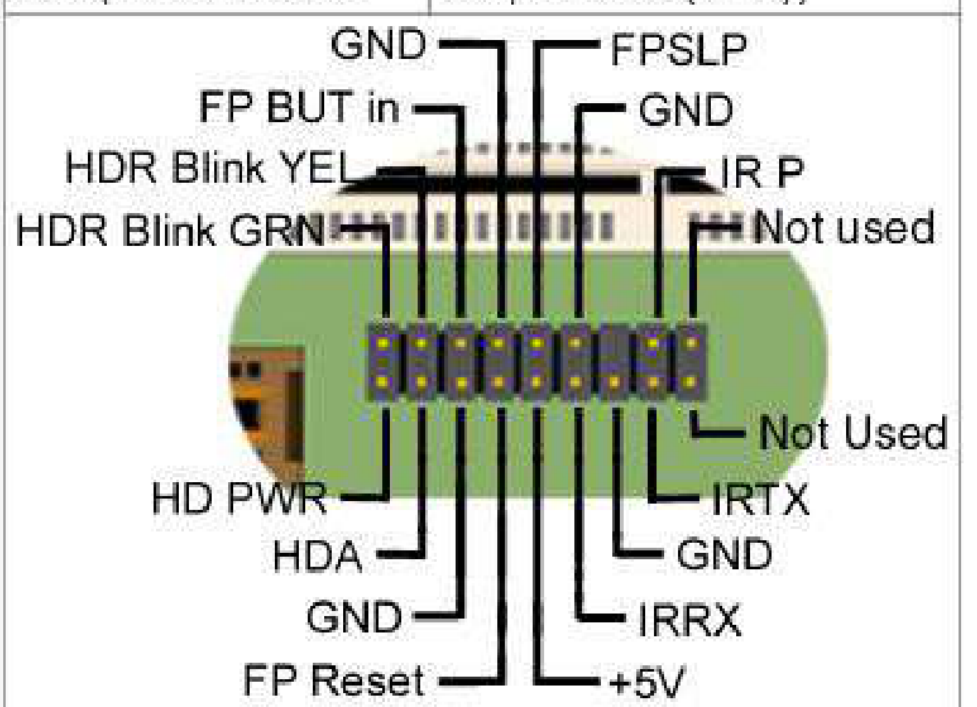


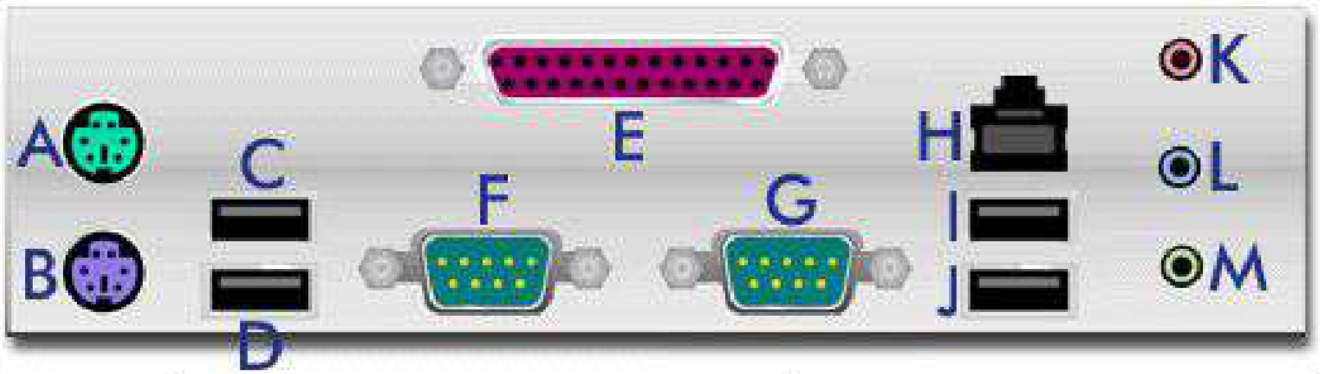
FSB:	SW1	SW2
100	2-3	1-2
133	1-2	1-2
166	1-2	2-3

Connectors

- 1 AGP slot with integrated retention mechanism
- 3 PCI slots
- 1 CNR slot
- 1 DB9 serial port (COM A)
- 1 DB9 serial port (COM B)
- 1 DB25 parallel port with SPP, ECP, EPP bidirectional modes
- PS/2 keyboard and PS/2 mouse ports (not exchangeable)
- 6 USB 2.0 ports 4 + 2 front USB
- 1 mono microphone input (Mic-In)
- 1 Line-In
- 1 Line-Out
- 2 IDE connectors
- 1 Floppy connector
- Panel connector
- 1 RJ45 connector

INTERNAL CONNECTORS		
DENOMINATION ON DRAWING	**NAME**	**TYPE**
CONN1	Power connector	20 pin Keyed Connector
SYSFA1	System fan connector	3 pin header
FDD1	Floppy drive connector	34 (2x17) pin Shrouded Header
IDE 1	Primary IDE connector	40 (2x20) pin header (blue)
IDE 2	Secondary IDE connector	40 (2x20) pin header (white)
PCI 1, 2 and 3	PCI connectors	standard PCI expansion slots
AGP1	Accelerated Graphics Port	standard AGP connector
CPU	CPU connector	462 Pin socket
CPU FAN	CPU fan connector	3 pin header
DIMM 1 & 2	DIMM sockets	184 pin standard sockets
JCD1	CD-ROM audio line in	4 pin header (black)
JAUD1	Connecting to front audio	10 pin jumper
BAT1	CMOS battery socket	
JFP1	Front panel Connector	2x5 pin header (-1 key)



BACK PANEL CONNECTORS		
NAME	**FUNCTION**	**TYPE**
		
A	PS/2 mouse port	6 pin mini-DIN
B	PS/2 keyboard port	6 pin mini-DIN
C	USB port 1	
D	USB port 2	
I	USB port 3	
J	USB port 4	
F	Serial port 1	9 pin SUB D
G	Serial port 2	9 pin SUB D
E	Parallel port	25 pin SUB D
K	Mono microphone in	jack socket
H	RJ45 LAN	
L	Audio line out	jack socket
M	Audio line in	jack socket

Instructie

BIOS

- Galaxy Motherboard BIOS Screens

21-02-2003

Verwante items

Download

- Galaxy PB BIOS
  Version: [1.40] WinXP

Produkt ondersteuning

- Videokaart blokkeert toegang tot DIMM-socket